**Ve270 Introduction to Logic Design Homework 8**

**Assigned: November 14, 2019**

**Due: November 21, 2019, 4:00pm.**

**The homework should be submitted in hard copies.**

1. Given a finite state machine described as the following state diagram, complete the timing diagrams of states and output Y according to the given inputs X and reset. Ignore delays. (10 Points)



reset

**Clock**



**Y**

**reset**

**State**

**X**

1. Repeat the same questions as in Problem 1 on the following state diagram. (10 Points)



reset

**Clock**



**Y**

**reset**

**State**

**X**

1. Problem 5.3 (15 points)
2. Problem 5.4 (20 points)
3. Problem 5.14. (25 points)
4. Problem 5.16 (20 points)