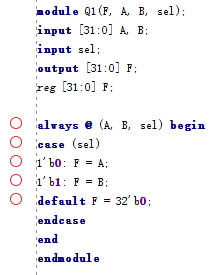
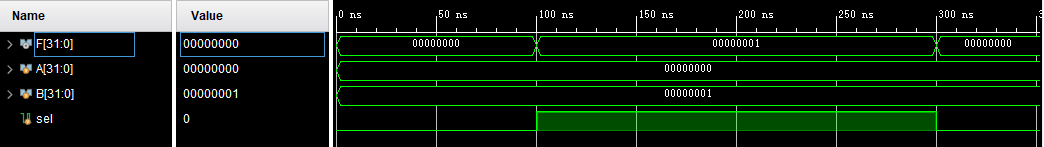
Q1

Verilog code:

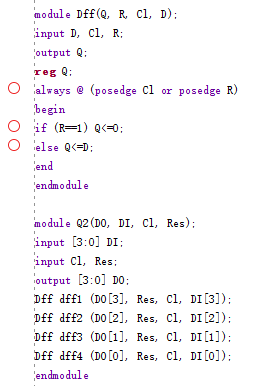


Simulation result:

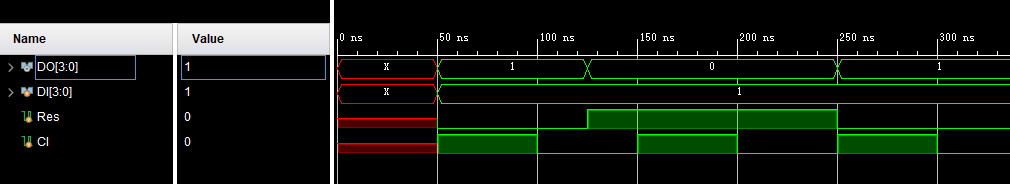


Q2

Verilog code:

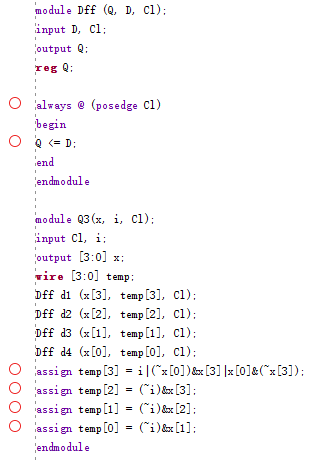


Simulation result:

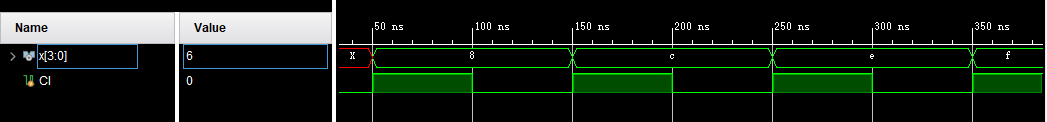


Q3

Verilog code:

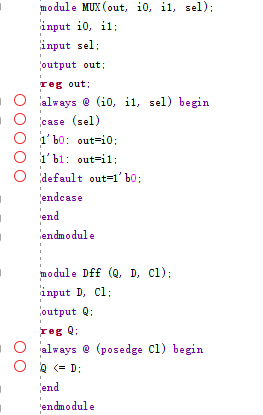


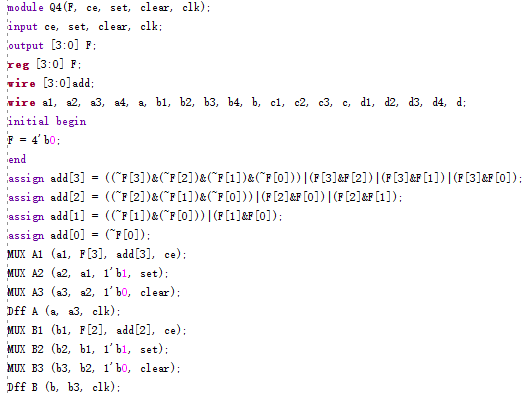
Simulation result:

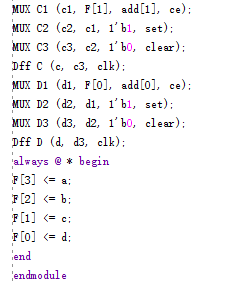


Q4

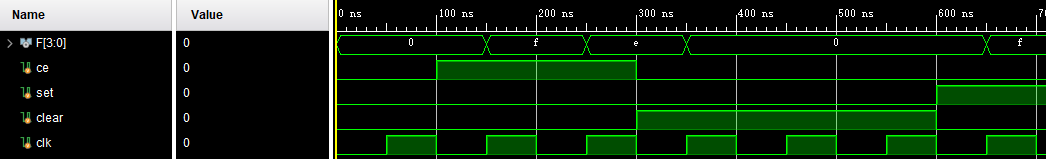
Verilog code:





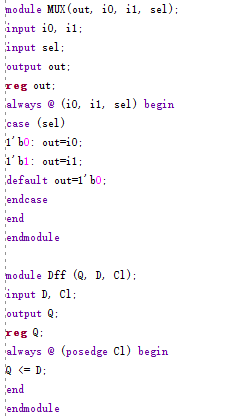


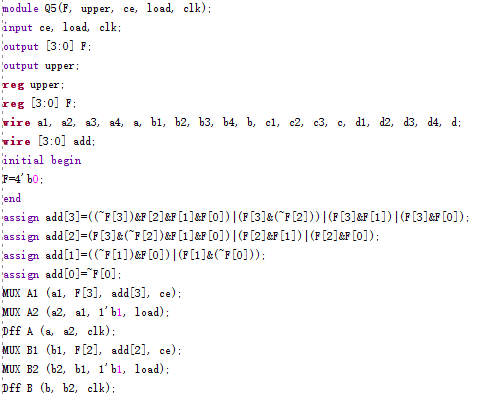
Simulation result:

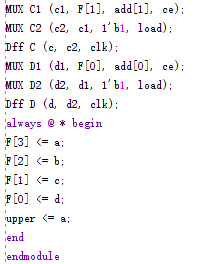


Q5

Verilog code:







Simulation result:

