Fall-2020 UM-SJTU JI Ve311 Homework #6

Instructor: Dr. Chang-Ching Tu

Due: 11:59 am, November 11, 2020 (Wednesday)

Note:

(1) Please use A4 size papers.

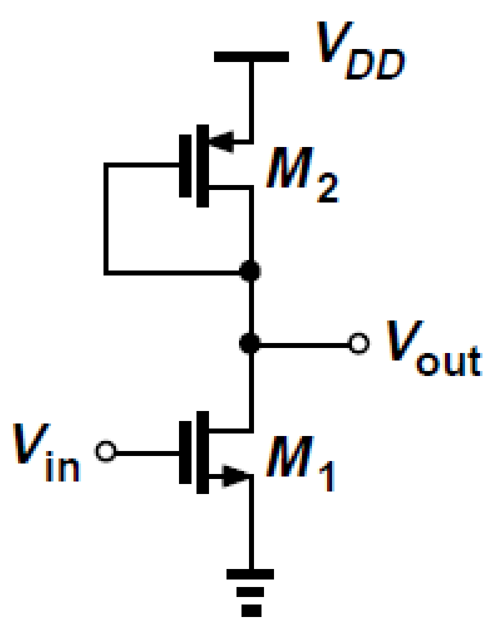
(2) Please use the SPICE model in page 3 for simulation and calculation.

1. [Common-Source with Diode-Connected Load]

   (a) [30%] Assume $\lambda = 0$ and $\gamma = 0$. For V_{DD} = 5 V, V_{in} = 1 V, $(W_{drawn}/L_{drawn})_2$ = 5 μm / 2 μm and $(W_{drawn}/L_{drawn})_1$ = x μm / 2 μm, what is the value of x to obtain a voltage gain $A_v = -6$? What is the range of V_{in} for M_1 to stay in the saturation region?

   (b) [10%] Using the design and biasing condition in (a), plot V_{out} and A_v as a function of V_{in} (from 0 V to 5 V) in Pspice. Compare the hand-calculation results in (a) with the simulation results here.

   (c) [10%] Using the design and biasing conditions in (a), plot V_{out} as a function of time (from 0 to 0.1 second) in Pspice, when $V_{in} = 1 + A \times \sin(2\pi 100)$ (V) and A = 0.01 V, 0.1 V and 1 V. What do you observe when the swing of V_{in} goes beyond the range in which M_1 is in the saturation region, as calculated in (a)?

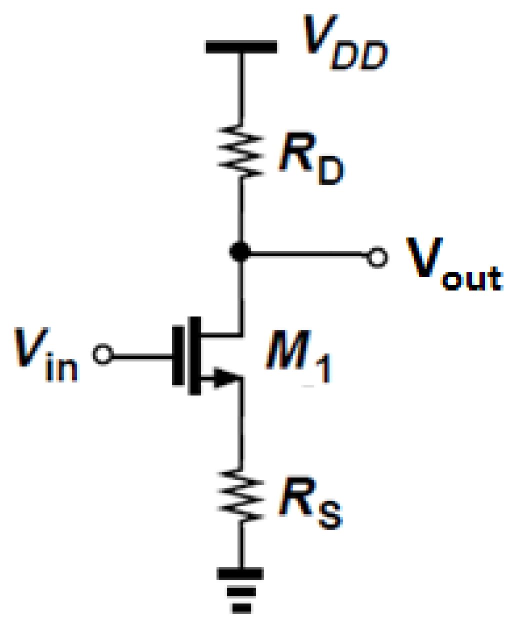


2. [Common-Source with Source Degradation]

(a) [30%] Assume $\lambda = 0$ and $\gamma = 0$. For V_{DD} = 5 V, V_{in} = 1.2 V, $(W_{drawn}/L_{drawn})_1$ = 200 µm / 2 µm, R_D = 100 kΩ and R_S = 20 kΩ, what is the voltage gain A_v? Does the voltage gain approach $-R_D$ / R_S as expected?

(b) [10%] Using the design and biasing condition in (a), plot V_{out} and A_v as a function of V_{in} (from 0 V to 5 V) in Pspice. Compare the hand-calculation results in (a) with the simulation results here.

(c) [10%] Using the design and biasing conditions in (a), plot V_{out} as a function of time (from 0 to 0.1 second) in Pspice, when $V_{in} = 1.2 + A \times \sin(2\pi 100)$ (V) and A = 0.01 V.



NMOS Model

LEVEL = 1	VTO = 0.7	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08e−6	UO = 350	LAMBDA = 0.1
TOX = 9e−9	PB = 0.9	CJ = 0.56e−3	CJSW = 0.35e−11
MJ = 0.45	MJSW = 0.2	CGDO = 0.4e−9	JS = 1.0e−8

PMOS Model

LEVEL = 1	VTO = −0.8	GAMMA = 0.4	PHI = 0.8
NSUB = 5e+14	LD = 0.09e−6	UO = 100	LAMBDA = 0.2
TOX = 9e−9	PB = 0.9	CJ = 0.94e−3	CJSW = 0.32e−11
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e−9	JS = 0.5e−8

VTO: threshold voltage with zero V_{SB} (unit: V)
GAMMA: body effect coefficient (unit: $V^{1/2}$)
PHI: $2\Phi_F$ (unit: V)
TOX: gate oxide thickness (unit: m)
NSUB: substrate doping (unit: cm^{-3})
LD: source/drain side diffusion (unit: m)
UO: channel mobility (unit: $cm^2/V/s$)
LAMBDA: channel-length modulation coefficient (unit: V^{-1})
CJ: source/drain bottom-plate junction capacitance per unit area (unit: F/m^2)
CJSW: source/drain sidewall junction capacitance per unit length (unit: F/m)
PB: source/drain junction built-in potential (unit: V)
MJ: exponent in CJ equation (unitless)
MJSW: exponent in CJSW equation (unitless)
CGDO: gate-drain overlap capacitance per unit width (unit: F/m)
CGSO: gate-source overlap capacitance per unit width (unit: F/m)
JS: source/drain leakage current per unit area (unit: A/m^2)

Vacuum permittivity (ϵ_o) $= 8.85 \times 10^{-12}$ (F / m)
Silicon oxide dielectric constant (ϵ_r) $= 3.9$