Fall-2020 UM-SJTU JI Ve311 Lab #4

Instructor: Dr. Chang-Ching Tu

Due: 11:59 am, December 11, 2020 (Friday)

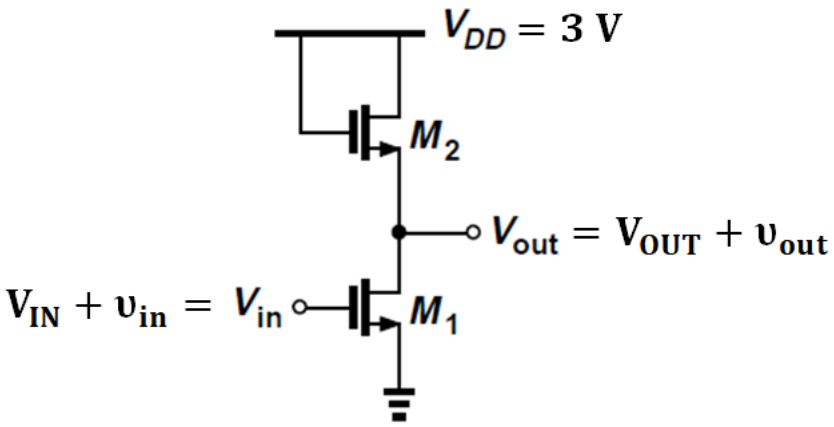
Note:

(1) Please use A4 size papers.

(2) The lab report should be submitted online individually.

(3) Use Proteus 8.10 for simulation before the lab session. In the Proteus library, you should be able to find all the components used in the schematics. **The lab report must include both the simulation and measurement results.**

1. [Common-Source with NMOS Diode-Connected Load]
   (a) [20%] Design and build a common-source with diode-connected load amplifier using NMOS (**VN0104**). Plot V_{OUT} vs V_{IN}. What is the voltage gain A_υ? *(Hint: Perform DC sweep of V_{IN} from 0 V to 3 V to find out a V_{IN} at which both transistors are in the saturation region. The voltage gain is the slope at the V_{IN}.)*
   Caution: the transistors could become very hot with high drain current. Don't touch with bare hands before they fully cool down.
   (b) [15%] Following (a), now put **two common-source NMOS in parallel**. Plot V_{OUT} vs V_{IN}. At the V_{IN} chosen in (a), does the voltage gain A_υ double? Briefly explain the reason. *(Note: Make sure all NMOS remain in the saturation region.)*
   (c) [15%] Following (b), for $V_{in} = V_{IN} + 0.01\sin(2\pi 10^2 \cdot \text{time})$, plot $V_{out} = V_{OUT} + \upsilon_{out}$ vs time. Confirm that the amplitude of υ_{out} is close to $0.01 \times A_\upsilon$.



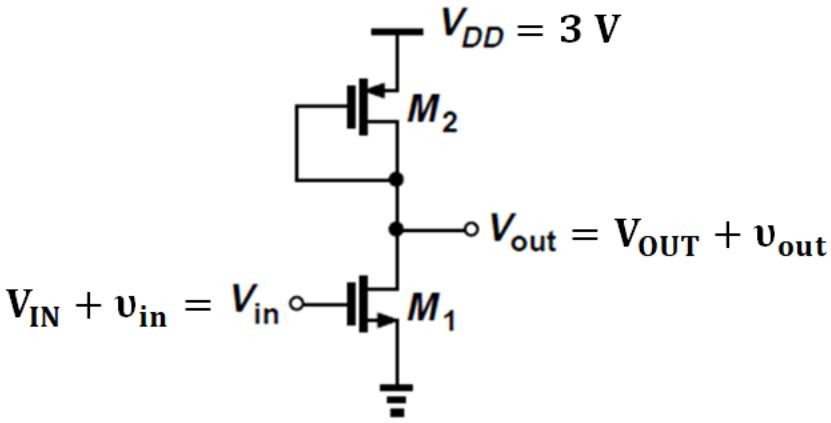
2. [Common-Source with PMOS Diode-Connected Load]

   (d) [20%] Design and build a common-source with diode-connected load amplifier using NMOS (**VN0104**) and PMOS (**VP0104**). Plot V_{OUT} vs V_{IN}. What is the voltage gain A_υ? *(Hint: Perform DC sweep of V_{IN} from 0 V to 3 V to find out a V_{IN} at which both transistors are in the saturation region. The voltage gain is the slope at the V_{IN}.)*

   Caution: the transistors could become very hot with high drain current. Don't touch with bare hands before they fully cool down.

   (a) [15%] Following (a), now put **two PMOS diode-connected loads in parallel**. Plot V_{OUT} vs V_{IN}. At the V_{IN} chosen in (a), how does the voltage gain A_υ change? Briefly explain the reason. *(Note: Make sure all NMOS and PMOS remain in the saturation region.)*

   (b) [15%] Following (b), for $V_{in} = V_{IN} + 0.01\sin(2\pi 10^2 \cdot \text{time})$, plot $V_{out} = V_{OUT} + \upsilon_{out}$ vs time. Confirm that the amplitude of υ_{out} is close to $0.01 \times A_\upsilon$.


$V_{DD} = 3\ \mathrm{V}$
M_2
$V_{out} = V_{OUT} + v_{out}$
$V_{IN} + v_{in} = V_{in}$
M_1

N-Channel Enhancement-Mode Vertical DMOS FET

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral source-drain diode
- High input impedance and high gain

Applications

- Motor controls
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

General Description

This enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven, silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Device	Package Option	Wafer / Die Options		
	TO-92	NW (Die in wafer form)	NJ (Die on adhesive tape)	ND (Die in waffle pack)
VN0104	VN0104N3-G	VN1504NW	VN1504NJ	VN1504ND

For packaged products, -G indicates package is RoHS compliant ('Green'). Devices in Wafer / Die form are RoHS compliant ('Green'). Refer to Die Specification VF15 for layout and dimensions.

Product Summary

BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (max) (Ω)	$I_{D(ON)}$ (min) (A)
40	3.0	2.0

Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration

TO-92 (N3)

Product Marking

YY = Year Sealed
WW = Week Sealed
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-92 (N3)

Thermal Characteristics

Package	I_D (continuous)† (mA)	I_D (pulsed) (A)	Power Dissipation @T_c = 25°C (W)	θ_{jc} (°C/W)	θ_{ja} (°C/W)	I_{DR}† (mA)	I_{DRM} (A)
TO-92	350	2.0	1.0	125	170	350	2.0

Notes:

† I_D *(continuous) is limited by max rated* T_j.

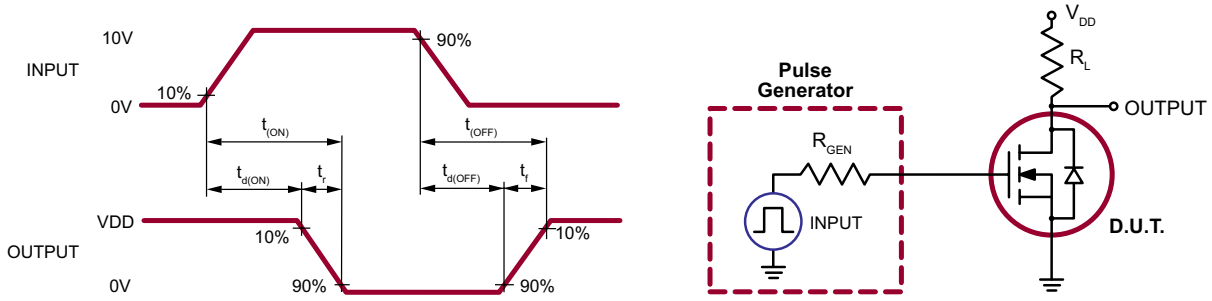
Electrical Characteristics *(T_A = 25°C unless otherwise specified)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	40	-	-	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate threshold voltage	0.8	-	2.4	V	V_{GS} = V_{DS}, I_D= 1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-3.8	-5.5	mV/°C	V_{GS} = V_{DS}, I_D= 1.0mA
I_{GSS}	Gate body leakage	-	-	100	nA	V_{GS} = ± 20V, V_{DS} = 0V
I_{DSS}	Zero gate voltage drain current	-	-	1.0	µA	V_{GS} = 0V, V_{DS} = Max Rating
		-	-	100		V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	On-state drain current	0.5	1.0	-	A	V_{GS} = 5.0V, V_{DS} = 25V
		2.0	2.5	-		V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	3.0	5.0	Ω	V_{GS} = 5.0V, I_D = 250mA
		-	2.5	3.0		V_{GS} = 10V, I_D = 1.0A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	0.70	1.0	%/°C	V_{GS} = 10V, I_D = 1.0A
G_{FS}	Forward transductance	300	450	-	mmho	V_{DS} = 25V, I_D = 500mA
C_{ISS}	Input capacitance	-	55	65	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz
C_{OSS}	Common source output capacitance	-	20	25		
C_{RSS}	Reverse transfer capacitance	-	5.0	8.0		
$t_{d(ON)}$	Turn-on delay time	-	3.0	5.0	ns	V_{DD} = 25V, I_D = 1.0A, R_{GEN} = 25Ω
t_r	Rise time	-	5.0	8.0		
$t_{d(OFF)}$	Turn-off delay time	-	6.0	9.0		
t_f	Fall time	-	5.0	8.0		
V_{SD}	Diode forward voltage drop	-	1.2	1.8	V	V_{GS} = 0V, I_{SD} = 1.0A
t_{rr}	Reverse recovery time	-	400	-	ns	V_{GS} = 0V, I_{SD} = 1.0A

Notes:

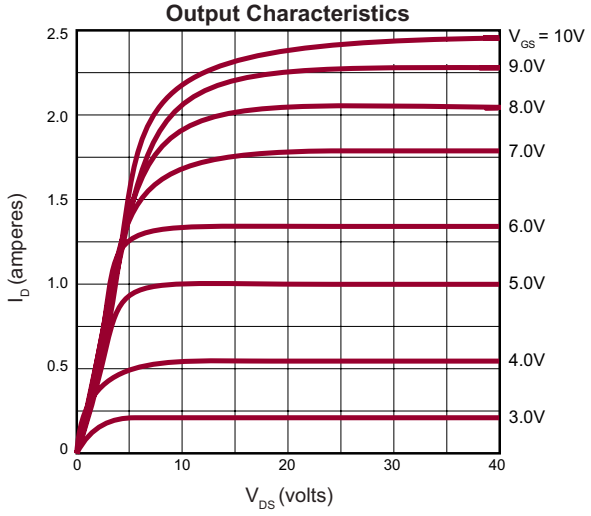
1. *All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)*
2. *All A.C. parameters sample tested.*

Switching Waveforms and Test Circuit

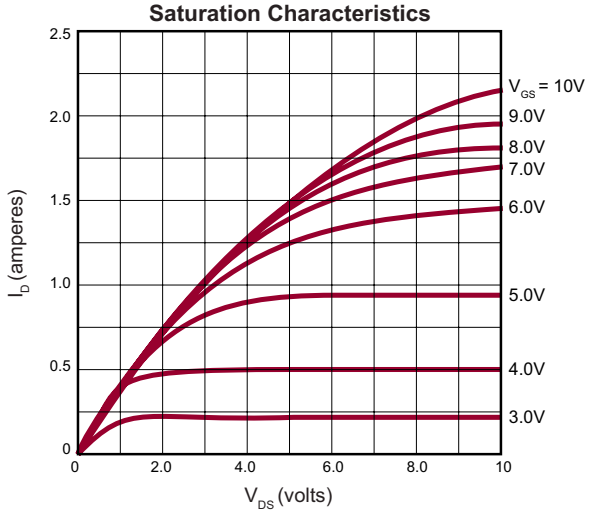


Typical Performance Curves

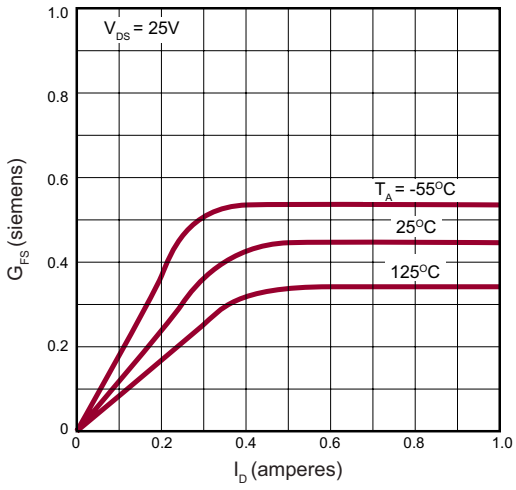
Output Characteristics



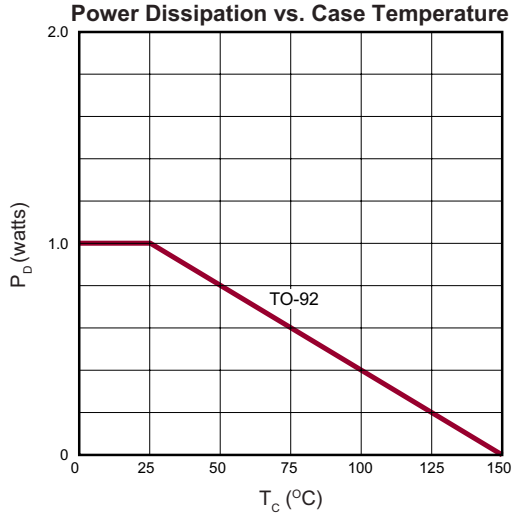
Saturation Characteristics



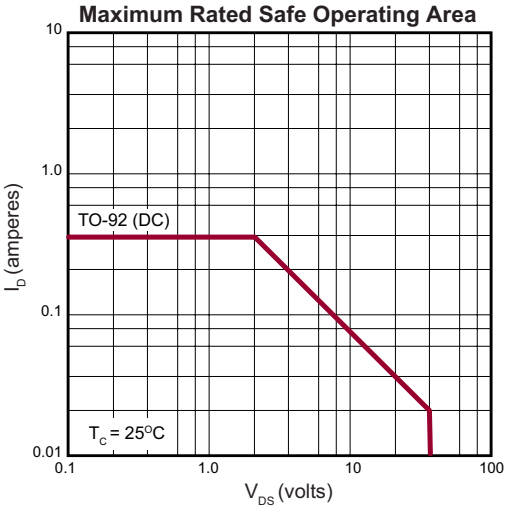
Transconductance vs. Drain Current



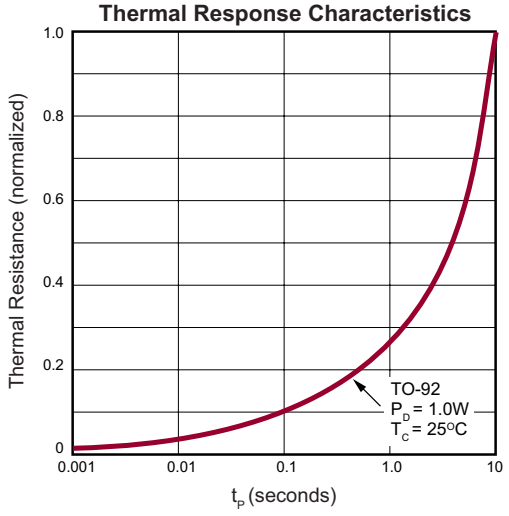
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

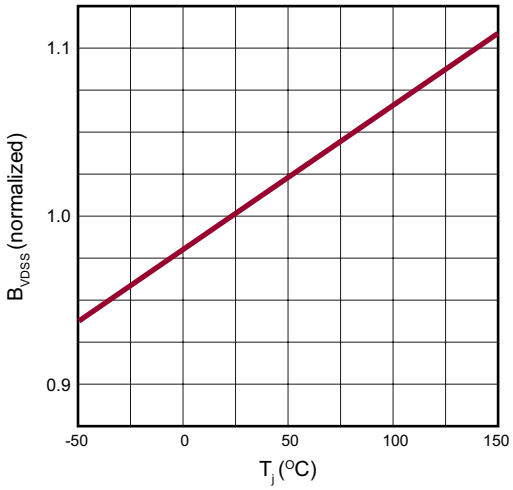


Thermal Response Characteristics

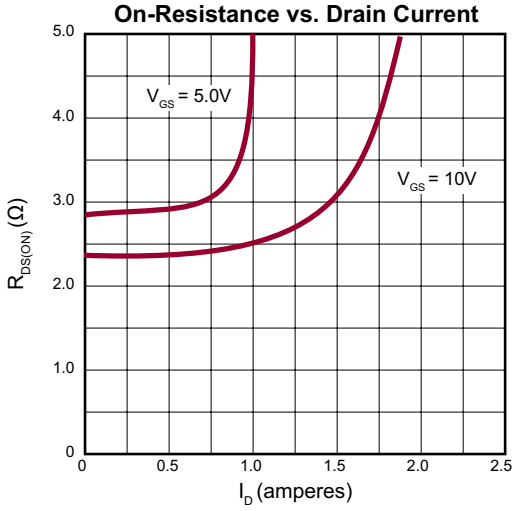


Typical Performance Curves *(cont.)*

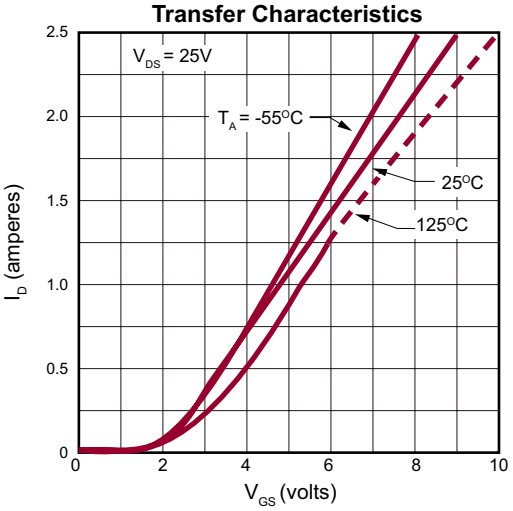
BV_{DSS} Variation with Temperature



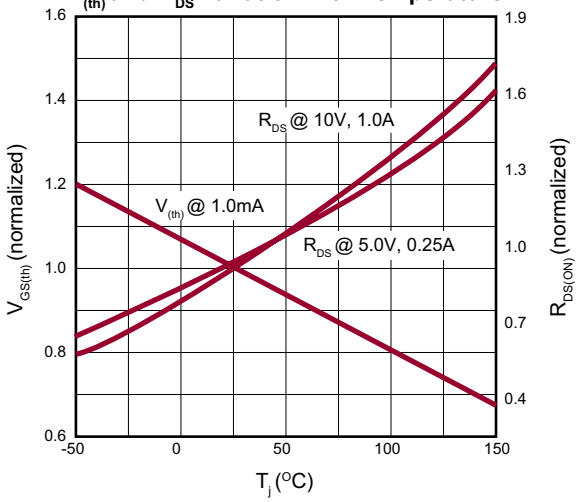
On-Resistance vs. Drain Current



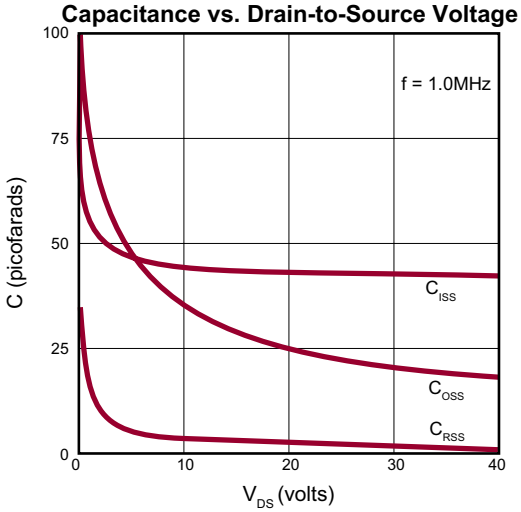
Transfer Characteristics



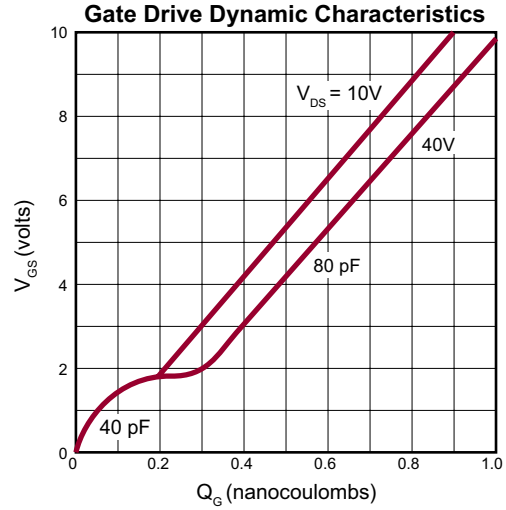
$V_{(th)}$ and R_{DS} Variation with Temperature



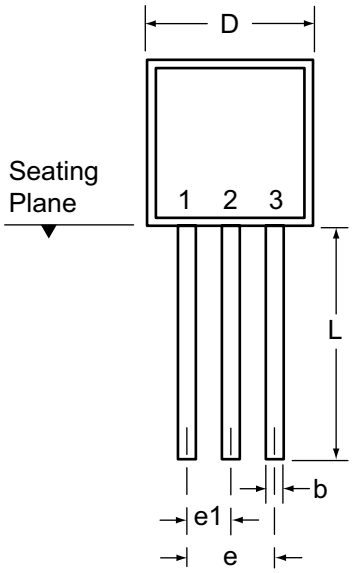
Capacitance vs. Drain-to-Source Voltage



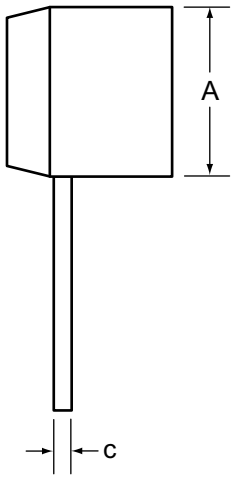
Gate Drive Dynamic Characteristics



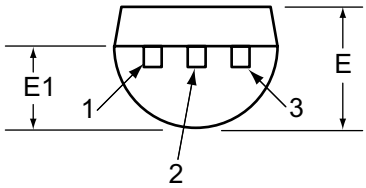
3-Lead TO-92 Package Outline (N3)



Front View



Side View



Bottom View

Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014†	.014†	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022†	.022†	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
***Supertex Doc.#:** DSPD-3TO92N3, Version E041009.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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1235 Bordeaux Drive, Sunnyvale, CA 94089
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VN0104N3-P014-G VN0104N3-P014 VN0104N3-P013 VN0104N3-P003 VN0104N3-P002 VN0104N3-G VN0104N3 VN0104N3-P013-G VN0104N3-P002-G VN0104N3-P003-G VN0104N3-G P002 VN0104N3-G P013 VN0104N3-G P005 VN0104N3-G P003 VN0104N3-G P014 VN0104N3-G-P013

P-Channel Enhancement-Mode Vertical DMOS FETs

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- High input impedance and high gain
- Excellent thermal stability
- Integral source-to-drain diode

Applications

- Motor controls
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

General Description

The Supertex VP0104 is an enhancement-mode (normally-off) transistor that utilizes a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors, and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Device	Package	Wafer / Die Options		
	TO-92	NW (Die in wafer form)	NJ (Die on adhesive tape)	ND (Die in waffle pack)
VP0104	VP0104N3-G	VP1504NW	VP1504NJ	VP1504ND

For packaged products, -G indicates package is RoHS compliant ('Green'). Devices in Wafer / Die form are RoHS compliant ('Green'). Refer to Die Specification VF15 for layout and dimensions.

Product Summary

Device	BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (max) (Ω)	$I_{D(ON)}$ (min) (mA)
VP0104N3-G	-40	8.0	-500

Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration

TO-92 (N3)

Product Marking

YY = Year Sealed
WW = Week Sealed
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-92 (N3)

Thermal Characteristics

Package	I_D (continuous)† (mA)	I_D (pulsed) (mA)	Power Dissipation @T_C = 25°C (W)	θ_{jc} (°C/W)	θ_{ja} (°C/W)	I_{DR}† (mA)	I_{DRM} (mA)
TO-92	-250	-800	1.0	125	170	-250	-800

Notes:

† I_D *(continuous) is limited by max rated* T_j.

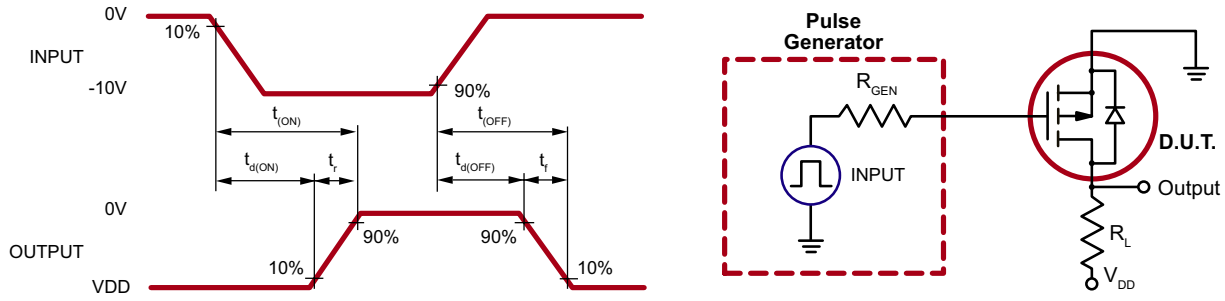
Electrical Characteristics *(T_A = 25°C unless otherwise specified)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	-40	-	-	V	V_{GS} = 0V, I_D = -1.0mA
$V_{GS(th)}$	Gate threshold voltage	-1.5	-	-3.5	V	V_{GS} = V_{DS}, I_D = -1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	5.8	6.5	mV/°C	V_{GS} = V_{DS}, I_D = -1.0mA
I_{GSS}	Gate body leakage current	-	-1.0	-100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero gate voltage drain current	-	-	-10	µA	V_{GS} = 0V, V_{DS} = Max Rating
		-	-	-1.0	mA	V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	On-state drain current	-0.15	-0.25	-	A	V_{GS} = -5.0V, V_{DS} = -25V
		-0.5	-1.2	-		V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	11	15	Ω	V_{GS} = -5.0V, I_D = -100mA
		-	6.0	8.0		V_{GS} = -10V, I_D = -500mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	0.55	1.0	%/°C	V_{GS} = -10V, I_D = -500mA
G_{FS}	Forward transconductance	150	190	-	mmho	V_{DS} = -25V, I_D = -500mA
C_{ISS}	Input capacitance	-	45	60	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz
C_{OSS}	Common source output capacitance	-	22	30		
C_{RSS}	Reverse transfer capacitance	-	3.0	8.0		
$t_{d(ON)}$	Turn-on delay time	-	4.0	6.0	ns	V_{DD} = -25V, I_D = -500mA, R_{GEN} = 25Ω
t_r	Rise time	-	3.0	10		
$t_{d(OFF)}$	Turn-off delay time	-	8.0	12		
t_f	Fall time	-	4.0	10		
V_{SD}	Diode forward voltage drop	-	-1.2	-2.0	V	V_{GS} = 0V, I_{SD} = -1.0A
t_{rr}	Reverse recovery time	-	400	-	ns	V_{GS} = 0V, I_{SD} = -1.0A

Notes:

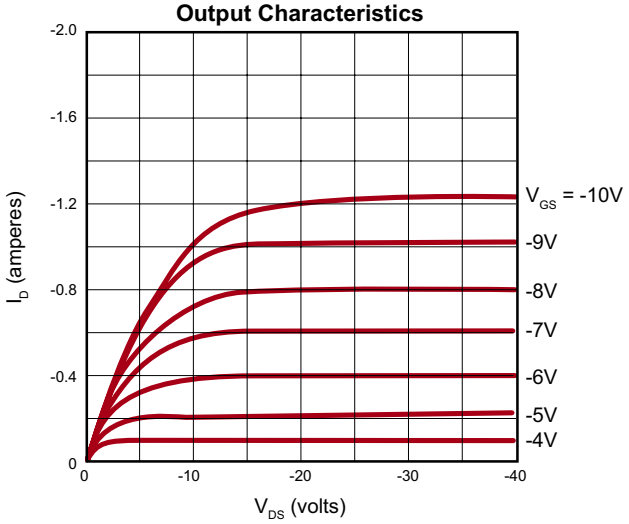
1. *All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)*
2. *All A.C. parameters sample tested.*

Switching Waveforms and Test Circuit

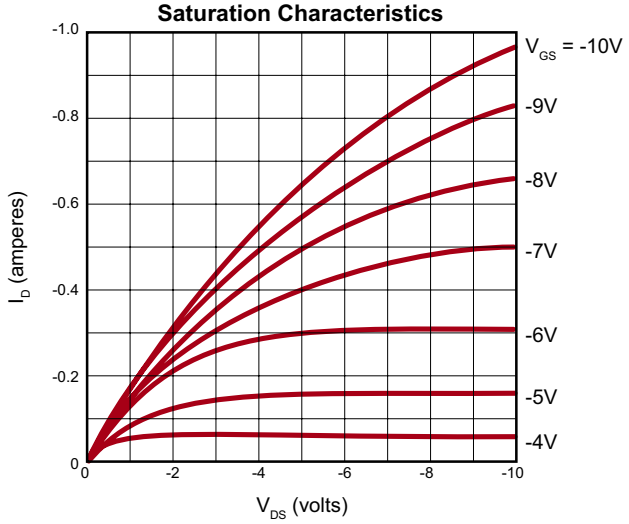


Typical Performance Curves

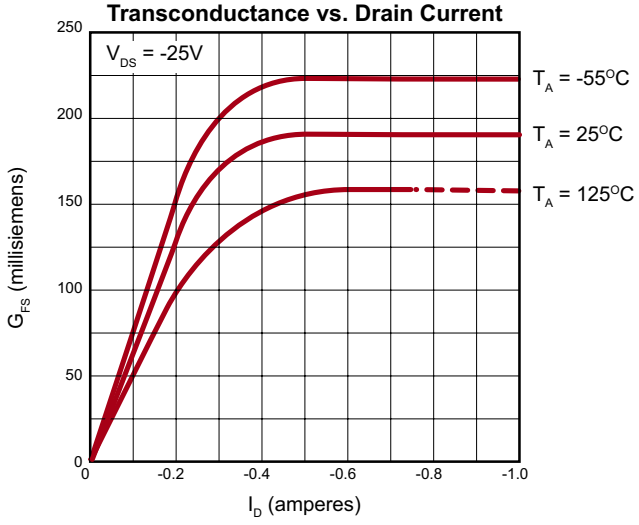
Output Characteristics



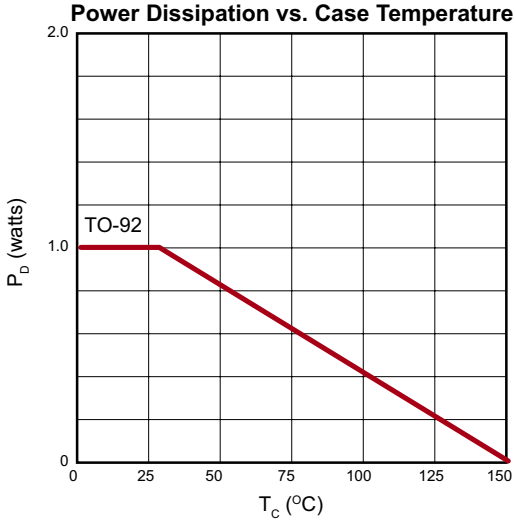
Saturation Characteristics



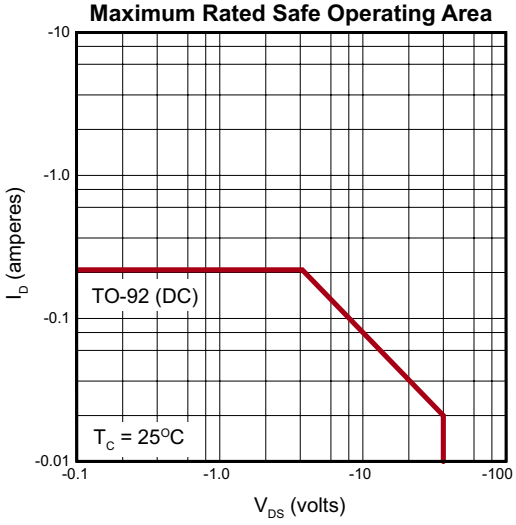
Transconductance vs. Drain Current



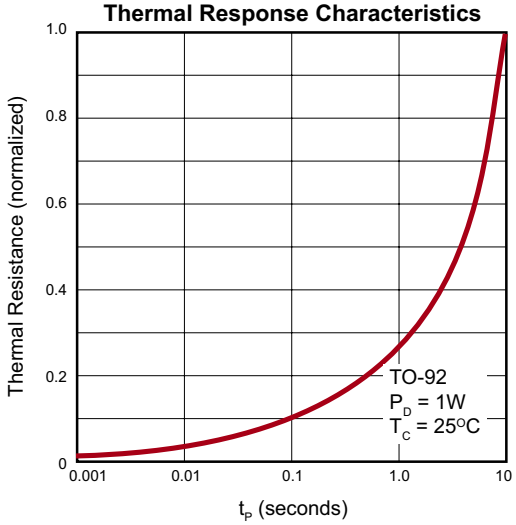
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

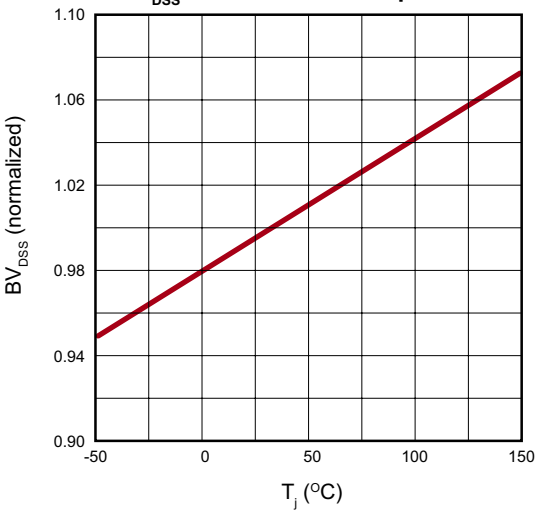


Thermal Response Characteristics

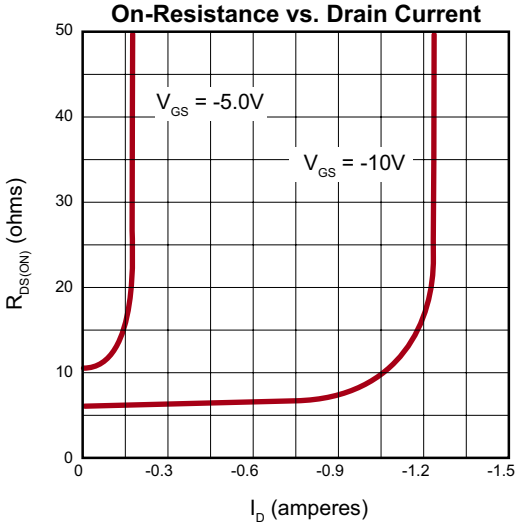


Typical Performance Curves *(cont.)*

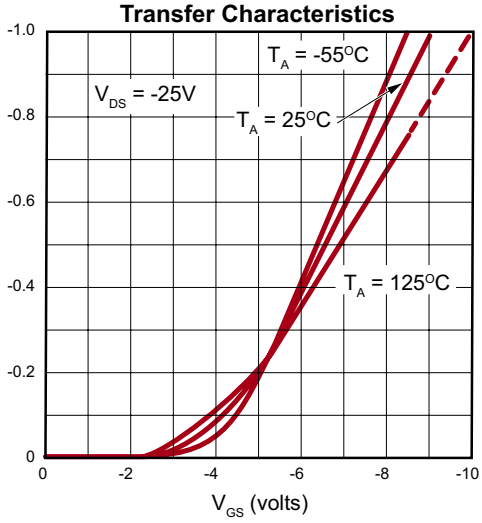
BV_{DSS} Variation with Temperature



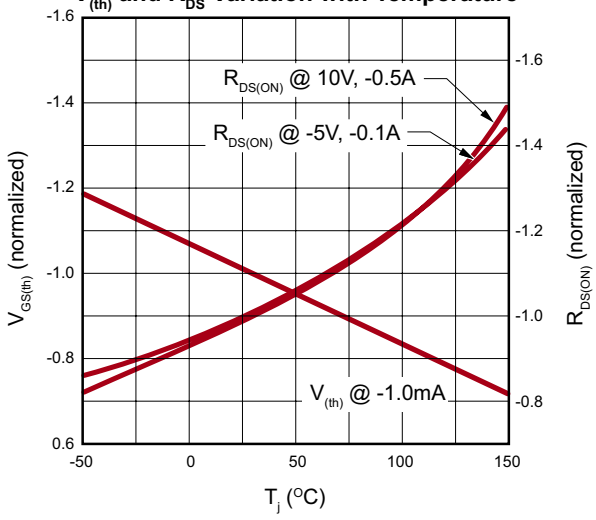
On-Resistance vs. Drain Current



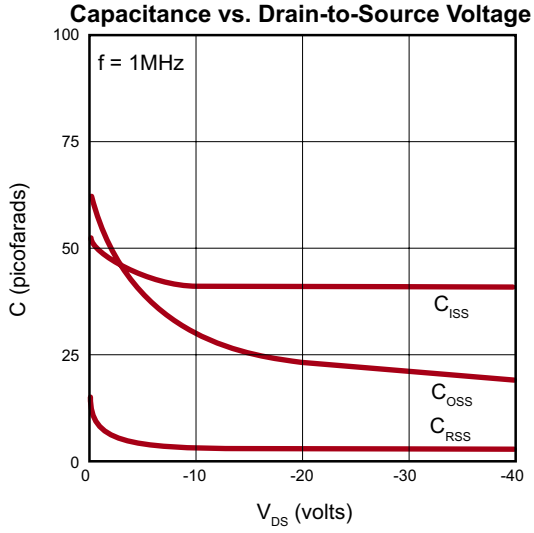
Transfer Characteristics



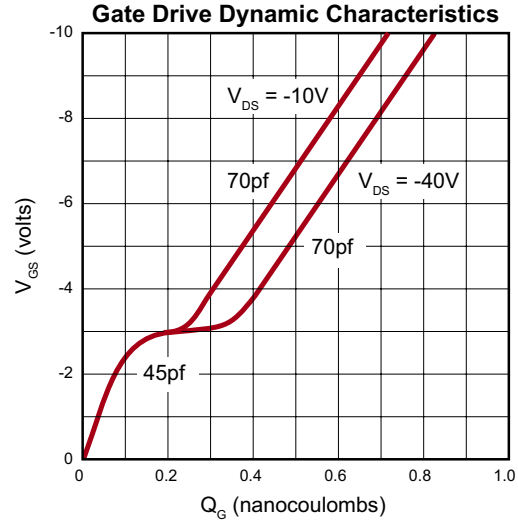
$V_{(th)}$ and R_{DS} Variation with Temperature



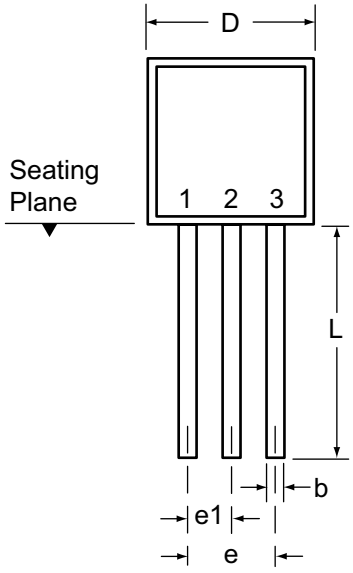
Capacitance vs. Drain-to-Source Voltage



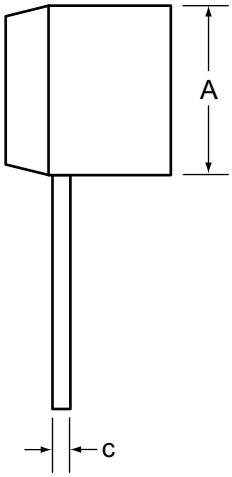
Gate Drive Dynamic Characteristics



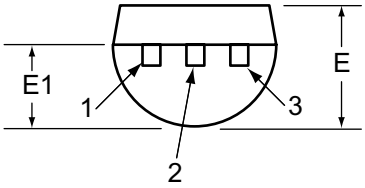
3-Lead TO-92 Package Outline (N3)



Front View



Side View



Bottom View

Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014†	.014†	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022†	.022†	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
***Supertex Doc.#:** DSPD-3TO92N3, Version E041009.*

(The package drawing (s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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