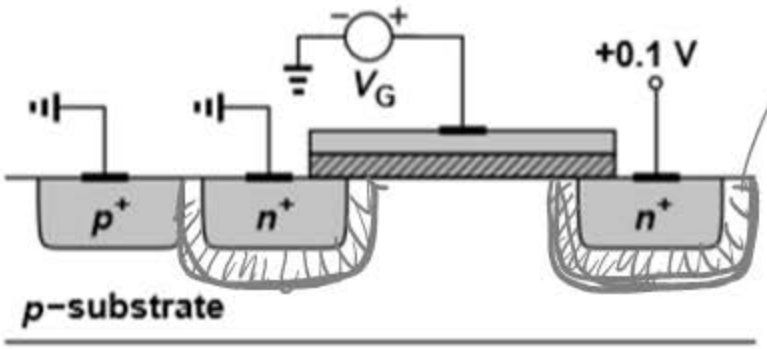
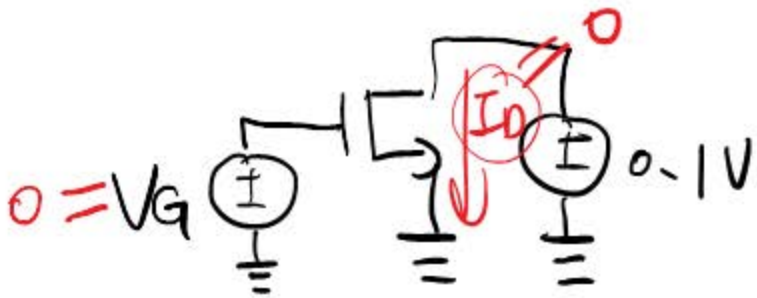
Threshold Voltage (V_{TH}) for NMOS

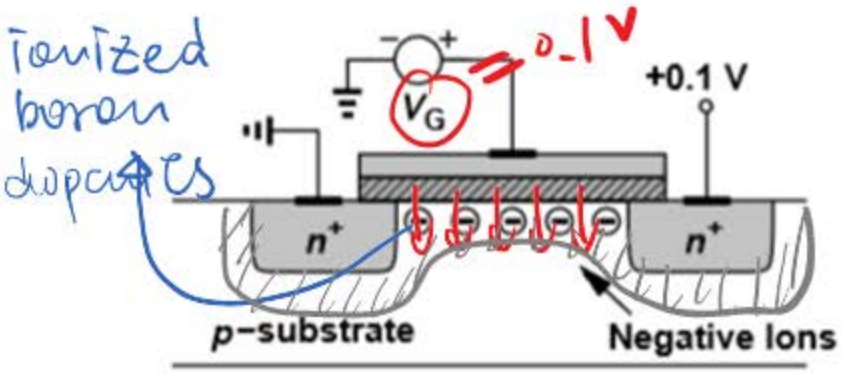


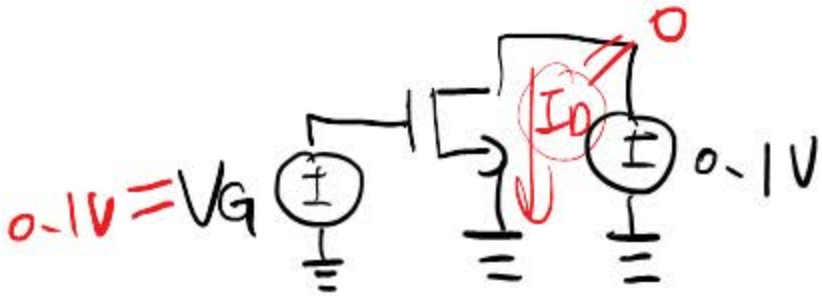
depletion region.

- $V_G = 0$ V
- No current flow



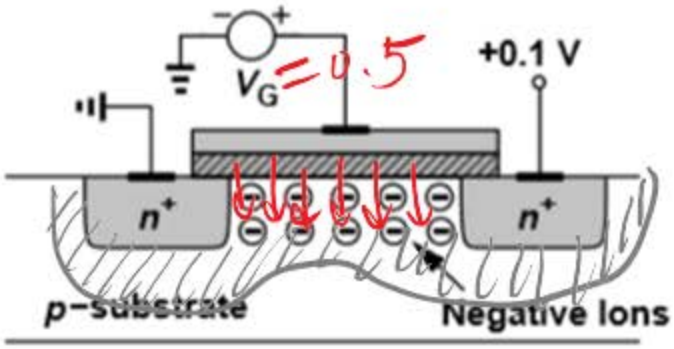
Threshold Voltage (V_{TH}) for NMOS

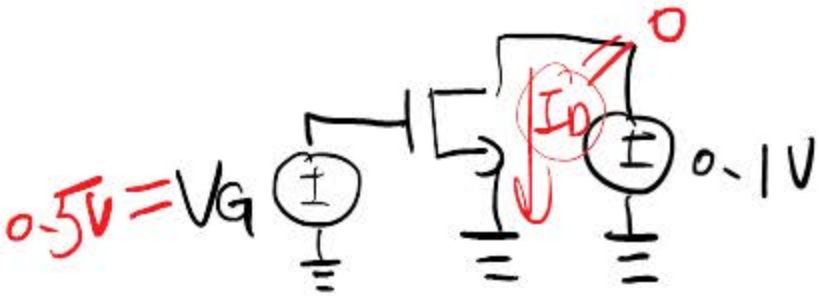




- As V_G increases from zero, holes in *p*-substrate are repelled, leaving negative ions (ionized boron dopants) behind to form a **depletion region**.
- Positive charges are mirrored at the gate.
- No charge carriers (electrons or holes) in the channel, so no current flow.

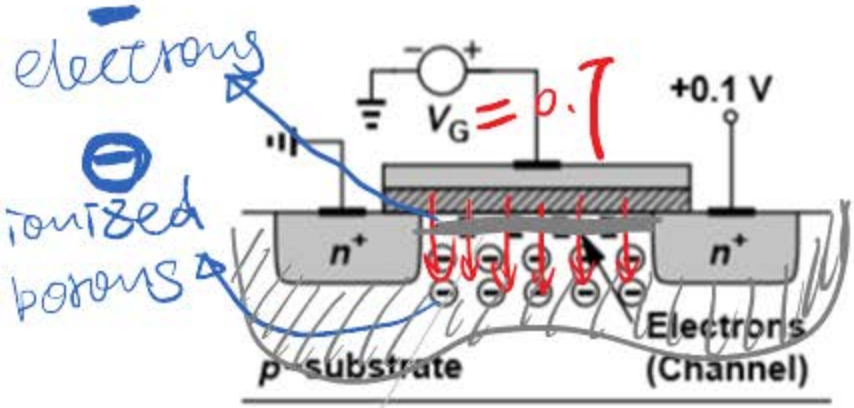
Threshold Voltage (V_{TH}) for NMOS





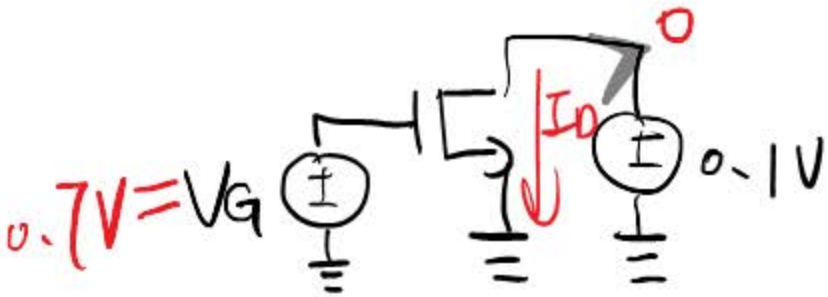
- Higher V_G further increases the width of the **depletion region**.

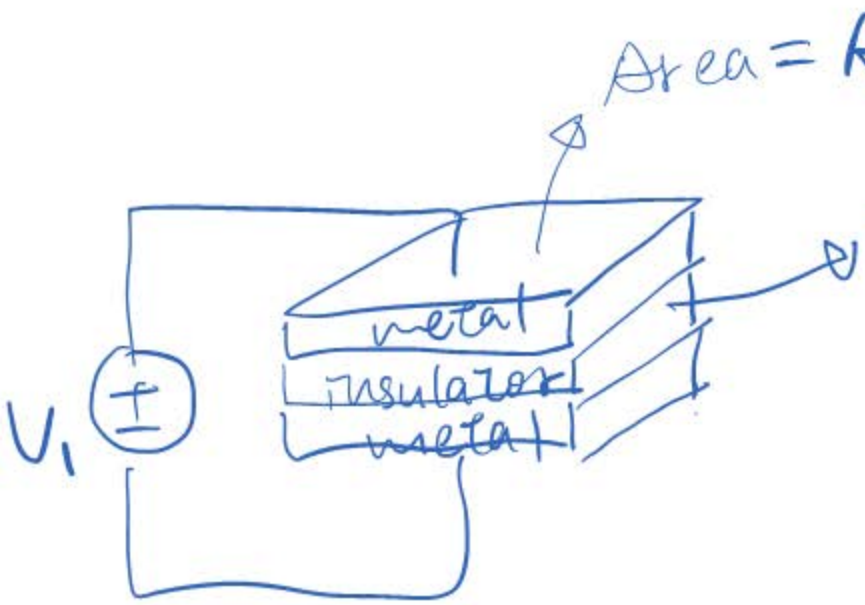
Threshold Voltage (V_{TH}) for NMOS



Interface as n-type as the substrate is p-type

- When V_G reaches a sufficiently positive value, a channel of electrons (**inversion layer**) is formed beneath the gate oxide.
- Electrons flow from "source" to "drain". Equivalently, current flows from "drain" to "source".
- The value of V_G at which the inversion layer forms is the **threshold voltage (V_{TH})**.
- If V_G rises further, the charges in the depletion region remain relatively constant, whereas the charges in the inversion layer increase rapidly.





thickness = t_{ox} (silicon oxide)

$$Q_1 = C V_1$$

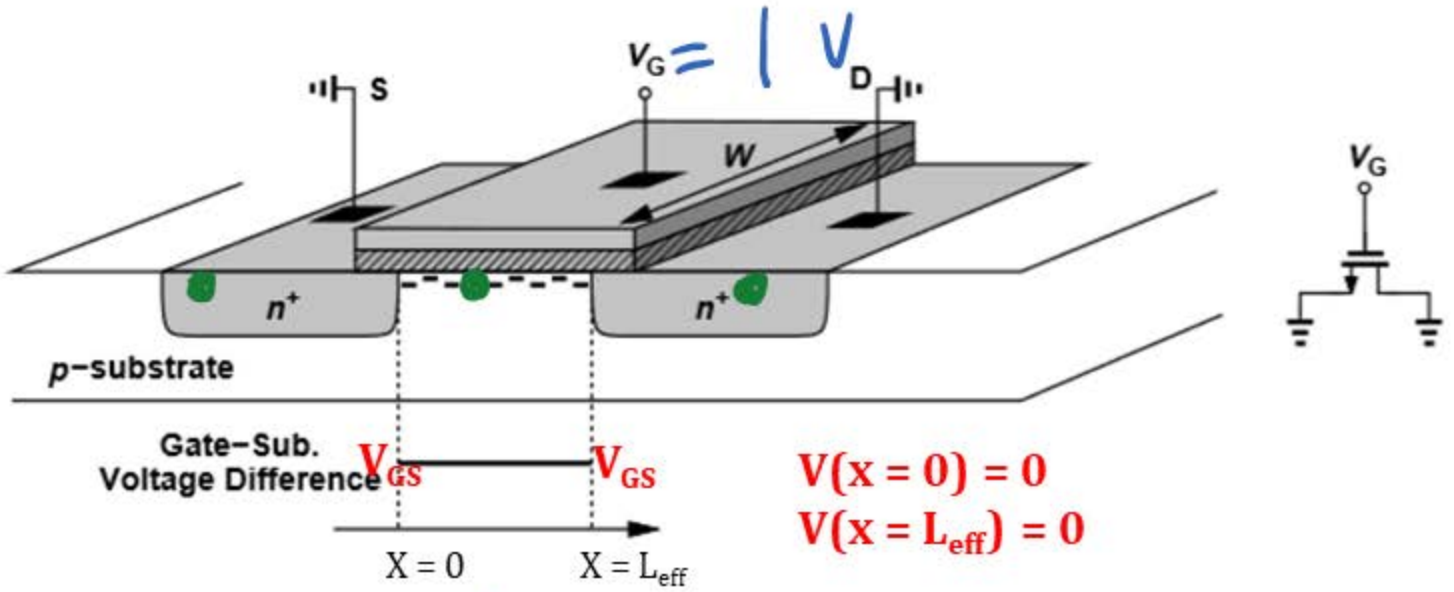
$$= \frac{A(\epsilon_0 \epsilon_r)}{t_{ox}} V_1$$

C_{ox}

ϵ_0: 8.85×10^{-12} F/m

ϵ_r: 3.9

I-V Characteristics for NMOS (Triode)



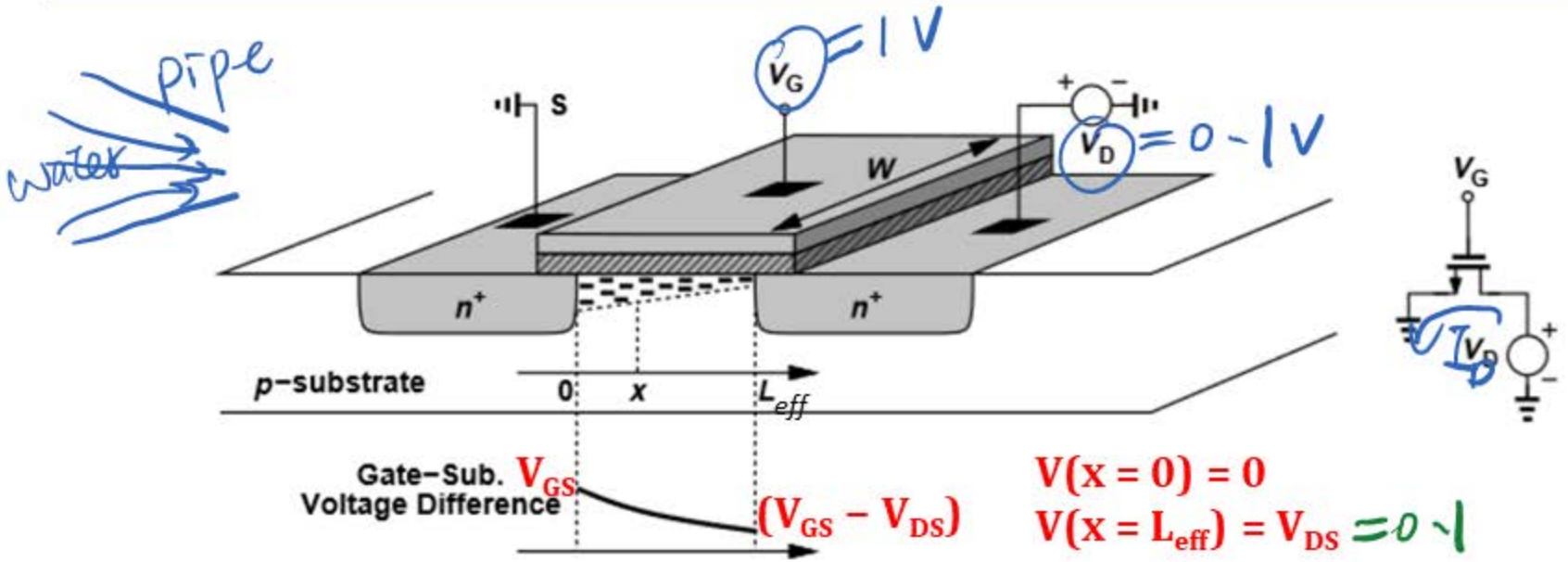
For $V_{GS} \geq V_{TH} = 0.7$ V

$Q = -WL_{eff}C_{ox}(V_{GS} - V_{TH})$ (unit: coulomb)

$Q_d = -WC_{ox}(V_{GS} - V_{TH})$ (unit: coulomb·m^{-1})

C_{ox} (gate oxide capacitance per unit area)
$= \epsilon_{silicon\ oxide} / t_{ox}$
$= [8.85 \times 10^{-12}\ (F/m) \times 3.9] / t_{ox}$ (F/m²)

I-V Characteristics for NMOS (Triode)



$V(x = 0) = 0$

$V(x = L_{eff}) = V_{DS} = 0 - 1$

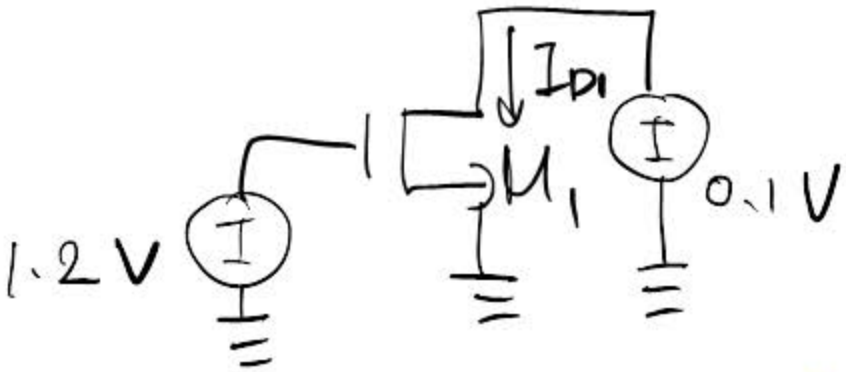
$$I_D = Q_d \times v = Q_d \times (\mu_n \mathcal{E}) = -WC_{ox}[V_{GS} - V_{TH} - V(x)] \times (\mu_n \mathcal{E}) \qquad \mathcal{E} = -dV(x)/dx$$

$$= WC_{ox}[V_{GS} - V_{TH} - V(x)] \times \mu_n \times \frac{dV(x)}{dx}$$

$$\int_{x=0}^{x=L_{eff}} I_D \cdot dx = \int_{V(0)=0}^{V(L)=V_{DS}} \mu_n C_{ox} W[V_{GS} - V_{TH} - V(x)] \cdot dV(x)$$

I_D: constant along channel

$$\boxed{I_D = \mu_n C_{ox} \frac{W}{L_{eff}} \left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]}$$



$$M_1: \frac{20\mu m}{5\mu m} = \frac{W_{drawn}}{L_{drawn}}$$

$$I_{D1} = 350\left(\frac{cm^2}{V \cdot sec}\right) C_{ox}\left[\frac{20\times10^{-6}}{(5\times10^{-6}) - 2(0.08\times10^{-6})}\right]\cdot$$

μm

$$\left[(1.2-0.7)0.1 - \frac{1}{2}0.1^2\right]$$

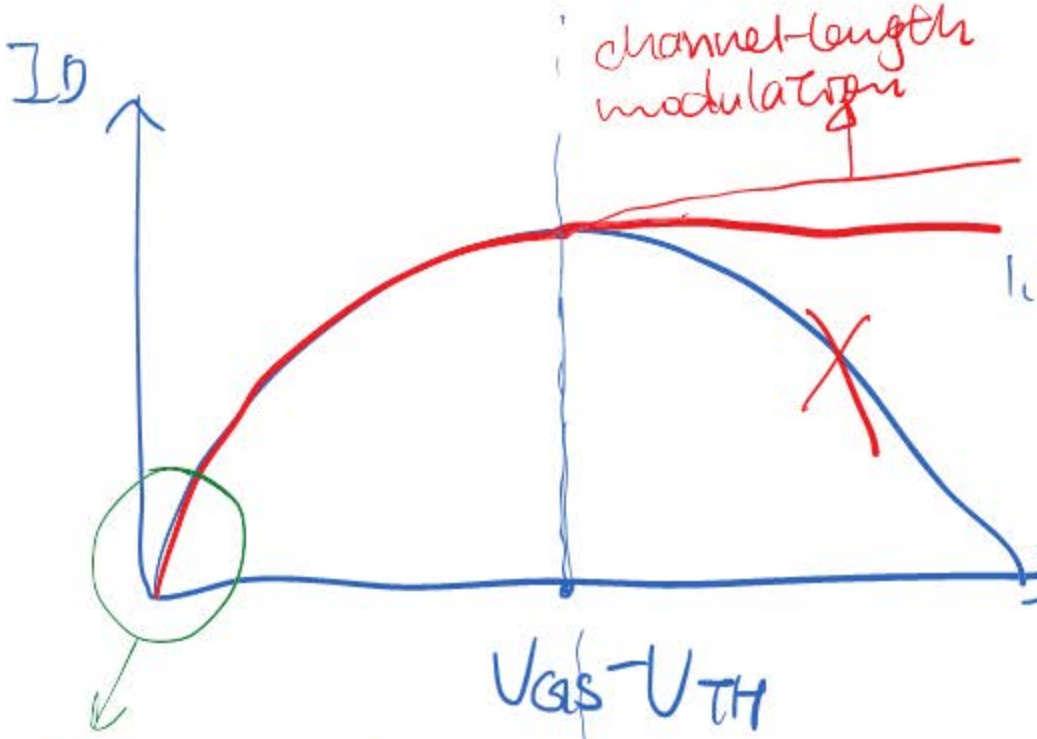
$$\mathbf{I_D = \mu_n C_{ox} \frac{W}{L_{eff}} [(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2]}$$

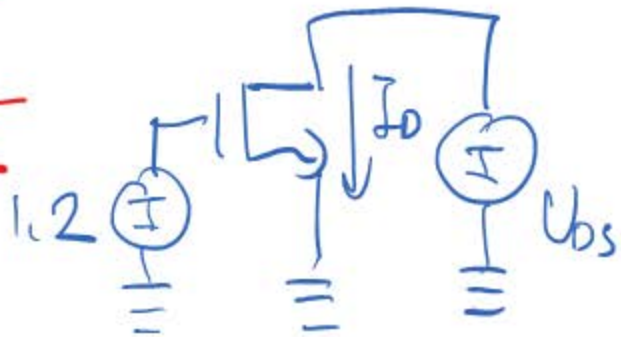
$L_{drawn} - 2LD$

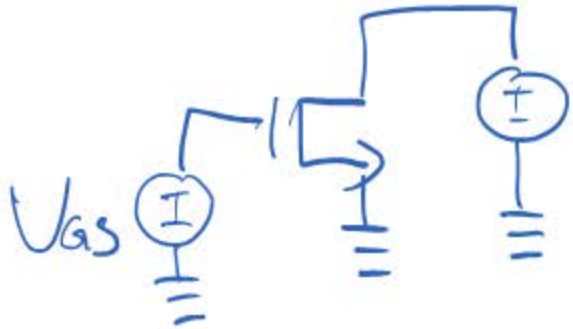
$I_D =$ constant V_{DS} ← can be neglected if V_{DS} small

$$I_D = \mu_n C_{ox} \frac{W}{L_{eff}} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

DC sweep I_D v.s. V_{DS} @ given $V_{GS} > V_{TH}$ (1.2 V)

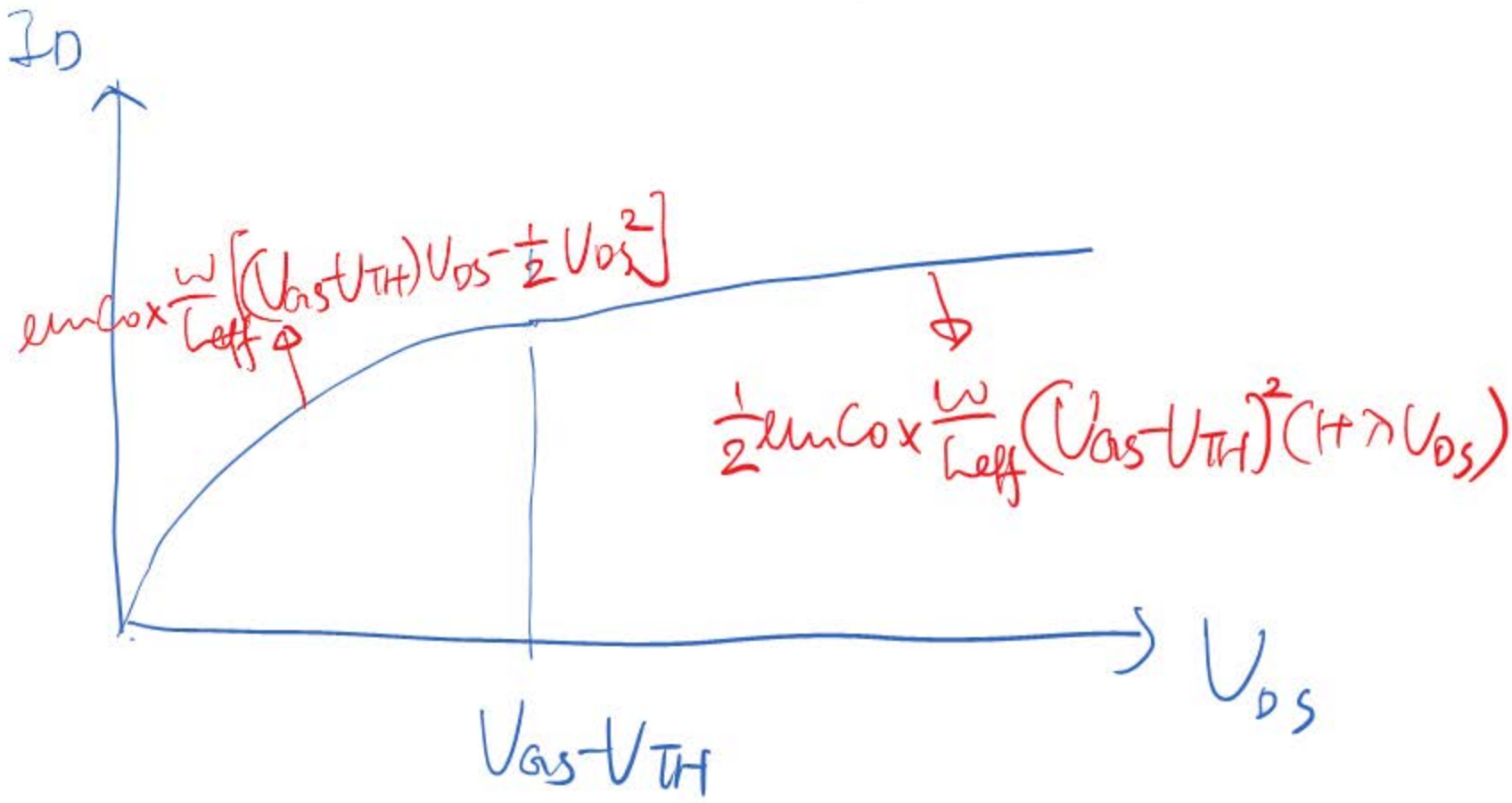






When $V_{GS} > V_{TH}$

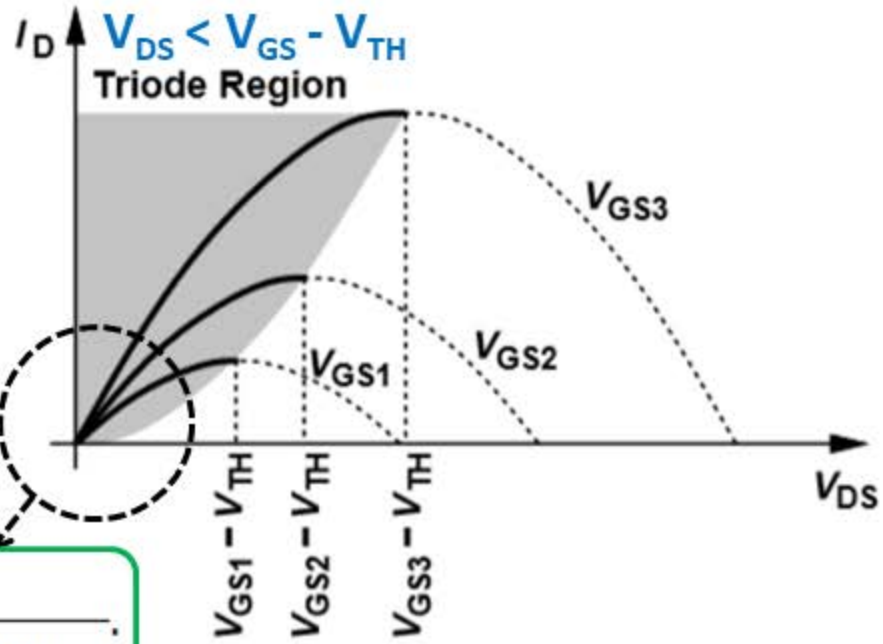
At given V_{GS}



I-V Characteristics for NMOS (Triode)

$$I_D = \mu_n C_{ox} \frac{W}{L_{eff}} [(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2]$$

$$I_{D,max} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L_{eff}} (V_{GS} - V_{TH})^2$$ $V_{DS} = V_{GS} - V_{TH}$

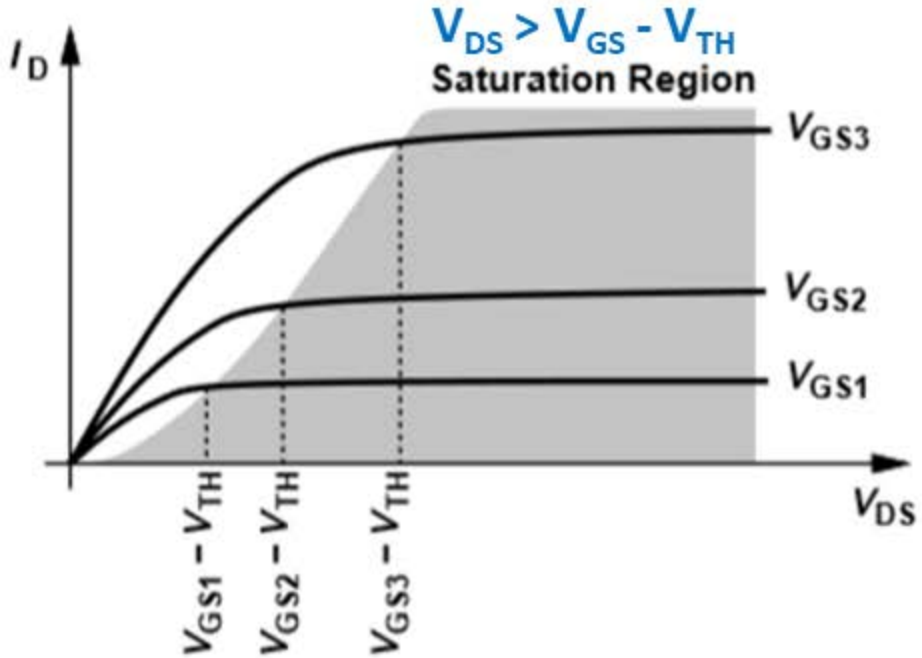


$V_{DS} << 2(V_{GS} - V_{TH})$
Deep triode region

$$R_{on} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L_{eff}}\right)(V_{GS} - V_{TH})}.$$

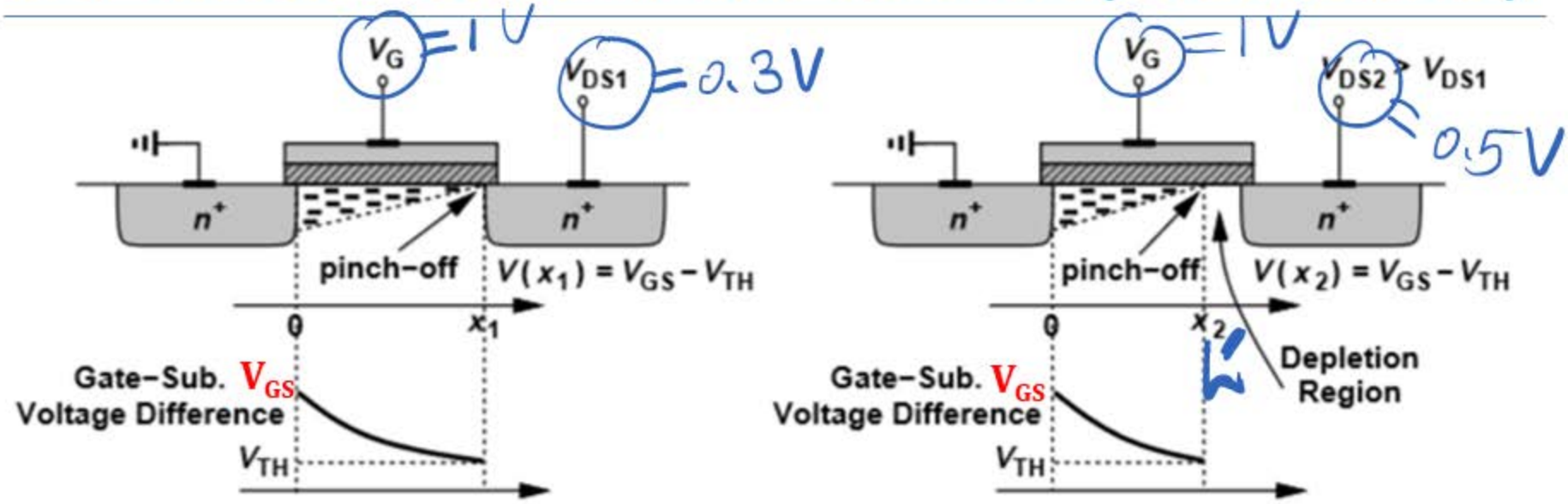
- For digital circuit, MOSFET, as a switch, usually operates in deep triode region.
- This is why reducing t_{ox} and L_{eff} can improve speed.

I-V Characteristics for NMOS (Saturation)



- In reality, for $V_{DS} > V_{GS} - V_{TH}$, I_D becomes relatively constant.
- $V_{DS} = V_{GS} - V_{TH}$ is the minimum value for the NMOS to operate in saturation region.

I-V Characteristics for NMOS (Saturation)



$$\int_{x=0}^{x=L'} I_D \cdot dx = \int_{V(0)=0}^{V(L')=V_{GS}-V_{TH}} \mu_n C_{ox} W[V_{GS} - V_{TH} - V(x)] \cdot dV(x)$$

$$\mathbf{I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L'}(V_{GS} - V_{TH})^2}$$

I_D: constant along channel

L': the point at which Q_d drops to zero

$V_{GS} - V_{TH}$: the overdrive voltage

- Electron velocity ($v = I_D / Q_d$) becomes tremendously high at the pinch off point ($Q_d \rightarrow 0$), such that electrons shoot through the depletion region and arrive at the drain terminal.

Channel-Length Modulation

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L'}(V_{GS} - V_{TH})^2$$

$$L' = L_{eff} - \Delta L$$

$$\frac{1}{L'} = \frac{1}{L_{eff} - \Delta L} = \frac{1}{L_{eff}} \cdot \frac{1}{1 - \frac{\Delta L}{L_{eff}}} \approx \frac{1}{L_{eff}} \cdot \left(1 + \frac{\Delta L}{L_{eff}}\right)$$

small

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L_{eff}}(V_{GS} - V_{TH})^2\left(1 + \frac{\Delta L}{L_{eff}}\right)$$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L_{eff}}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

$\lambda = 0$ means don't consider "channel-length modulation"

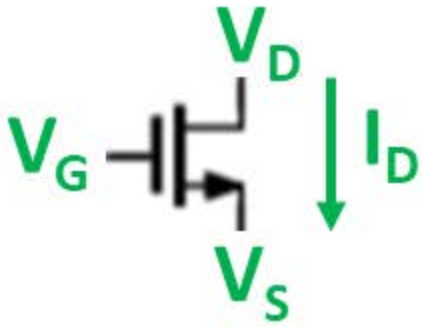
Channel-Length Modulation

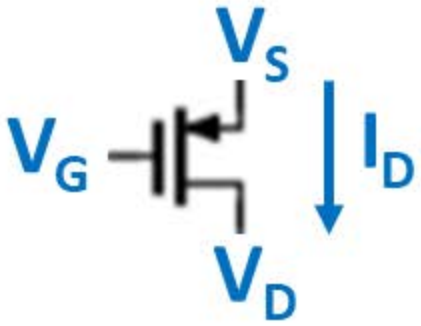
$$\mathbf{r_o} = \frac{\partial V_{DS}}{\partial I_D} = 1 \Big/ \frac{\partial I_D}{\partial V_{DS}}$$

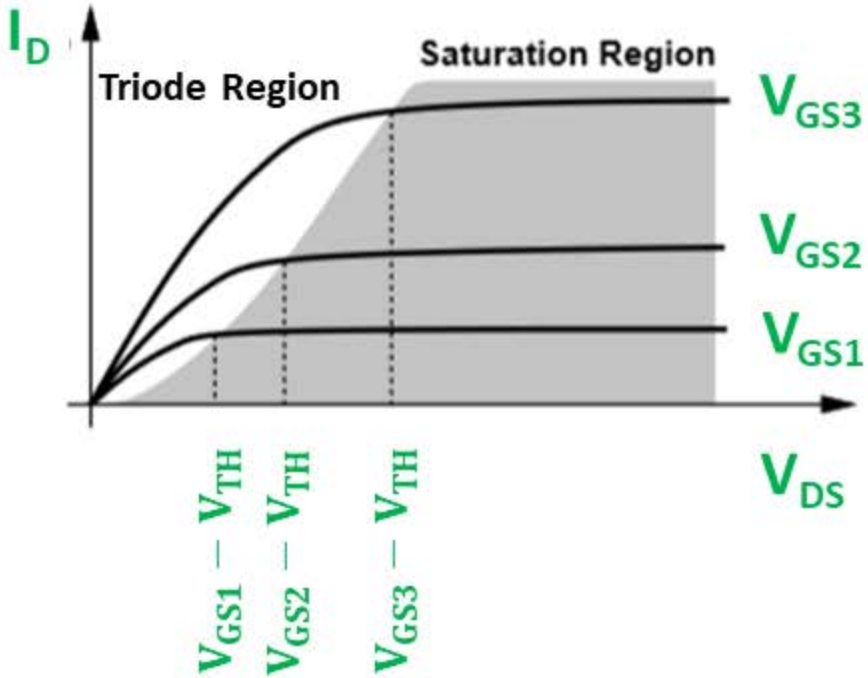
$$= \frac{1}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \cdot \lambda}$$

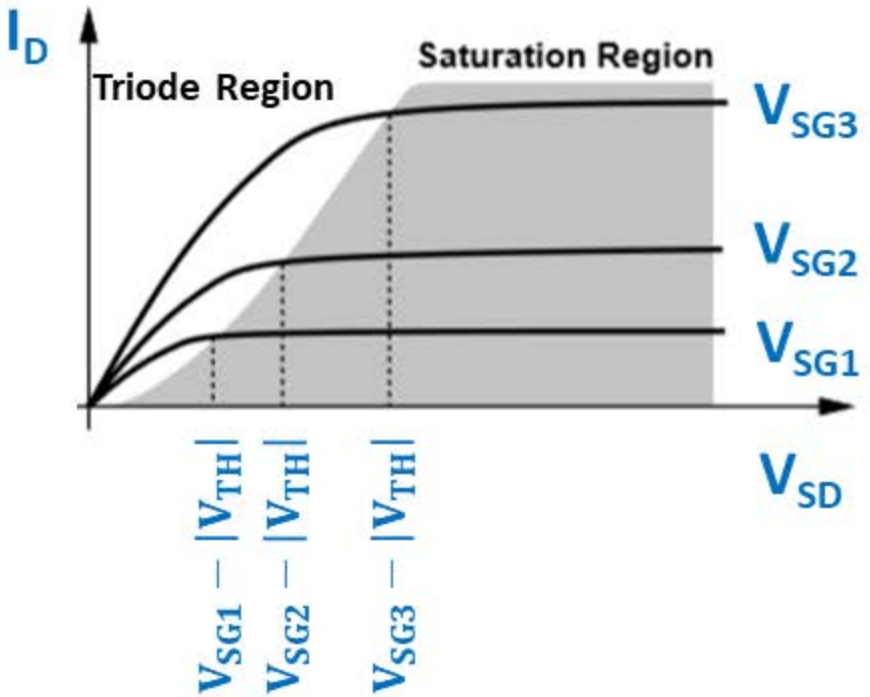
$$\approx \frac{\mathbf{1}}{\mathbf{I_D \cdot \lambda}}$$

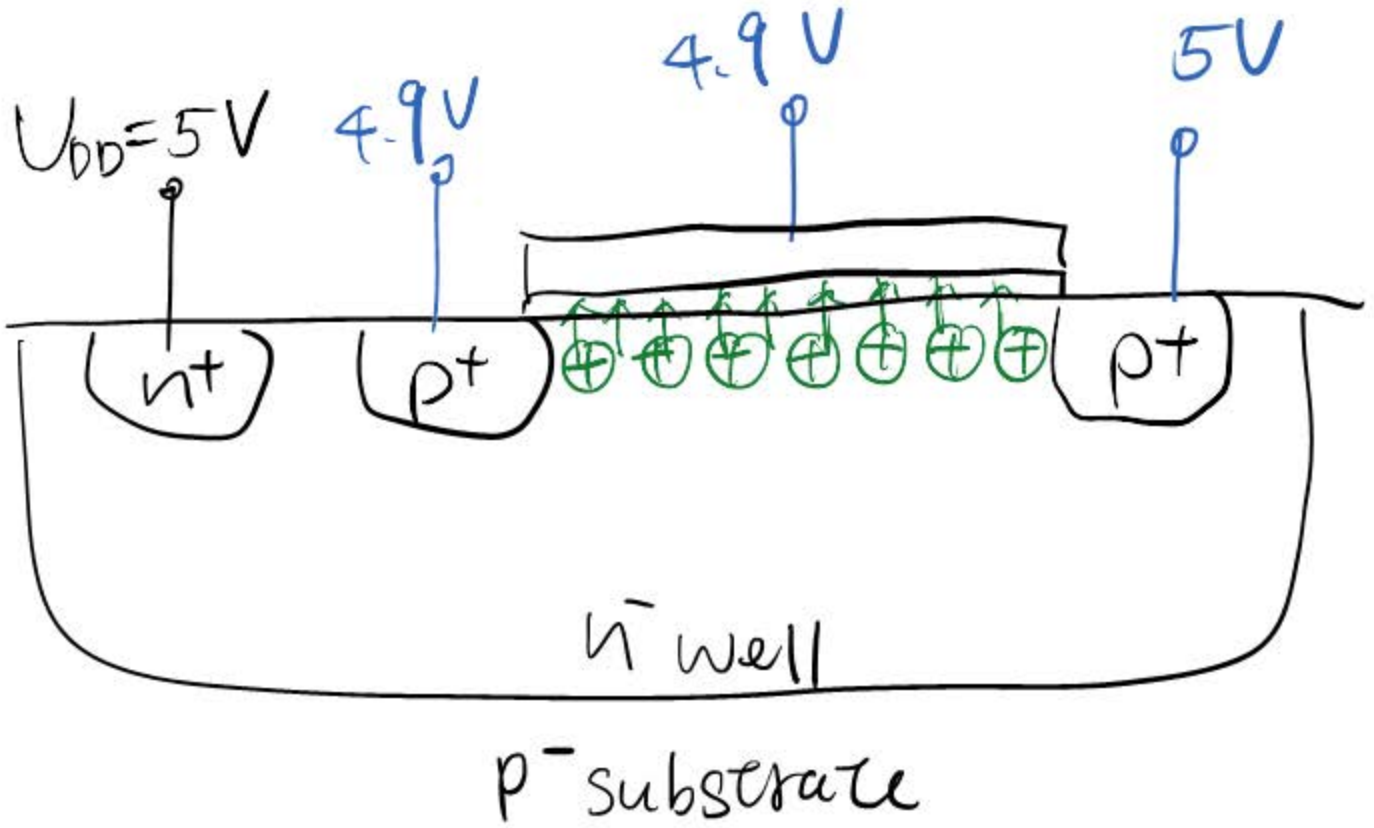
NMOS vs PMOS


V_D
V_G
I_D
V_S


V_S
V_G
I_D
V_D


I_D
Triode Region
Saturation Region
V_{GS3}
V_{GS2}
V_{GS1}
V_{DS}
$V_{GS1} - V_{TH}$
$V_{GS2} - V_{TH}$
$V_{GS3} - V_{TH}$


I_D
Triode Region
Saturation Region
V_{SG3}
V_{SG2}
V_{SG1}
V_{SD}
$V_{SG1} - |V_{TH}|$
$V_{SG2} - |V_{TH}|$
$V_{SG3} - |V_{TH}|$


V_{DD}=5V
4.9V
4.9V
5V
n+
p+
p+
n⁻ well
p⁻ substrate