Fall-2020 UM-SJTU JI Ve311 Homework #4

Instructor: Dr. Chang-Ching Tu

Due: 11:59 am, October 21, 2020 (Wednesday)

Note:

(1) Please use A4 size papers.

(2) Please use the SPICE model on page 3 for simulation and calculation.

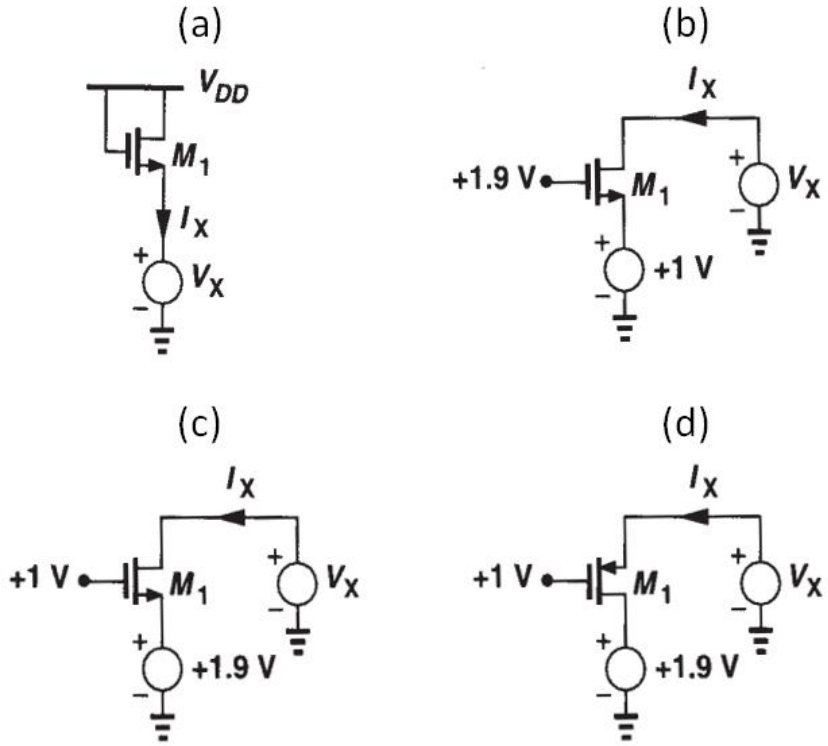
1. [MOSFET DC Biasing, 60%] Don't consider channel-length modulation and body effect. Use the drain current equations below. Assuming W_{drawn} / L_{drawn} = 20 μm / 2 μm, sketch I_X of M_1 as a function of V_X increasing from 0 V to V_{DD} = 5 V. (Note: finish this part before the midterm exam)

$$I_D = \mu_n C_{ox} \frac{W}{L_{eff}} [(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2] \text{ (NMOS in triode region)}$$

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L_{eff}} (V_{GS} - V_{TH})^2 \text{ (NMOS in saturation region)}$$

$$I_D = \mu_p C_{ox} \frac{W}{L_{eff}} [(V_{SG} - |V_{TH}|)V_{SD} - \frac{1}{2}V_{SD}^2] \text{ (PMOS in triode region)}$$

$$I_D = \frac{1}{2}\mu_p C_{ox} \frac{W}{L_{eff}} (V_{SG} - |V_{TH}|)^2 \text{ (PMOS in saturation region)}$$



2. [MOSFET Small-Signal Model] Assume W_{drawn} / L_{drawn} = 20 μm / 2 μm.
   (a) [20%] Use Pspice to plot the drain current of a NMOS as a function of V_{DS} increasing from 0 V to 5 V, at V_{GS} = 1 V, 1.5 V and 2 V. Label the off, triode and saturation regions for each curve. Derive r_o from each curve in the saturation region and compare it with hand-calculation result.
   (b) [20%] Use Pspice to plot the drain current of a NMOS as a function of V_{GS} increasing from 0 V to 3 V, at V_{DS} = 5 V. Derive gm from the curve when V_{GS} = 2 V and compare it with hand-calculation result.

NMOS Model			
LEVEL = 1	**VTO = 0.7**	**GAMMA = 0.45**	**PHI = 0.9**
NSUB = 9e+14	**LD = 0.08e−6**	**UO = 350**	**LAMBDA = 0.1**
TOX = 9e−9	**PB = 0.9**	**CJ = 0.56e−3**	**CJSW = 0.35e−11**
MJ = 0.45	**MJSW = 0.2**	**CGDO = 0.4e−9**	**JS = 1.0e−8**
PMOS Model			
LEVEL = 1	**VTO = −0.8**	**GAMMA = 0.4**	**PHI = 0.8**
NSUB = 5e+14	**LD = 0.09e−6**	**UO = 100**	**LAMBDA = 0.2**
TOX = 9e−9	**PB = 0.9**	**CJ = 0.94e−3**	**CJSW = 0.32e−11**
MJ = 0.5	**MJSW = 0.3**	**CGDO = 0.3e−9**	**JS = 0.5e−8**

VTO: threshold voltage with zero V_{SB} (unit: V)
GAMMA: body effect coefficient (unit: $V^{1/2}$)
PHI: $2\Phi_F$ (unit: V)
TOX: gate oxide thickness (unit: m)
NSUB: substrate doping (unit: cm^{-3})
LD: source/drain side diffusion (unit: m)
UO: channel mobility (unit: $cm^2/V/s$)
LAMBDA: channel-length modulation coefficient (unit: V^{-1})
CJ: source/drain bottom-plate junction capacitance per unit area (unit: F/m^2)
CJSW: source/drain sidewall junction capacitance per unit length (unit: F/m)
PB: source/drain junction built-in potential (unit: V)
MJ: exponent in CJ equation (unitless)
MJSW: exponent in CJSW equation (unitless)
CGDO: gate-drain overlap capacitance per unit width (unit: F/m)
CGSO: gate-source overlap capacitance per unit width (unit: F/m)
JS: source/drain leakage current per unit area (unit: A/m^2)

Vacuum permittivity (ϵ_o) $= 8.85 \times 10^{-12}$ (F / m)
Silicon oxide dielectric constant (ϵ_r) $= 3.9$