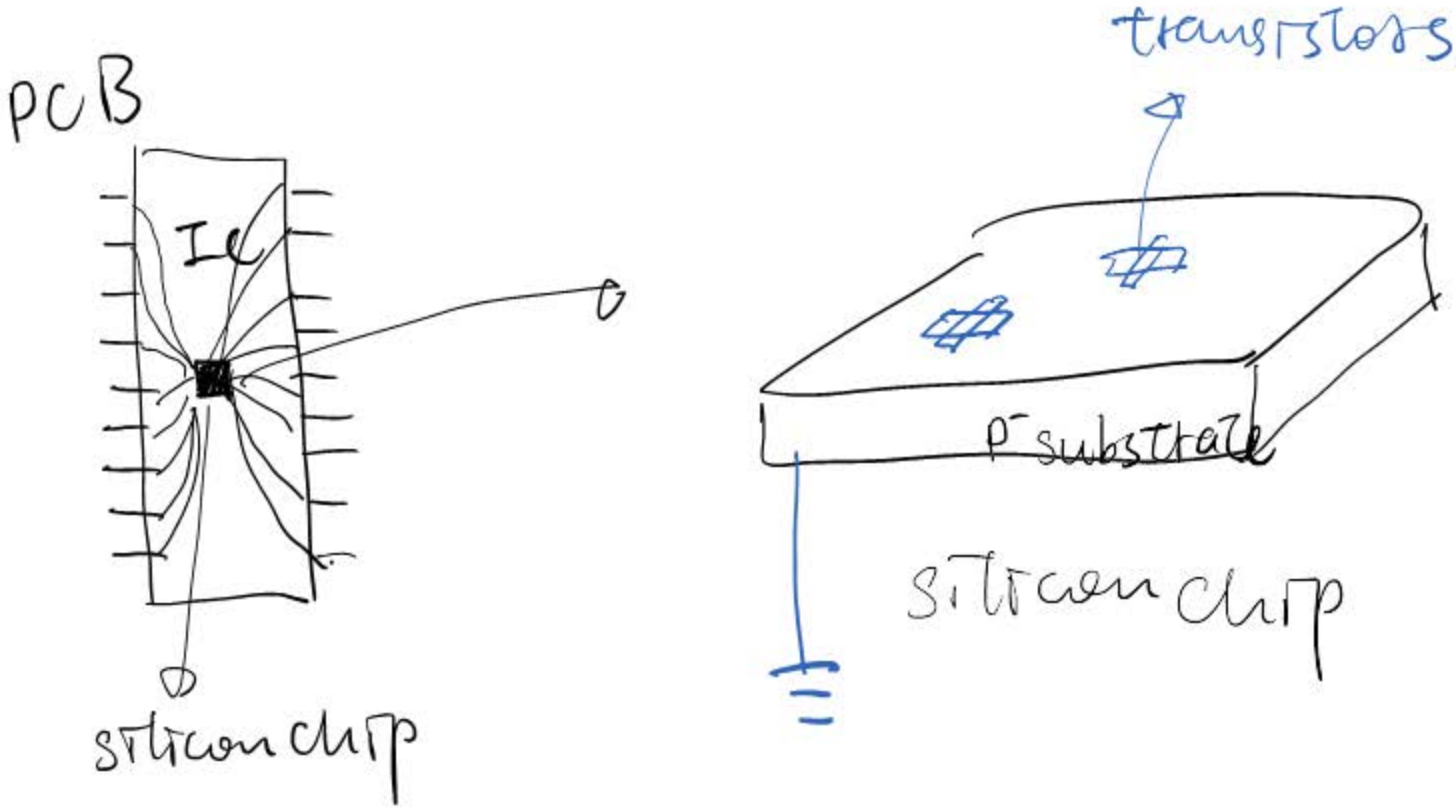
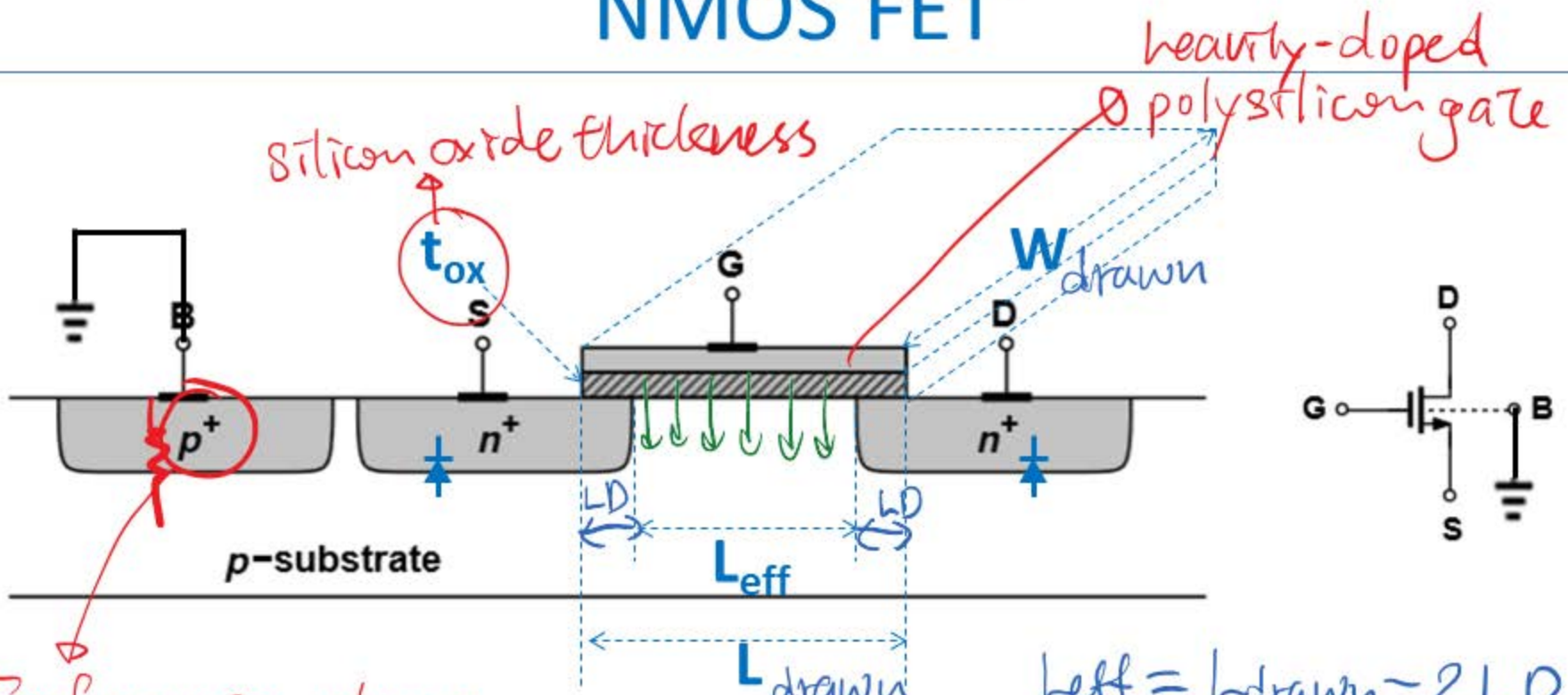

PCB
IC
silicon chip
transistors.
P- substrate
silicon chip

NMOS FET



- MOS = Metal-Oxide-Semiconductor
- FET = Field effect Transistor
- CMOS Technology keeps on reducing t_{ox} and L_{eff} (Moore's Law).
- Substrate (Body) of NMOS is generally connected to ground.
- See Chapter 17 for the introduction of CMOS fabrication technology.

Latest: TSMC 5 nm FinFET Technology

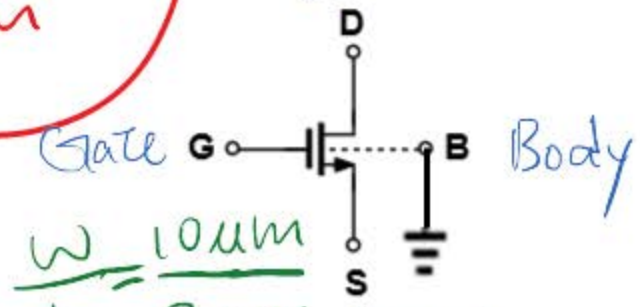
CMOS

Schematic Design

NMOS

Diam

PMOS



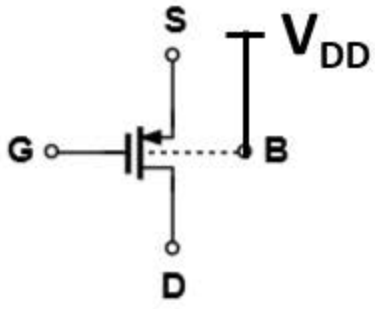
Gate

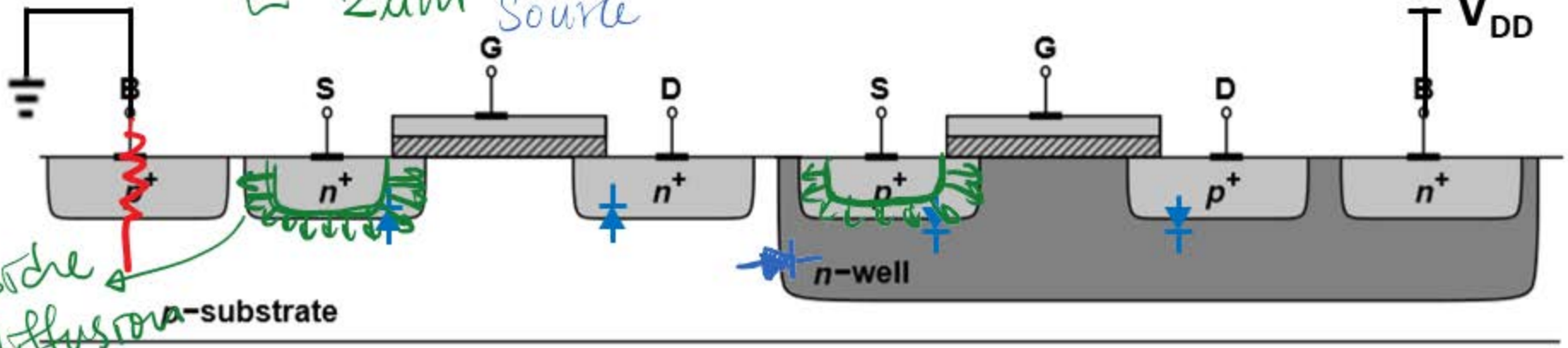
Body

W = 10um

L = 2um

Source





Side diffusion

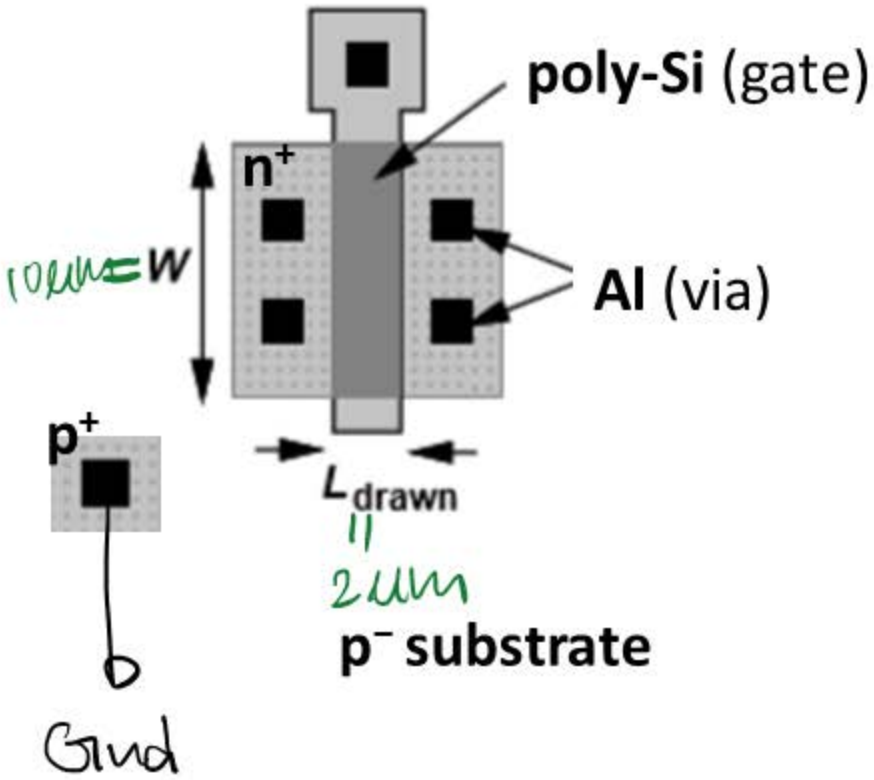
NMOS and PMOS can share one p^--Sub.

- CMOS = Complementary MOS (a fabrication technology)
- Substrate (Body) of NMOS is generally connected to ground.
- N-well (Body) of PMOS is generally connected to V_{DD}.

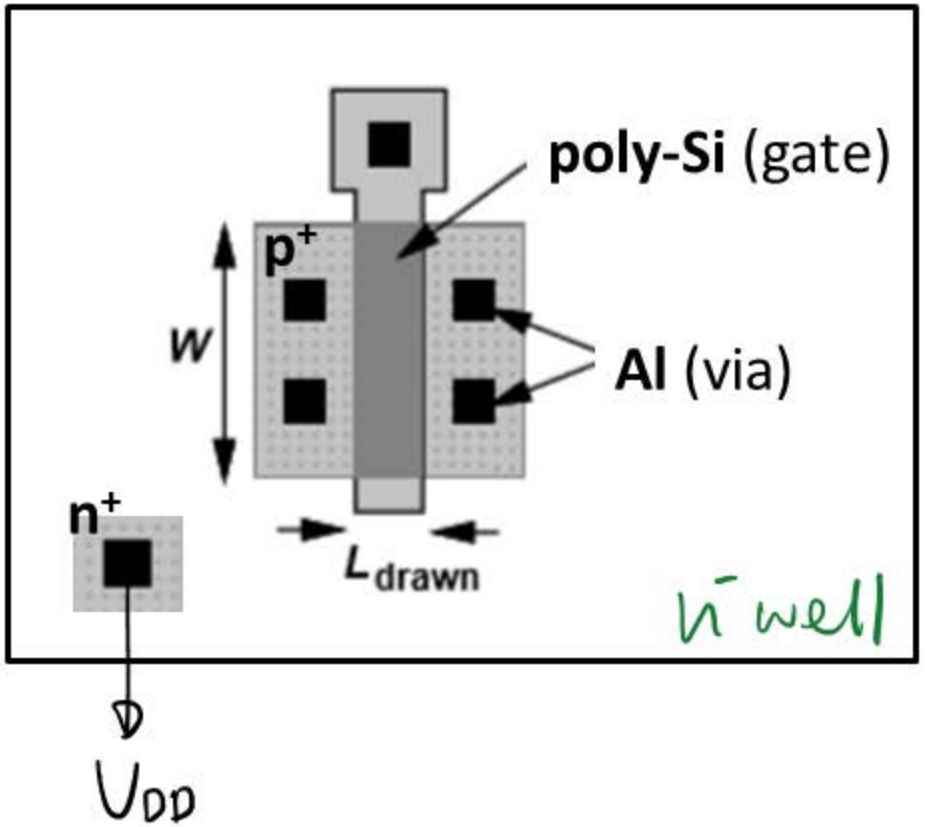
Layout

Layout Design

NMOS

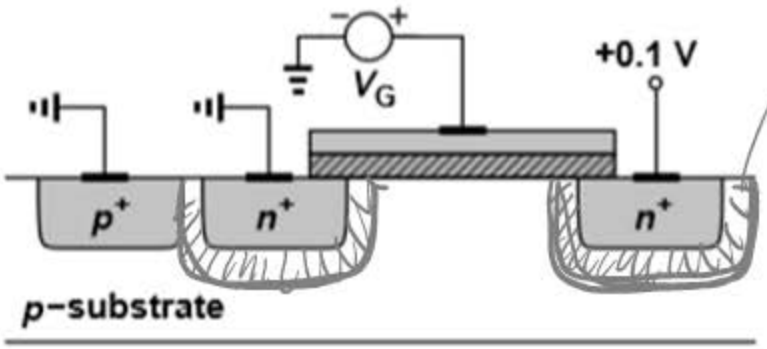


PMOS

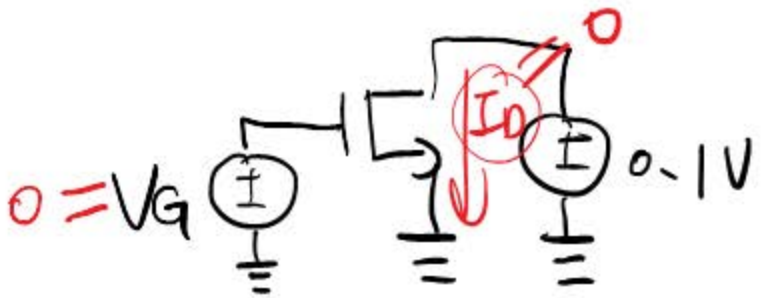


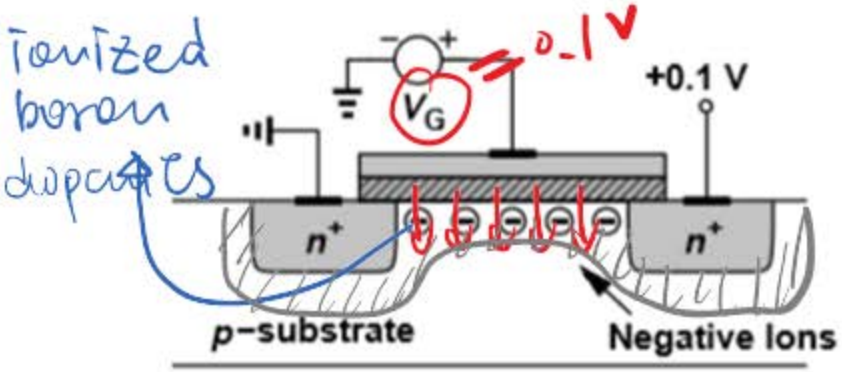
$$L_{eff} = L_{drawn} - 2LD = (2\times10^{-6}) - 2(0.08\times10^{-6})$$

Threshold Voltage (V_{TH}) for NMOS

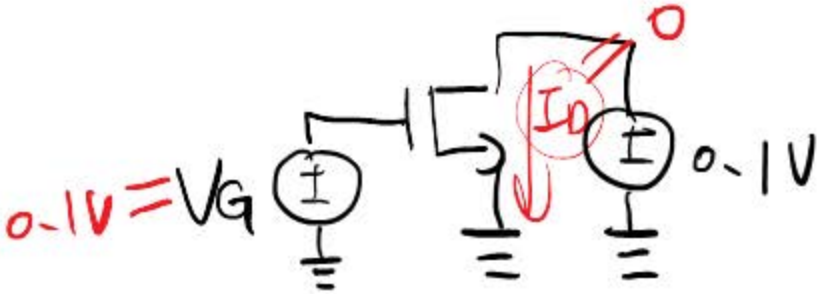


- $V_G = 0$ V
- No current flow

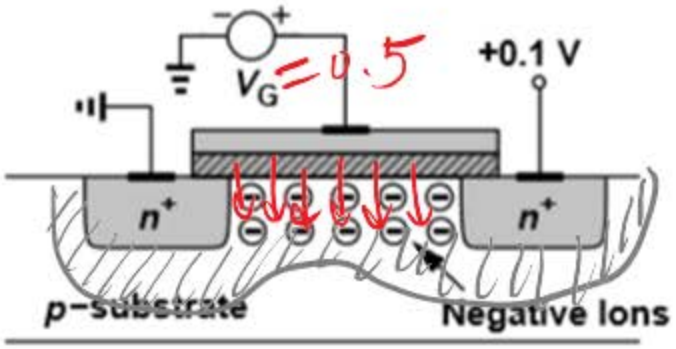


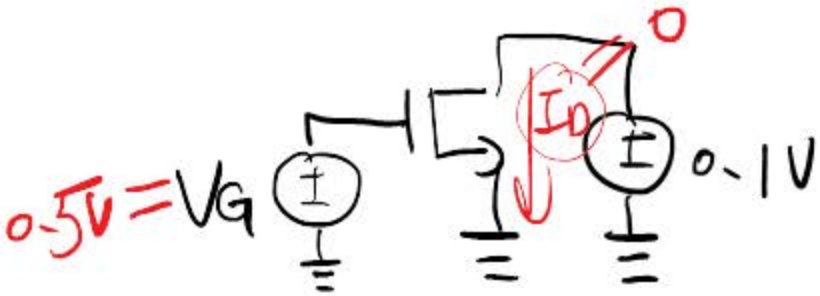


- As V_G increases from zero, holes in *p*-substrate are repelled, leaving negative ions (ionized boron dopants) behind to form a **depletion region**.
- Positive charges are mirrored at the gate.
- No charge carriers (electrons or holes) in the channel, so no current flow.



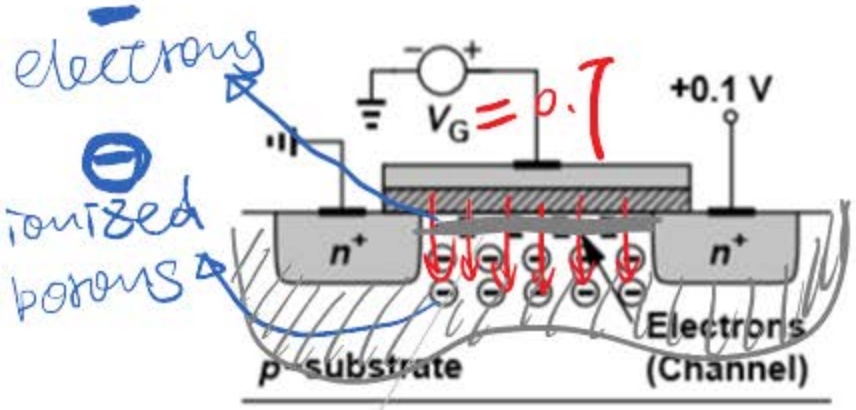
Threshold Voltage (V_{TH}) for NMOS



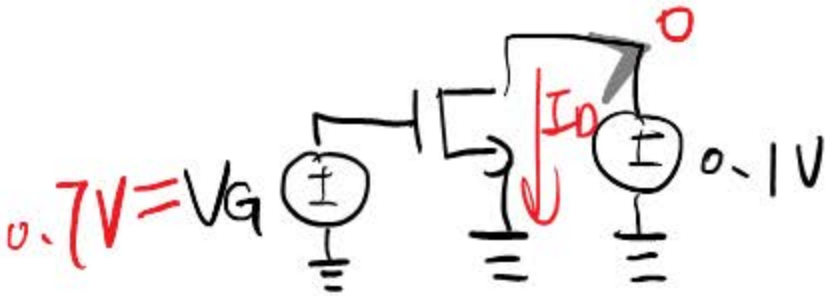


- Higher V_G further increases the width of the **depletion region**.

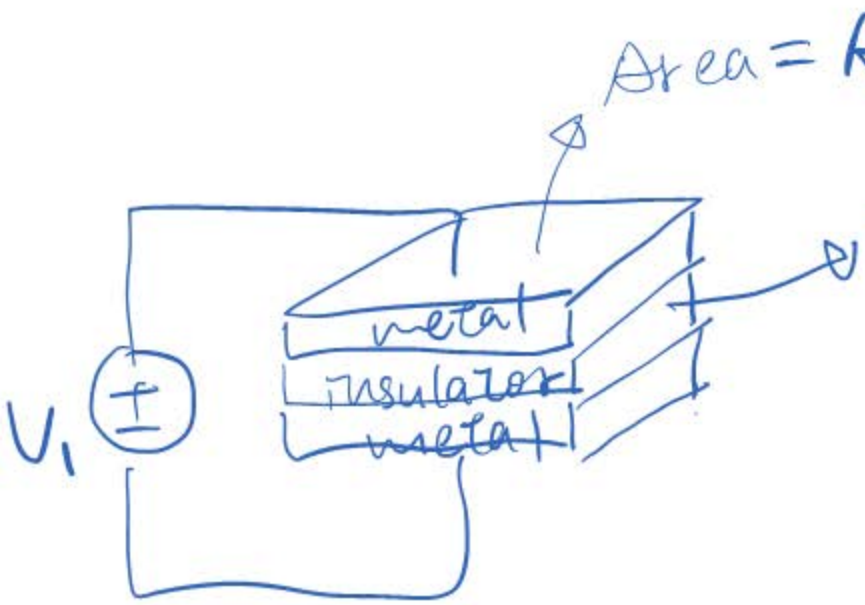
Threshold Voltage (V_{TH}) for NMOS



Interface as n-type as the substrate is p-type



- When V_G reaches a sufficiently positive value, a channel of electrons (**inversion layer**) is formed beneath the gate oxide.
- Electrons flow from "source" to "drain". Equivalently, current flows from "drain" to "source".
- The value of V_G at which the inversion layer forms is the **threshold voltage (V_{TH})**.
- If V_G rises further, the charges in the depletion region remain relatively constant, whereas the charges in the inversion layer increase rapidly.



thickness = t_{ox} (silicon oxide)

$$Q_1 = C V_1$$

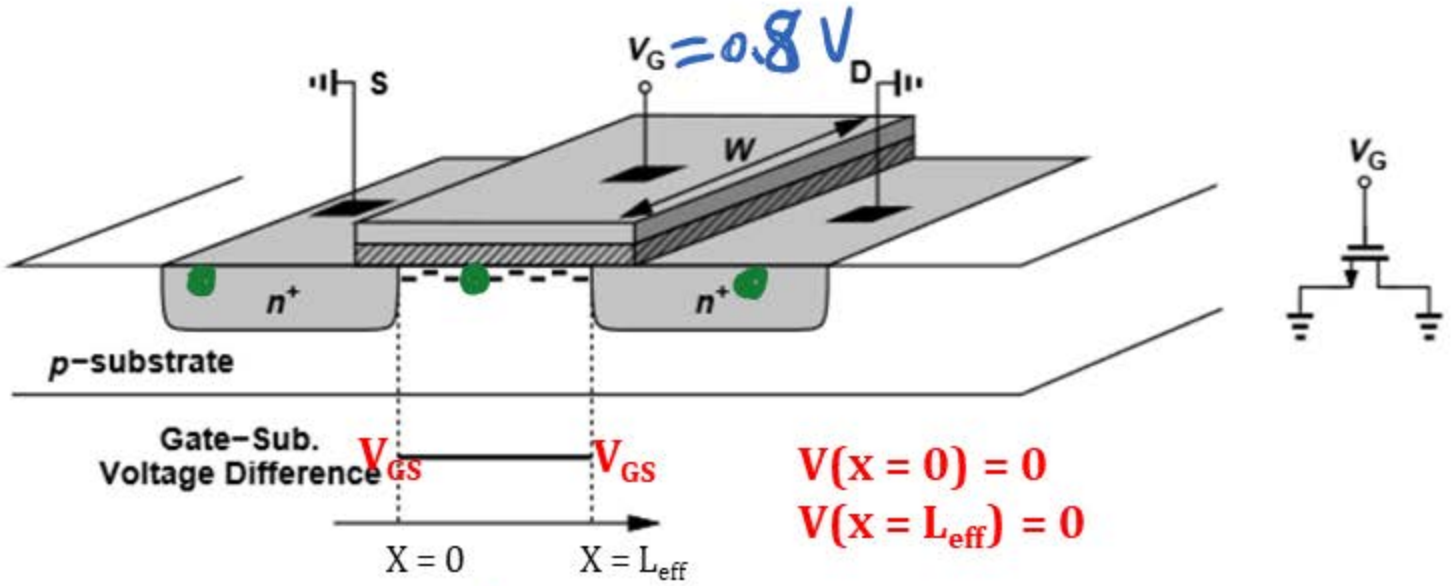
$$= \frac{A(\epsilon_0 \epsilon_r)}{t_{ox}} V_1$$

C_{ox}

ϵ_0: 8.85×10^{-12} F/m

ϵ_r: 3.9

I-V Characteristics for NMOS (Triode)



For $V_{GS} \geq V_{TH} = 0.7\,V$

$Q = -WL_{eff}C_{ox}(V_{GS} - V_{TH})$ (unit: coulomb)

$Q_d = -WC_{ox}(V_{GS} - V_{TH})$ (unit: coulomb·m^{-1})

C_{ox} (gate oxide capacitance per unit area)
$= \epsilon_{silicon\ oxide} / t_{ox}$
$= [8.85 \times 10^{-12}\ (F/m) \times 3.9] / t_{ox}$