Summer-2020 UM-SJTU JI Ve311 Final

Instructor: Dr. Chang-Ching Tu

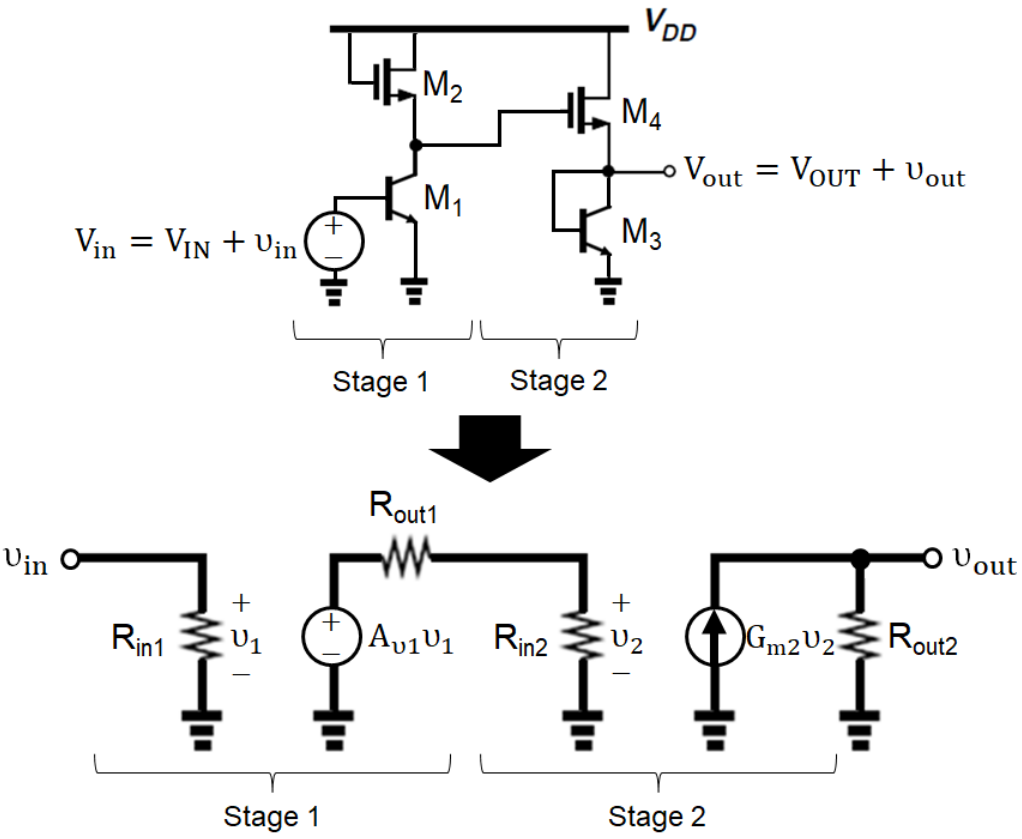
Due: August 05, 2020 (Wednesday) in class

Note:

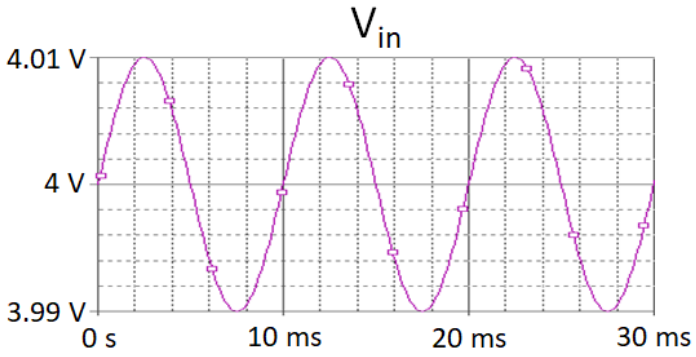
(1) Please write your answer on A4- or Letter-size papers.

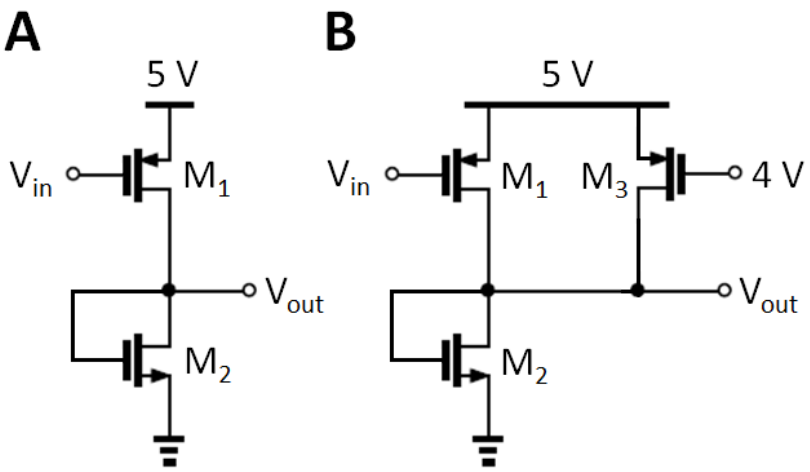
(2) One A4- or Letter-size double-sided paper of notes is allowed.

1. [Small-Signal Equivalent Circuit, 30%] Assume M_1 and M_3 operate in the forward-active region and M_2 and M_4 operate in the saturation region. ***Take Early Effect, Channel-Length Modulation and Body Effect into consideration.*** Derive the analytical expressions of R_{in1} [5%], R_{out1} [5%], A_{v1} [5%], R_{in2} [5%], R_{out2} [5%] and G_{m2} [5%].

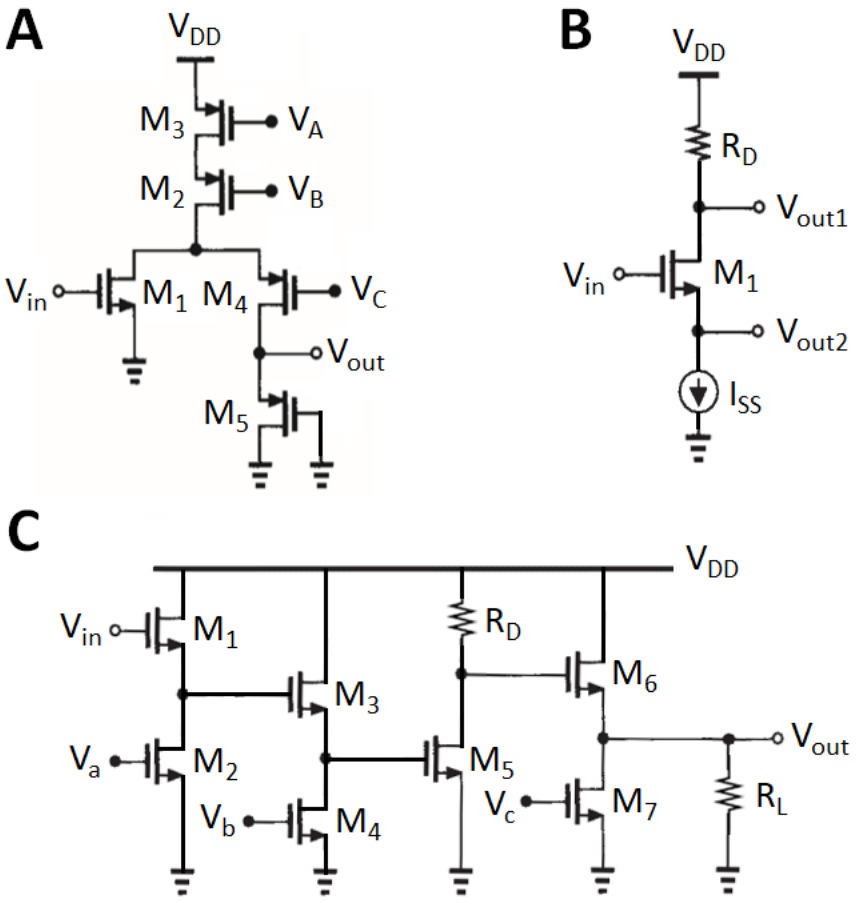


2. [Common-Source with Diode-Connected Load, 30%] Assume $\lambda = \gamma = 0$.
   A. [15%] $(W_{drawn}/L_{drawn})_1$ = 100 µm/2.18 µm and $(W_{drawn}/L_{drawn})_2$ = 1 µm/5.16 µm. Draw the waveform of V_{out}.
   B. [15%] For circuit B, $(W_{drawn}/L_{drawn})_1$ = $(W_{drawn}/L_{drawn})_3$ = 50 µm/2.18 µm and $(W_{drawn}/L_{drawn})_2$ = 1 µm/5.16 µm. Draw the waveform of V_{out}.

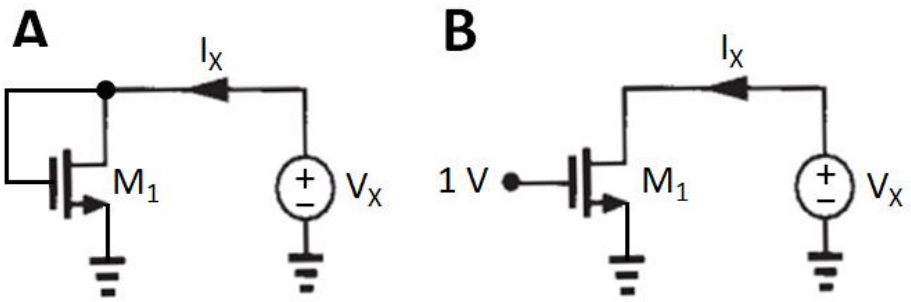




3. [Small-Signal Analysis, 21%] Assume all transistors operate in saturation. All answers in analytical expressions.
   A. [7%] ($\lambda = 0$ and $\gamma = 0$) V_A, V_B and V_C are DC biasing voltages. Derive the voltage gain, $A_\upsilon = \frac{\upsilon_{out}}{\upsilon_{in}}$.
   B. [3% and 4%] ($\lambda \neq 0$ and $\gamma \neq 0$) I_{SS} is ideal current source. Derive the voltage gains, $A_{\upsilon 1} = \frac{\upsilon_{out1}}{\upsilon_{in}}$ and $A_{\upsilon 2} = \frac{\upsilon_{out2}}{\upsilon_{in}}$.
   C. [7%] ($\lambda = 0$ and $\gamma = 0$) V_a, V_b and V_c are DC biasing voltages. Derive the voltage gain, $A_\upsilon = \frac{\upsilon_{out}}{\upsilon_{in}}$.



4. [Diode-Connected Load, 9%, and Current Source Load, 10%] Assume $\lambda \neq 0$ and $\gamma \neq 0$. The size of M_1 is $W_{drawn}/L_{drawn} = 20\ \mu m/2.16\ \mu m$. Plot I_X versus V_X increasing from 0 V to 3 V.



NMOS Model			
LEVEL = 1	**VTO = 0.7**	**GAMMA = 0.45**	**PHI = 0.9**
NSUB = 9e+14	**LD = 0.08e−6**	**UO = 350**	**LAMBDA = 0.1**
TOX = 9e−9	**PB = 0.9**	**CJ = 0.56e−3**	**CJSW = 0.35e−11**
MJ = 0.45	**MJSW = 0.2**	**CGDO = 0.4e−9**	**JS = 1.0e−8**
PMOS Model			
LEVEL = 1	**VTO = −0.8**	**GAMMA = 0.4**	**PHI = 0.8**
NSUB = 5e+14	**LD = 0.09e−6**	**UO = 100**	**LAMBDA = 0.2**
TOX = 9e−9	**PB = 0.9**	**CJ = 0.94e−3**	**CJSW = 0.32e−11**
MJ = 0.5	**MJSW = 0.3**	**CGDO = 0.3e−9**	**JS = 0.5e−8**

VTO: threshold voltage with zero V_{SB} (unit: V)
GAMMA: body effect coefficient (unit: $V^{1/2}$)
PHI: $2\Phi_F$ (unit: V)
TOX: gate oxide thickness (unit: m)
NSUB: substrate doping (unit: cm^{-3})
LD: source/drain side diffusion (unit: m)
UO: channel mobility (unit: $cm^2/V/s$)
LAMBDA: channel-length modulation coefficient (unit: V^{-1})
CJ: source/drain bottom-plate junction capacitance per unit area (unit: F/m^2)
CJSW: source/drain sidewall junction capacitance per unit length (unit: F/m)
PB: source/drain junction built-in potential (unit: V)
MJ: exponent in CJ equation (unitless)
MJSW: exponent in CJSW equation (unitless)
CGDO: gate-drain overlap capacitance per unit width (unit: F/m)
CGSO: gate-source overlap capacitance per unit width (unit: F/m)
JS: source/drain leakage current per unit area (unit: A/m^2)

Vacuum permittivity (ϵ_o) $= 8.85 \times 10^{-12}$ (F / m)
Silicon oxide dielectric constant (ϵ_r) $= 3.9$

In case you cannot upload your pdf file to Canvas, please email it or send WeChat photo to TA immediately. Thanks.

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