JOINT INSTITUTE

交大密西根学院

FET

Ve311 Electronic Circuits (Fall 2020)

Dr. Chang-Ching Tu

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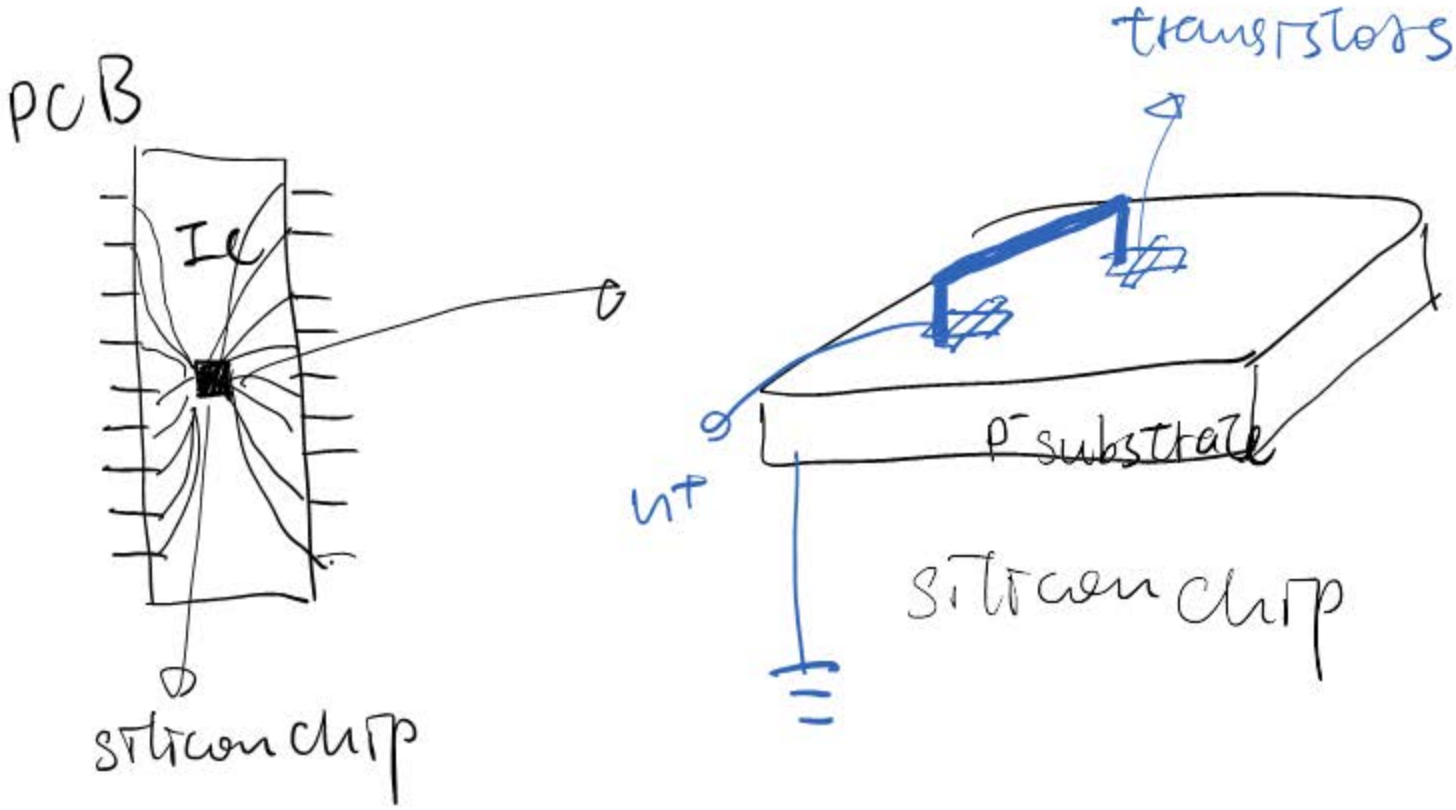
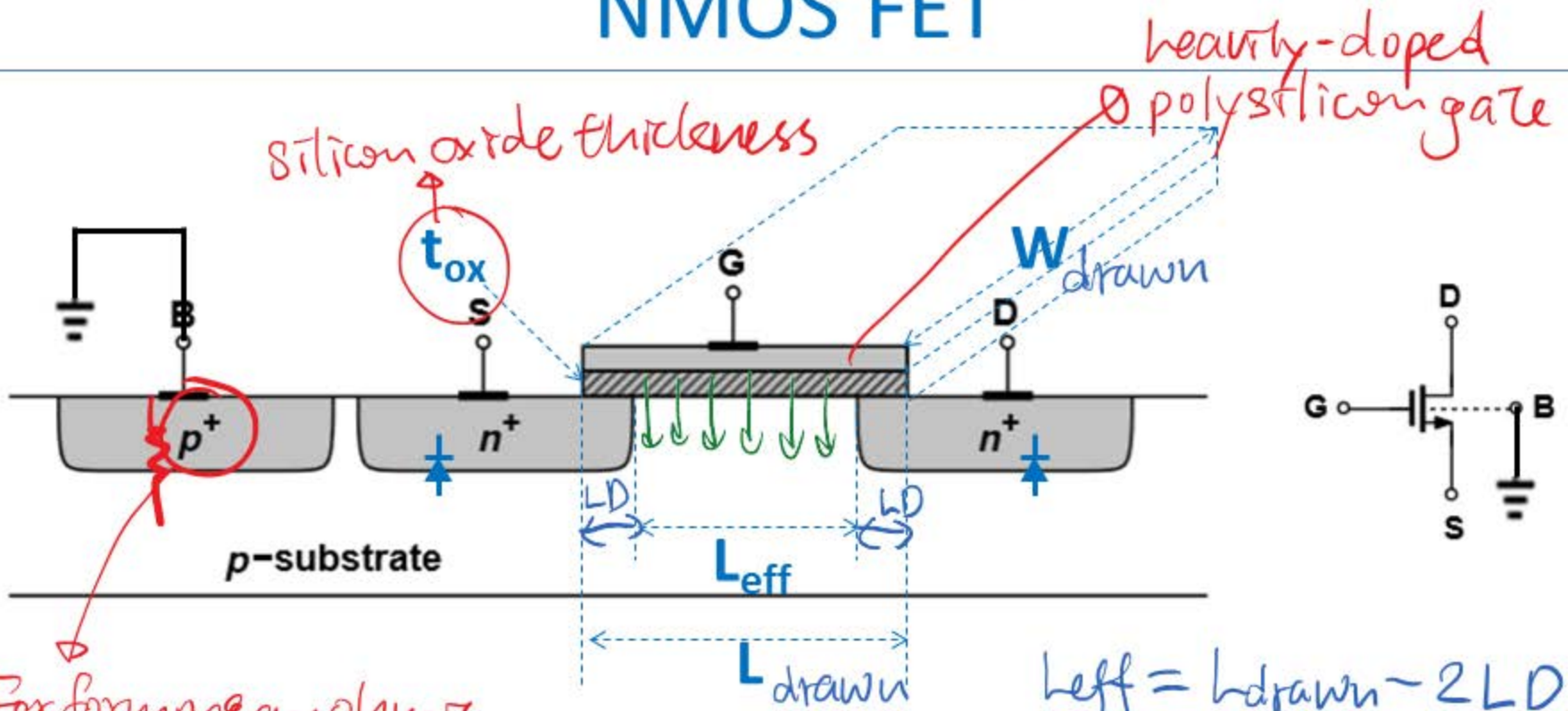

PCB
IC
silicon chip
transistors.
p- substrate
silicon chip

NMOS FET



- MOS = Metal-Oxide-Semiconductor
- FET = Field effect Transistor
- CMOS Technology keeps on reducing t_{ox} and L_{eff} (Moore's Law).
- Substrate (Body) of NMOS is generally connected to ground.
- See Chapter 17 for the introduction of CMOS fabrication technology.

Latest: TSMC 5 nm FinFET Technology

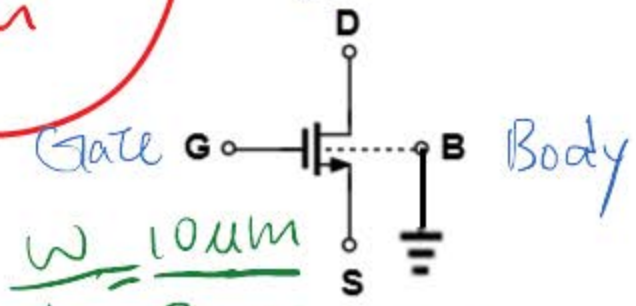
CMOS

Schematic Design

NMOS

Drain

PMOS



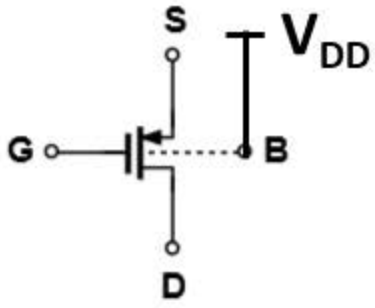
Gate

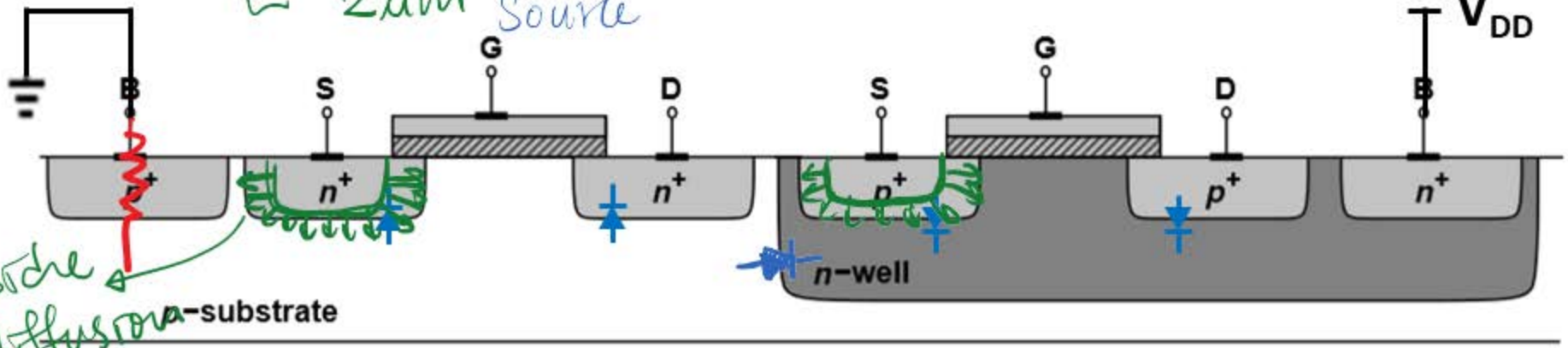
Body

W = 10um

L = 2um

Source





Side diffusion

NMOS and PMOS can share one p-Sub.

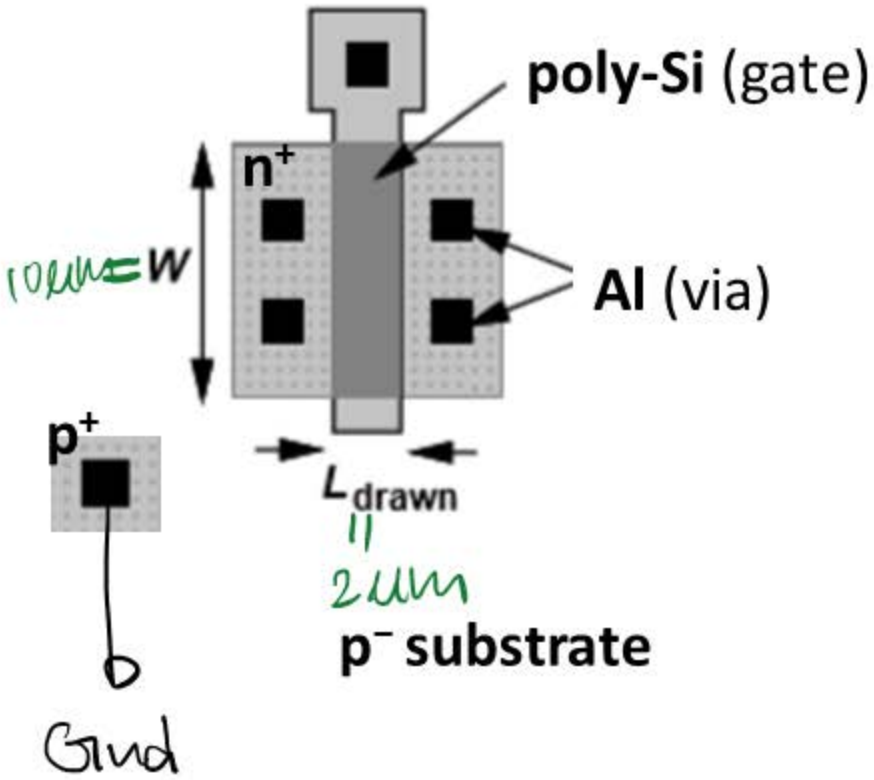
- CMOS = Complementary MOS (a fabrication technology)
- Substrate (Body) of NMOS is generally connected to ground.
- N-well (Body) of PMOS is generally connected to V_{DD}.

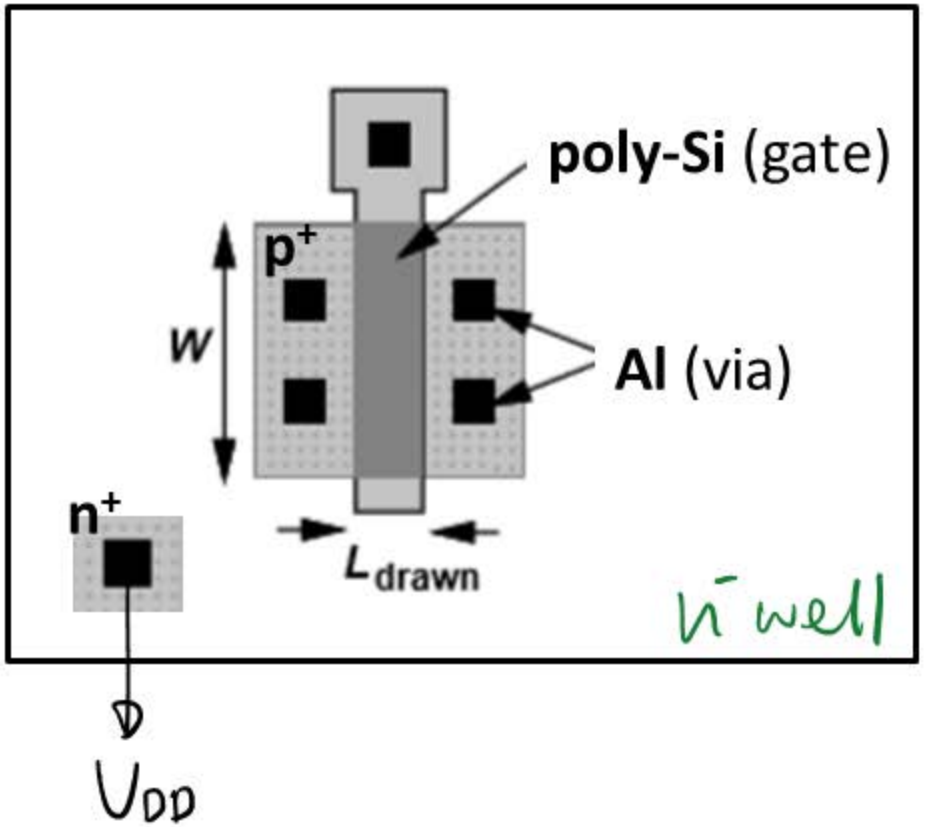
Layout

Layout Design

NMOS

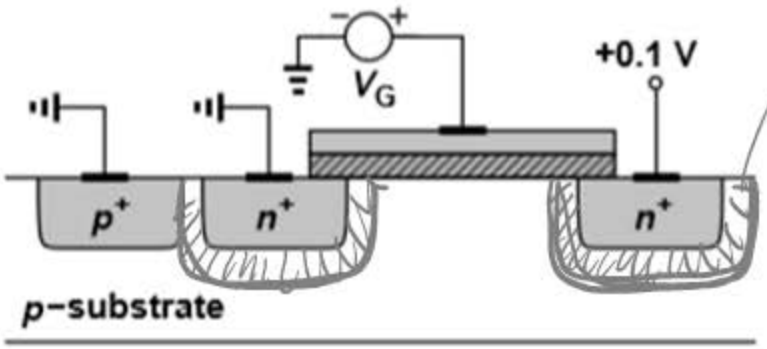
PMOS





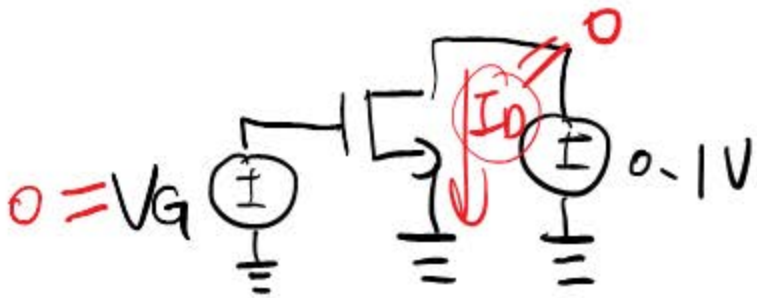
$$L_{eff} = L_{drawn} - 2LD = (2\times10^{-6}) - 2(0.08\times10^{-6})$$

Threshold Voltage (V_{TH}) for NMOS

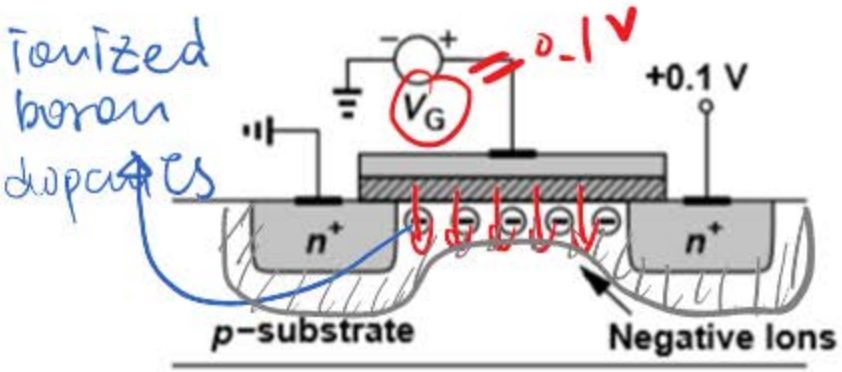


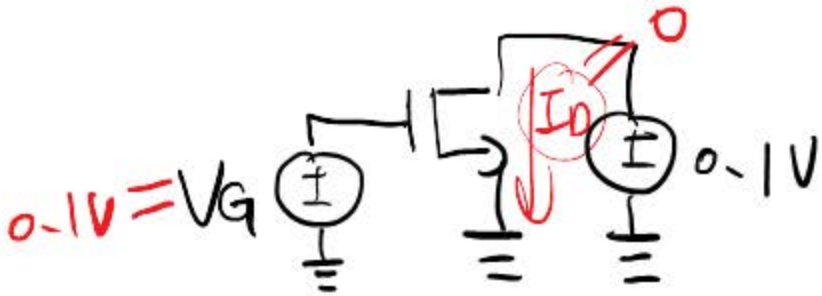
depletion region.

- $V_G = 0$ V
- No current flow



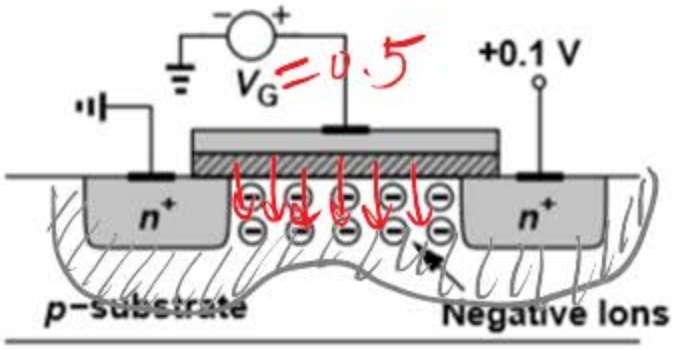
Threshold Voltage (V_{TH}) for NMOS

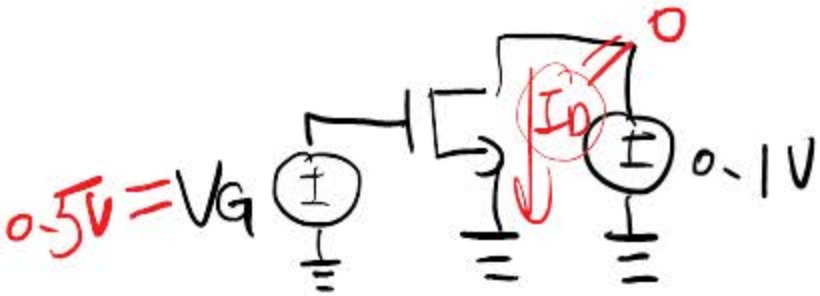




- As V_G increases from zero, holes in *p*-substrate are repelled, leaving negative ions (ionized boron dopants) behind to form a **depletion region**.
- Positive charges are mirrored at the gate.
- No charge carriers (electrons or holes) in the channel, so no current flow.

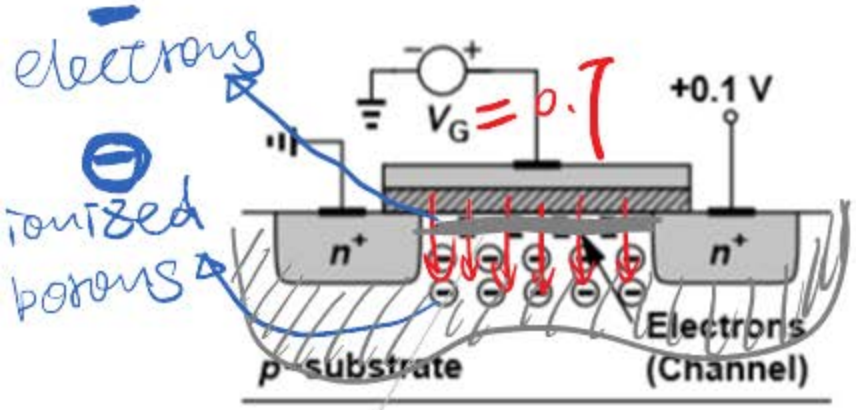
Threshold Voltage (V_{TH}) for NMOS





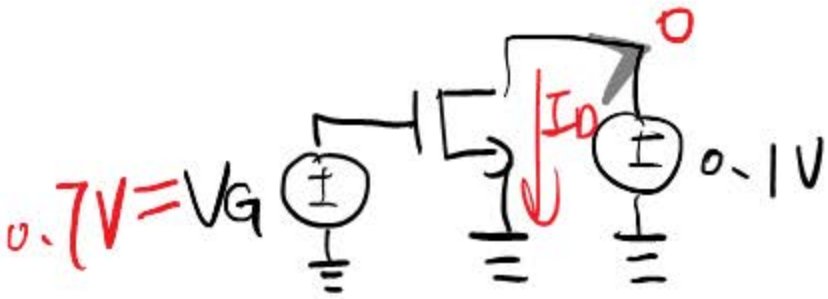
- Higher V_G further increases the width of the **depletion region**.

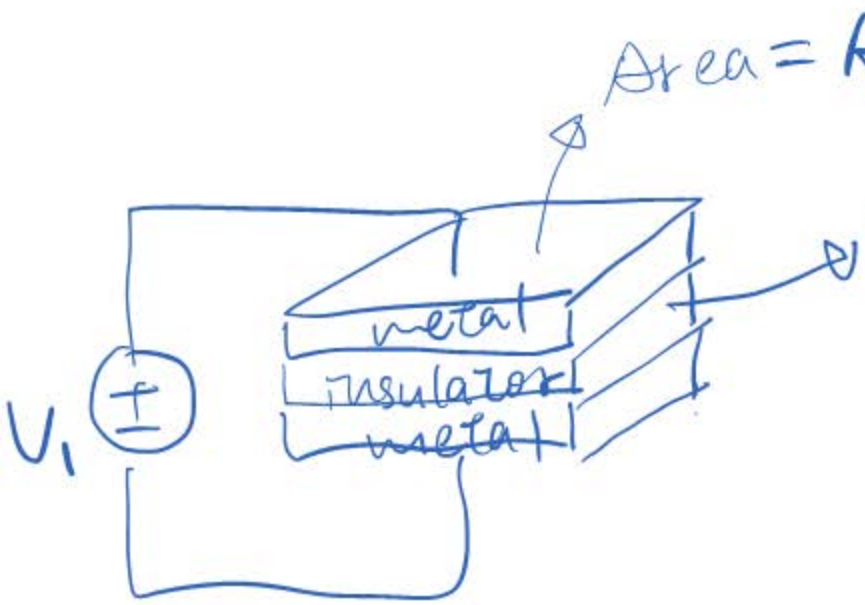
Threshold Voltage (V_{TH}) for NMOS



Interface as n-type as the substrate is p-type

- When V_G reaches a sufficiently positive value, a channel of electrons (**inversion layer**) is formed beneath the gate oxide.
- Electrons flow from "source" to "drain". Equivalently, current flows from "drain" to "source".
- The value of V_G at which the inversion layer forms is the **threshold voltage (V_{TH})**.
- If V_G rises further, the charges in the depletion region remain relatively constant, whereas the charges in the inversion layer increase rapidly.





thickness = t_{ox} (silicon oxide)

$$Q_1 = C V_1$$

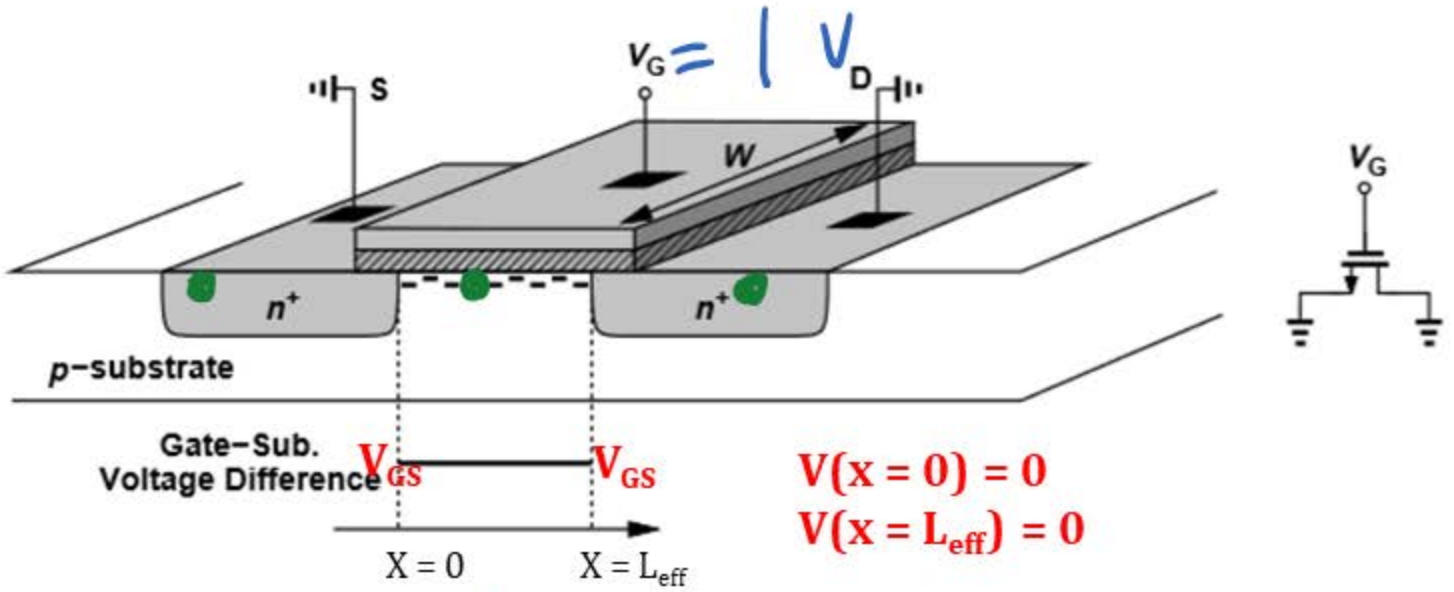
$$= \frac{A(\epsilon_0 \epsilon_r)}{t_{ox}} V_1$$

C_{ox}

ϵ_0: 8.85×10^{-12} F/m

ϵ_r: 3.9

I-V Characteristics for NMOS (Triode)



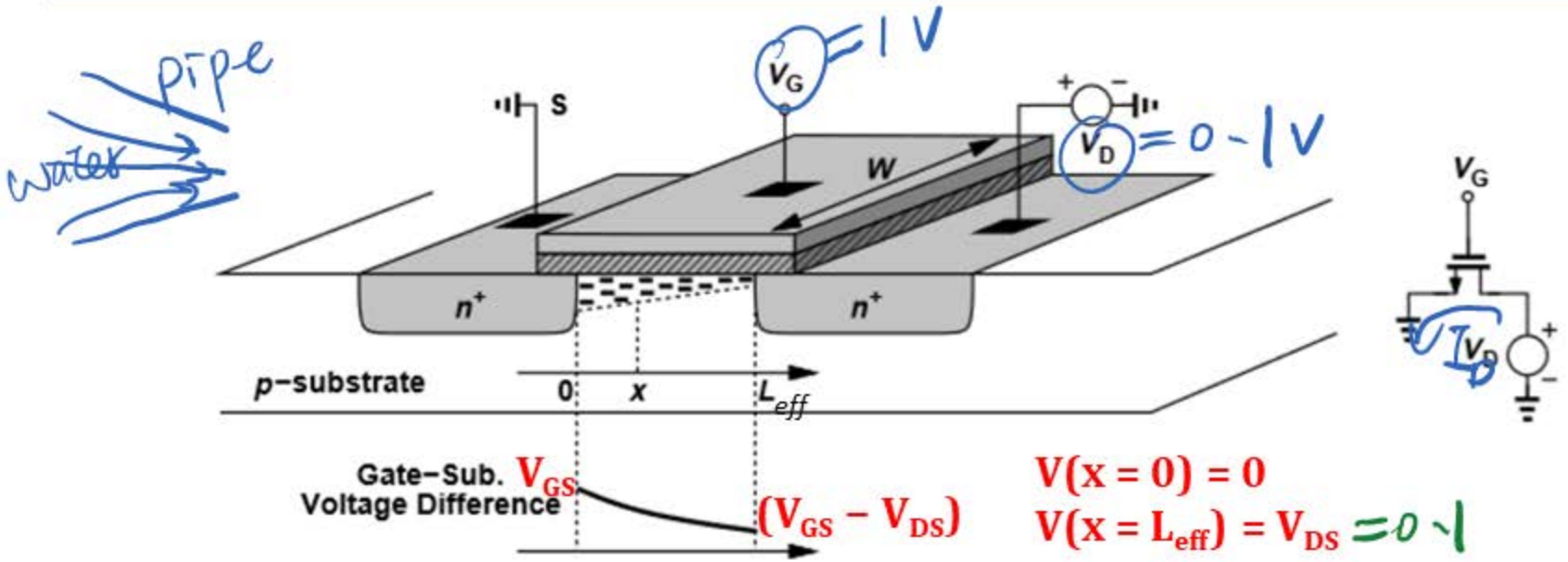
For $V_{GS} \geq V_{TH}$ = 0.7 V

$Q = -WL_{eff}C_{ox}(V_{GS} - V_{TH})$ (unit: coulomb)

$Q_d = -WC_{ox}(V_{GS} - V_{TH})$ (unit: coulomb·m^{-1})

C_{ox} (gate oxide capacitance per unit area)
$= \epsilon_{silicon\ oxide} / t_{ox}$
$= [8.85 \times 10^{-12}\ (F/m) \times 3.9] / t_{ox}$ (F/m²)

I-V Characteristics for NMOS (Triode)



$$I_D = Q_d \times v = Q_d \times (\mu_n \mathcal{E}) = -WC_{ox}[V_{GS} - V_{TH} - V(x)] \times (\mu_n \mathcal{E})$$

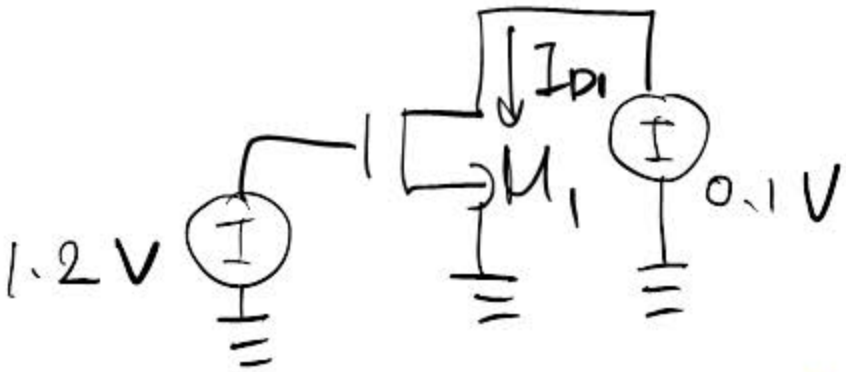
$$= WC_{ox}[V_{GS} - V_{TH} - V(x)] \times \mu_n \times \frac{dV(x)}{dx}$$

$$\mathcal{E} = -dV(x)/dx$$

$$\int_{x=0}^{x=L_{eff}} I_D \cdot dx = \int_{V(0)=0}^{V(L)=V_{DS}} \mu_n C_{ox} W[V_{GS} - V_{TH} - V(x)] \cdot dV(x)$$

I_D: constant along channel

$$\mathbf{I_D = \mu_n C_{ox} \frac{W}{L_{eff}} [(V_{GS} - V_{TH})V_{DS} - \frac{1}{2} V_{DS}^2]}$$



$$M_1: \frac{20\mu m}{5\mu m} = \frac{W_{drawn}}{L_{drawn}}$$

$$I_{D1} = 350\left(\frac{cm^2}{V \cdot sec}\right) C_{ox}\left[\frac{20\times10^{-6}}{(5\times10^{-6}) - 2(0.08\times10^{-6})}\right]\cdot$$

μm

$$\left[(1.2-0.7)0.1 - \frac{1}{2}0.1^2\right]$$

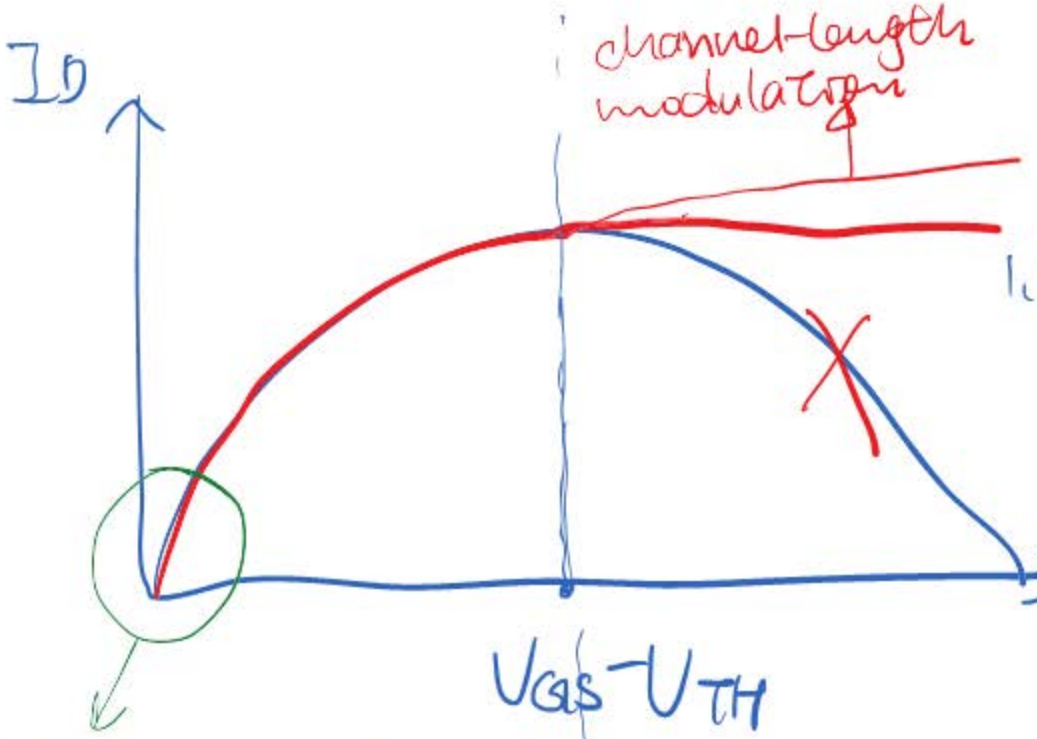
$$\mathbf{I_D = \mu_n C_{ox} \frac{W}{L_{eff}} [(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2]}$$

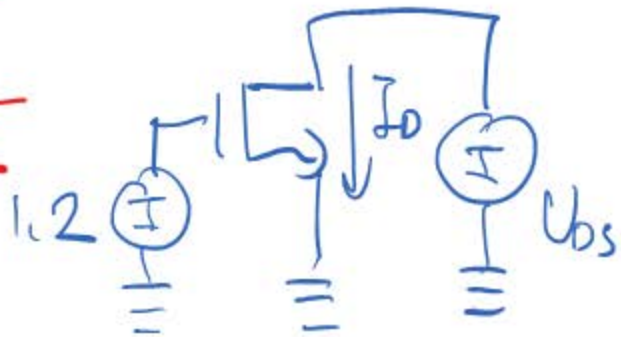
$L_{drawn} - 2LD$

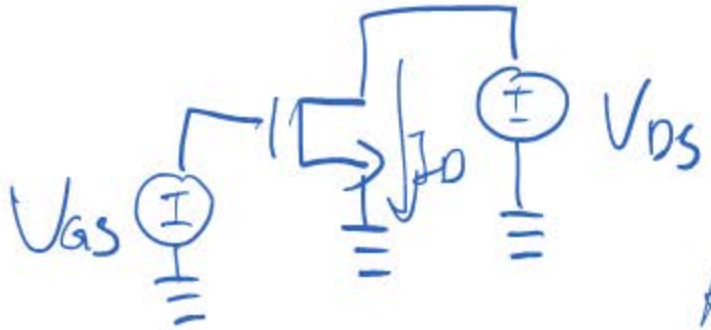
$I_D =$ constant V_{DS} ← can be neglected if V_{DS} small

$$I_D = \mu_n C_{ox} \frac{W}{L_{eff}} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

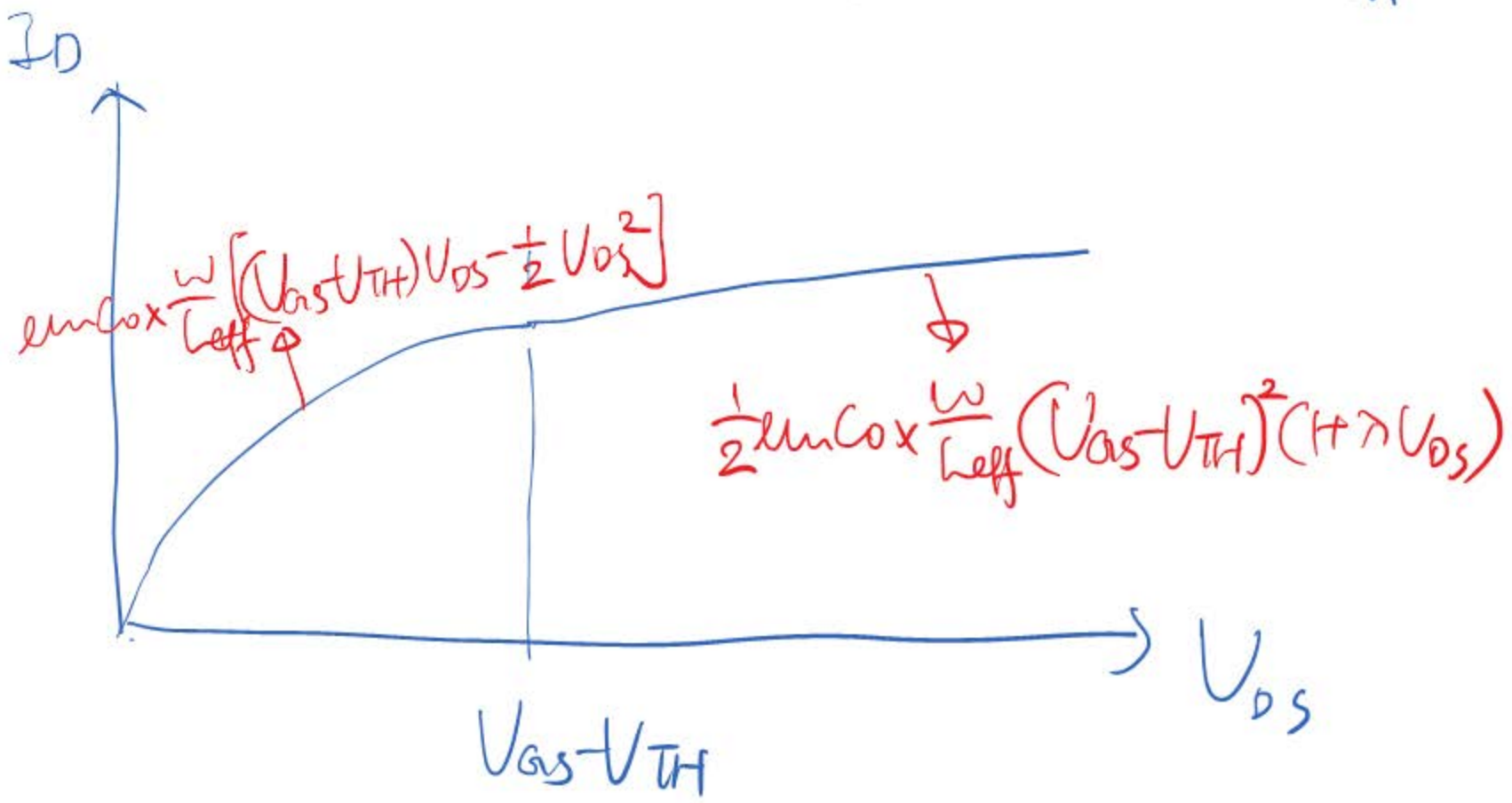
DC sweep I_D v.s. V_{DS} @ given $V_{GS} > V_{TH}$ (1.2 V)







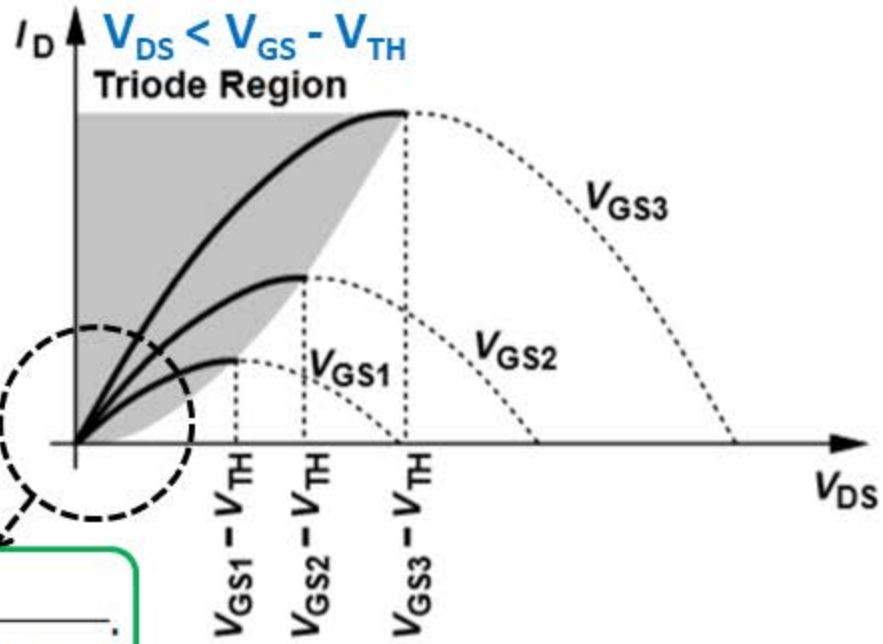
At given $V_{GS} > V_{TH}$



I-V Characteristics for NMOS (Triode)

$$I_D = \mu_n C_{ox} \frac{W}{L_{eff}} [(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2]$$

$$I_{D,max} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L_{eff}} (V_{GS} - V_{TH})^2$$ $V_{DS} = V_{GS} - V_{TH}$

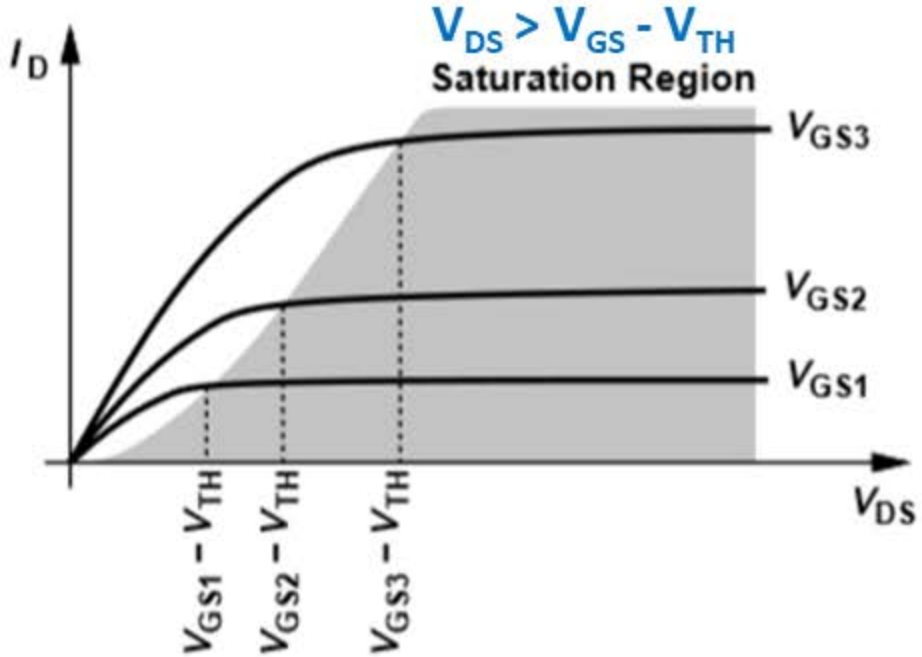


$V_{DS} << 2(V_{GS} - V_{TH})$
Deep triode region

$$R_{on} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L_{eff}}\right)(V_{GS} - V_{TH})}.$$

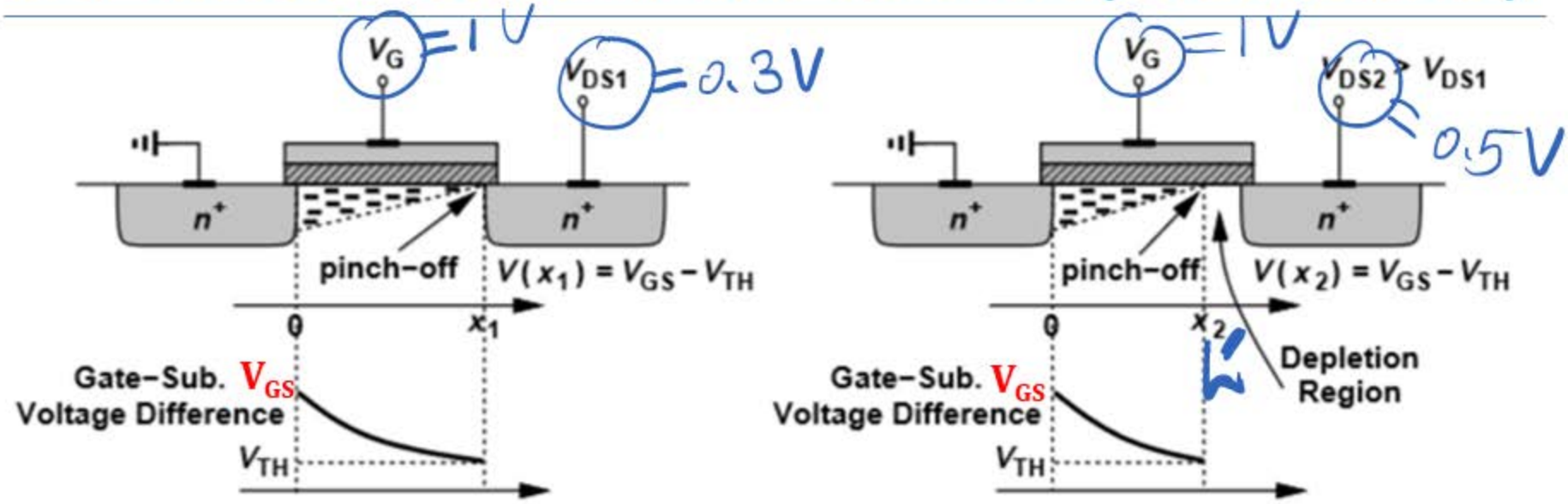
- For digital circuit, MOSFET, as a switch, usually operates in deep triode region.
- This is why reducing t_{ox} and L_{eff} can improve speed.

I-V Characteristics for NMOS (Saturation)



- In reality, for $V_{DS} > V_{GS} - V_{TH}$, I_D becomes relatively constant.
- $V_{DS} = V_{GS} - V_{TH}$ is the minimum value for the NMOS to operate in saturation region.

I-V Characteristics for NMOS (Saturation)



$$\int_{x=0}^{x=L'} I_D \cdot dx = \int_{V(0)=0}^{V(L')=V_{GS}-V_{TH}} \mu_n C_{ox} W[V_{GS} - V_{TH} - V(x)] \cdot dV(x)$$

$$\mathbf{I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L'}(V_{GS} - V_{TH})^2}$$

I_D: constant along channel

L': the point at which Q_d drops to zero

$V_{GS} - V_{TH}$: the overdrive voltage

- Electron velocity ($v = I_D / Q_d$) becomes tremendously high at the pinch off point ($Q_d \rightarrow 0$), such that electrons shoot through the depletion region and arrive at the drain terminal.

Channel-Length Modulation

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L'}(V_{GS} - V_{TH})^2$$

$$L' = L_{eff} - \Delta L$$

$$\frac{1}{L'} = \frac{1}{L_{eff} - \Delta L} = \frac{1}{L_{eff}} \cdot \frac{1}{1 - \frac{\Delta L}{L_{eff}}} \approx \frac{1}{L_{eff}} \cdot \left(1 + \frac{\Delta L}{L_{eff}}\right)$$

small

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L_{eff}}(V_{GS} - V_{TH})^2\left(1 + \frac{\Delta L}{L_{eff}}\right)$$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L_{eff}}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

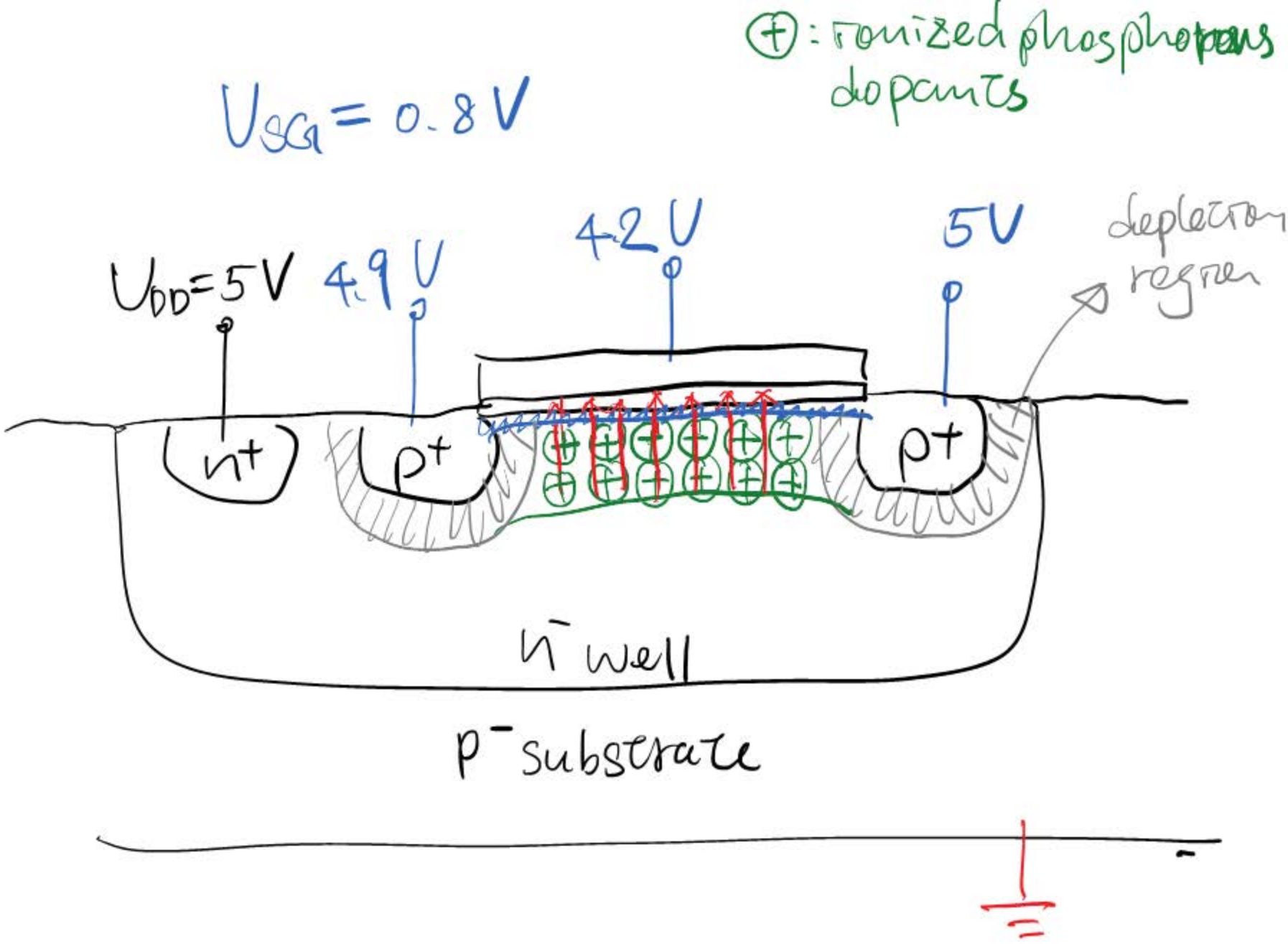
$\lambda = 0$ means don't consider "channel-length modulation"

Channel-Length Modulation

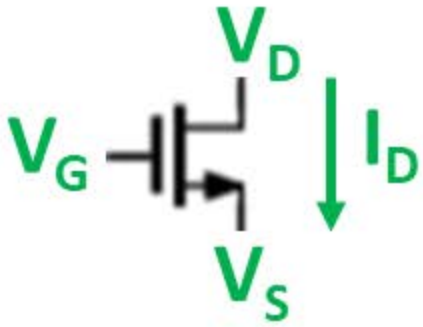
$$\mathbf{r_o} = \frac{\partial V_{DS}}{\partial I_D} = 1 \Big/ \frac{\partial I_D}{\partial V_{DS}}$$

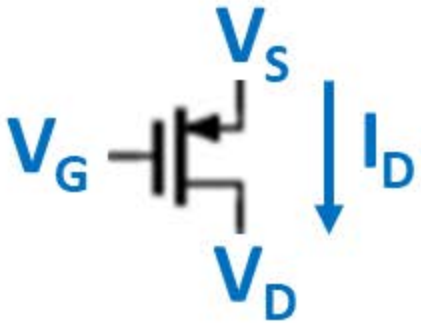
$$= \frac{1}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L_{eff}}(V_{GS} - V_{TH})^2 \cdot \lambda}$$

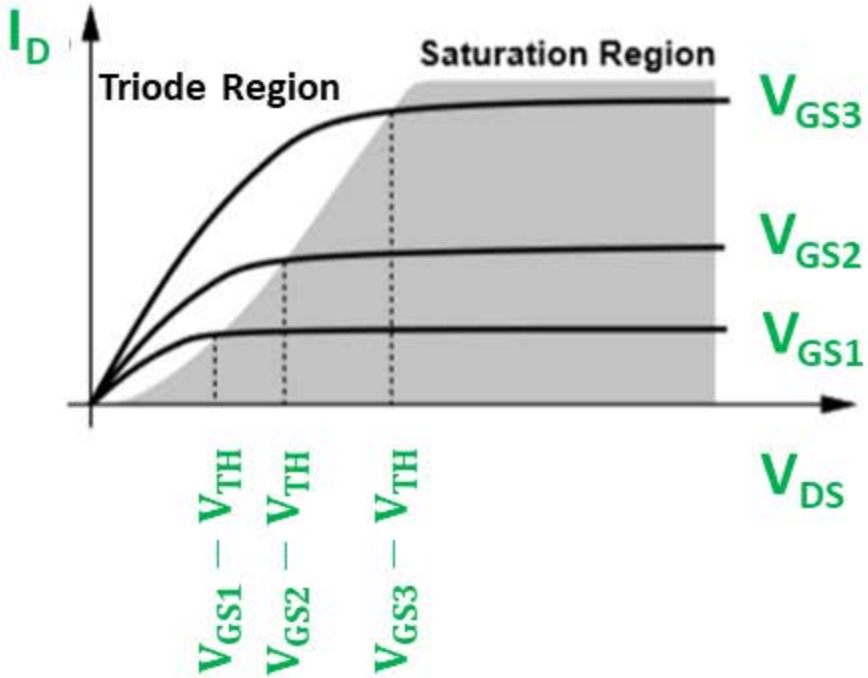
$$\approx \frac{\mathbf{1}}{\mathbf{I_D \cdot \lambda}}$$

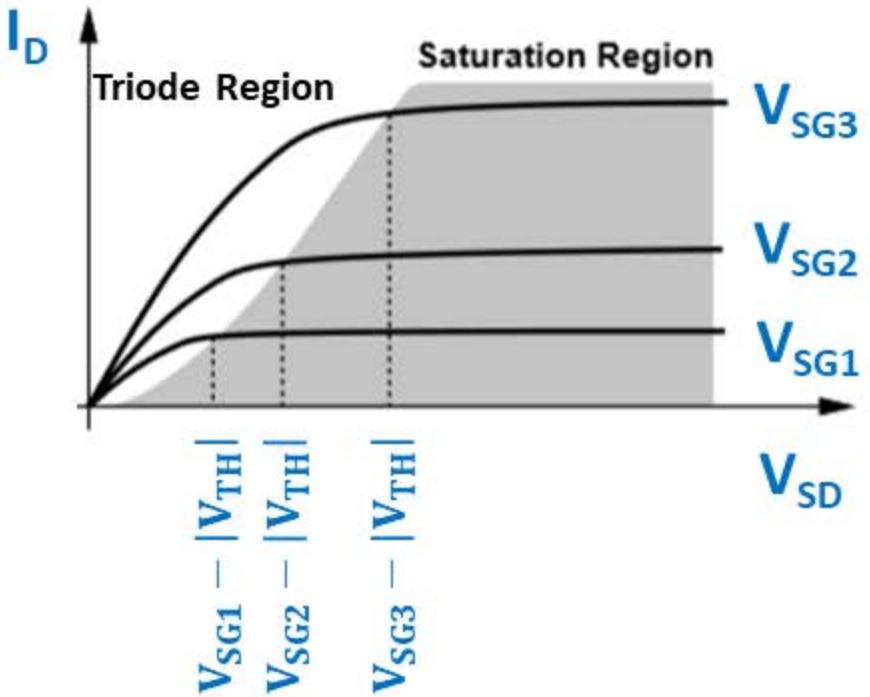

⊕: ionized phosphorus dopants
$V_{SG} = 0.8\,V$
$V_{DD} = 5V$
4.9 V
4.2 V
5V
depletion region
n+
p+
p+
n- well
p- substrate

NMOS vs PMOS


V_D
V_G
I_D
V_S

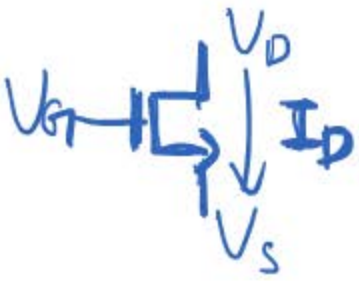

V_S
V_G
I_D
V_D


I_D
Triode Region
Saturation Region
V_{GS3}
V_{GS2}
V_{GS1}
V_{DS}
$V_{GS1} - V_{TH}$
$V_{GS2} - V_{TH}$
$V_{GS3} - V_{TH}$


I_D
Triode Region
Saturation Region
V_{SG3}
V_{SG2}
V_{SG1}
V_{SD}
$V_{SG1} - |V_{TH}|$
$V_{SG2} - |V_{TH}|$
$V_{SG3} - |V_{TH}|$

NMOS vs PMOS

NMOS



triode: $I_D = \mu_n C_{ox} \left(\frac{W}{L_{eff}}\right)\left[(V_{GS} - V_{THN})V_{DS} - \frac{1}{2}V_{DS}^2\right]$

sat: $I_D = \frac{1}{2}\mu_n C_{ox} \left(\frac{W}{L_{eff}}\right)(V_{GS} - V_{THN})^2 (1 + \lambda V_{DS})$

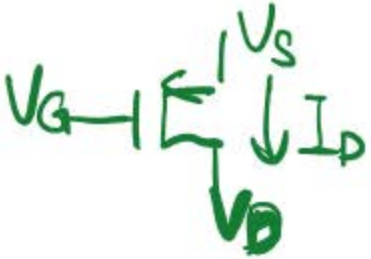
$V_{GS} \rightarrow V_{SG}$

$V_{THN} \rightarrow |V_{THP}|$

$V_{DS} \rightarrow V_{SD}$

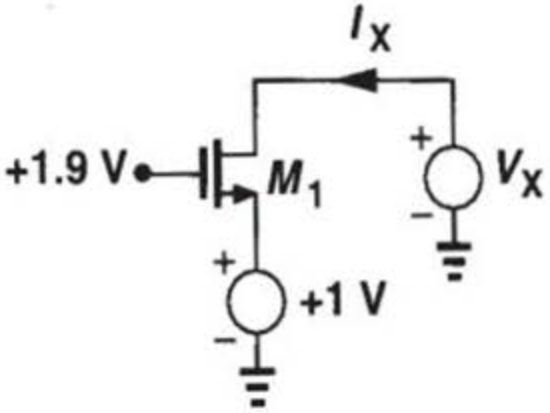
$\mu_n \rightarrow \mu_p$

PMOS

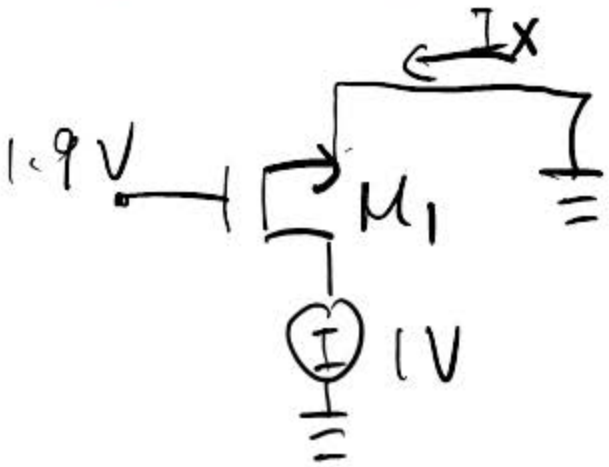


triode: $I_D = \mu_p C_{ox} \left(\frac{W}{L_{eff}}\right)\left[(V_{SG} - |V_{THP}|)V_{SD} - \frac{1}{2}V_{SD}^2\right]$

sat: $I_D = \frac{1}{2}\mu_p C_{ox} \left(\frac{W}{L_{eff}}\right)(V_{SG} - |V_{THP}|)^2 (1 + \lambda V_{SD})$



When $V_X = 0$



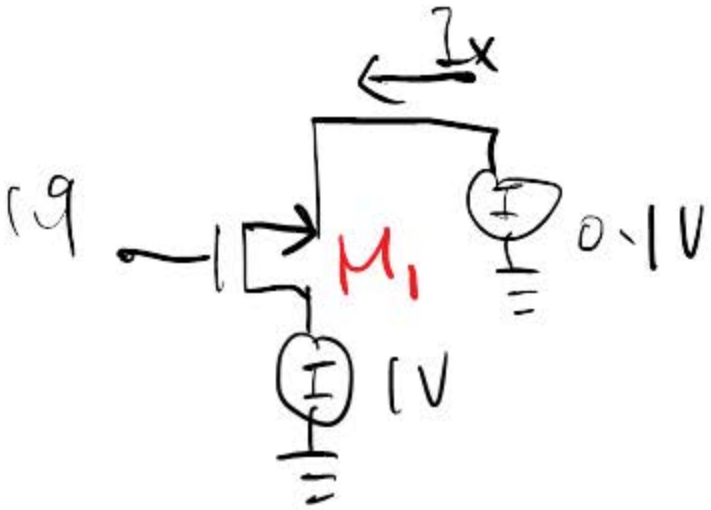
$V_{DS} = 1\ V$

$V_{GS} = 1.9\ V$

$V_{DS} < V_{GS} - 0.7$

(triode)

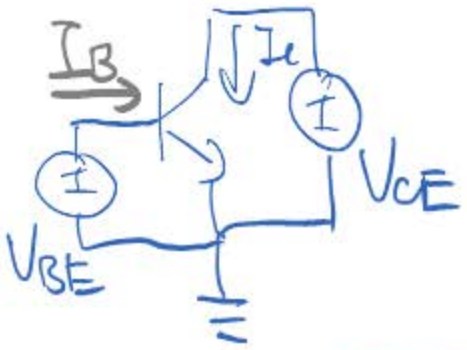
When $V_X = 0.1$



$V_{DS} = 0.9\ V$

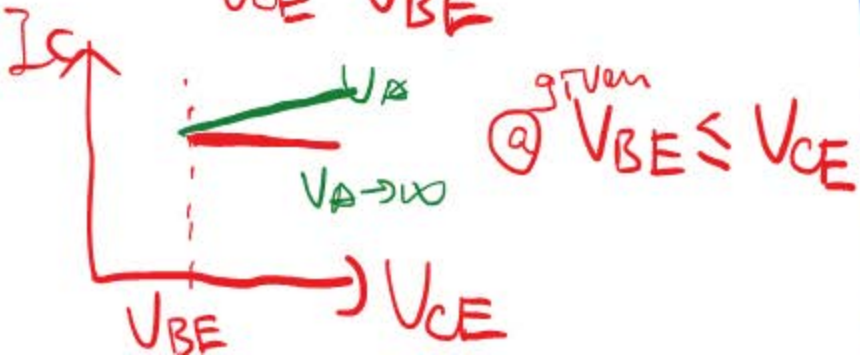
$V_{GS} = 1.8\ V$

npn BJT

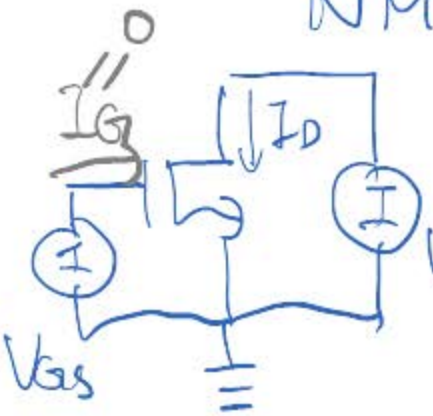


For $V_{CE} \geq V_{BE}$ in forward-active

$$I_C = I_S\left(e^{\frac{qV_{BE}}{kT}} - 1\right)\left(1 + \frac{V_{CE}}{V_A}\right)$$



NMOS

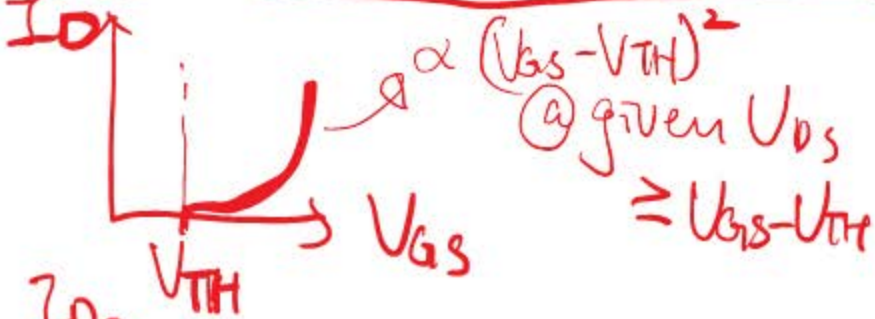


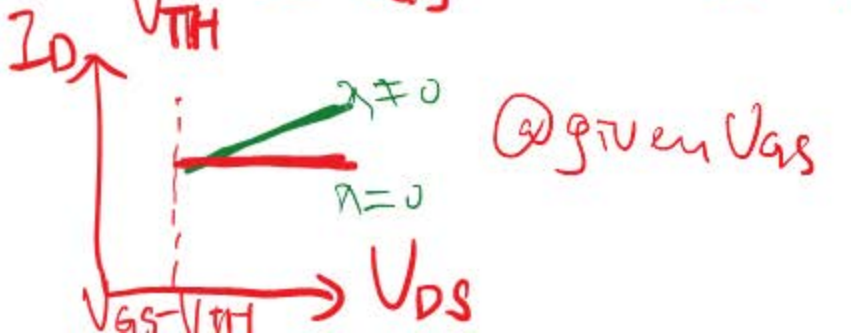
$V_{GS} > V_{TH}$

For $V_{DS} \geq V_{GS} - V_{TH}$ in sat.

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{TH})^2$$

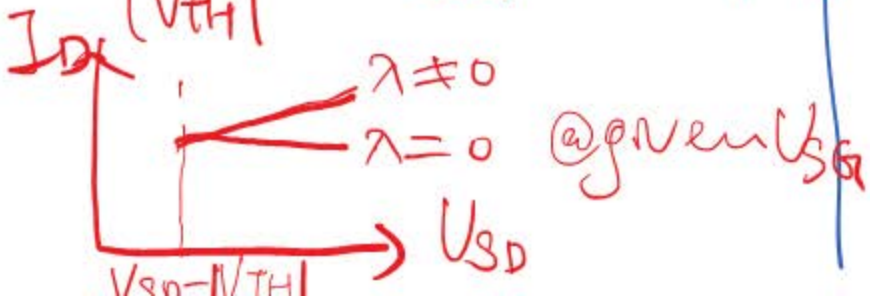
$$= \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L_{eff}}\right)(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$





PMOS

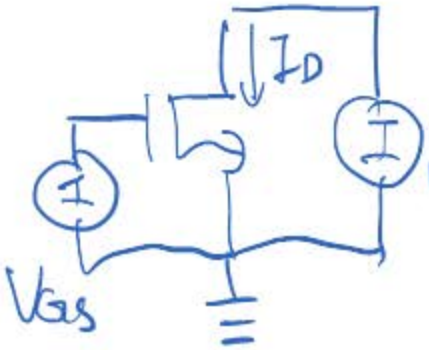
$$I_D = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L_{eff}}\right)(V_{SG}-|V_{TH}|)^2(1+\lambda V_{SD})$$



NMOS

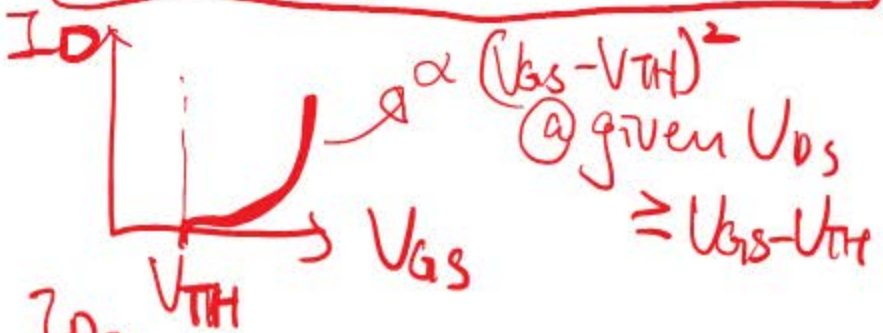
$V_{GS} > V_{TH}$

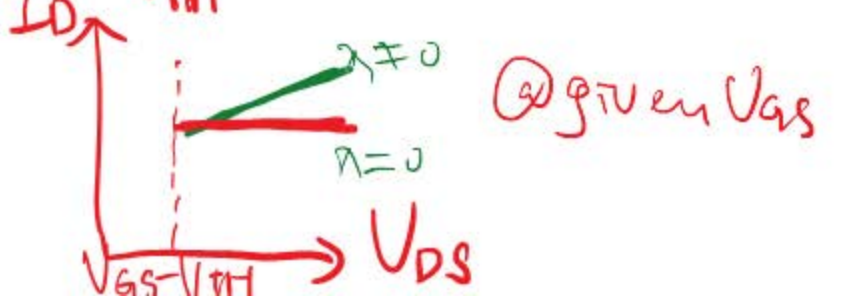
For $V_{DS} \geq V_{GS}-V_{TH}$



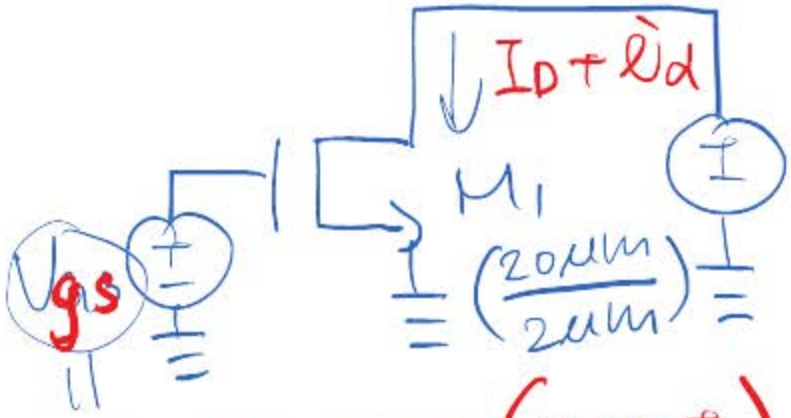
$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_{TH})^2$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L_{eff}}\right)(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$





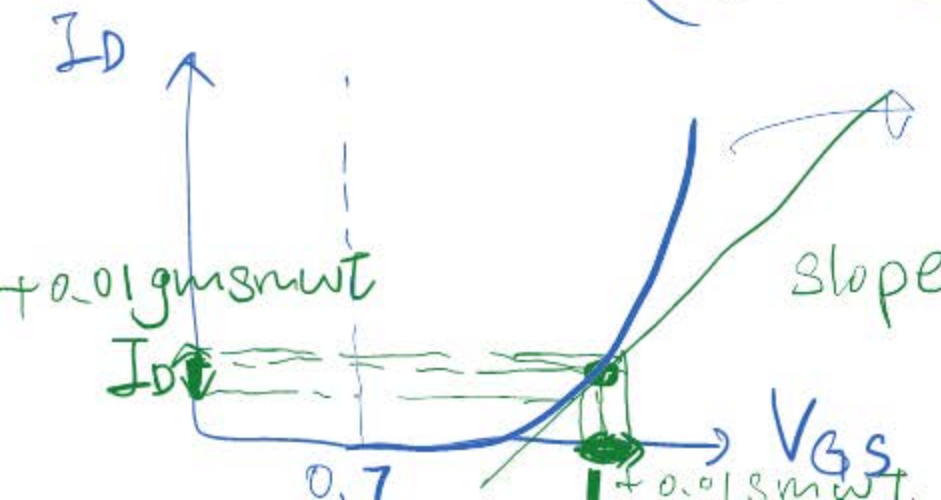
$I_D = ?$ $\hat{v}_d = ?$



$V_{DS} = 1V$

$V_{DS} = 1V$
$> V_{GS} - V_{TH} = 0.3V$
$\Rightarrow M_1$ in sat.

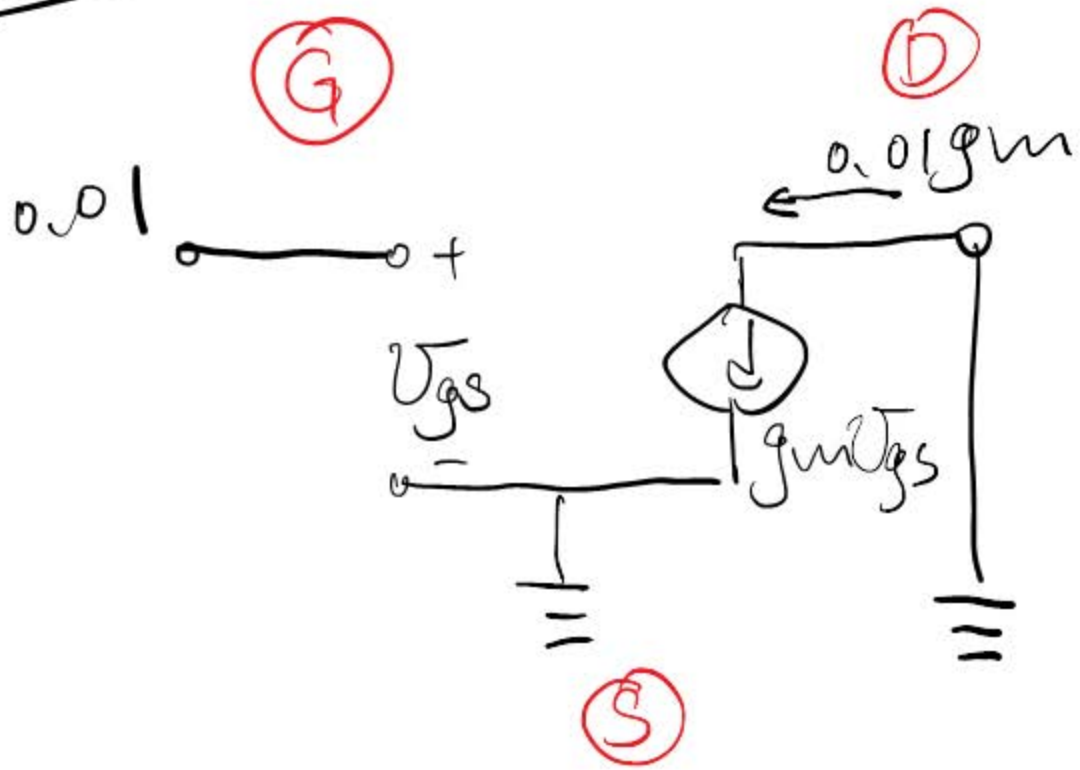
$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{20\times10^{-6}}{2\times10^{-6} - 2L_D}\right)(1-0.7)^2(1+\lambda\cdot 1)$$



$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L_{eff}}(V_{GS}-0.7)^2((+\lambda\cdot 1)$$

$$\text{Slope} = g_m = \frac{dI_D}{dV_{GS}}\Big|_{@\ V_{GS}=1V}$$

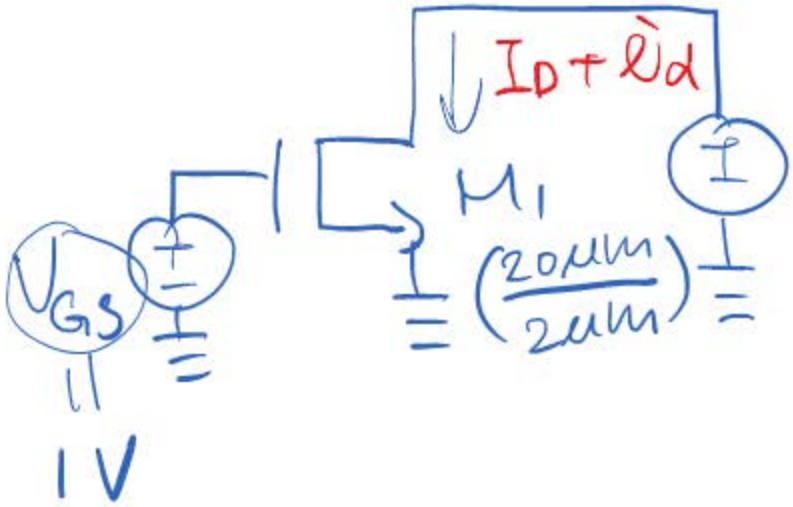
small-signal



$$g_m = \frac{dI_D}{dV_{GS}} = \mu_n C_{ox}\left(\frac{W}{L_{eff}}\right)(V_{GS}-V_{TH})(1+\lambda V_{DS})$$

$$= \mu_n C_{ox}\left(\frac{20\times10^{-6}}{2\times10^{-6}-2L_D}\right)(1-0.7)(1+\lambda\cdot 1)$$

$I_D = ?$ $\hat{v}_d = ?$

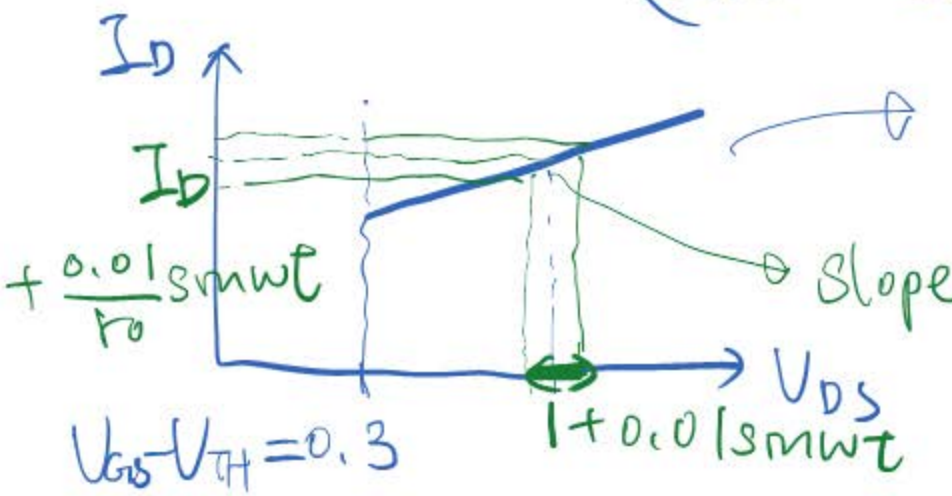


$V_{DS} = 1V$

$> V_{GS} - V_{TH} = 0.3V$

$\Rightarrow M_1$ in sat.

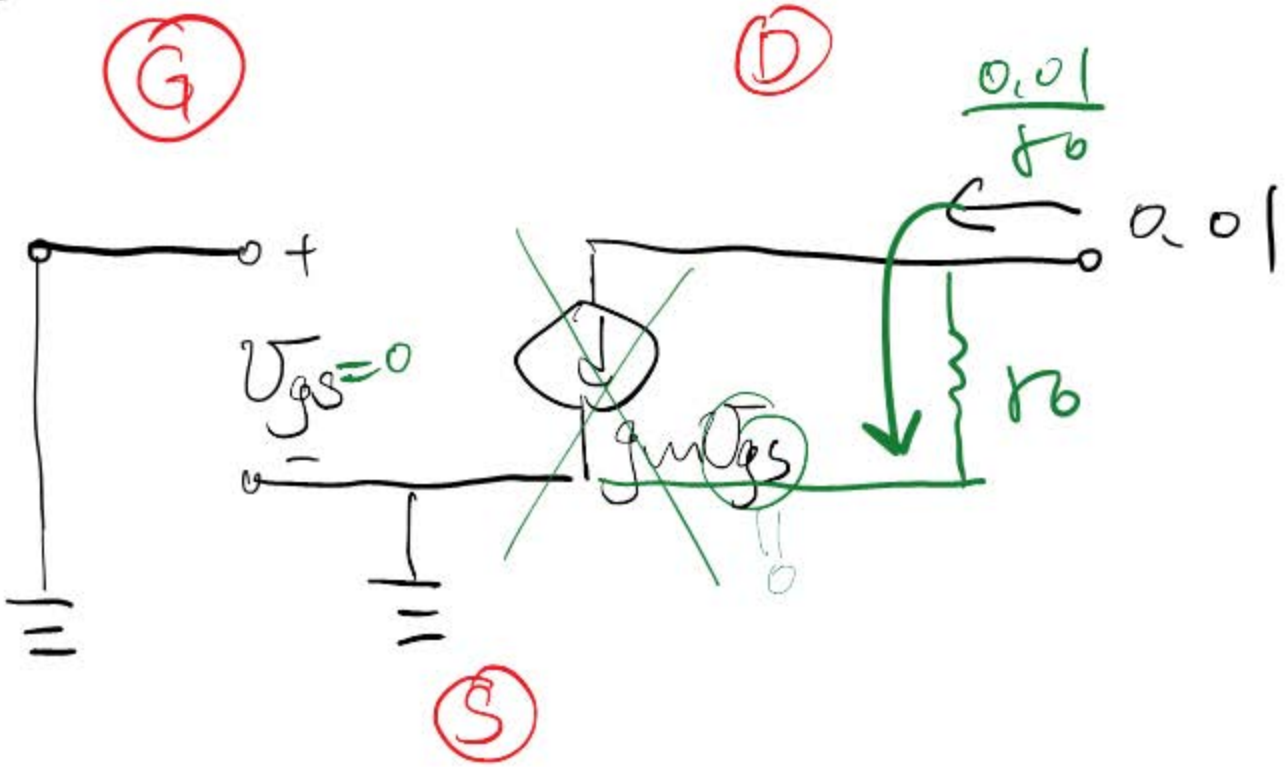
$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{20\times10^{-6}}{2\times10^{-6} - 2L_D}\right)(1-0.7)^2(1+\lambda\cdot 1)$$



$\frac{1}{2}\mu_n C_{ox}\frac{W}{L_{eff}}(1-0.7)^2(1+\lambda\cdot V_{DS})$

$\text{Slope} = \frac{1}{r_o} = \frac{dI_D}{dV_{DS}}\Big|_{@\, V_{DS}=1V}$

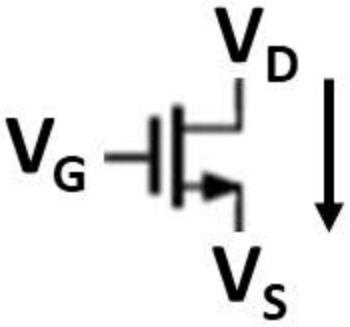
small-signal



$$r_o = \frac{1}{\text{slope}} = \frac{1}{dI_D/dV_{DS}} \cong \frac{1}{I_D \lambda}$$

Transconductance

- For the NMOS operating in the saturation region ($V_{DS} \geq V_{GS} - V_{TH}$):



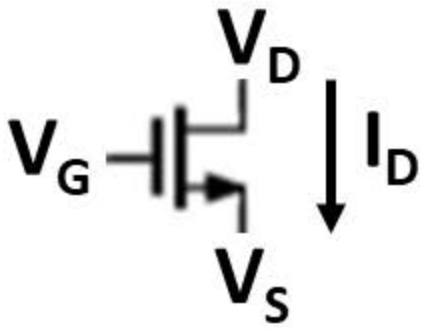
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L_{eff}}(V_{GS} - V_{TH})^2 (1+\lambda V_{DS})$$

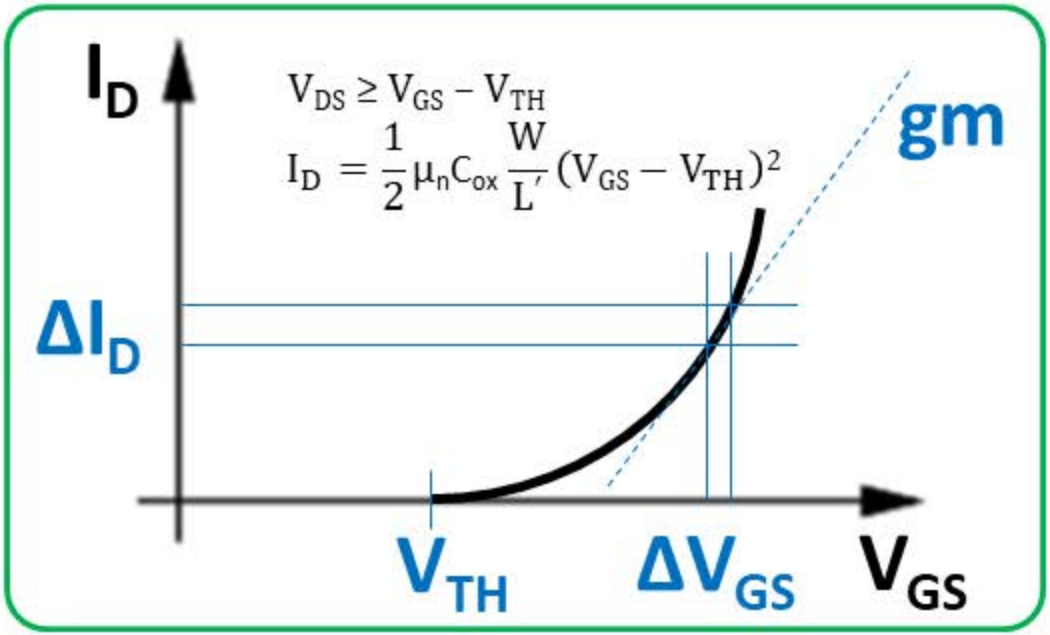
- ΔV_{GS} results in $\Delta I_D = gm \times \Delta V_{GS}$.

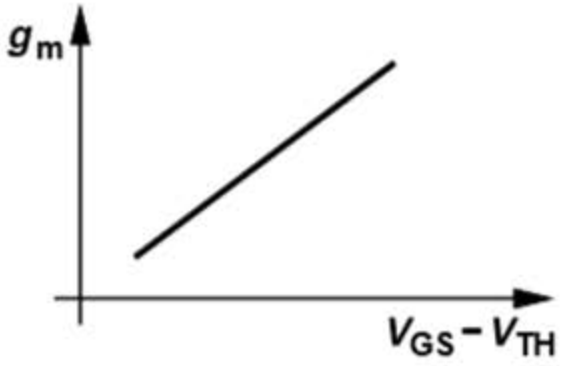
$$gm = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox}\frac{W}{L_{eff}}(V_{GS} - V_{TH})(1+\lambda V_{DS})$$

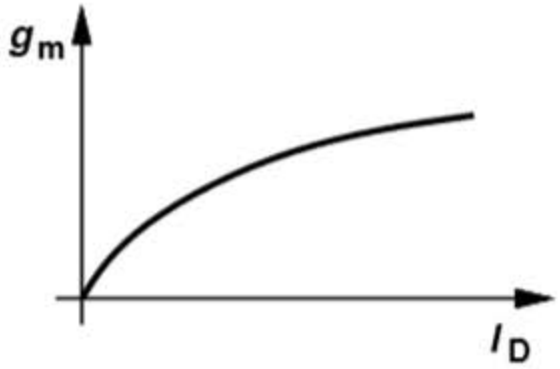
$$= \sqrt{2\mu_n C_{ox}\frac{W}{L_{eff}} I_D} = \frac{2I_D}{V_{GS} - V_{TH}} \cdot (1+\lambda V_{DS})$$

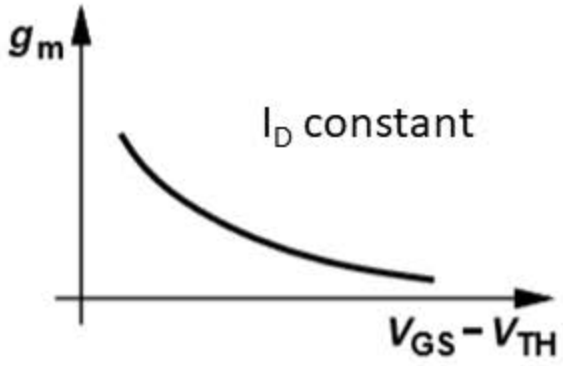
Transconductance











- For a given NMOS, gm changes according to the DC biasing condition.
- If a small signal is applied to a NMOS with defined biasing values, we assume the signal amplitude is small enough that the variation in gm is negligible.

Body Effect

$$|V_{TH}| = |V_{TH0}| + \left(\gamma\sqrt{|2\Phi_F + V_{BS}|} - \sqrt{|2\Phi_F|}\right)$$ for PMOS

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}\right)$$ for NMOS

$$\Phi_F = \frac{kT}{q}\ln\frac{N_{sub}}{n_i} \qquad \gamma = \frac{\sqrt{2q\epsilon_{Si}N_{sub}}}{C_{ox}}$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L'}(V_{GS} - V_{TH})^2$$

Ignored in Ve311
will learn in Ve320.

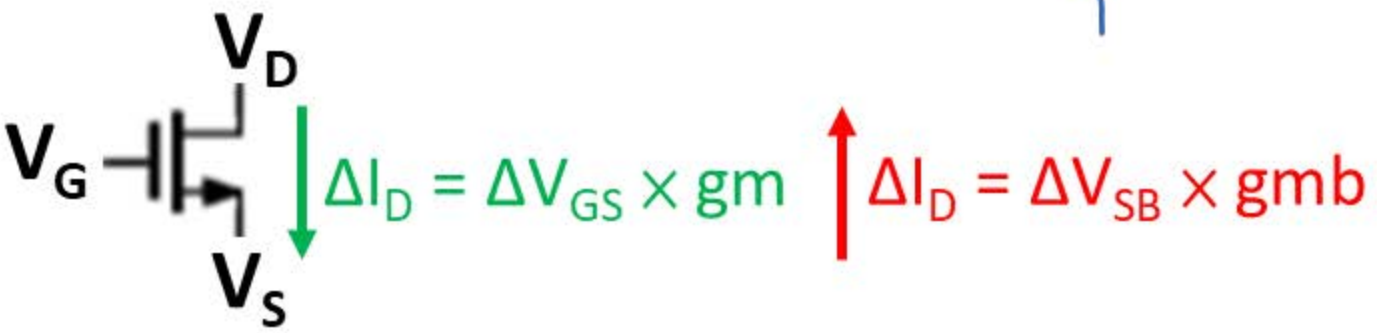
Body Effect

$$\mathbf{gmb} = \frac{\partial I_D}{\partial V_{SB}} = \frac{\partial I_D}{\partial V_{TH}} \cdot \frac{\partial V_{TH}}{\partial V_{SB}}$$

$$= -\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) \cdot \frac{\partial V_{TH}}{\partial V_{SB}}$$

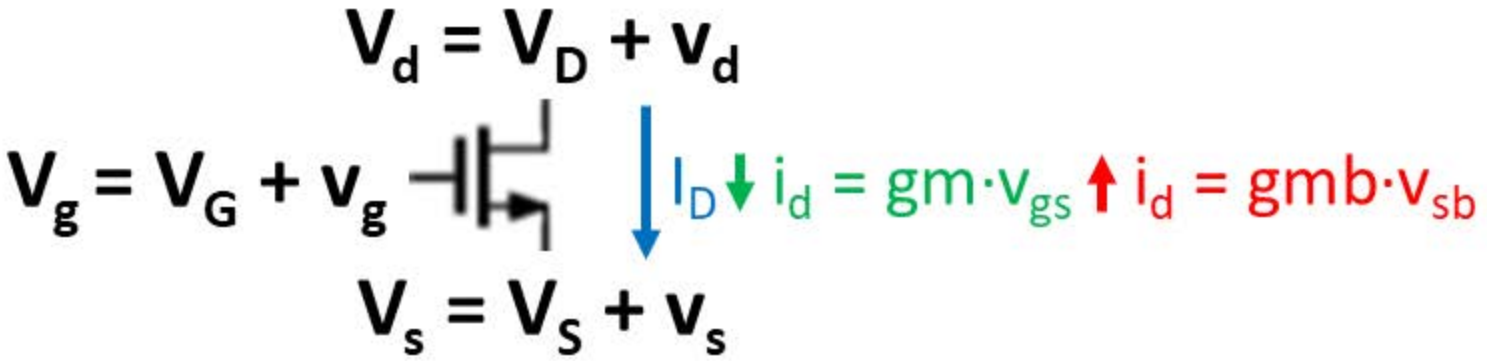
$$= -\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) \cdot \frac{\gamma}{2} \frac{1}{\sqrt{|2\Phi_F + V_{SB}|}}$$

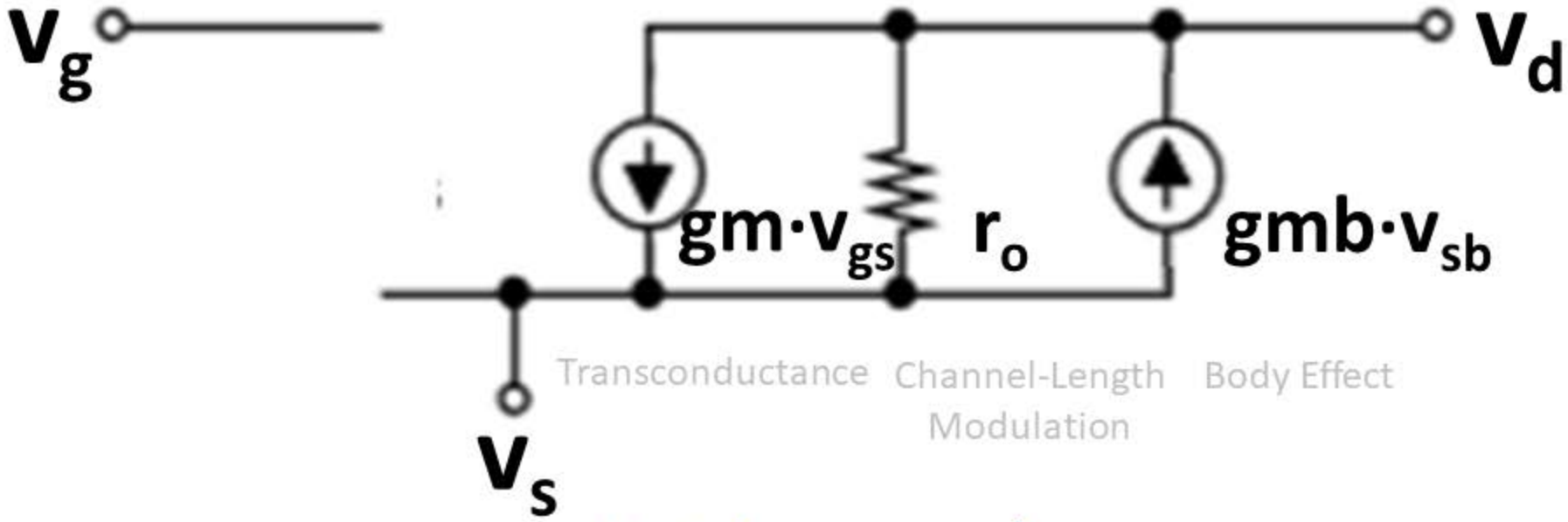
$$= -\mathbf{gm} \cdot \boldsymbol{\eta}$$



- V_{GS} increases, I_D increases.
- V_{SB} increases, V_{TH} increases and thus I_D decreases.

Small-Signal Model for NMOS





$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L_{eff}}\right)(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

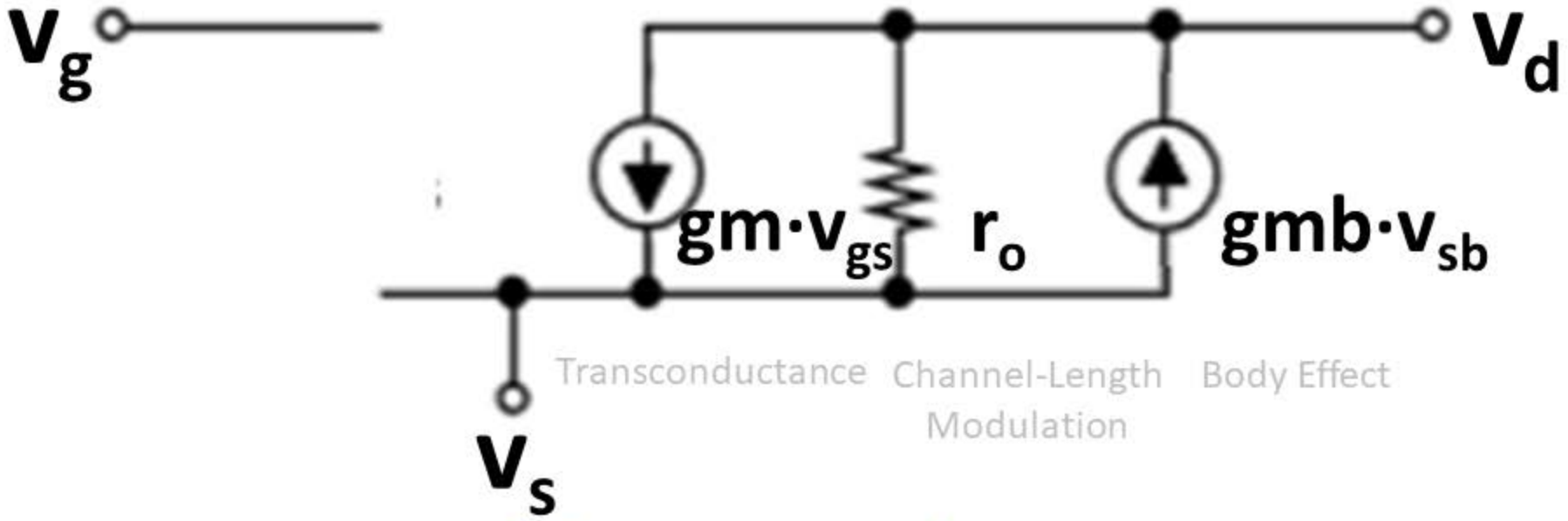
Small-Signal Model for PMOS

$V_s = V_S + v_s$

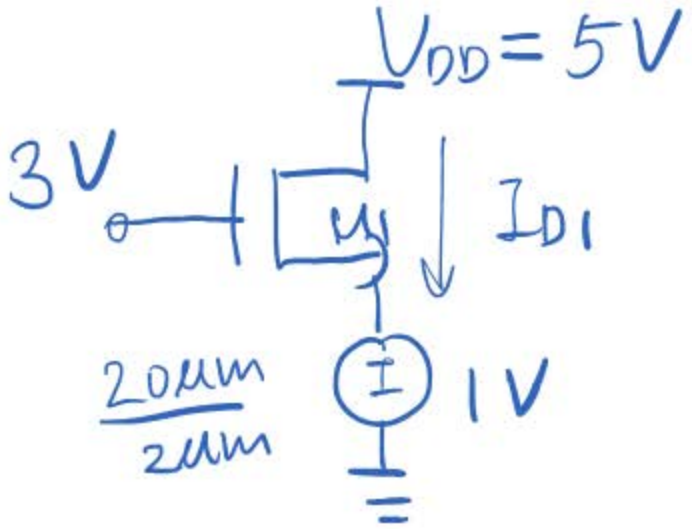
$V_g = V_G + v_g$

$V_d = V_D + v_d$

$I_D \uparrow\ i_d = gm \cdot v_{gs} \downarrow\ i_d = gmb \cdot v_{sb}$



$$I_D = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L_{eff}}\right)(V_{SG} - |V_{TH}|)^2(1 + \lambda V_{SD})$$



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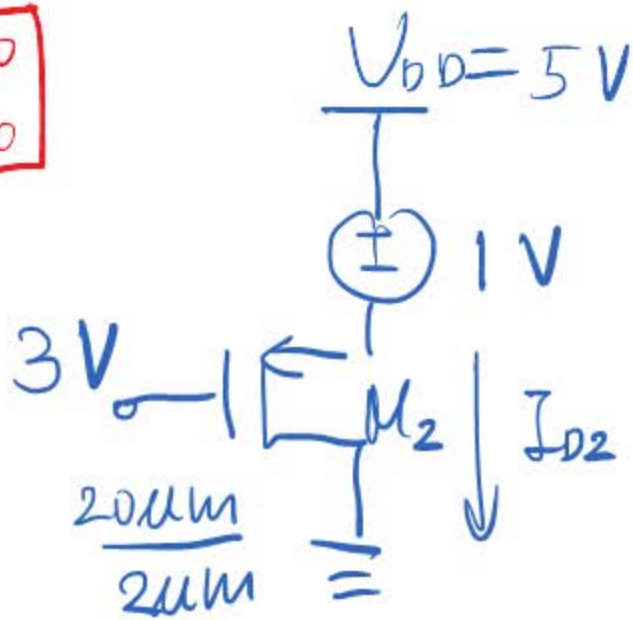


$V_{DS1}=4V$ $V_{SB}=1V$

$V_{GS1}=2V$

$V_{TH1}=0.7+0.45(\sqrt{0.9+1}-\sqrt{0.9})$

$V_{DS1} > V_{GS1}-V_{TH1}$

$V_{SD2}=4V$

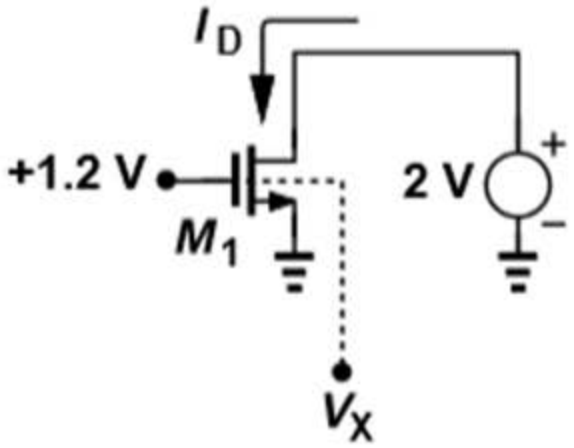
$V_{SG2}=1V$ $V_{BS2}=1V$

$|V_{TH2}|=0.8+0.4(\sqrt{0.8+1}-\sqrt{0.8})$

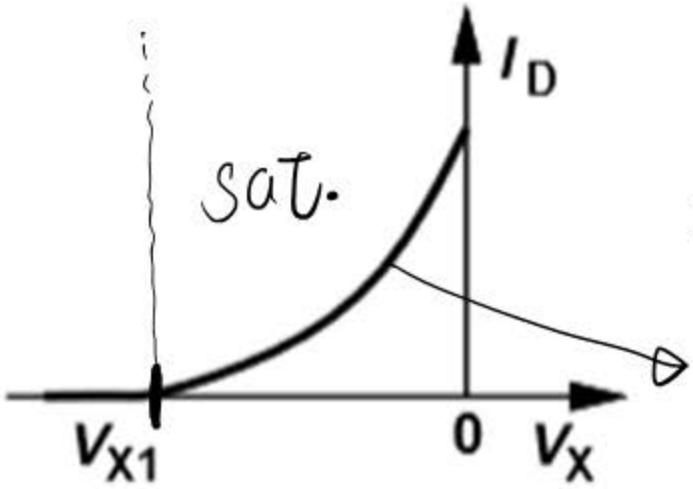
$V_{SD2} > V_{SG2}-|V_{TH2}|$

Example

Sketch I_D as a function of V_X increasing from $-\infty$ to 0. Assume V_{TH0} = 0.6 V, γ = 0.4 $V^{1/2}$ and $2\Phi_F$ = 0.7 V.



Solution:



$= -4.76$ V

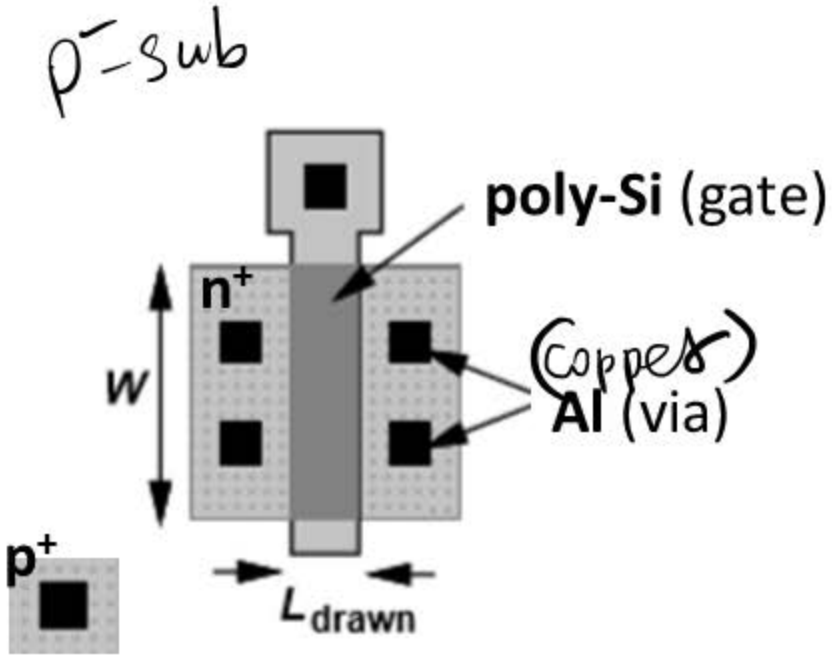
$$1.2 = 0.6 + 0.4(\sqrt{0.7 - V_{X1}} - \sqrt{0.7}),\ V_{X1} = -4.76\ \text{V}.$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L_{eff}}\right)(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

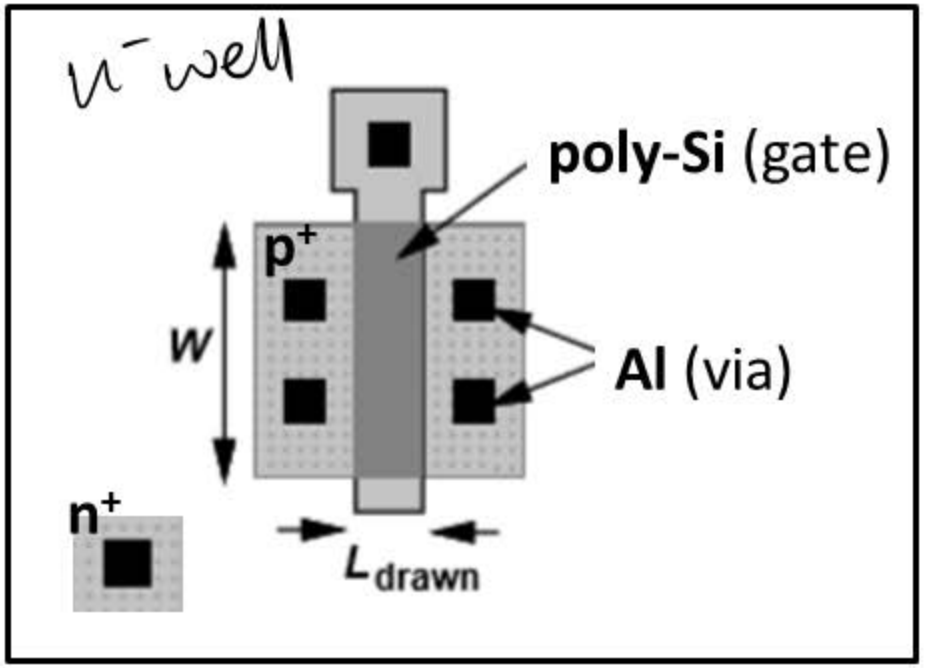
$V_{GS} = 1.2$, $V_{DS} = 2$

Layout

NMOS



PMOS



- W/L is chosen to determine gm. Minimum L is dictated by the process.
- Design rules: (1) Poly-Si extends beyond the channel area by some amount. (2) Enough n^+, p^+ or poly-Si area surrounding each via. (3) Enough distance between two vias. (4) Many others.

SPICE Model

NMOS Model

LEVEL = 1	VTO = 0.7	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08e−6	UO = 350	LAMBDA = 0.1
TOX = 9e−9	PB = 0.9	CJ = 0.56e−3	CJSW = 0.35e−11
MJ = 0.45	MJSW = 0.2	CGDO = 0.4e−9	JS = 1.0e−8

related to parasitic capacitances will learn how to use these in Ve413

PMOS Model

LEVEL = 1	VTO = −0.8	GAMMA = 0.4	PHI = 0.8
NSUB = 5e+14	LD = 0.09e−6	UO = 100	LAMBDA = 0.2
TOX = 9e−9	PB = 0.9	CJ = 0.94e−3	CJSW = 0.32e−11
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e−9	JS = 0.5e−8

- Simulators such as SPICE and Cadence need accurate models for each device.
- Above is the simplest MOS SPICE model, known as “Level 1,” and provide typical values for each parameter corresponding to 0.5-µm technology.

VTO: threshold voltage with zero V_{SB} (unit: V)
GAMMA: body effect coefficient (unit: $V^{1/2}$)
PHI: $2\Phi_F$ (unit: V)
TOX: gate oxide thickness (unit: m)
NSUB: substrate doping (unit: cm^{-3})
LD: source/drain side diffusion (unit: m)
UO: channel mobility (unit: $cm^2/V/s$)
LAMBDA: channel-length modulation coefficient (unit: V^{-1})
CJ: source/drain bottom-plate junction capacitance per unit area (unit: F/m^2)
CJSW: source/drain sidewall junction capacitance per unit length (unit: F/m)
PB: source/drain junction built-in potential (unit: V)
MJ: exponent in CJ equation (unitless)
MJSW: exponent in CJSW equation (unitless)
CGDO: gate-drain overlap capacitance per unit width (unit: F/m)
CGSO: gate-source overlap capacitance per unit width (unit: F/m)
JS: source/drain leakage current per unit area (unit: A/m^2)

NMOS vs PMOS in Performance

- PMOS devices are quite inferior to NMOS in most CMOS technology.
- Lower mobility of holes ($\mu_p C_{ox} \approx 0.5\mu_n C_{ox}$) yield lower current drive and conductance.
- NMOS exhibit higher output resistance, providing more ideal current sources and higher voltage gain.
- It is preferable to use NMOS rather than PMOS wherever possible.