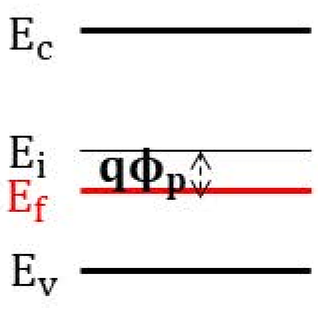
Summary

p-type

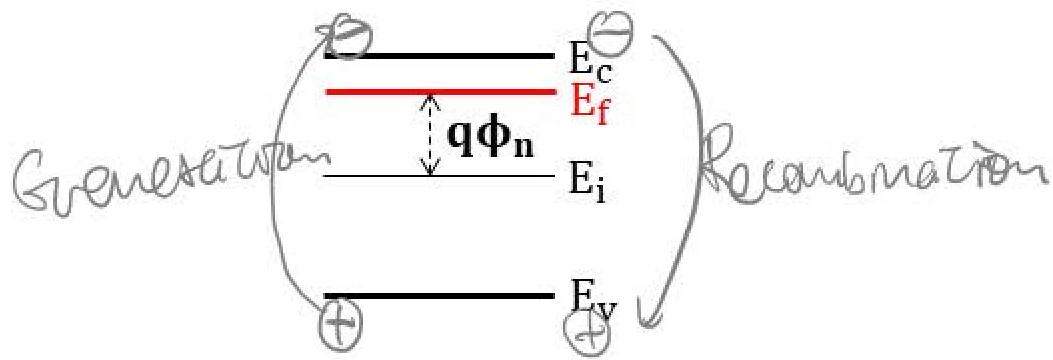


$$p = N_a = n_i e^{\frac{E_i - E_f}{kT}} = n_i e^{\frac{q\phi_p}{kT}}$$

$$n = \frac{{n_i}^2}{N_a} = n_i e^{\frac{E_f - E_i}{kT}} = n_i e^{\frac{-q\phi_p}{kT}}$$

$$np = {n_i}^2$$

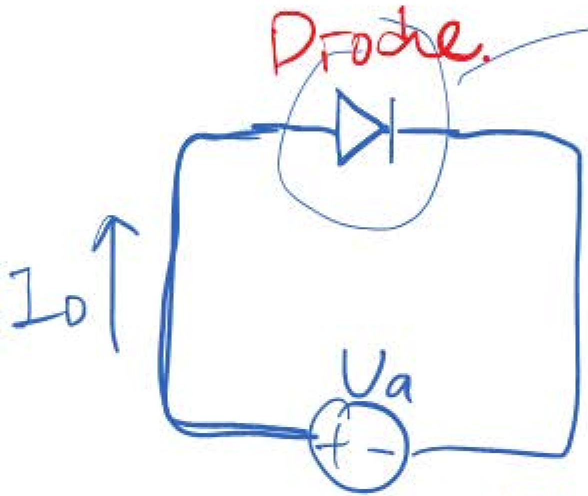
n-type



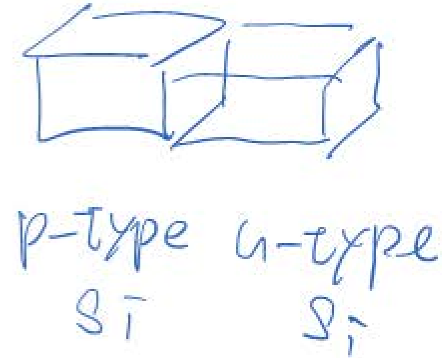
$$n = N_d = n_i e^{\frac{E_f - E_i}{kT}} = n_i e^{\frac{q\phi_n}{kT}}$$

$$p = \frac{{n_i}^2}{N_d} = n_i e^{\frac{E_i - E_f}{kT}} = n_i e^{\frac{-q\phi_n}{kT}}$$

$$np = {n_i}^2$$



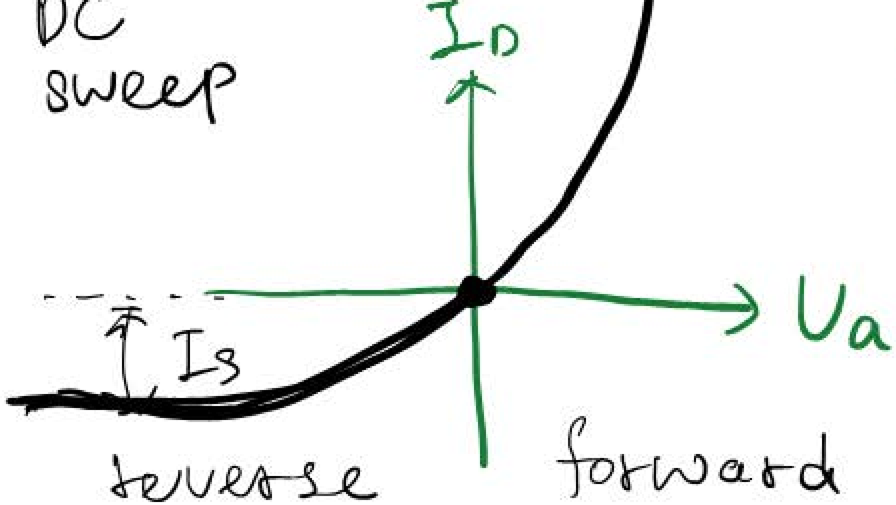
At 300 K



$$I_D = I_s\left(e^{\frac{qU_a}{kT}} - 1\right) = I_s\left(e^{\frac{U_a}{(kT/q)}} - 1\right)$$

$$= I_s\left(e^{\frac{U_a}{0.026}} - 1\right)$$

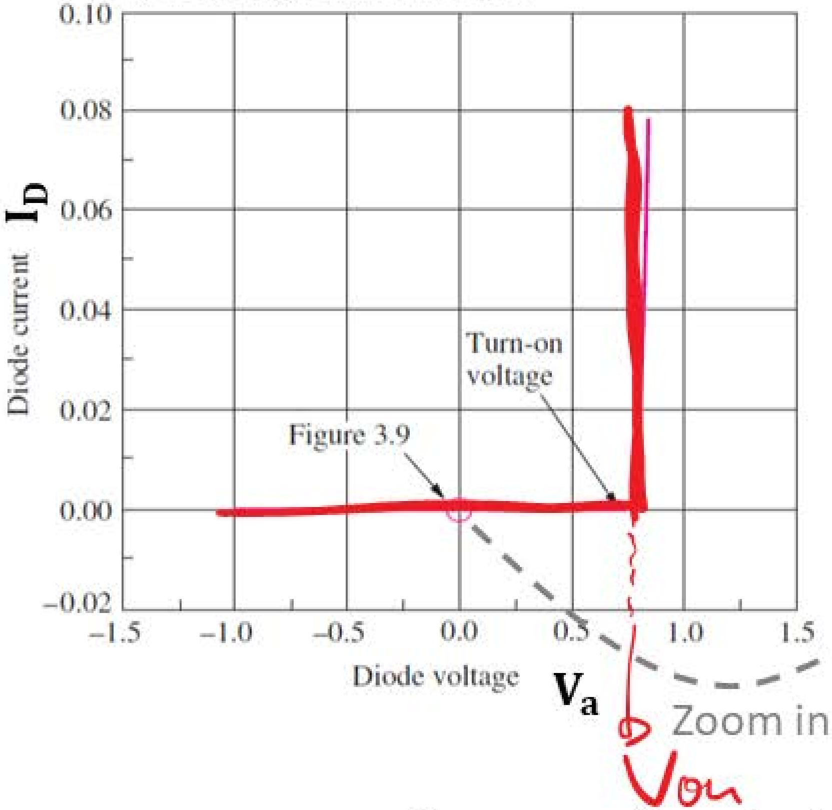
DC sweep

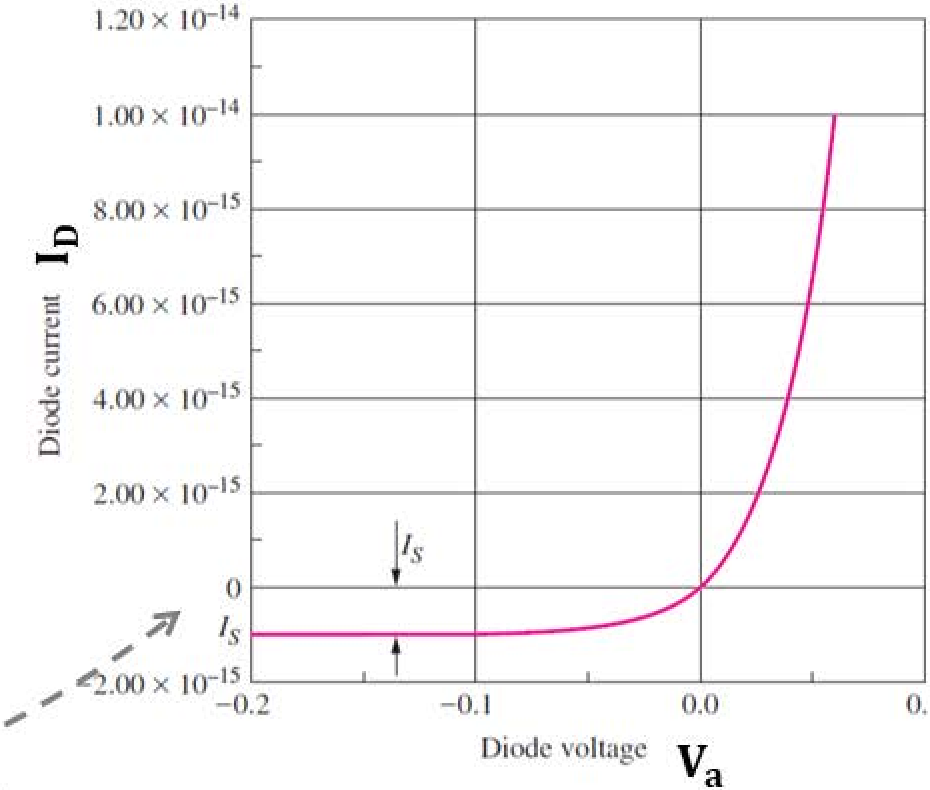


Si Diode I-V Characteristics

$$\mathbf{I_D = I_S\left(e^{\frac{qV_a}{kT}} - 1\right)}$$

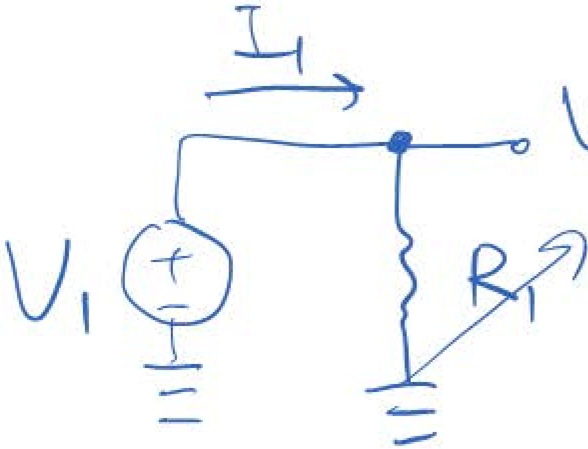
Source: Microelectronic Circuit Design, 4th Edition, by R. C. Jaeger and T. N. Blalock





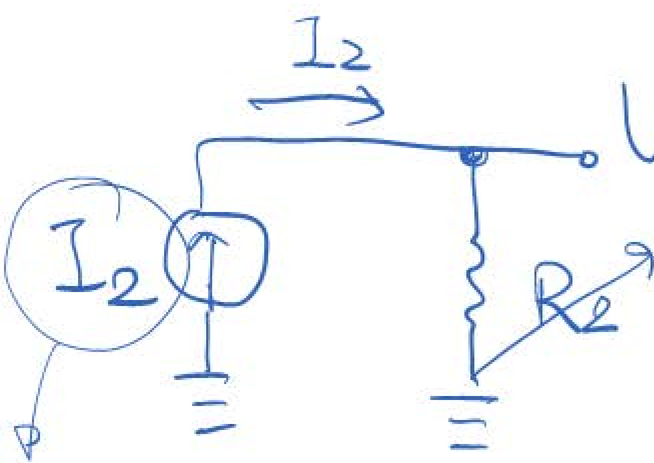
- Turn-on voltage typically 0.5 to 0.7 V
- Saturation current (I_S) typically 10^{-18} to 10^{-9} A
- $kT/q = 0.025875$ V at 300 K

constant



$$V_{out1} = V_1, \quad I_1 = \frac{V_1}{R_1}$$

constant



$$V_{out2} = I_2 R_2, \quad I_2$$

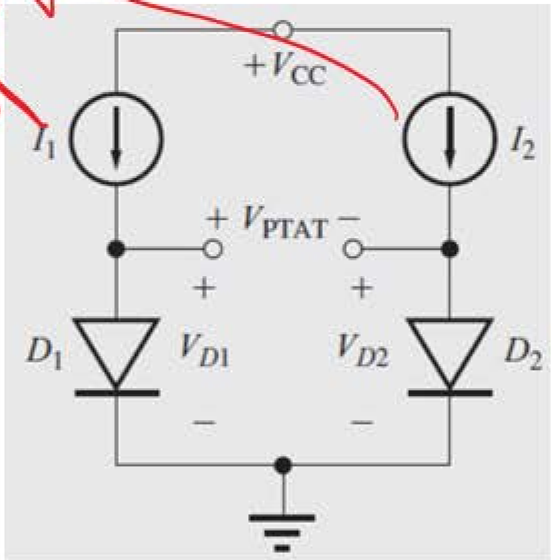
Ideal current source

A Voltage Proportional to Absolute Temperature

- For a fixed $I_D \gg I_S$:

$$I_D = I_S\left(e^{\frac{qV_a}{kT}} - 1\right) \Rightarrow V_a = \frac{kT}{q}\ln\left(\frac{I_D}{I_S} + 1\right) \cong \frac{kT}{q}\ln\frac{I_D}{I_S}$$

Ideal current sources



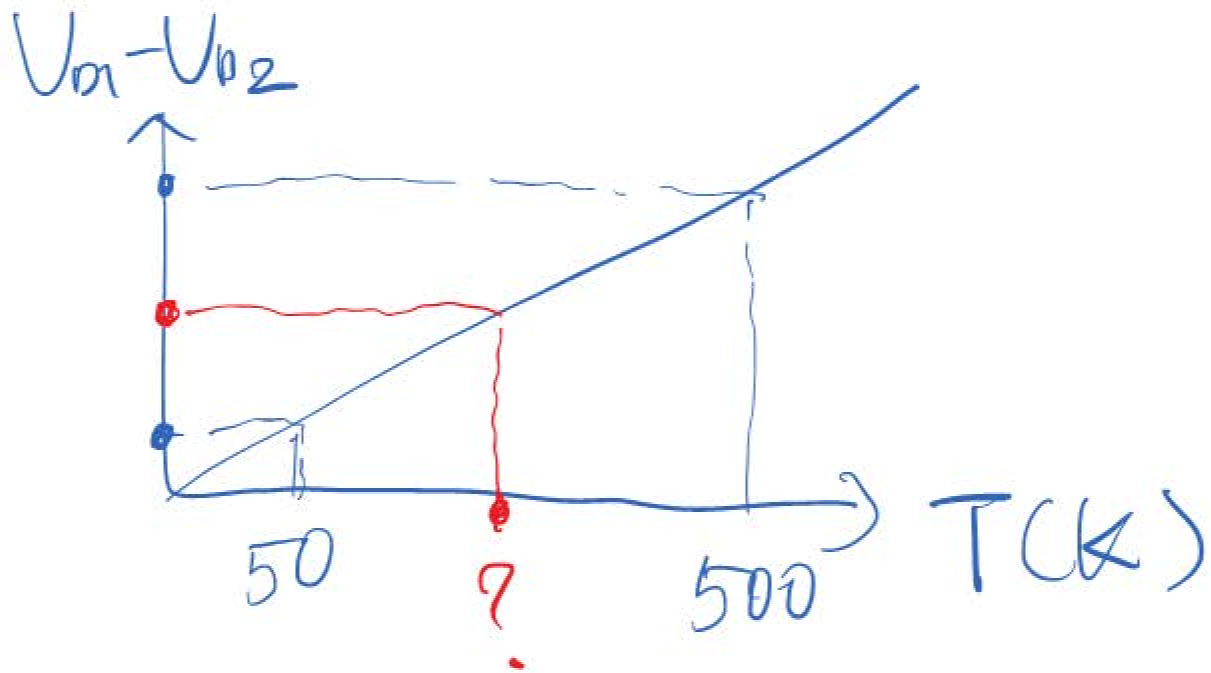
Source: Microelectronic Circuit Design, 4th Edition, by R. C. Jaeger and T. N. Blalock

$$\begin{cases} V_{D1} = \dfrac{kT}{q}\ln\dfrac{I_1}{I_S} \\ V_{D2} = \dfrac{kT}{q}\ln\dfrac{I_2}{I_S} \end{cases}$$

I_1 and I_2 are ideal current source.

$$\boxed{V_{PTAT} = V_{D1} - V_{D2} = \frac{kT}{q}\ln\frac{I_1}{I_2} = T \times \text{constant}}$$

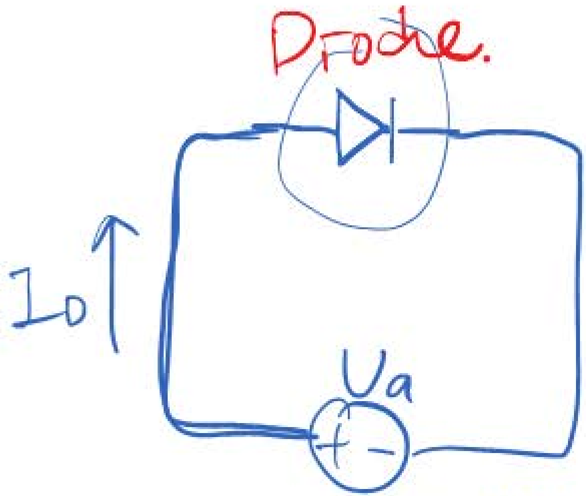
constant.



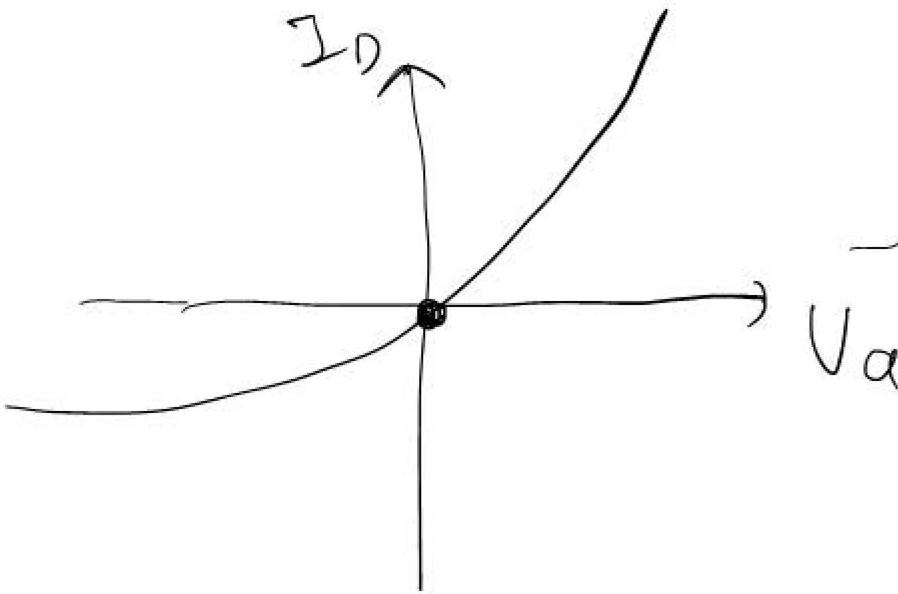
$V_{D1}-V_{D2}$
50
?
500
T(K)

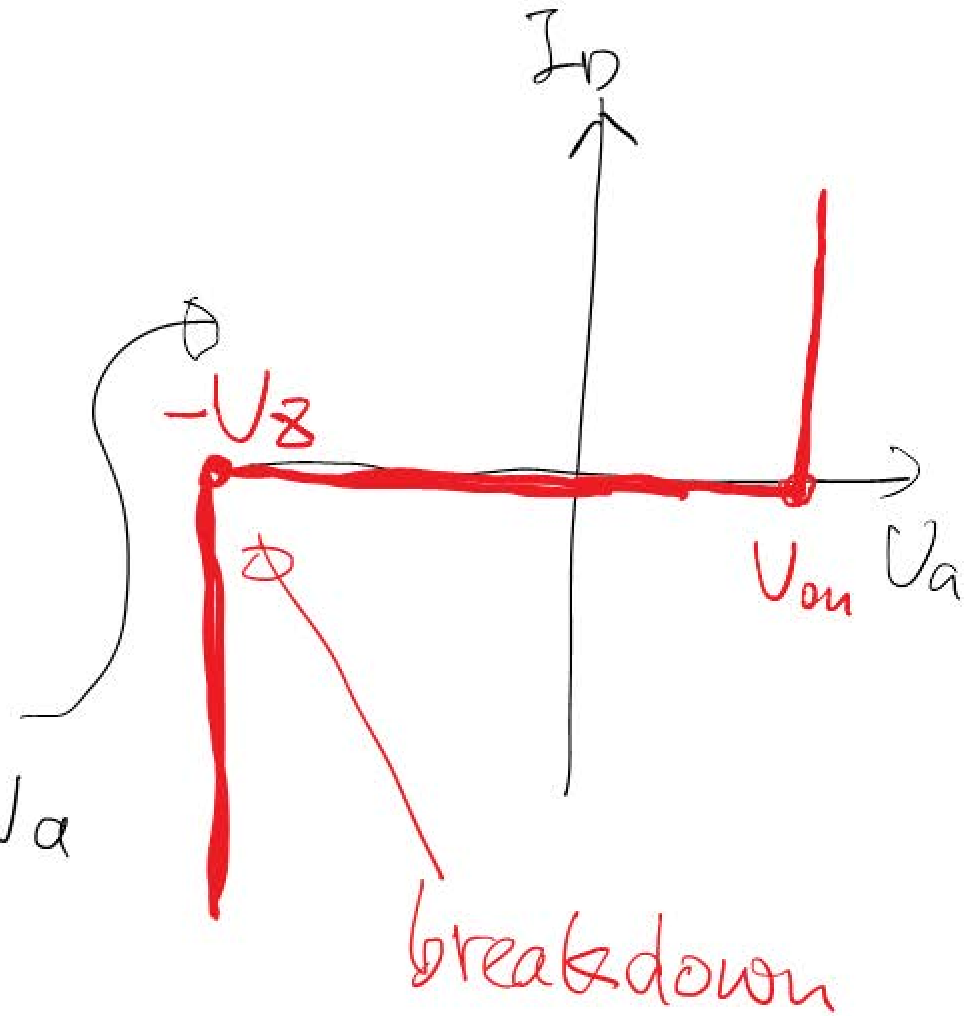
Diode in Reverse Bias

(IV curve)

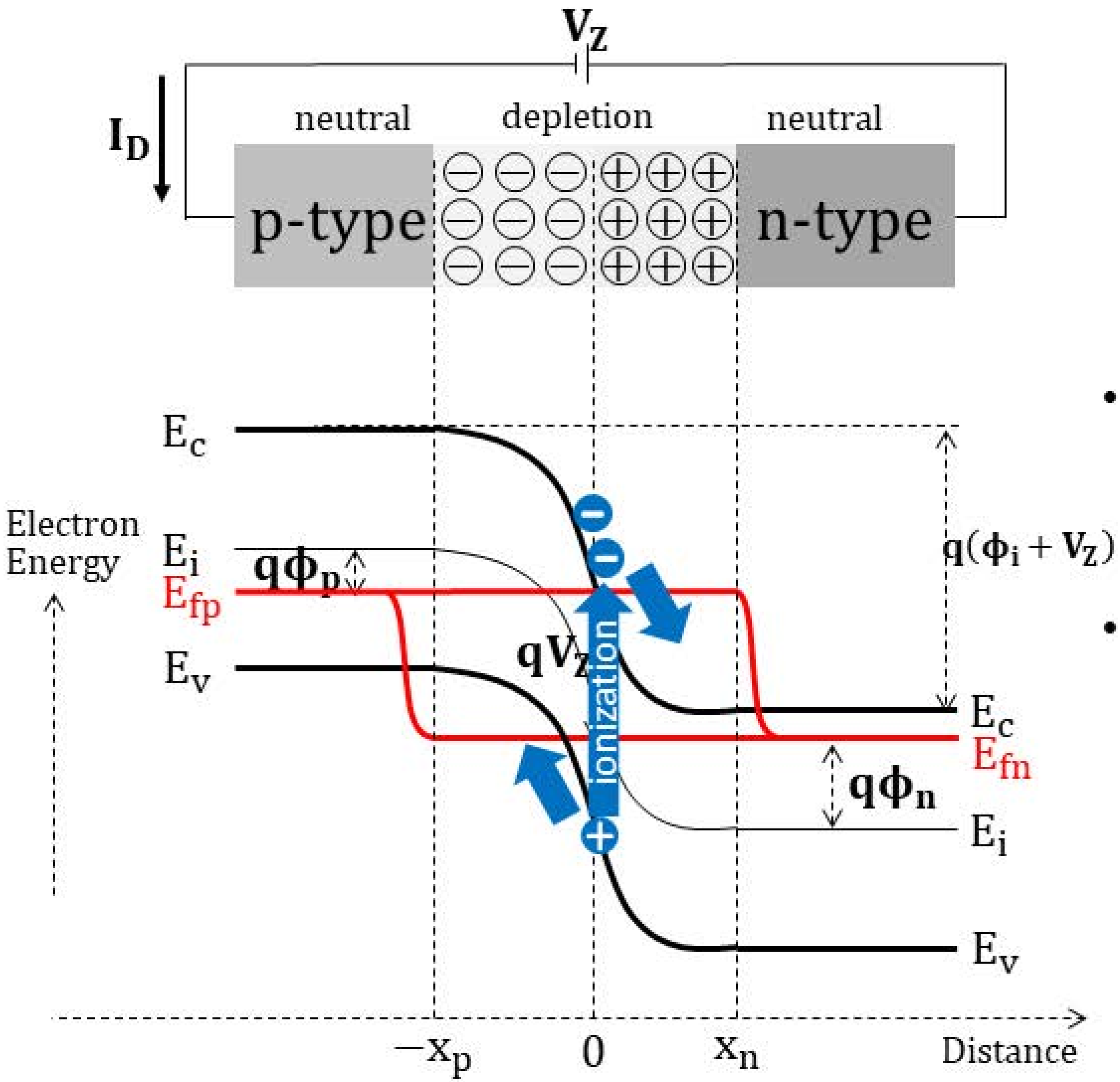


$$I_D = I_S\left(e^{\frac{qV_a}{kT}} - 1\right)$$



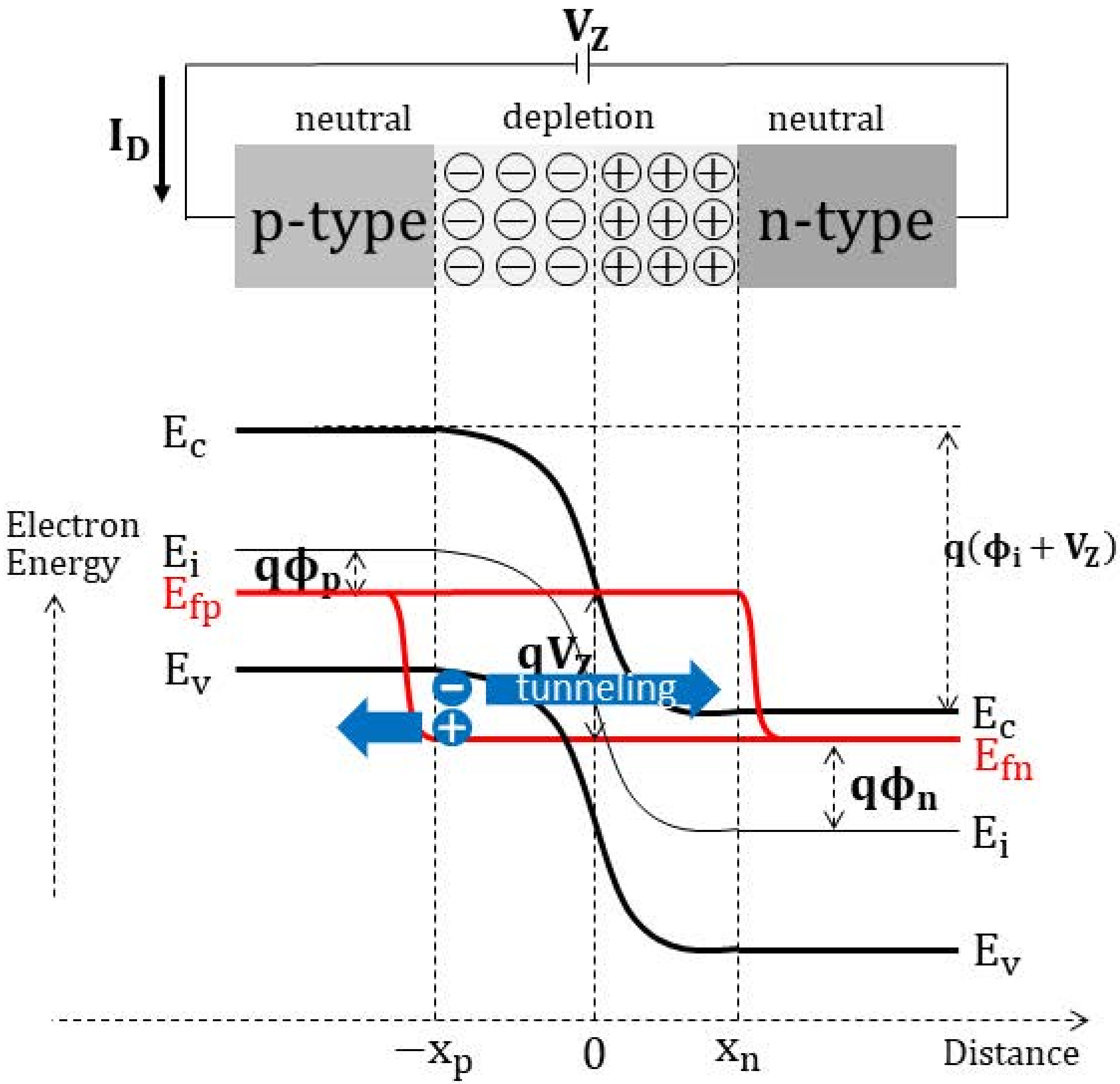


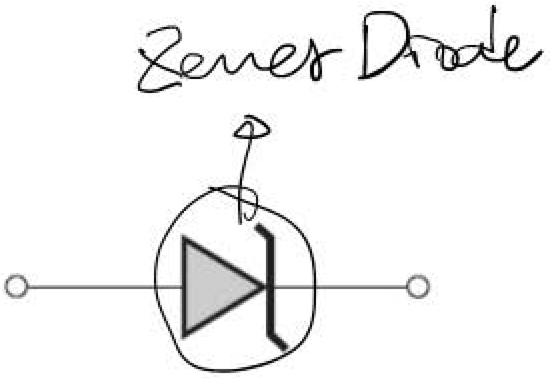
Avalanche Breakdown in Reverse Bias



- Si diode with breakdown voltages greater than about 5.6 V enter breakdown through an avalanche mechanism.
- Carriers accelerated by electric field gain sufficient energy to break covalent bonds upon impact, thereby creating electron-hole pairs.

Zener Breakdown in Reverse Bias





- **Si diode with very heavy doping (i.e. very narrow depletion region)** easily enter into Zener breakdown under reverse bias.
- Electrons tunnel directly between valence and conduction bands.

Diode Spice Model and Layout

Diode Spice Model

$$I_D = \mathbf{IS}\left[\exp\left(\frac{qV_a}{\mathbf{N}kT}\right) - 1\right]$$

$\frac{1}{sC} = \frac{1}{j\omega C}$

parasitic capacitance

$$\boxed{C_D = \mathbf{TT}\frac{I_D}{\mathbf{N}(kT/q)} \qquad C_j = \frac{\mathbf{CJO}}{(1 - \frac{V_a}{\mathbf{VJ}})^{\mathbf{M}}}\mathbf{RAREA}}$$

Not covered in Ve311

TABLE 3.1

SPICE Diode Parameter Equivalences

PARAMETER	SPICE	TYPICAL DEFAULT VALUES
Saturation current	IS	10 fA
Ohmic series resistance	RS	0 Ω
Ideality factor or emission coefficient	N	1
Transit time	TT	0 sec
Zero-bias junction capacitance for a unit area diode RAREA = 1	CJO	0 F/m^2
Built-in potential	VJ	1 V
Junction grading coefficient	M	0.5
Relative junction area	RAREA	1 m^2

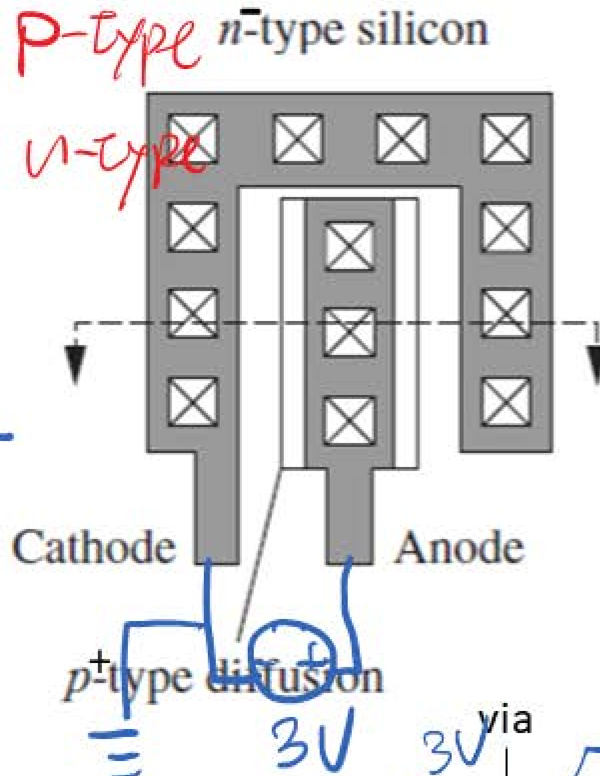
Source: Microelectronic Circuit Design, 4th Edition, by R. C. Jaeger and T. N. Blalock

Diode Layout

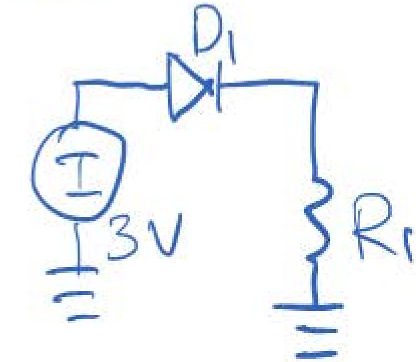
p+: heavily doped P-type

n-: lightly doped n-type

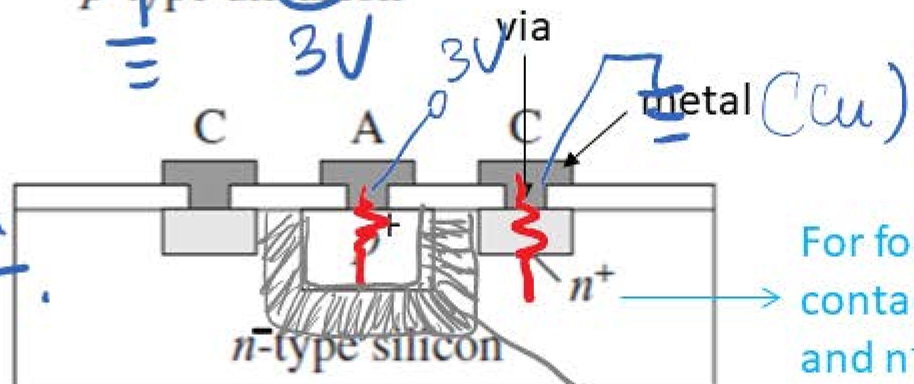
Top View



Schematic.



Cross Section

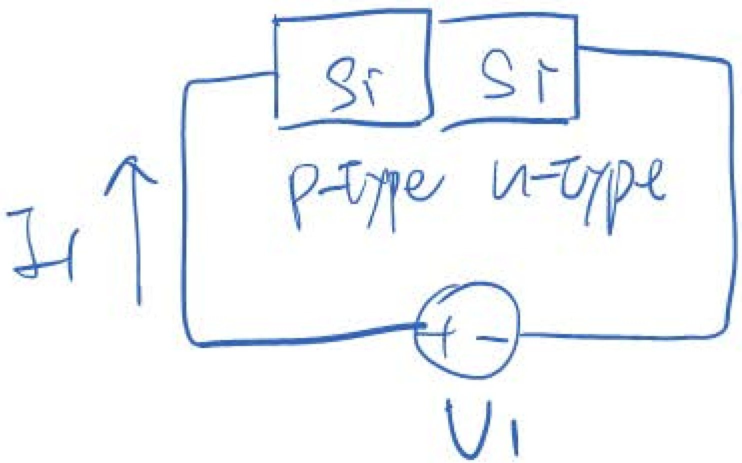


pn junction diode

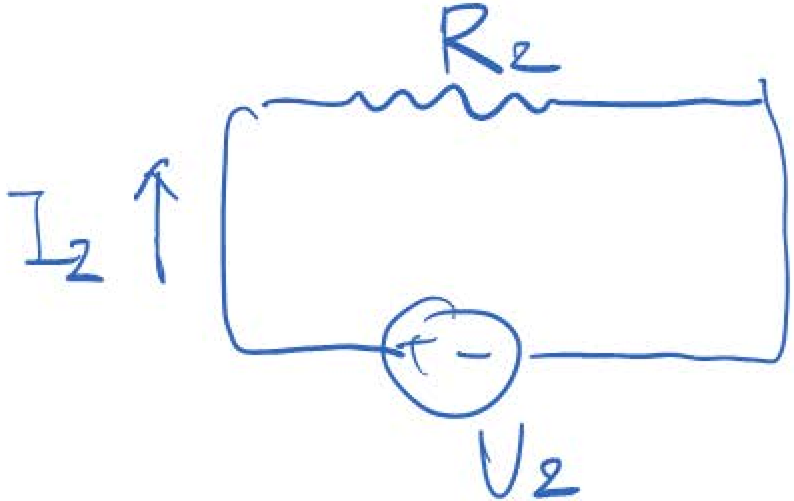
For forming a ohmic contact between metal and n^- type silicon

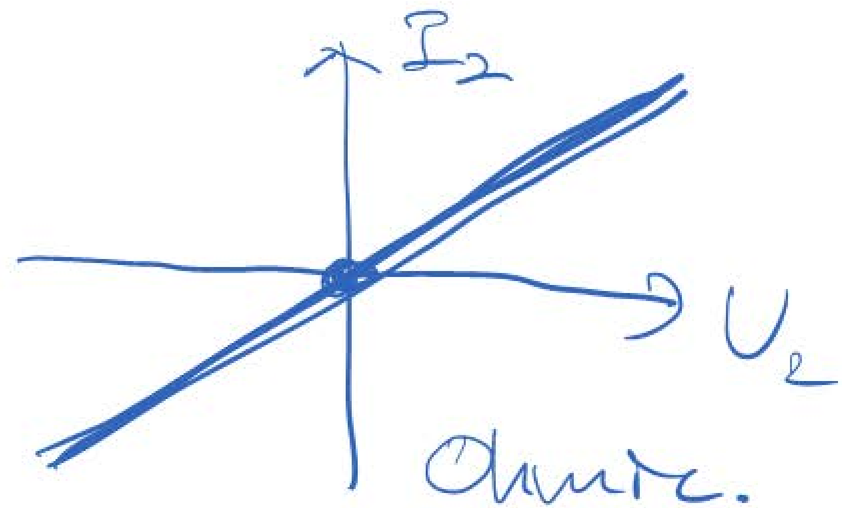
depletion region

Source: Microelectronic Circuit Design, 4th Edition, by R. C. Jaeger and T. N. Blalock



Rectifying





Ohmic.