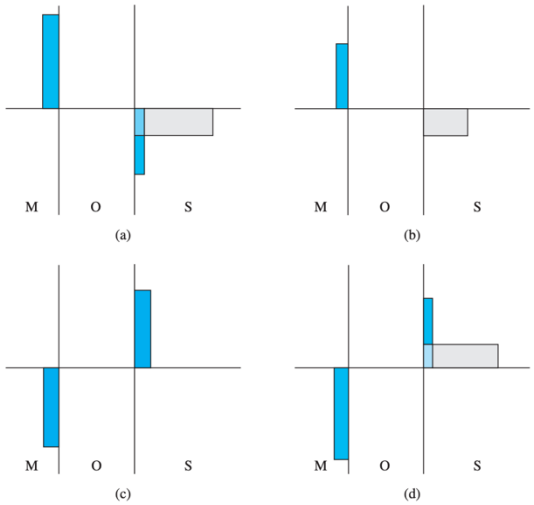
VE320 Homework Eight
Due: 2021/7/28 23:59

1. The dc charge distributions of four ideal MOS capacitors are shown in the figure below. For each case:
   (a) Is the semiconductor n or p type?
   (b) Is the device biased in the accumulation, depletion, or inversion mode?
   (c) Draw the energy band diagram in the semiconductor region.



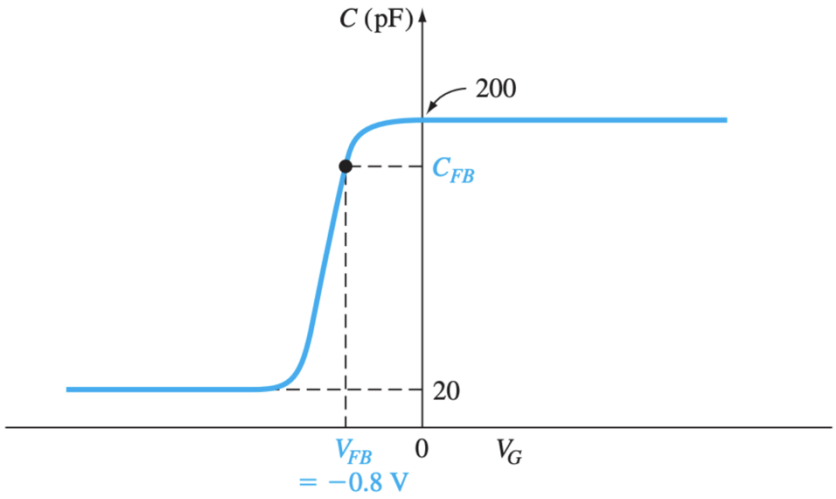
2. (a) Consider an n^+ polysilicon-silicon dioxide-n-type silicon MOS structure. Let $N_d = 4 \times 10^{15}$ cm^{-3}. Calculate the ideal flat-band voltage for $t_{ox} = 20$ nm $= 200$Å
   (b) Considering the results of part (a), determine the shift in flat-band voltage for (i) $Q'_{ss} = 4 \times 10^{10}$ cm^{-2} and (ii) $Q'_{ss} = 10^{11}$ cm^{-2}.
   (c) Repeat parts (a) and (b) for an oxide thickness of $t_{ox} = 12$ nm $= 120$Å

3. A MOS device with an aluminum gate is fabricated on a p-type silicon substrate. The oxide thickness is $t_{ox} = 22$ nm $= 220$Å and the trapped oxide charge is $Q'_{ss} = 4 \times 10^{10}$ cm^{-2}. The measured threshold voltage is $V_T = +0.45$ V. Determine the p-type doping concentration.

4. An n^+ polysilicon gate-silicon dioxide-silicon MOS capacitor has an oxide thickness of $t_{ox} = 18$ nm $= 180$Å and a doping of $N_a = 10^{15}$ cm^{-3}. The oxide charge density is $Q'_{ss} = 6 \times 10^{10}$ cm^{-2}. Calculate the (a) flat-band voltage and (b) threshold voltage.

5. The high-frequency $C - V$ characteristic curve of a MOS capacitor is shown in the figure below. The area of the device is 2×10^{-3} cm^2. The metal-semiconductor work function difference is $\phi_{ms} = -0.50$ V, the oxide is SiO_2, the semiconductor is silicon, and the semiconductor doping concentration is 2×10^{16} cm^{-3}.
   (a) Is the semiconductor n or p type?
   (b) What is the oxide thickness?
   (c) What is the equivalent trapped oxide charge density?

(d) Determine the flat-band capacitance.



6. Consider a p-channel MOSFET with the following parameters: $k_p' = 0.12\ \text{mA/V}^2$ and $W/L = 20$. The drain current is $100\mu\text{A}$ with applied voltages of $V_{SG} = 0$, $V_{BS} = 0$, and $V_{SD} = 1.0$ V.
   (a) Determine the V_T value.
   (b) Determine the drain current I_D for $V_{SG} = 0.4$ V, $V_{SB} = 0$, and $V_{SD} = 1.5$ V.
   (c) What is the value of I_D for $V_{SG} = 0.6$ V, $V_{SB} = 0$, and $V_{SD} = 0.15$ V?

7. An NMOS device has the following parameters: n^+ poly gate, $t_{\text{ox}} = 400\text{Å}$, $N_a = 10^{15}\ \text{cm}^{-3}$, and $Q_{ss}' = 5 \times 10^{10}\ \text{cm}^{-2}$
   (a) Determine V_T.
   (b) Is it possible to apply a V_{SB} voltage such that $V_T = 0$? If so, what is the value of V_{SB}?