**VE320 Homework Nine**
**Due: 2021/8/6 23:59**

**(Note: In the following problems, assume the semiconductor and oxide in the MOS system are silicon and silicon dioxide, respectively, and assume the temperature is $T = 300$ K unless otherwise stated.)**

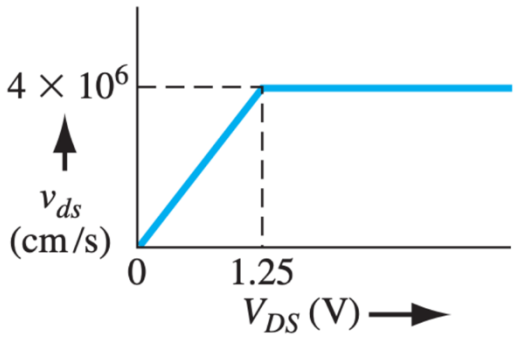
1. Assume that the subthreshold current of a MOSFET is given by

$$I_D = 10^{-15}\exp\left(\frac{V_{GS}}{(2.1)V_t}\right)$$

over the range $0 \le V_{GS} \le 1$ volt and where the factor 2.1 takes into account the effect of interface states. Assume that $10^6$ identical transistors on a chip are all biased at the same $V_{GS}$ and at $V_{DD} = 5$ V.
(a) Calculate the total current that must be supplied to the chip at $V_{GS} = 0.5, 0.7,$ and 0.9 V.
(b) Calculate the total power dissipated in the chip for the same $V_{GS}$ values.

2. Consider an n-channel silicon MOSFET. The parameters are $k_n' = 75\mu\text{A/V}^2$, $W/L = 10$, and $V_T = 0.35$ V. The applied drain-to-source voltage is $V_{DS} = 1.5$ V
(a) For $V_{GS} = 0.8$ V, find $(i)$ the ideal drain current, $(ii)$ the drain current if $\lambda = 0.02\ \text{V}^{-1}$, and $(iii)$ the output resistance for $\lambda = 0.02\ \text{V}^{-1}$.
(b) Repeat part (a) for $V_{GS} = 1.25$ V.

3. The parameters of an n-channel enhancement-mode MOSFET are $V_T = 0.40$ V, $t_{ox} = 20$ nm $= 200$Å, $L = 1.0\mu$m, and $W = 10\mu$m.
(a) Assuming a constant mobility of $\mu_n = 475\ \text{cm}^2/\text{V}\cdot s$, calculate $I_D$ for $V_{GS} - V_T = 2.0$ V when biased at (i) $V_{DS} = 0.5$ V, (ii) $V_{DS} = 1.0$ V, (iii) $V_{DS} = 1.25$ V and (iv) $V_{DS} = 2.0$ V
(b) Consider the piecewise linear model of the carrier velocity versus $V_{DS}$ shown in the figure below. Calculate $I_D$ for the same voltage values given in part (a).
[See equation $I_D(\text{sat}) = WC_{\text{ox}}(V_{GS} - V_T)v_{\text{sat}}$]
(c) Determine the $V_{DS}(\text{sat})$ values for parts (a) and (b).




**(Note: In the following problems, use the transistor geometry shown in Figure**

**12.13. Assume $T = 300$ K unless otherwise stated.)**

4. Consider a $p^{++}n^{+}p$ bipolar transistor, uniformly doped in each region. Sketch the energy-band diagram for the case when the transistor is
   (a) in thermal equilibrium,
   (b) biased in the forward-active mode,
   (c) biased in the inverse-active region, and
   (d) biased in cutoff with both the $B-E$ and $B-C$ junctions reverse biased.

5. A uniformly doped silicon npn bipolar transistor at $T = 300$ K is biased in the forward-active mode. The doping concentrations are $N_E = 8 \times 10^{17}$ cm$^{-3}$, $N_B = 2 \times 10^{16}$ cm$^{-3}$, and $N_C = 10^{15}$ cm$^{-3}$.
   (a) Determine the thermal-equilibrium values $p_{E0}, n_{B0}$, and $p_{C0}$.
   (b) For $V_{BE} = 0.640$ V, calculate the values of $n_B$ at $x = 0$ and $p_E$ at $x' = 0$.
   (c) Sketch the minority carrier concentrations through the device and label each curve.

6. A uniformly doped pnp silicon bipolar transistor has a base doping of $N_B = 10^{16}$ cm$^{-3}$, a collector doping of $N_C = 10^{15}$ cm$^{-3}$, a metallurgical base width of $x_{B0} = 0.70\mu$m, a base minority carrier diffusion coefficient of $D_B = 10\text{cm}^2/s$, and a B-E cross-sectional area of $A_{BE} = 10^{-4}$ cm$^2$. The transistor is biased in the forward-active mode with $V_{EB} = 0.625$ V. Neglecting the $B-E$ space charge width and assuming $x_B \ll L_B$,
   (a) determine the change in neutral base width as $V_{BC}$ changes from 1 to 5 V,
   (b) find the corresponding change in collector current,
   (c) estimate the Early voltage
   (d) find the output resistance.