VE370 HW6 周维炀 518021911039

1. IF. ID. EX stage: IF.Flush = ID.Flush = Ex.Flush = 0
Cause = X, EPC = X, MUX_Input = X, MUX_Sel = X

MEM stage: IF.Flush = ID.Flush = EX.Flush = 1
EPC = Address of "sw" + 4, MUX_Sel = 01
Cause = the code of memory access exception.
MUX_Input = the address of handler of memory access exception.

2. (1). I, J
(2). A[J][I]

3. (1).

	Binary address	tag	index	Hit/Miss
4:	100	0	100	M
12:	1100	1	100	M
33:	100001	100	001	M
6:	110	0	110	M
187:	10111011	10111	011	M
65:	1000001	1000	001	M
186:	10111010	10111	010	M
19:	10011	10	011	M
125:	1111101	1111	101	M
43:	101011	101	011	M
152:	10011000	10011	000	M
253:	11111101	11111	101	M

(2).

	Binary address	tag	index	Hit/Miss
4:	100	0	10	M
12:	1100	1	10	M
33:	100001	100	00	M
6:	110	0	11	M
187:	10111011	10111	01	M
65:	1000001	1000	00	M
186:	10111010	10111	01	H
19:	10011	10	01	M
125:	1111101	1111	10	M
43:	101011	101	01	M
152:	10011000	10011	00	M
253:	11111101	11111	10	M

(3). C1: 0 hit $(35+2)\times 12 = 444$

C2: 1 hit $(35+3)\times 11 + 3 = 421$

C3: 0 hit $(35+5)\times 12 = 480$

Therefore, C2 is the best cache design

4. (1). bit 1 to 0: byte offset
bit 6 to 2: word offset $\Rightarrow$ $2^5 = 32$ words in one block
bit 11 to 7: index $\Rightarrow$ $2^5 = 32$ lines

For one line: $32\times 32 + 1 + 1 + 20 = 1046$ bits

Size of cache: $32 \times 1046 = 33472$ bits

(2). Ratio $= \frac{33472}{32^3} = 1.0215$

(3).

	Binary address	tag	index	Hit/Miss
0	0	0	00000	M
4	100	0	00000	H
20	10100	0	00000	H
136	10001000	0	00001	M
232	11101000	0	00001	H
164	10100100	0	00001	H
1024	10000000000	0	01000	M
30	11110	0	00000	H
140	10001100	0	00001	H
3100	110000011100	0	11000	M
176	10110000	0	00001	H
2180	100010000100	0	10001	M

0 blocks are replaced.

(4). hit ratio $= \frac{7}{12} = 58.33\%$

(5). < 00000, 0, word[0] word[1] ··· word[31] >

< 00001, 0, word[32] word[33] ··· word[63] >

< 01000, 0, word[256] word[257] ··· word[287] >

< 10001, 0, word[544] word[545] ··· word[575] >

< 11000, 0, word[768] word[769] ··· word[799] >