VE370 HW8 Sample Solution

Problem 1

1. $1.18 + 0.073 \cdot 5.34 + 0.073 \cdot 0.015 \cdot 70 = 1.65\text{ns}$
2. $1.65/1.18 \cdot 0.36 + 1 \cdot 0.64 = 1.14$

Problem 2

1.

Block Address	Hit/Miss	Evicted Block	Contents of cache	
			Set 0	Set 1
1	Miss	-		Block[1]
3	Miss	-		Block[1] Block[3]
5	Miss	1		Block[5] Block[3]
1	Miss	3		Block[5] Block[1]
3	Miss	5		Block[3] Block[1]
1	Hit	-		Block[3] Block[1]
3	Hit	-		Block[3] Block[1]
5	Miss	1		Block[3] Block[5]
3	Hit	-		Block[3] Block[5]

3 hits

2.

Block Address	Hit/Miss	Evicted Block	Contents of cache	
			Set 0	Set 1
1	Miss	-		Block[1]
3	Miss	-		Block[1] Block[3]
5	Miss	3		Block[1] Block[5]
1	Hit	-		Block[1] Block[5]
3	Miss	1		Block[3] Block[5]
1	Miss	3		Block[1] Block[5]
3	Miss	1		Block[3] Block[5]
5	Hit	-		Block[3] Block[5]
3	Hit	-		Block[3] Block[5]

3 hits

3. 4 hits or fewer

Problem 3

1. 4 KB pages => 12 bits page offset

Virtual Address (decimal)	Virtual Address (hexadecimal)	Hit in TLB/ Hit in page table/ Page fault
12948	3294	Hit in TLB
49419	C10B	Page fault => Physical page 13 => T LB slot 3
46814	B6DE	Hit in TLB
13975	3697	Hit in TLB
40004	9C44	Page fault => Physical page 14 => T LB slot 1
12707	31A3	Hit in TLB
52236	CC0C	Hit in TLB

TLB:

Valid	Tag	Physical Page Number
1	11	12
1	9	14
1	3	6
1	12	13

Page Table:

Valid	Physical Page Number
1	5
0	Disk
0	Disk
1	6
1	9
1	11
0	Disk
1	4
0	Disk
1	14
1	3
1	12
1	13

2. 16 KB pages => 14 bits page offsets

Virtual Address (decimal)	Virtual Address (hexadecimal)	Virtual Page Number	Hit in TLB/ Hit in page table/ Page fault
12948	3294	0	Hit in page table => TLB slot 3
49419	C10B	3	Hit in TLB
46814	B6DE	2	Page fault => Physical page 13 => TLB slot 0
13975	3697	0	Hit in TLB
40004	9C44	2	Hit in TLB
12707	31A3	0	Hit in TLB
52236	CC0C	3	Hit in TLB

TLB:

Valid	Tag	Physical Page Number
1	2	13
1	7	4
1	3	6
1	0	5

Page table:

Valid	Physical Page Number
1	5
0	Disk
1	13
1	6
1	9
1	11
0	Disk
1	4
0	Disk
0	Disk
1	3
1	12

3. Larger page sizes allow for more addresses to be stored in a single page, potentially decreasing the amount of pages that must be brought in from disk and increasing the coverage of the TLB.
   However, if a program uses addresses in a sparse fashion (for example randomly addressing a large matrix), then there will be an extra penalty from transferring larger pages compared to smaller pages.
4. If you assume the TLB is empty at first, then

Virtual Address (decimal)	Virtual Address (hexadecimal)	Index	Tag	Hit in TLB/ Hit in page table/ Page fault
12948	3294	1	001	Hit in page table
49419	C10B	0	110	Page fault => Physical page 13 => TLB slot 0
46814	B6DE	1	101	Hit in page table
13975	3697	1	001	Hit in TLB
40004	9C44	1	100	Page fault => Physical page 14 => TLB slot 3
12707	31A3	1	001	Hit in TLB
52236	CC0C	0	110	Hit in TLB

TLB:

Index	Valid	Tag	Physical Page Number
0	1	6	13
	0		
1	1	1	6
	1	4	14

If you assume the TLB is the same as in (1), then the TLB:

Index	Valid	Tag	Physical Page Number
0	1	6	13
	1	7	4
1	1	4	14
	1	1	6