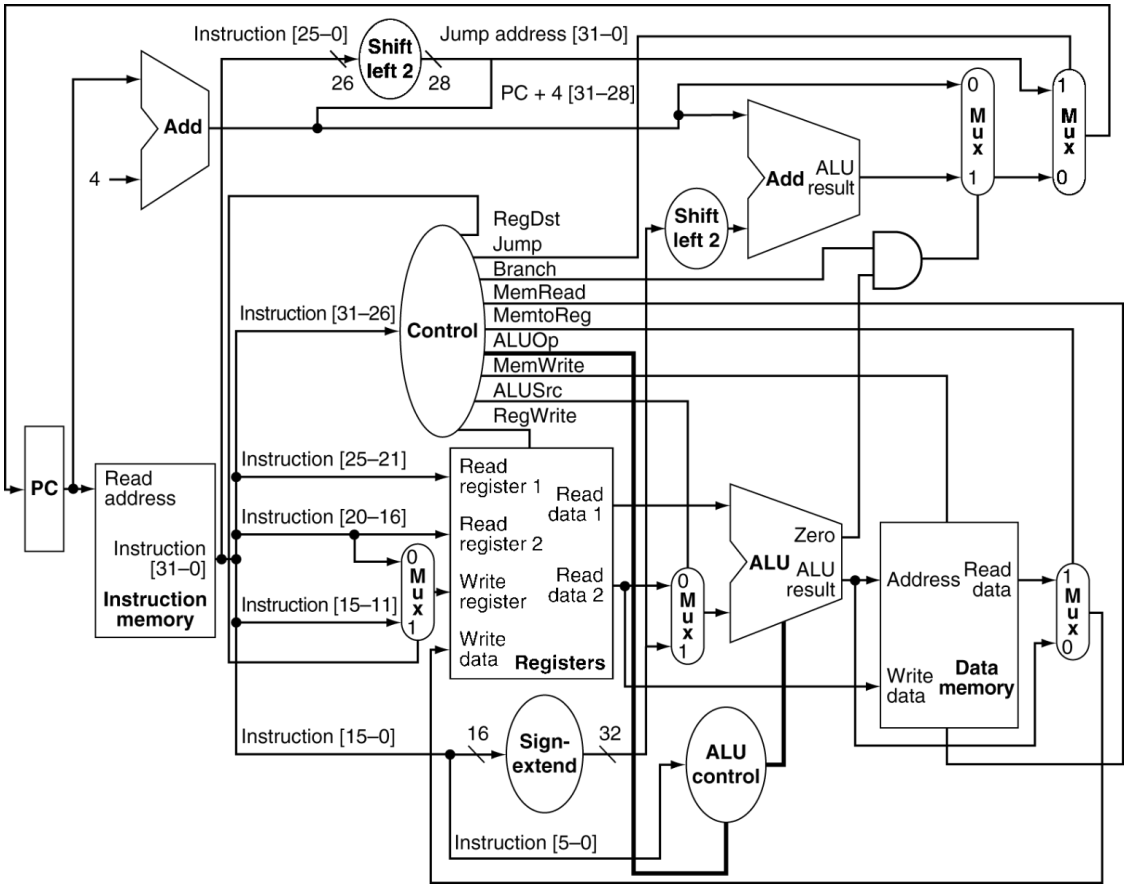
JOINT INSTITUTE
交大密西根学院

## Ve370 Introduction to Computer Organization

# Homework 3

All questions refer to the following figure.




1. (10 points) Given MIPS assembly instruction:
   `slti Rt, Rs, Imm`

   What are the values of the following control signals for this instruction?

   a. ALUSrc:
   b. RegDst:
   c. ALUOp
   d. MemWrite:
   e. MemRead:
   f. Branch:
   g. MemtoReg:
   h. RegWrite:

2. (5 points) Given MIPS assembly instruction:
   `andi Rt, Rs, Imm`

   Which resources (blocks) produce outputs, but their outputs are not used for this instruction?

a. Instruction Memory
b. Data Memory
c. Register File
d. ALU
e. Adder for PC+4
f. Adder for Branch target calculation
g. Sign Extend

3. (5 points) Given MIPS assembly instruction:
```
SW Rt, Offs(Rs)
```

Which resources produce no outputs for this instruction?
a. Instruction Memory
b. Data Memory
c. Register File
d. ALU
e. Adder for PC+4
f. Adder for Branch target calculation
g. Sign Extend

4. (10 points) Given latencies of blocks, determine the maximum clock frequency of the signal-cycle computer.

| **Inst. Mem** | **Add** | **Mux** | **ALU** | **Reg File** | **Data Mem** | **Control** | **Sign Extend** | **Shift-left-2** |
|---|---|---|---|---|---|---|---|---|
| 400ps | 100ps | 80ps | 150ps | 180ps | 320ps | 100ps | 50ps | 10ps |

5. (10 points) When silicon chips are fabricated, defects in materials (e.g., silicon) and manufacturing errors can result in defective circuits. A very common defect is for one wire to affect the signal in another. This is called a cross-talk fault. A special class of cross-talk faults is when a signal is connected to a wire that has a constant logical value (e.g., a power supply wire). In this case we have a stuck-at-0 or a stuck-at-1 fault, and the affected signal always has a logical value of 0 or 1, respectively.

Let us assume that processor testing is done by filling the PC, registers, and data and instruction memories with some values (you can choose which values), letting a single instruction execute, then reading the PC, memories, and registers. These values are then examined to determine if a particular fault is present. Can you design a test (values for PC, memories, and registers) and an instruction that would determine if there is a stuck-at-0 fault on bit 16 of output of the Instruction Memory?

6. (15 points) Assume the following instruction word is fetched from the instruction memory:
10101100011000100000000000010100
Assume that data memory is all zeros and that the processor's registers have the following decimal values at the beginning of the cycle in which the above instruction word is fetched:

| **$0** | **$1** | **$2** | **$3** | **$4** | **$5** | **$6** | **$8** | **$12** | **$31** |
|---|---|---|---|---|---|---|---|---|---|
| 0 | -16 | -2 | 4 | -4 | -10 | 6 | -1 | 8 | -32 |

For each Mux, show the values of its data output during the execution of this instruction. For the ALU and the two add units, what are their data input values? What are the values of all inputs for the "Registers" unit?

7. (15 points) Modify the MIPS single cycle implementation to support the instruction JR.

8. (15 points) Assume the logic blocks used to implement the datapath of a processor have the following latencies:

| **Inst. Mem** | **Add** | **Mux** | **ALU** | **Reg File** | **Data Mem** | **Sign Extend** | **Shift-left-2** | **ALU Ctrl** |
|---|---|---|---|---|---|---|---|---|
| 200ps | 80ps | 30ps | 120ps | 100ps | 300ps | 10ps | 10ps | 50ps |

(5 points) To avoid lengthening the critical path of the datapath, how much time can the control unit take to generate the MemWrite signal?

(10 points) Which control signal is the most critical to generate quickly and how much time does the control unit have to generate it if it wants to avoid being on the critical path?

9. (15 points) Assume that individual stages of the pipeline datapath have the following latencies:

| **IF** | **ID** | **EX** | **MEM** | **WB** |
|---|---|---|---|---|
| 300ps | 200ps | 280ps | 360ps | 180ps |

1) What is the minimum clock cycle time of the processor?
2) What is the total latency of an LW instruction in the processor?
3) What is the execution time to run 2000 instructions in the processor? What is the CPI (Clock Cycle Per Instruction)?