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1. (1). At the end of the ID stage, there is a comparator compares [Rs] and [Rd] of the beq. and generate signd "Eq". Also, Control unit produces "branch" signal. When they are both 1, we should use the branch address and set IF/ID.Flush=1. Otherwise, we can continue.

(2). MEM stage:

lw nop beq lw nop beq nop nop nop beq nop nop nop sw

14+4 = 18 cc

ID stage:

lw nop nop beq lw nop nop beq nop beq nop sw

12+4 = 16 cc

Therefore 2 cc speed up.

(3). R2 between line 1 and line 2

R3 between line 3 and line 4.

(4). { Forwarding path: EX/MEM.WriteData to comparator in the ID stage.
condition: EX/MEM.RegWrite && EX/MEM.Reg != 0 &&
EX/MEM.Rt == IF/ID.Rs

{ Forwarding path: MEM/WB.WriteData to comparator in the ID stage
condition: MEM/WB.RegWrite && MEM/WB.Reg != 0 &&
MEM/WB.Reg == IF/ID.Rs && !(EX/MEM.RegWrite &&
EX/MEM.Reg != 0 && EX/MEM.Reg == IF/ID.Rs)

2. (a). For mispredict always-taken, it will cause 2 extra stalls.

$30\% \times (1-45\%) \times 2 = 0.33$

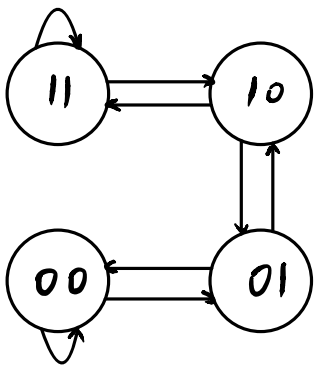
(b). If jump is determined in ID stage, for mispredict, it will cause 1 extra stall. Also, branch determined in EX stage, no data hazards, no delay slots used.

$30\% \times (1-55\%) \times 2 + 5\% \times 1 = 0.32$

3.

decision	value	result
T	00	F
NT	01	T
NT	00	T
T	00	F
T	01	F
T	10	T
T	11	T
NT	11	F
T	10	T
NT	11	F
NT	10	F
T	01	F
T	10	T
T	11	T
T	11	T
NT	11	F

Assume 00: strong not taken
01: not taken
10: taken
11: strong taken



We can find that accuracy = 50%