VE370 HW7 Sample Solution

Problem 1

1. 32 sets, each set contains 2 blocks, and each block has 1b valid, 1b dirty, 20b tag and 32 words, so

   $32 \cdot 2 \cdot (1 + 1 + 20 + 32 \cdot 32) = 66944$

2. 7/12 = 58.3%

Address	Index	Hit/Miss
0	00000	Miss
4	00000	Hit
20	00000	Hit
136	00001	Miss
232	00001	Hit
164	00001	Hit
1024	01000	Miss
30	00000	Hit
140	00001	Hit
3100	11000	Miss
176	00001	Hit
2180	10001	Miss

3. <00000, 20'b0, Mem[0] Mem[1] · · · Mem[31]>

   ...

   <00001, 20'b0, Mem[32] Mem[33] · · · Mem[63]>

   ...

   <01000, 20'b0, Mem[256] Mem[257] · · · Mem[287]>

   ...

<10001, 20'b0, Mem[544] Mem[545] · · · Mem[575]>

...

<11000, 20'b0, Mem[768] Mem[769] · · · Mem[799]>

...

All the Mem[] refers to a word

Problem 2

1. P1: 1/1.18ns = 847MHz
   P2: 1/2.22ns = 450MHz
2. P1: 0.043·70 + 1.18 = 4.19ns
   P2: 0.027·70 + 2.22 = 4.11ns
3. CPI:
   P1: 1 + 0.36·0.043·70/1.18 = 1.91
   P2: 1 + 0.36·0.027·70/2.22 = 1.31

   Time:
   P1: 1.91·1.18 = 2.25ns
   P2: 1.31·2.22 = 2.91ns
   P1 is faster.

Problem 3

1.

Byte Address	Word Address	Index	Tag	Word/byte Offset	Hit/Miss
3	0	00	0000	0/11	Miss
180	0101101	10	0101	1/00	Miss
43	0001010	01	0001	0/11	Miss
3	0	00	0000	0/11	Hit
191	0101111	11	0101	1/11	Miss
89	0010110	11	0010	0/01	Miss
190	0101111	11	0101	1/10	Hit
14	0000011	01	0000	1/10	Miss
181	0101101	10	0101	1/01	Hit
44	0001011	01	0001	1/00	Hit
186	0101110	11	0101	0/10	Hit
252	0111111	11	0111	1/00	Miss

Final cache contents:

Index	Valid	Tag	Word0	Word1
00	Y	0000	Mem[0]	Mem[1]
	N			
	N			
01	Y	0001	Mem[10]	Mem[11]
	Y	0000	Mem[2]	Mem[3]
	N			
10	Y	0101	Mem[44]	Mem[45]
	N			
	N			
11	Y	0101	Mem[46]	Mem[47]
	Y	0010	Mem[22]	Mem[23]
	Y	0111	Mem[62]	Mem[63]

2.

Byte Address	Word Address	Tag	Hit/Miss
3	0	0000000	Miss
180	0101101	0101101	Miss
43	0001010	0001010	Miss
3	0	0000000	Hit
191	0101111	0101111	Miss
89	0010110	0010110	Miss
190	0101111	0101111	Hit
14	0000011	0000011	Miss
181	0101101	0101101	Hit
44	0001011	0001011	Miss
186	0101110	0101110	Miss
252	0111111	0111111	Miss

Final cache contents:

Index	Valid	Tag	Word
	Y	0000000	Mem[0]
	Y	0101101	Mem[45]
	Y	0111111	Mem[63]
	Y	0101111	Mem[47]
	Y	0010110	Mem[22]
	Y	0000011	Mem[3]
	Y	0001011	Mem[11]
	Y	0101110	Mem[46]

3. LRU:

Byte Address	Word Address	Tag	Word Offset	Hit/Miss
3	0	000000	0	Miss
180	0101101	010110	1	Miss
43	0001010	000101	0	Miss
3	0	000000	0	Hit
191	0101111	010111	1	Miss
89	0010110	001011	0	Miss
190	0101111	010111	1	Hit
14	0000011	000001	1	Miss
181	0101101	010110	1	Miss
44	0001011	000101	1	Miss
186	0101110	010111	0	Hit
252	0111111	011111	1	Miss

Miss rate: 9/12 = 75%

MRU:

Byte Address	Word Address	Tag	Word Offset	Hit/Miss
3	0	000000	0	Miss
180	0101101	010110	1	Miss
43	0001010	000101	0	Miss
3	0	000000	0	Hit
191	0101111	010111	1	Miss
89	0010110	001011	0	Miss
190	0101111	010111	1	Miss
14	0000011	000001	1	Miss
181	0101101	010110	1	Hit
44	0001011	000101	1	Hit
186	0101110	010111	0	Miss
252	0111111	011111	1	Miss

Miss rate: 9/12 = 75%

The best possible replacement policy should get all 3/3, 180/181, 43/44 and 191/190/186 hit.
Miss rate = 7/12 = 58.3%