Homework 4

All questions refer to the following figure.
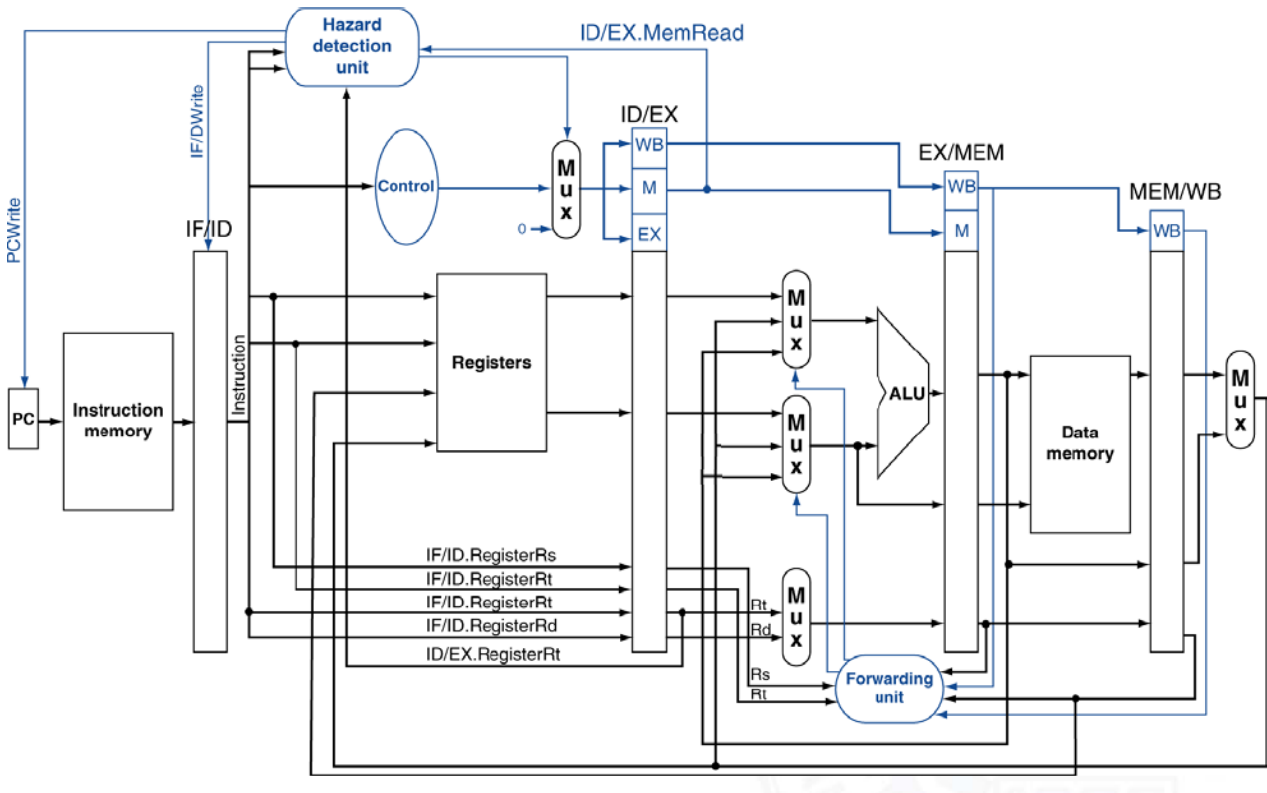
1. (10 points) Given this instruction:
    ```
    lw $t0, -4($sp)
    ```

    As the instruction goes through the pipeline, what are stored in the pipeline registers:
    IF: what's in PC
    ID: what's in IF/ID
    EX: what's in ID/EX?
    MEM: what's in EX/MEM
    WB: what's in MEM/WB?

2. (35 points) Given the following MIPS assembly instructions:
    ```
    L1: sw  $18,-12($8)
    L2: lw  $3,8($18)
    L3: add $6,$3,$3
    L4: or  $8,$9,$6
    ```
    a) Indicate data dependencies, if any, in above instruction sequence. (which register between which instructions) (5 points)
    b) Assume there is no forwarding in this pipelined processor. Indicate hazards and add NOP instructions to eliminate them. How many clock cycles will it take to execute the instructions? (10 points)

c) Assume there is ALU-ALU forwarding. Indicate hazards and add NOP instructions to eliminate them. How many clock cycles will it take to execute the instructions? (10 points)

d) Assume there is full forwarding. Indicate hazards and add NOP instructions to eliminate them. How many clock cycles will it take to execute the instructions? (10 points)

3. (30 points) Assume the following instruction is added to the MIPS instruction set architecture (ISA), thus must be supported by the pipelined processor:

```
beqm Rd, Rt, Offs(Rs)    #if Rt=Mem[Offs+Rs] then PC = Rd
```

a) Give a sequence of existing MIPS instructions that are replaced by this instruction. (5 points)

b) What must be changed in the pipelined datapath to support this instruction? (10 points)

c) Which new control signal(s) must be added to your pipeline based on your suggested changes in b? (5 points)

d) Does support for this instruction introduce any new hazards? Give an example. (10 points)

4. (25 points) Given this MIPS assembly instruction sequence executed by the pipelined processor:

```
sub $6, $2, $1
lw  $3, 8($6)
lw  $2, 0($6)
or  $3, $5, $3
sw  $3, 0($5)
```

a) If the processor has forwarding, but we forgot to implement the hazard detection unit, what happens when this code executes? (5 points)

b) If there is forwarding, for the first five cycles during the execution of this code, specify which signals are asserted in each cycle by hazard detection and forwarding units. (10 points)

c) If there is no forwarding, what new inputs and output signals do we need for the hazard detection unit? Using this instruction sequence as an example, explain why each signal is needed. (10 points)