JOINT INSTITUTE
交大密西根学院

Ve370 Introduction to Computer Organization

Homework 2

1. (10 points) Following memory location has address 0x0F000000 and content 0x15478933.

	0	1	2	3
0x0F000000	15	68	47	33

Write MIPS assembly instructions to load the byte 47 to register $s1, then show the content of $s1 after the operations.

2. (10 points) The MIPS assembly program below computes the factorial of a given input (n!). The integer input is passed through register $a0, and the result is returned in register $v0. In the assembly code, there are a few errors. Correct the errors.

```
FACT: addi $sp, $sp, 8
      sw $ra, 4($sp)
      sw $a0, 0($sp)
      add $s0, $0, $a0
      slti $t0, $a0, 2
      beq $t0, $0, L1
      mul $v0, $s0, $v0
      addi $sp, $sp, -8
      jr $ra
L1:   addi $a0, $a0, -1
      jal FACT
      addi $v0, $0, 1
      lw $a0, 4($sp)
      lw $ra, 0($sp)
      addi $sp, $sp, -8
      jr $ra
```

3. (5 points) Given a 32-bit machine instruction: 0000 0001 0110 1010 0100 1000 0010 0010,
   1) What MIPS assembly instruction does it represent?
   2) What type (R-type, I-type, J-type) of instruction is it?

4. (5 points) Given MIPS assembly instruction: lw $s1, -32($s2),

1) What is the corresponding binary representation?

2) What type (R-type, I-type, J-type) of instruction is it?

5. (10 points) If the MIPS processor is modified to have 128 registers rather than 32 registers:

   1) show the size of the bit fields of an R-type format instruction. What is the total number of bits needed for each instruction?

   2) show the size of the bit fields of an I-type format instruction. What is the total number of bits needed for each instruction?

6. (10 points) If the MIPS processor is modified to have 64 registers rather than 32 registers:

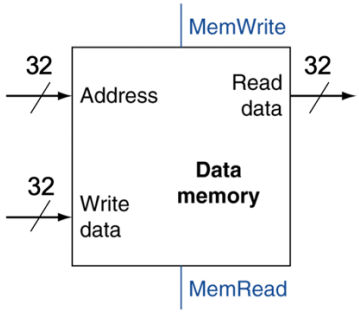
   1) What is the impact on the range of addresses for a beq instruction? Assume that all instructions remain 32 bits long and the size of opcode field doesn't change.

   2) What is the impact on the range of addresses for a jr instruction, assuming that each instruction must be 32 bits and the size of opcode field doesn't change.

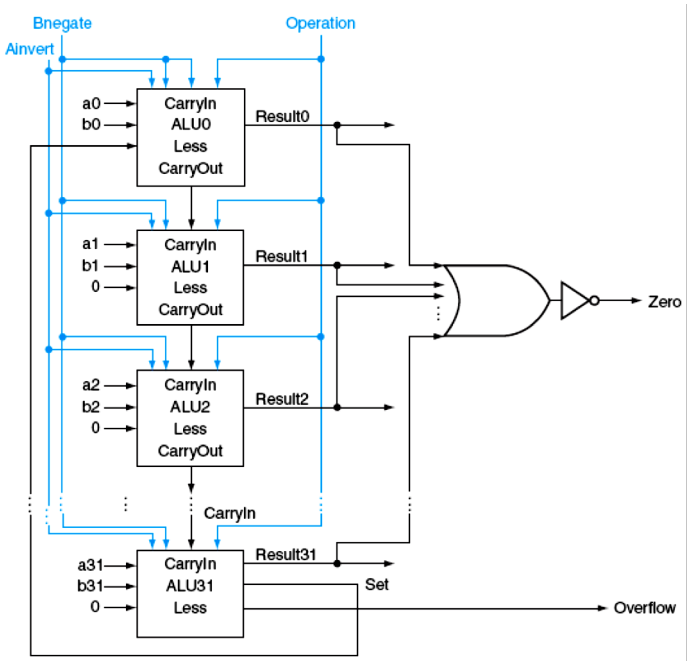
7. (15 points) Convert the following assembly code fragment into machine code, assuming the memory location of the first instruction is 0x1000F400

```
LOOP:   slt  $t5, $zero, $t0
        bne  $t5, $zero, ELSE
        j    DONE
ELSE:   addi $s3, $s3, 2
        addiu $t2, $t2, 1
        j    LOOP
DONE:   …
```

8. (10 points) Model the memory block shown below in Verilog HDL. Verify the function of your design.



9. (15 points) Model the following 32-bit ALU in Verilog HDL. Verify the function of your design.



10. (10 points) The table below contains the link-level details of two different procedures.

b.	Procedure A				Procedure B			
	Text Segment	Address	Instruction		Text Segment	Address	Instruction	
		0	lui $at, 0			0	sw $a0, 0($gp)	
		4	ori $a0, $at, 0			4	jmp 0	
		…	…			…	…	
		0x84	jr $ra			0x180	jal 0	
		…	…			…	…	
	Data Segment	0	(X)		Data Segment	0	(Y)	
		…	…			…	…	
	Relocation Info	Address	Instruction Type	Dependency	Relocation Info	Address	Instruction Type	Dependency
		0	lui	X		0	sw	Y
		4	ori	X		4	jmp	FOO
						0x180	jal	A
	Symbol Table	Address	Symbol		Symbol Table	Address	Symbol	
		–	X			–	Y	
						0x180	FOO	
						–	A	

Link the object files above to form the executable file header. Assume that Procedure A has a text size of 0x140 and data size of 0x40 and Procedure B has a text size of 0x300 and data size of 0x50. Also assume PC is initialized at 0x00400000, $gp is initialized at 0x10008000, $sp is initialized at 0x7ffffffc. If you cannot see the table, refer to Files → homework.