# Topic 0

## Course Introduction

# Instructional Support

- **Instructor:** Gang Zheng, Ph.D.
- **Office:** JI New Building 400E
- **Contact:** (021) 3420-6765 x4005, gzheng@sjtu.edu.cn
- **Teaching mode:** concurrent classroom and online (zoom)
- **Office Hours:** W 4:00 – 6:00pm / Th 10:00am – noon, or on Piazza, or by appointment
- **TAs：** Mr. SHI Li, shili2017@sjtu.edu.cn
  Ms. TAO Chenyun, tcy1999@sjtu.edu.cn
  Mr. HE Zhengfei, hzf1213@sjtu.edu.cn
- **Recitation:** TBD
- **TA Office Hours:** TBD

# What will be taught?

- How computers execute programs?
- What's the correspondence between different levels of languages: C/C++, assembly, and machine language?
- How to design a processor (datapath and controller) as a digital system?
- What are the difficulties and tricks in the design of a CPU? How to resolve? How to improve?
- How memory works as part of a computer, and how is it organized?
- How processor, memory, and I/O devices work together as a computer?

# Minimum Expectations

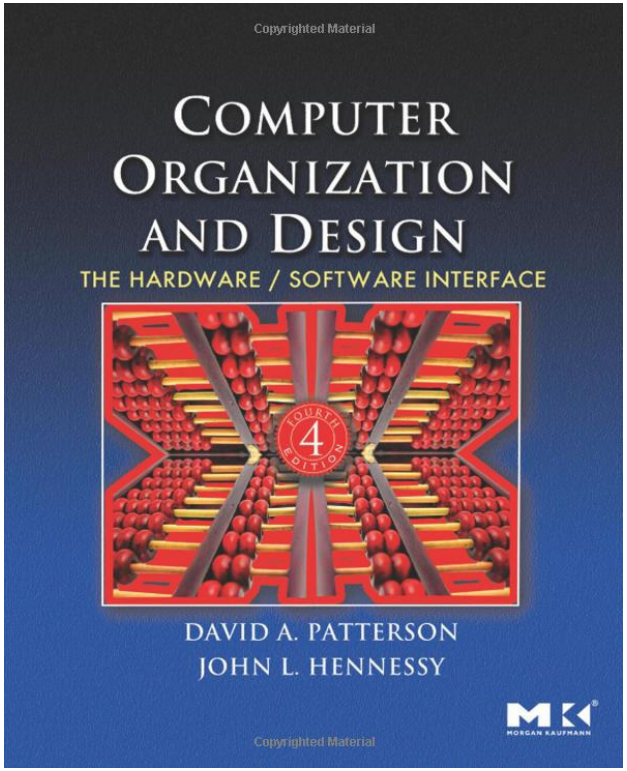
- Write an assembly language program that implements a task, translate the program into machine-level instructions, and trace the execution of the program.
- Model the computer hardware including datapath and control logic for a given instruction-set architecture by using hardware description languages (HDLs).
- Be able to identify and resolve potential data and control hazards
- Understand memory hierarchy including cache, main memory, hard disk, and how data is stored, understand memory hits and misses
- Understand the memory mapped I/O concept and how I/O devices interface the CPU
- Be able to use library and internet resources for literature search to learn the comtemporary issues, technologies, and future development trends in computing

# Topics to Cover

- Introduction to computer
- Software
  - MIPS instruction set, operands, operations, assembly programming
  - Instruction encoding, addressing mode
  - Procedures, memory usage, procedure calling conventions
- Hardware – CPU
  - Single cycle processor implementation
  - Pipelined datapath and control
  - Data hazards, control hazards, exceptions
- Hardware – Memory and other peripherals
  - Cache, virtual memory, virtual machine
  - I/Os devices and interfaces
- *Advanced topics*
  - *Parallelism, Multicores, multiprocessors, clusters*

# Textbook

- David Patterson and John Hennessy, *Computer Organization and Design - Hardware/Software Interface*, 4th edition, Morgan Kaufmann, 2008, ISBN 978-0-12-374493-7



# Tentative Schedule

- On Syllabus

# Course Policies

- **Honor Code:**
  - Honor Code of the Joint Institute
  - ***Addendum to the Honor Code for Online Teaching***.
- **Test:**
  - Test procedure will be announced prior to the tests. Anyone violating the test procedure will be given an 'F' for the test.
- **Attendance:**
  - Strongly encouraged for better understanding of difficult concepts and student engagement during class time
- **Participation:**
  - Active participation is highly expected for all students. This involves:
    - Participation in interactive activities during the lecture time
    - Active involvement in projects
    - Proper assistance to other students in group studying
    - Contributions to the Q&A on Piazza, etc.

# Course Policies

- **Individual Assignments:**
  - Project 1, portion of 2,  4, and homework
  - OK to discuss course topics and help each other understand the project/homework requirements better
  - NOT OK for duplicated submission
- **Group Assignments:**
  - Portion of Project 2 and Project 3 are team efforts
  - Teams of 4 students
- **Submission:**
  - Electronic submission on Canvas before deadline

# Assessment Methods

- **Homework:**
  - About 8 homework assignments
- **Homework for literature search:**
  - The ability to search and find literatures relevant to a specific topic, and to learn tools that may facilitate the searching process.
- **Examination:**
  - Two online or paper-based examinations.
  - The typical types of exam problems include conceptual understanding, computation, procedural development, short answer, analysis and design, and etc.

# Assessment Methods

- **Project:**
  - 4 projects, 1 software design, 2 hardware simulation or implementation, 1 literature review
- **Participation and Etiquette:**
  - Classroom interaction with the instructor and other students
  - effective contribution on Piazza
  - active participation in team-based projects.
  - Vandalism, spam messages, verbal and other forms of abuse, violation of English-only policies and disturbance of the learning experience of other students are not permitted

# Grading Policy

| | |
|---|---|
| Participation & Etiquette | 5% |
| Homework* | 10% |
| Literature search homework* | 2% |
| Midterm Exam | 20% |
| Final Exam | 20% |
| Project 1* | 5% |
| Project 2*/** | 25% |
| Project 3** | 10% |
| Project 4* | 3% |
| **Total** | **100%** |

*Individual assignments

**Group assignments

Note: final letter grades may be curved