JOINT INSTITUTE
交大密西根学院

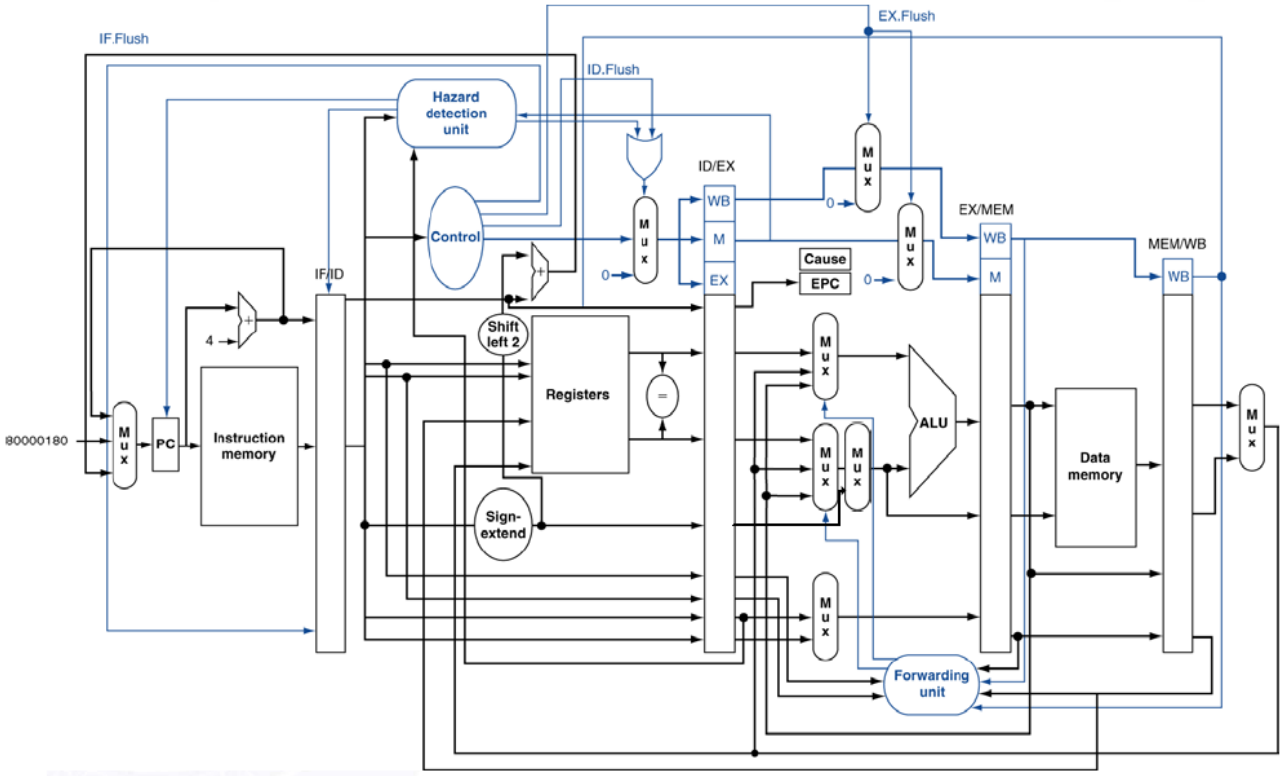
Ve370 Introduction to Computer Organization

Homework 6

1. Refer to the following figure. Assume there is a memory access exception with this instruction:

   ```
   sw R2, -120(R4)
   ```

   For each stage of the pipeline, determine the values of exception-related control signals as this instruction passes through that pipeline stage. (5 points)



2. The following code is written in C, where elements within the same row are stored contiguously.

   ```
   for (J=0; J<8000; J++)
       for (I=0; I<8; I++)
           A[I][J]=B[I][0]+A[J][I];
   ```

   (1) References to which variables exhibit temporal locality? (5 points)

   (2) References to which variables exhibit spatial locality? (5 points)

3. Below is a list of 32-bit memory address references, given as word addresses:

   4, 12, 33, 6, 187, 65, 186, 19, 125, 43, 152, 253

(1) For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with 8 one-word blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty. (15 points)

(2) For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with two-word blocks and a total size of 4 blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty. (15 pints)

(3) You are asked to optimize a cache design for the given references. There are three direct-mapped cache designs possible, all with a total of 8 words of data: C1 has 1-word blocks, C2 has 2-word blocks, and C3 has 4-word blocks. In terms of miss rate, which cache design is the best? If the miss stall time is 35 cycles, and C1 has an access time of 2 cycles, C2 takes 3 cycles, and C3 takes 5 cycles, which is the best cache design? (20 points)

4. For a direct-mapped cache with a 32-bit address and write back mechanism, the partition of the 32 bits are as follows:
   - Offset: bit 6 to 0
   - Index: bit 11-7

   (1) What is the size of the cache in terms of bits? (5 points)

   (2) What is the ratio between total bits required for such a cache implementation over the data storage bits? (5 points)

   Starting from power on, the following byte addresses were used to access the cache memory: 0, 4, 20, 136, 232, 164, 1024, 30, 140, 3100, 176, 2180

   (3) How many blocks were replaced? (10 points)

   (4) What is the hit ratio? (5 points)

   (5) Show the final state of the cache, with each valid line represented as <index, tag, data>. (10 points)