VE370 RC (Final Part 2)

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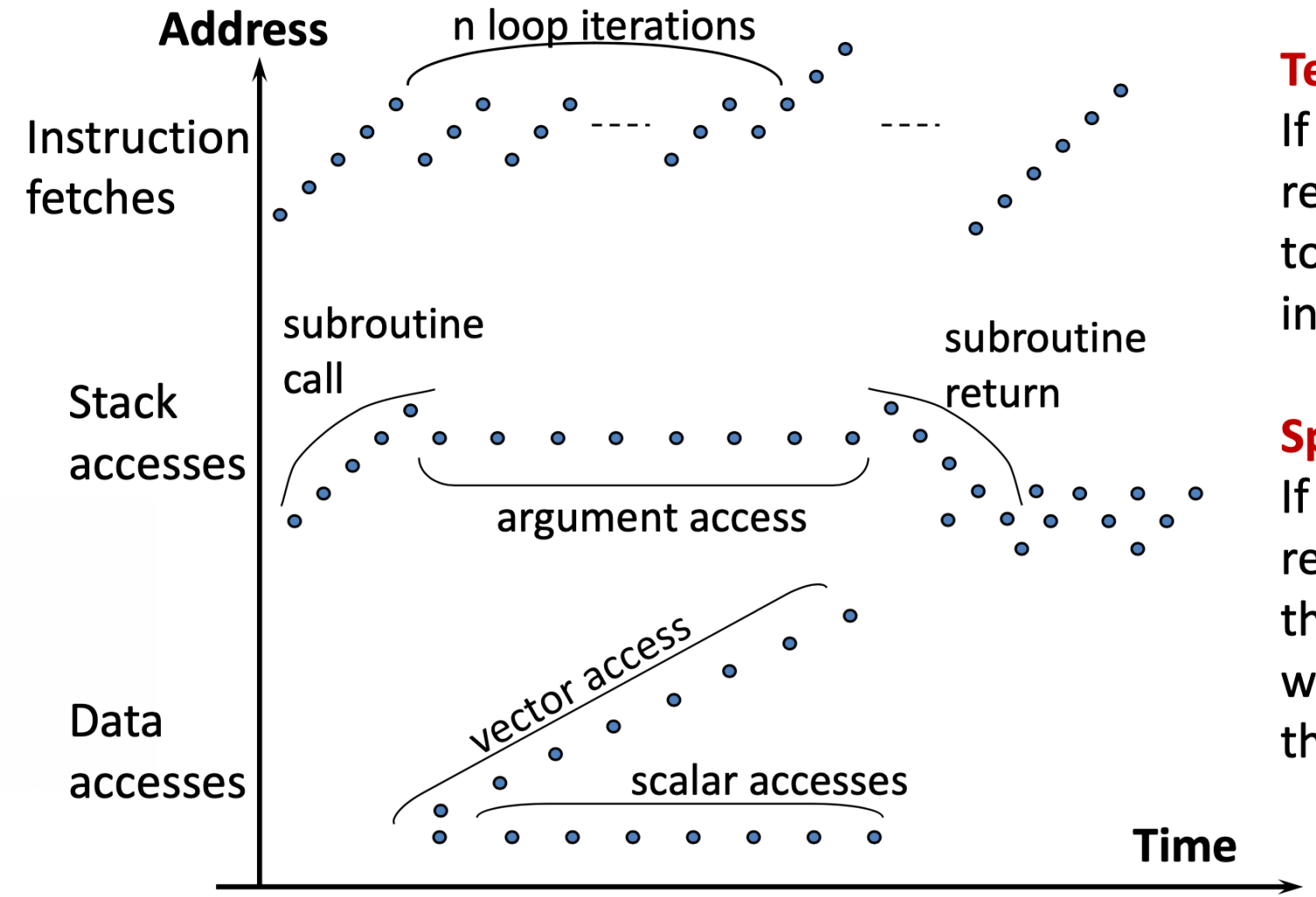
Concept 1: Motivation of using cache Principle of locality (temporal & spatial)



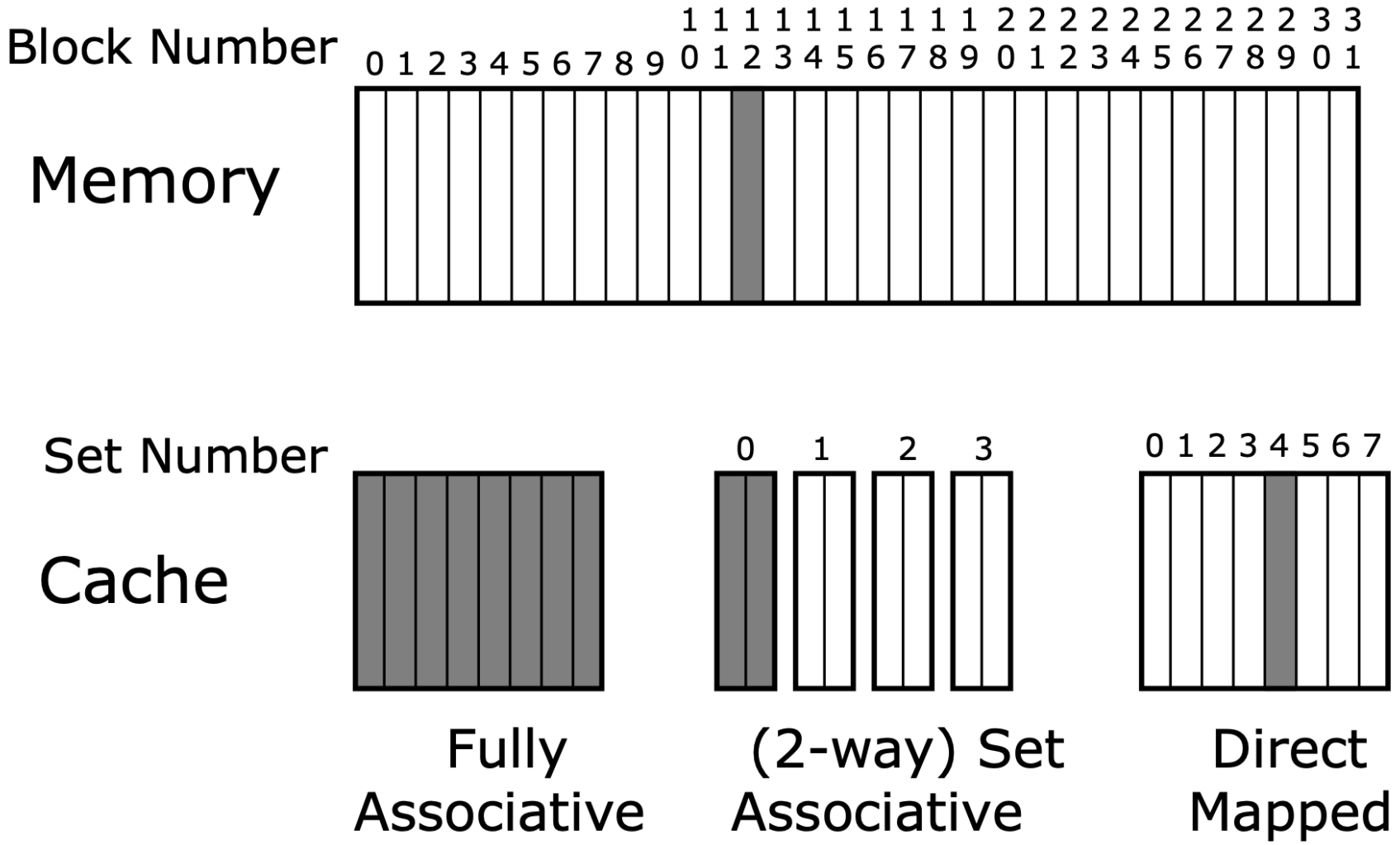
Temporal Locality:
If a location is reference it is likely to be reference again in the near future

Spatial Locality:
If a location is referenced it is likely that locations near it will be referenced in the near future

Concept 2: Key characteristics of cache

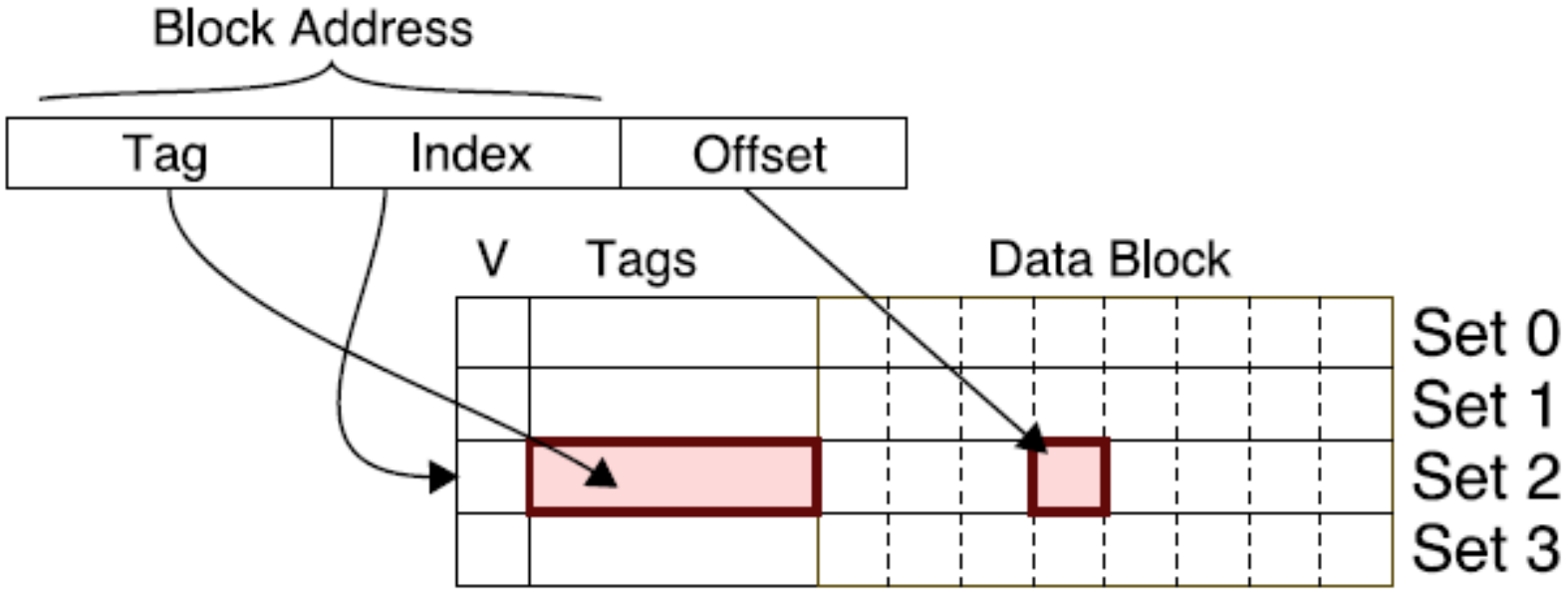
- **Block placement**: Where can a block be placed in the cache?
- **Block identification**: How a block is found if it is in the cache?
- **Block replacement**: Which block should be replaced on a miss?
- **Write strategy**: What happens on a write?

Concept 2: Key characteristics of cache Block placement



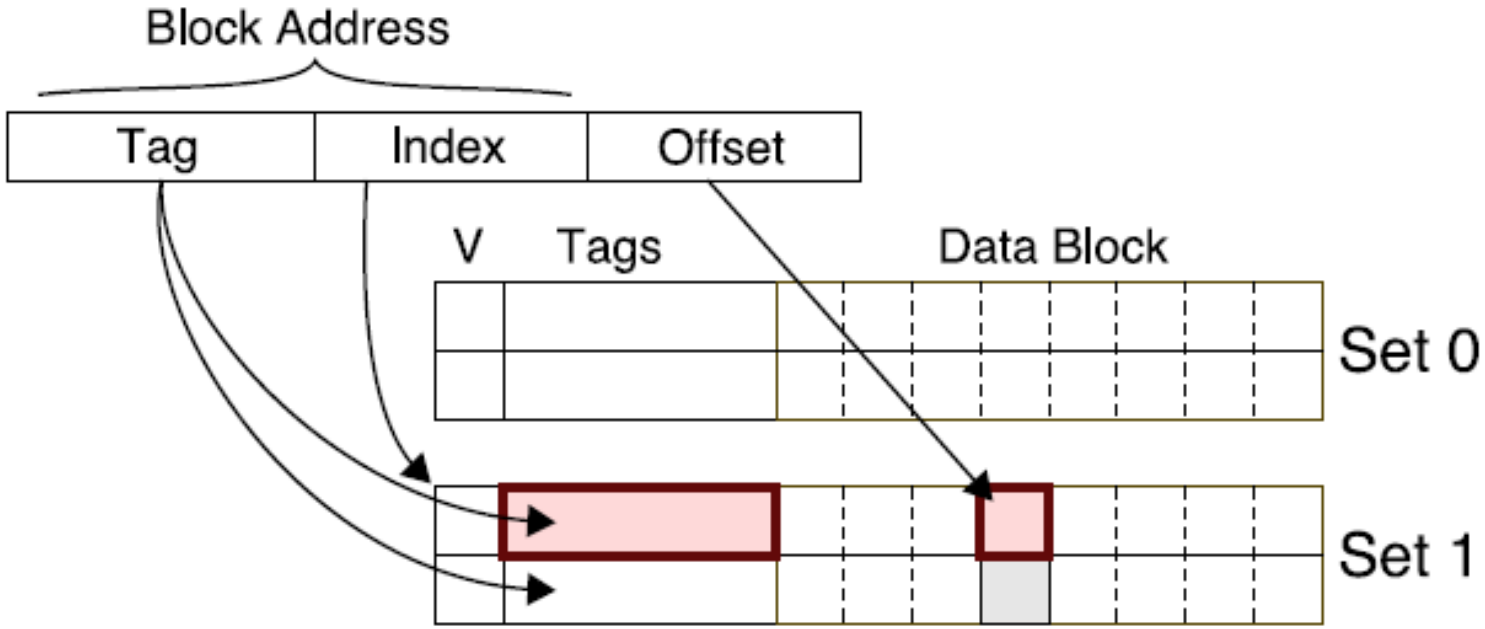
Concept 2: Key characteristics of cache Block identification

- Example: directed map, 8-word block, 4-line cache
- Simple exercise 1
  - Where does the data byte with address `010110110100` in memory locate in this example cache?



Concept 2: Key characteristics of cache Block identification

- Example: 2-way associative, 8-word block, 4-line cache
- Simple exercise 2
  - Where does the data byte with address `010110110100` in memory locate in this example cache?



Concept 2: Key characteristics of cache Block replacement (for associative cache)

- Replacement policy
  - Random
  - Least-recently used (LRU)
  - First in, first out (FIFO) aka Round-Robin
- Which one is the best?
  - It depends
  - LRU works well for 2-way/4-way
  - But random works as good as LRU for higher associativity

Concept 2: Key characteristics of cache Write strategy

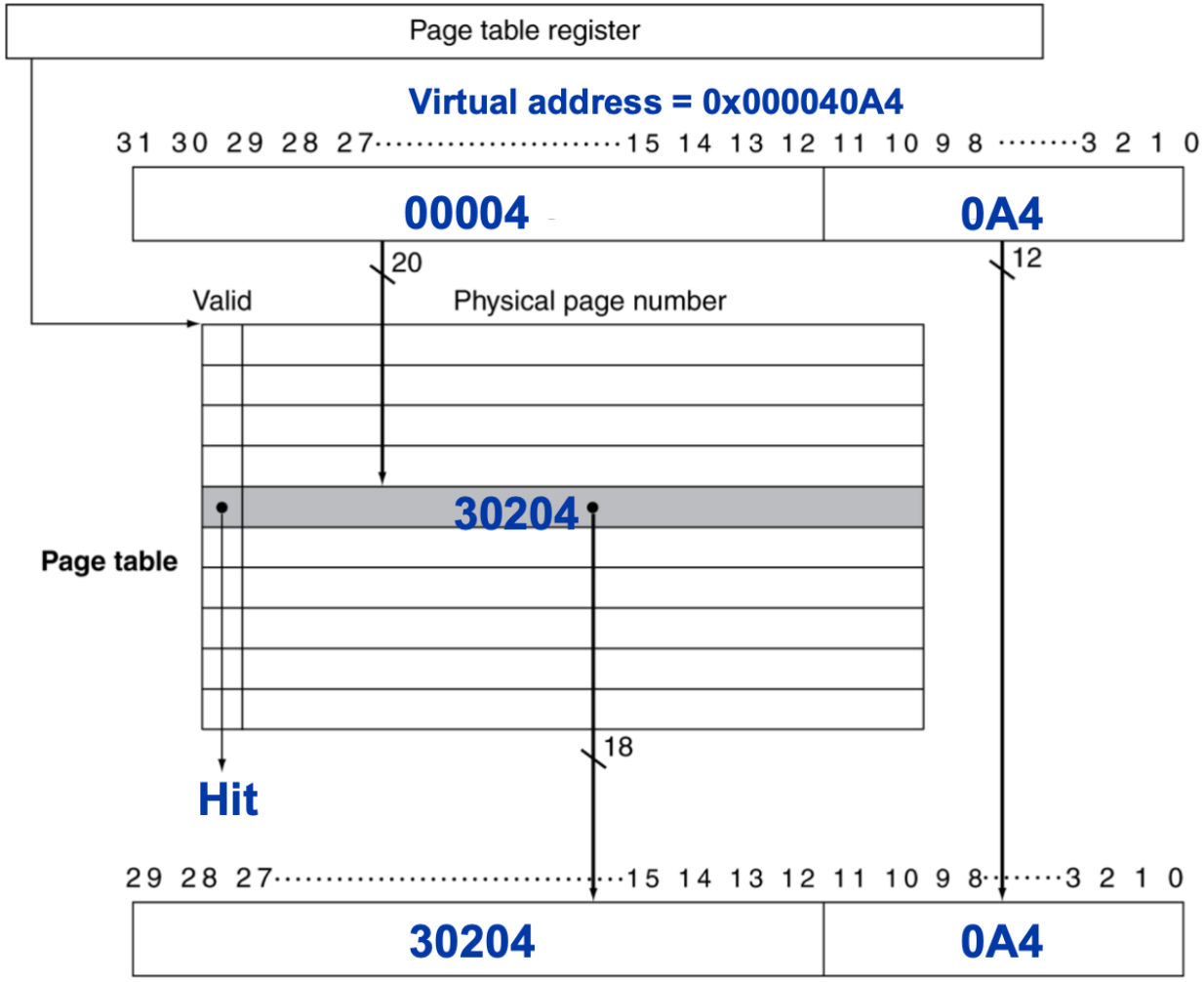
- **Cache Hit**
  - **Write Through** – write both cache and memory, generally higher traffic but simpler to design
  - **Write Back** – write cache only, memory is written when evicted, dirty bit per block avoids unnecessary write backs, more complicated
- **Cache Miss**
  - **No Write Allocate** – only write to main memory
  - **Write Allocate** – fetch block into cache, then write only to cache
- Common combinations
  - Write Through & No Write Allocate
  - Write Back & Write Allocate

Concept 3: Cache performance

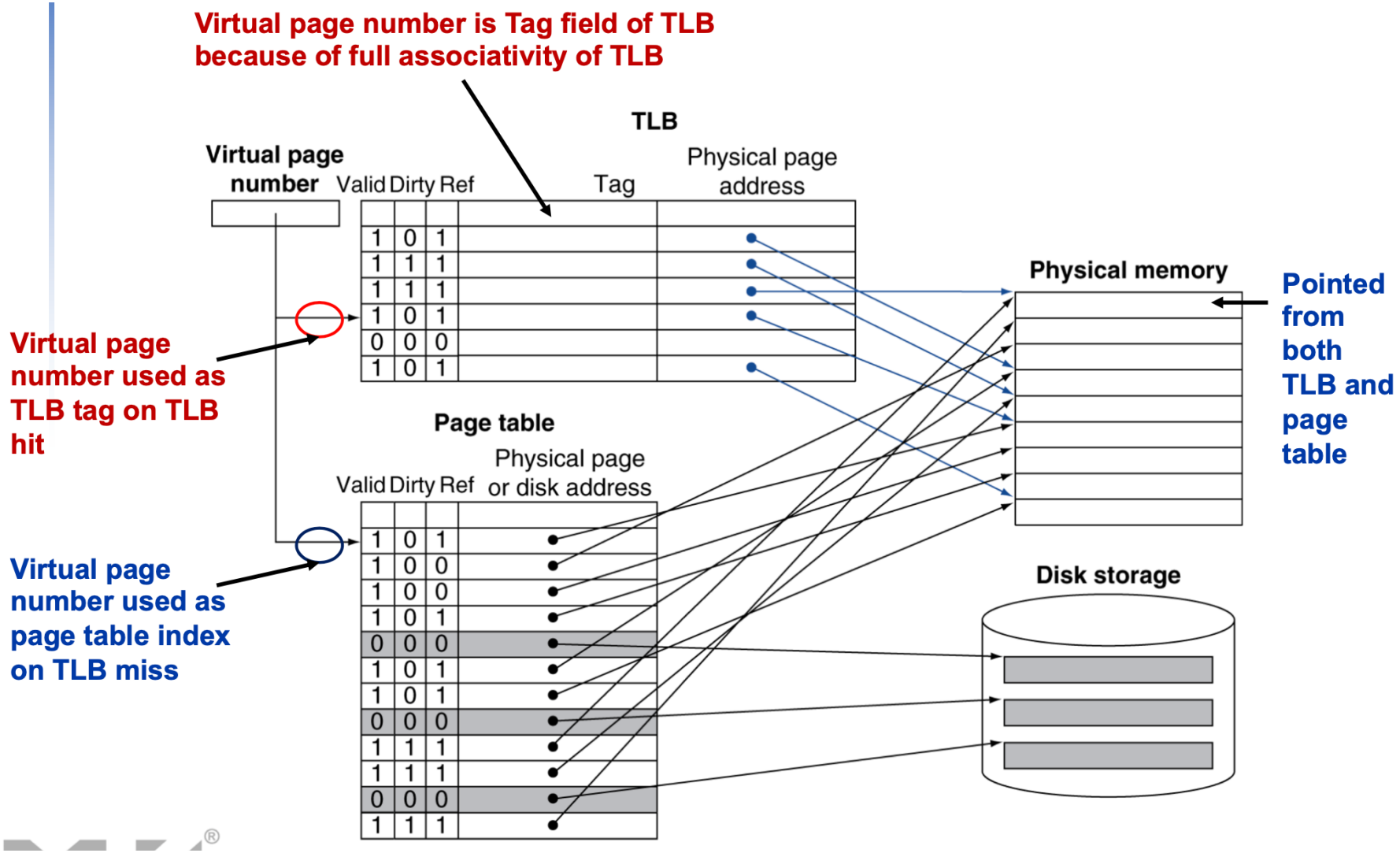
- Total CPI = base CPI + Miss (stall) cycles per instruction
- Average memory access time (AMAT)
  - AMAT = Hit Time + (Miss Rate * Miss Penalty)

- How about 2-level cache?
  - CPI = base CPI + L1 miss L2 hit t(L2)+ L1 miss L2 miss (t(L2)+ t(Mem))
    = base CPI + L1 miss (t(L2) + L2 miss t(Mem))

Concept 4: VM & Page Table Address translation



Concept 5: TLB
How to use TLB? (T14 – Page 24)



Concept 5: TLB
TLB hit & miss

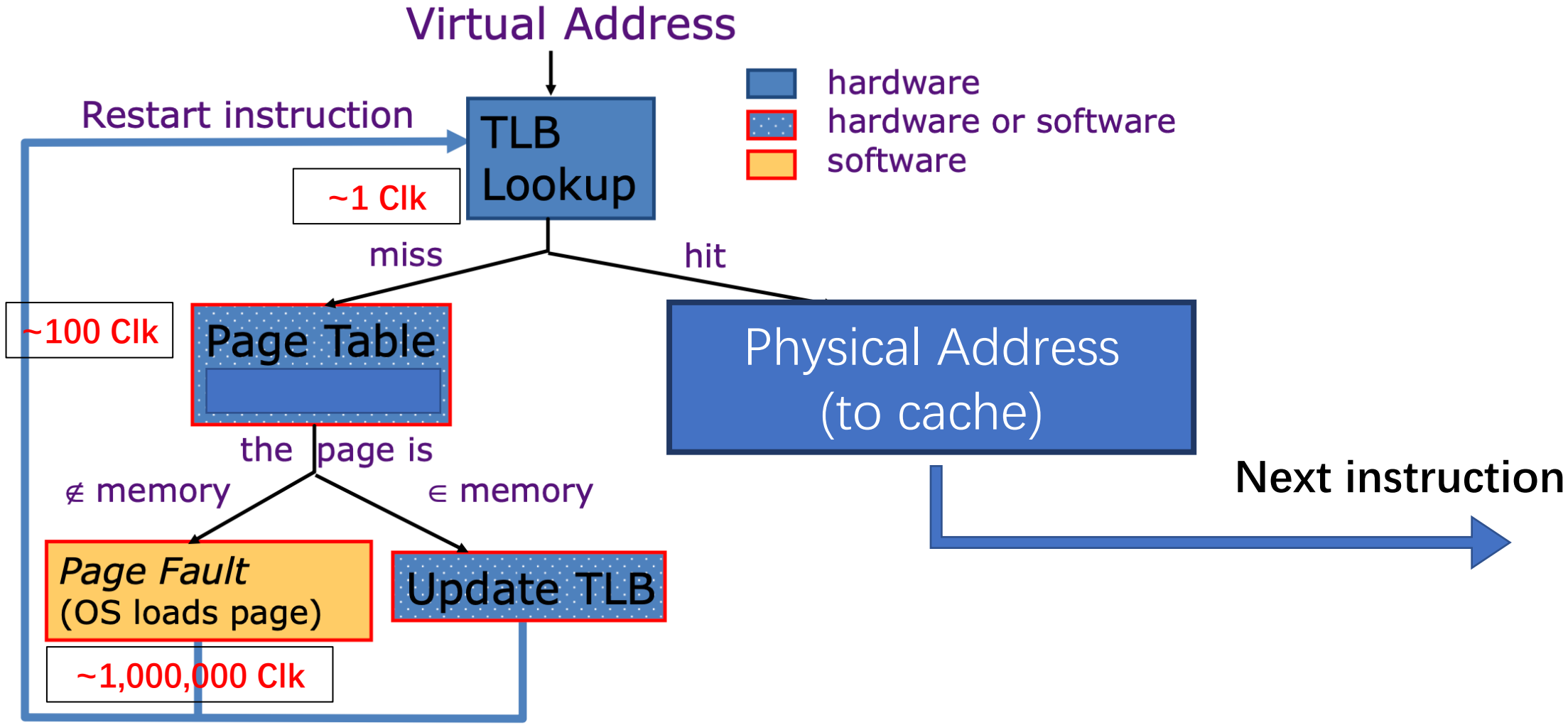
TLB Hit

- Provide physical address
- Reference bit 0/1→1
- If write:
  - dirty bit 0/1→1
- Go to next instruction

TLB Miss

- Page table hit:
  - Load page table entry to TLB
- Page table miss:
  - Page fault exception
  - OS loads the page from disk
  - Update page table & TLB
- Restart current instruction

Concept 5: TLB
TLB hit & miss



Concept 6: 3C Model
Sources of misses

- Compulsory misses (aka cold start misses)
  - First access to a block
- Capacity misses
  - Due to finite cache size
  - A replaced block is later accessed again
- Conflict misses (aka collision misses)
  - In a non-fully associative cache
  - Due to competition for blocks in a set
  - Would not occur in a fully associative cache of the same total size

Homework review 1: 7.3 (1) & (2)

Given the following byte addresses for memory access:

3, 180, 43, 3, 191, 89, 190, 14, 181, 44, 186, 252

(1) Show the final cache contents for a 3-way set associative cache with two-word blocks and a total size of 24 words. Use LRU replacement. For each reference identify the index bits, the tag bits, the offset bits, and if it is a hit or a miss. (20 points)

(2) Show the final cache contents for a fully associative cache with one-word blocks and a total size of 8 words. Use LRU replacement. For each reference identify the index bits, the tag bits, and if it is a hit or a miss. (20 points)

Homework review 1: 7.3 (1)

Index	Valid	Tag	Word0	Word1
00				
01				
10				
11				

Homework review 1: 7.3 (2)

Index	Valid	Tag	Word0
-			

Homework review 1: 8.3 (1)

- 4 KB pages / 4-entry fully associative TLB / LRU replacement.
- If pages must be brought in from disk, increment to the next largest page number.
- Access to the memory by the following virtual address (decimal): 12948, 49419, 46814, 13975, 40004, 12707, 52236
- Convert to hexadecimal
- `0x3294, 0xC10B, 0xB6DE, 0x3697,`
- `0x9C44, 0x31A3, 0xCC0C`

V	Tag	PPN
1	11	12
1	7	4
1	3	6
0	4	9

TLB

#	V	PPN
0	1	5
1	0	Disk
2	0	Disk
3	1	6
4	1	9
5	1	1
6	0	Disk
7	1	4
8	0	Disk
9	0	Disk
10	1	3
11	1	12

Page Table

Homework review 1: 8.3 (1)

- 4 KB pages / 4-entry fully associative TLB / LRU replacement.
- `0x3294, 0xC10B, 0xB6DE, 0x3697, 0x9C44, 0x31A3, 0xCC0C`

- Physical address: `0x6294`

TLB Hit

V	Tag	PPN
1	11	12
1	7	4
1	3	6
0	4	9

TLB

#	V	PPN
0	1	5
1	0	Disk
2	0	Disk
3	1	6
4	1	9
5	1	1
6	0	Disk
7	1	4
8	0	Disk
9	0	Disk
10	1	3
11	1	12

Page Table

Homework review 1: 8.3 (1)

- 4 KB pages / 4-entry fully associative TLB / LRU replacement.
- `0x3294, 0xC10B, 0xB6DE, 0x3697, 0x9C44, 0x31A3, 0xCC0C`

- Physical address: `0xD10B`

Page Fault

V	Tag	PPN
1	11	12
1	7	4
1	3	6
1	12	13

TLB

#	V	PPN
0	1	5
1	0	Disk
2	0	Disk
3	1	6
4	1	9
5	1	1
6	0	Disk
7	1	4
8	0	Disk
9	0	Disk
10	1	3
11	1	12
12	1	13

Page Table

Homework review 1: 8.3 (1)

- 4 KB pages / 4-entry fully associative TLB / LRU replacement.
- `0x3294, 0xC10B, 0xB6DE, 0x3697, 0x9C44, 0x31A3, 0xCC0C`

- Physical address: **`0xC6DE`**

TLB Hit

V	Tag	PPN
1	11	12
1	7	4
1	3	6
1	12	13

TLB

#	V	PPN
0	1	5
1	0	Disk
2	0	Disk
3	1	6
4	1	9
5	1	1
6	0	Disk
7	1	4
8	0	Disk
9	0	Disk
10	1	3
11	1	12
12	1	13

Page Table

Homework review 1: 8.3 (1)

- 4 KB pages / 4-entry fully associative TLB / LRU replacement.
- `0x3294, 0xC10B, 0xB6DE, 0x3697, 0x9C44, 0x31A3, 0xCC0C`

- Physical address: `0x6697`

TLB Hit

V	Tag	PPN
1	11	12
1	7	4
1	3	6
1	12	13

TLB

#	V	PPN
0	1	5
1	0	Disk
2	0	Disk
3	1	6
4	1	9
5	1	1
6	0	Disk
7	1	4
8	0	Disk
9	0	Disk
10	1	3
11	1	12
12	1	13

Page Table

Homework review 1: 8.3 (1)

- 4 KB pages / 4-entry fully associative TLB / LRU replacement.
- `0x3294, 0xC10B, 0xB6DE, 0x3697, 0x9C44, 0x31A3, 0xCC0C`

- Physical address: **`0xEC44`**

Page Fault

V	Tag	PPN
1	11	12
1	9	14
1	3	6
1	12	13

TLB

#	V	PPN
0	1	5
1	0	Disk
2	0	Disk
3	1	6
4	1	9
5	1	1
6	0	Disk
7	1	4
8	0	Disk
9	1	14
10	1	3
11	1	12
12	1	13

Page Table

Homework review 1: 8.3 (4)

- 4 KB pages / 4-entry 2-way associative TLB / LRU replacement.
- If pages must be brought in from disk, increment to the next largest page number.
- Access to the memory by the following virtual address (decimal): 12948, 49419, 46814, 13975, 40004, 12707, 52236
- Convert to hexadecimal
- `0x3294, 0xC10B, 0xB6DE, 0x3697,`
- `0x9C44, 0x31A3, 0xCC0C`

I	V	Tag	PPN
0			
1			

TLB

#	V	PPN
0	1	5
1	0	Disk
2	0	Disk
3	1	6
4	1	9
5	1	1
6	0	Disk
7	1	4
8	0	Disk
9	0	Disk
10	1	3
11	1	12

Page Table