1.

IF: IF.Flush=0, PCWrite=1, IF/IDWrite=1, PCsrc=00;

ID: ID.Flush=0;

EX: EX.Flush=0;

MEM: Data memory detects memory access exception. The Cause and EPC registers store the relevant information. To flush the instructions mistakenly loaded in the ID and EX stage as well as the current instruction, now IF.Flush=1, ID.Flush=1, EX.Flush=1, MEM.Flush=1. To prevent the instruction in the IF stage from entering the succeeding stages, IF/IDWrite=0. PCsrc=01 such that the MUX in front of the PC register now chooses the address of the exception handler as the next instruction.

WB: The instruction was flushed at MEM stage. It will never reach the WB stage.

2.

(1). I, J, A[k][k]
(2). A[J][I].

3.

(1).

Word address	Binary address (32-bit binary)	Hit or miss
4	0000_0000_0000_0000_0000_0001_0000	Miss
12	0000_0000_0000_0000_0000_0011_0000	Miss
33	0000_0000_0000_0000_0000_1000_0100	Miss
6	0000_0000_0000_0000_0000_0001_1000	Miss
187	0000_0000_0000_0000_0010_1110_1100	Miss
65	0000_0000_0000_0000_0001_0000_0100	Miss
186	0000_0000_0000_0000_0010_1110_1000	Miss
19	0000_0000_0000_0000_0000_0100_1100	Miss
125	0000_0000_0000_0000_0001_1111_0100	Miss
43	0000_0000_0000_0000_0000_1010_1100	Miss
152	0000_0000_0000_0000_0010_0110_0000	Miss
253	0000_0000_0000_0000_0011_1111_0100	Miss
Word address	Tag (27-bit binary)	Cache index (3-bit binary)
4	0000_0000_0000_0000_0000_000	100
12	0000_0000_0000_0000_0000_001	100
33	0000_0000_0000_0000_0000_100	001
6	0000_0000_0000_0000_0000_000	110
187	0000_0000_0000_0000_0010_111	011
65	0000_0000_0000_0000_0001_000	001
186	0000_0000_0000_0000_0010_111	010

19	0000_0000_0000_0000_0000_010	011
125	0000_0000_0000_0000_0001_111	101
43	0000_0000_0000_0000_0000_101	011
152	0000_0000_0000_0000_0010_011	000
253	0000_0000_0000_0000_0011_111	101

(2).

Word address	Binary address (32-bit binary)	Hit or miss
4	0000_0000_0000_0000_0000_0001_0000	Miss
12	0000_0000_0000_0000_0000_0011_0000	Miss
33	0000_0000_0000_0000_0000_1000_0100	Miss
6	0000_0000_0000_0000_0000_0001_1000	Miss
187	0000_0000_0000_0000_0010_1110_1100	Miss
65	0000_0000_0000_0000_0001_0000_0100	Miss
186	0000_0000_0000_0000_0010_1110_1000	Hit
19	0000_0000_0000_0000_0000_0100_1100	Miss
125	0000_0000_0000_0000_0001_1111_0100	Miss
43	0000_0000_0000_0000_0000_1010_1100	Miss
152	0000_0000_0000_0000_0010_0110_0000	Miss
253	0000_0000_0000_0000_0011_1111_0100	Miss
Word address	Tag (27-bit binary)	Cache index (2-bit binary)
4	0000_0000_0000_0000_0000_000	10
12	0000_0000_0000_0000_0000_001	10
33	0000_0000_0000_0000_0000_100	00
6	0000_0000_0000_0000_0000_000	11
187	0000_0000_0000_0000_0010_111	01
65	0000_0000_0000_0000_0001_000	00
186	0000_0000_0000_0000_0010_111	01
19	0000_0000_0000_0000_0000_010	01
125	0000_0000_0000_0000_0001_111	10
43	0000_0000_0000_0000_0000_101	01
152	0000_0000_0000_0000_0010_011	00
253	0000_0000_0000_0000_0011_111	10

(3).

C1 and C2 are demonstrated in the two previous sub-questions.

For C3, the binary addresses and tags are the same. The cache indexes and hit/miss outcomes are shown below.

Word address	Cache index (1-bit binary)	Hit or miss
4	1	Miss
12	1	Miss
33	0	Miss

6	1	Miss
187	0	Miss
65	0	Miss
186	0	Miss
19	0	Miss
125	1	Miss
43	0	Miss
152	0	Miss
253	1	Miss

In terms of miss rate, C2 is the best with 0.083, while the other two is 0.

For C1, the total time needed is $12 \times 35 + 12 \times 2 = 444$ cycles.

For C2, the total time needed is $11 \times 35 + 12 \times 3 = 421$ cycles.

For C3, the total time needed is $12 \times 35 + 12 \times 5 = 480$ cycles.

C2 is still the best design.

4.

(1).

Each word has 2^5 bits.

7-bit offset → 2-bit byte offset and 5-bit word offset → 2^5 words in a block.

5-bit index → 2^5 blocks in the cache.

So, the size of the data stored in the cache is $2^5 \times 2^5 \times 2^5 = 2^{15}$ bits.

Besides data storage, for each block, the cache needs one valid bit, one dirty bit and 20 tag bits, which is $22 \times 2^5 = 704$ bits in total.

Thus, the size of the cache is $2^{15} + 704 = 33472$ bits.

(2)

Ratio = $33472/2^{15}=1.0215$

(3).

No.	Byte address	Word number	Block number	Block index in cache	Hit/miss
1	0	0	0	0	Miss
2	4	1	0	0	Hit
3	20	5	0	0	Hit
4	136	34	1	1	Miss
5	232	58	1	1	Hit
6	164	41	1	1	Hit
7	1024	256	8	8	Miss
8	30	7	0	0	Hit
9	140	35	1	1	Hit
10	3100	775	24	24	Miss
11	176	44	1	1	Hit
12	2180	545	17	17	Miss

According to the table above, no block was replaced because no two blocks have the same block index but different block numbers.

(4).

hit ratio: 7/12 = 0.583.

(5).

<	0,	0,	Word No. 0 to word No. 31	>
<	1,	0,	Word No. 32 to word No. 63	>
<	8,	0,	Word No. 256 to word No. 287	>
<	17,	0,	Word No. 544 to word No. 575	>
<	24,	0,	Word No. 768 to word No. 799	>