Two-Wire Serial EEPROM

4K (8-bit wide)

FEATURES

- Low voltage and low power operations:
  - FT24C04A-KXX: VCC = 1.8V to 5.5V, Industrial temperature range (-40℃ to 85℃).
- 16 bytes page write mode.
- Partial page write operation allowed.
- Internally organized: 512 × 8 (4K).
- Standard 2-wire bi-directional serial interface.
- Write protect pin for hardware data protection.
- Schmitt trigger, filtered inputs for noise protection.
- Self-timed programming cycle (5ms maximum).
- 1 MHz (2.5V-5V), 400 kHz (1.8V) Compatibility.
- Automatic erase before write operation.
- High reliability: typically 1,000,000 cycles endurance.
- 100 years data retention.
- Standard 8-pin DIP/SOP/MSOP/TSSOP/DFN and 5-pin SOT-23/TSOT-23 Pb-free packages.

DESCRIPTION

The FT24C04A-KXX is 4096 bits of serial Electrical Erasable and Programmable Read Only Memory, commonly known as EEPROM. They are organized as 512 words of 8 bits (1 byte) each. The devices are fabricated with proprietary advanced CMOS process for low power and low voltage applications. These devices are available in standard 8-lead DIP, 8-lead SOP, 8-lead MSOP, 8-lead TSSOP, 8-lead DFN and 5-lead SOT-23/TSOT-23 packages. A standard 2-wire serial interface is used to address all read and write functions. Our extended V_{CC} range (1.8V to 5.5V) devices enables wide spectrum of applications.

PIN CONFIGURATION

Pin Name	Pin Function
A2, A1	Device Address Inputs
SDA	Serial Data Input / Open Drain Output
SCL	Serial Clock Input
VCC	Power Supply
WP	Write Protect
GND	Ground
NC	No-Connect

Table 1

All these packaging types come in conventional or Pb-free certified.

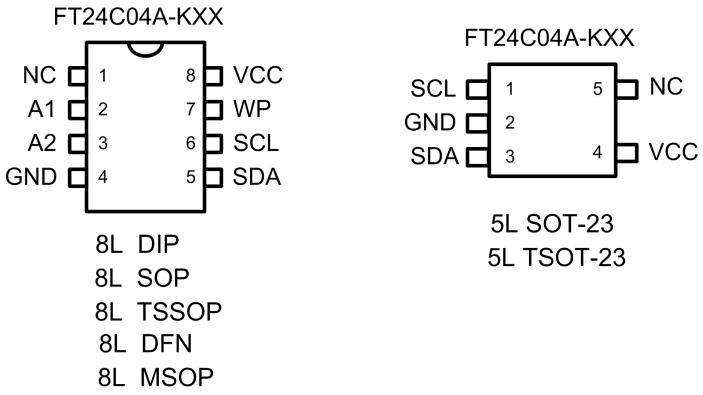


Figure 1: Package types

ABSOLUTE MAXIMUM RATINGS

Industrial operating temperature:	-40℃ to 85℃
Storage temperature:	-50℃ to 125℃
Input voltage on any pin relative to ground:	-0.3V to V_{CC} + 0.3V
Maximum voltage:	8V
ESD protection on all pins:	>2000V

** Stresses exceed those listed under "Absolute Maximum Rating" may cause permanent damage to the device. Functional operation of the device at conditions beyond those listed in the specification is not guaranteed. Prolonged exposure to extreme conditions may affect device reliability or functionality.*

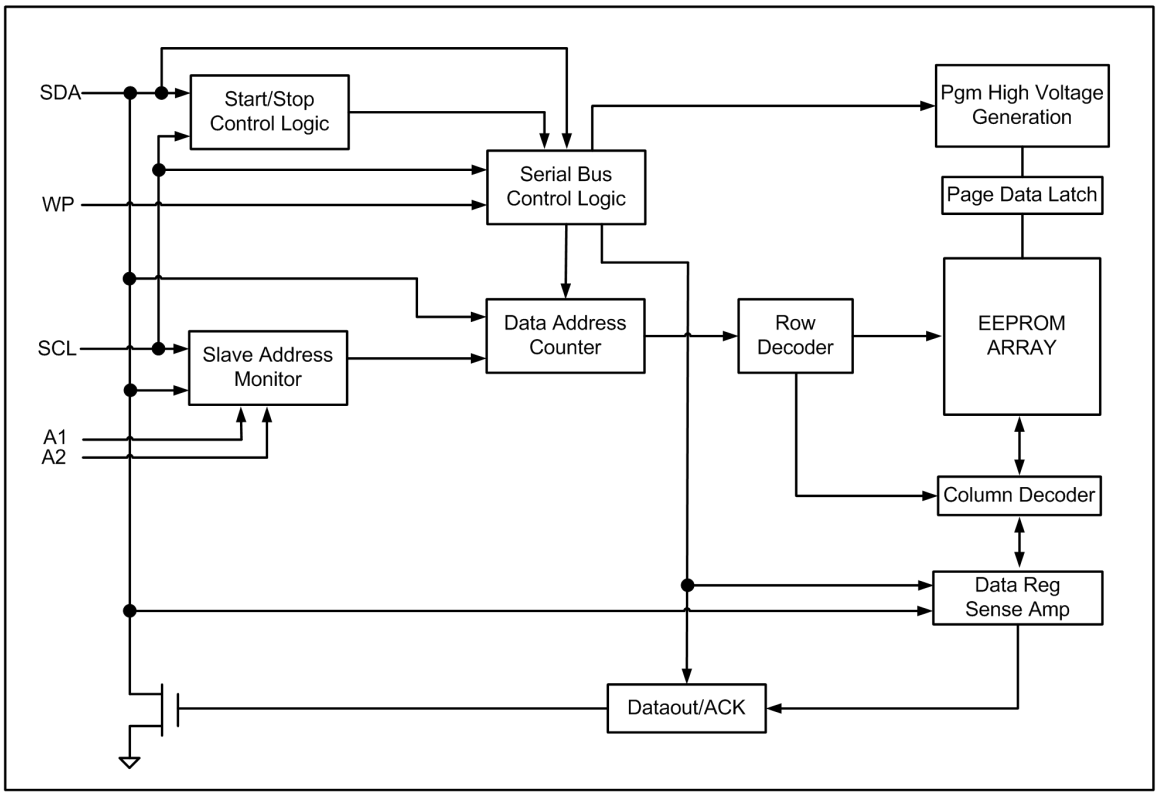


Figure 2: Block Diagram

PIN DESCRIPTIONS

(A) SERIAL CLOCK (SCL)

The rising edge of this SCL input is to latch data into the EEPROM device while the falling edge of this clock is to clock data out of the EEPROM device.

(B) SERIAL DATA LINE (SDA)

SDA data line is a bi-directional signal for the serial devices. It is an open drain output signal and can be wired-OR with other open-drain output devices.

(C) DEVICE / CHIP SELECT ADDRESSES (A2, A1)

These are the chip select input signals for the serial EEPROM devices. Typically, these signals are hardwired to either V_{IH} or V_{IL}. If left unconnected, they are internally recognized as V_{IL}. However, due to capacitive coupling that may appear in customer applications, FMD recommends always connecting the address pins to a known state. When using a pull-up or pull-down resistor, FMD recommends using 10kΩ or less.

(D) WRITE PROTECT (WP)

The FT24C04A-KXX devices have a WP pin to protect the whole EEPROM array from programming. Programming operations are allowed if WP pin is left un-connected or input to V_{IL}. Conversely all programming functions are disabled if WP pin is connected to V_{IH} or V_{CC}. Read operations is not affected by the WP pin's input level. If left unconnected, it is internally recognized as V_{IL}. However, due to capacitive coupling that may appear in customer applications, FMD recommends always connecting the WP pin to a known state. When using a pull-up or pull-down resistor, FMD recommends using 10kΩ or less.

MEMORY ORGANIZATION

The FT24C04A-KXX devices have 32 pages. Since each page has 16 bytes, random word addressing to FT24C04A-KXX will require 9 bits data word addresses.

DEVICE OPERATION

(A) SERIAL CLOCK AND DATA TRANSITIONS

The SDA pin is typically pulled to high by an external resistor. Data is allowed to change only when Serial clock SCL is at V_{IL}. Any SDA signal transition may interpret as either a START or STOP condition as described below.

(B) START CONDITION

With SCL $\geqslant$ V_{IH}, a SDA transition from high to low is interpreted as a START condition. All valid commands must begin with a START condition.

(C) STOP CONDITION

With SCL ⩾ V_{IH}, a SDA transition from low to high is interpreted as a STOP condition. All valid read or write commands end with a STOP condition. The device goes into the STANDBY mode if it is after a read command. A STOP condition after page or byte write command will trigger the chip into the STANDBY mode after the self-timed internal programming finish.

(D) ACKNOWLEDGE

The 2-wire protocol transmits address and data to and from the EEPROM in 8 bit words. The EEPROM acknowledges the data or address by outputting a "0" after receiving each word. The ACKNOWLEDGE signal occurs on the 9th serial clock after each word.

(E) STANDBY MODE

The EEPROM goes into low power STANDBY mode after a fresh power up, after receiving a STOP bit in read mode, or after completing a self-time internal programming operation.

(F) SOFT RESET

After an interruption in protocol power loss or system reset, any two-wire part can be reset by following these steps:

1. Creat a START condition,
2. Clock eighteen data bits “1”,
3. Creat a start condition as SDA is high.

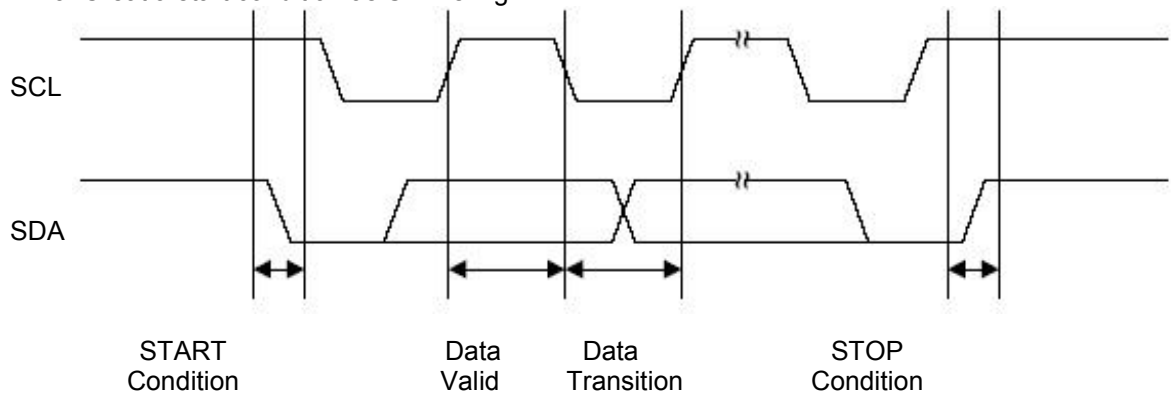


Figure 3: Timing diagram for START and STOP conditions

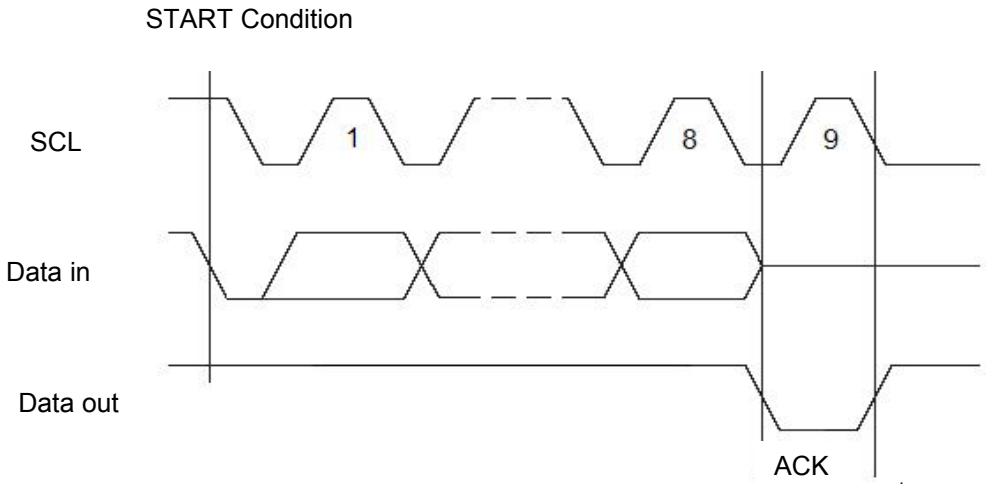


Figure 4: Timing diagram for output ACKNOWLEDGE

DEVICE ADDRESSING

The 2-wire serial bus protocol mandates an 8 bits device address word after a START bit condition to invoke a valid read or write command. The first four most significant bits of the device address must be 1010, which is common to all serial EEPROM devices. The next two bits are device address bits. These two device address bits (5^{th} and 6^{th}) are to match with the external chip select/address pin states. If a match is made, the EEPROM device outputs an ACKNOWLEDGE signal after the 8^{th} read/write bit, otherwise the chip will go into STANDBY mode. However, matching may not be needed for some or all device address bits (5^{th} and 6^{th}) as noted below. The seventh bit of the device address (P0) is a memory page address bit. The last or 8th bit is a read/write command bit. If the 8th bit is at V_{IH} then the chip goes into read mode. If a "0" is detected, the device enters programming mode.

WRITE OPERATIONS

(A) BYTE WRITE

A write operation requires the seventh bit of the device address (P0) and 8-bit data word address following the device address word and ACKNOWLEDGE signal. Upon receipt of this address, the EEPROM will respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will again output a "0". The addressing device, such as a microcontroller, must terminate the write sequence with a STOP condition. At this time the EEPROM enters into an internally-timed write cycle state. All inputs are disabled during this write cycle and the EEPROM will not respond until the writing is completed.

(B) PAGE WRITE

A page write is similar to a byte write with the exception that one to sixteen bytes can be programmed along the same page or memory row. All FT24C04A-KXX are organized to have 16 bytes per memory row or page. With the same write command as the byte write, the micro-controller does not

issue a STOP bit after sending the 1st byte data and receiving the ACKNOWLEDGE signal from the EEPROM on the 27th clock cycle. Instead it sends out a second 8-bit data word, with the EEPROM acknowledging at the 36th cycle. This data sending and EEPROM acknowledging cycle repeats until the micro-controller sends a STOP bit after the n × 9th clock cycle. After which the EEPROM device will go into a self-timed partial or full page programming mode. After the page programming completes after a time of T_{WC}, the devices will return to the STANDBY mode.

The least significant 4 bits of the word address (column address) increments internally by one after receiving each data word. The rest of the word address bits (row address) do not change internally, but pointing to a specific memory row or page to be programmed. The first page write data word can be of any column address. Up to 16 data words can be loaded into a page. If more then 16 data words are loaded, the 9th data word will be loaded to the 1st data word column address. The 10th data word will be loaded to the 2nd data word column address and so on. In other word, data word address (column address) will "roll" over the previously loaded data.

(C) ACKNOWLEDGE POLLING

ACKNOWLEDGE polling may be used to poll the programming status during a self-timed internal programming. By issuing a valid read or write address command, the EEPROM will not acknowledge at the 9th clock cycle if the device is still in the self-timed programming mode. However, if the programming completes and the chip has returned to the STANDBY mode, the device will return a valid ACKNOWLEDGE signal at the 9th clock cycle.

READ OPERATIONS

The read command is similar to the write command except the 8th read/write bit in address word is set to "1". The three read operation modes are described as follows:

(A) CURRENT ADDRESS READ

The EEPROM internal address word counter maintains the last read or write address plus one if the power supply to the device has not been cut off. To initiate a current address read operation, the micro-controller issues a START bit and a valid device address word with the read/write bit (8th) set to "1". The EEPROM will response with an ACKNOWLEDGE signal on the 9th serial clock cycle. An 8-bit data word will then be serially clocked out. The internal address word counter will then automatically increase by one. For current address read the micro-controller will not issue an ACKNOWLEDGE signal on the 18th clock cycle. The micro-controller issues a valid STOP bit after the 18th clock cycle to terminate the read operation. The device then returns to STANDBY mode.

(B) SEQUENTIAL READ

The sequential read is very similar to current address read. The micro-controller issues a START bit and a valid device address word with read/write bit (8th) set to "1". The EEPROM will response with an ACKNOWLEDGE signal on the 9th serial clock cycle. An 8-bit data word will then be serially clocked out. Meanwhile the internally address word counter will then automatically increase by one. Unlike current address read, the micro-controller sends an ACKNOWLEDGE signal on the 18th clock

cycle signaling the EEPROM device that it wants another byte of data. Upon receiving the ACKNOWLEDGE signal, the EEPROM will serially clocked out an 8-bit data word based on the incremented internal address counter. If the micro-controller needs another data, it sends out an ACKNOWLEDGE signal on the 27th clock cycle. Another 8-bit data word will then be serially clocked out. This sequential read continues as long as the micro-controller sends an ACKNOWLEDGE signal after receiving a new data word. When the internal address counter reaches its maximum valid address, it rolls over to the beginning of the memory array address. Similar to current address read, the micro-controller can terminate the sequential read by not acknowledging the last data word received, but sending a STOP bit afterwards instead.

(C) RANDOM READ

Random read is a two-steps process. The first step is to initialize the internal address counter with a target read address using a "dummy write" instruction. The second step is a current address read.

To initialize the internal address counter with a target read address, the micro-controller issues a START bit first, follows by a valid device address with the read/write bit (8th) set to "0". The EEPROM will then acknowledge. The micro-controller will then send the address word. Again the EEPROM will acknowledge. Instead of sending a valid written data to the EEPROM, the micro-controller performs a current address read instruction to read the data. Note that once a START bit is issued, the EEPROM will reset the internal programming process and continue to execute the new instruction - which is to read the current address.

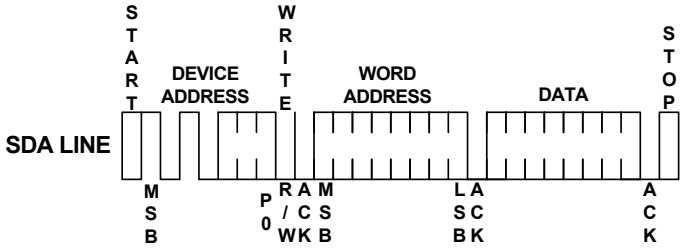


Figure 5: Byte Write

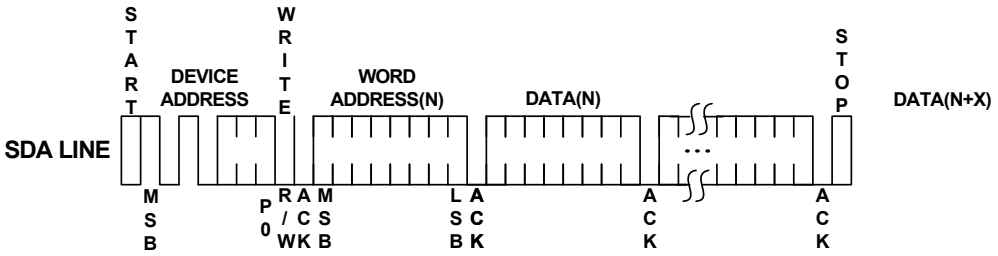


Figure 6: Page Write

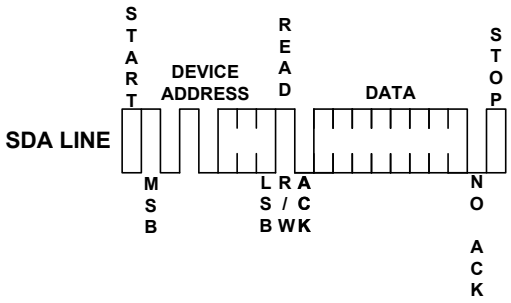


Figure 7: Current Address Read

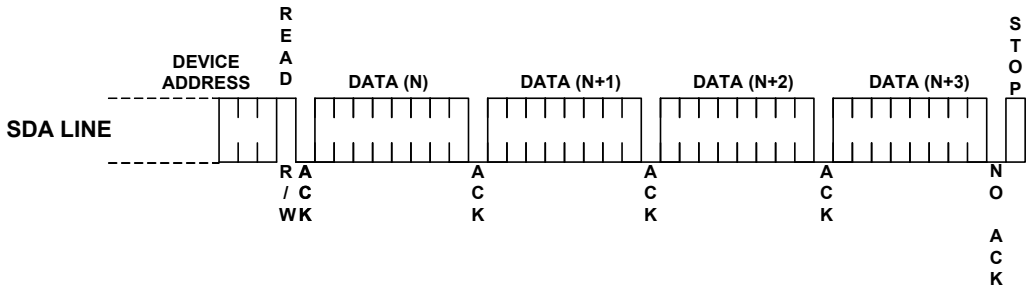


Figure 8: Sequential Read

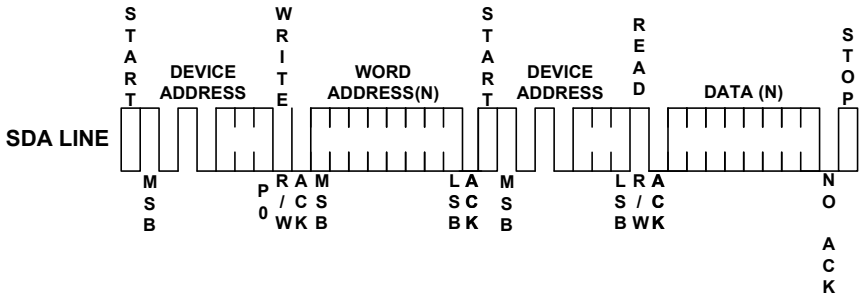


Figure 9: Random Read

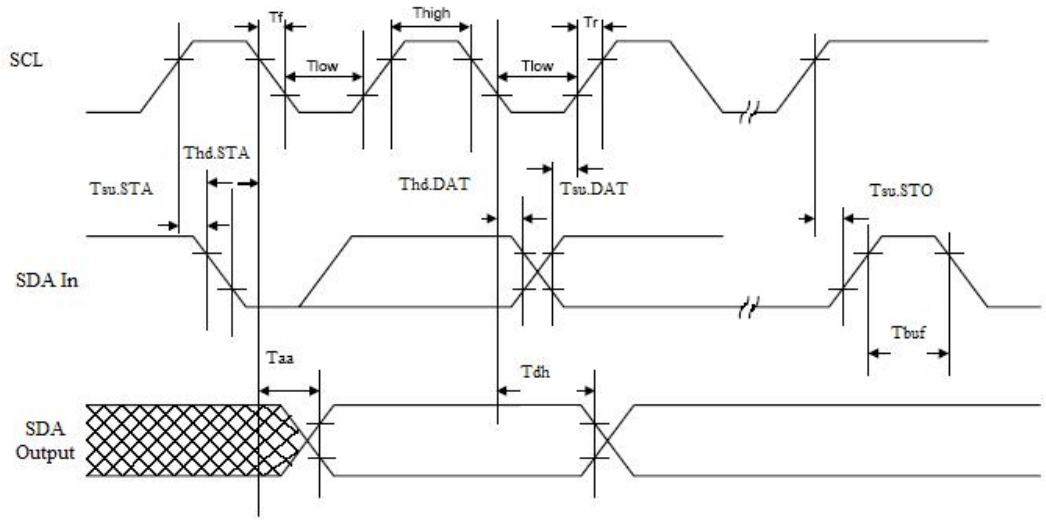


Figure 10: SCL and SDA Bus Timing

Electrical Specifications

(A)Power-Up Requirements

During a power-up sequence, the VCC supplied to the device should monotonically rise from GND to the minimum VCC level, with a slew rate no faster than 0.05 V/μs and no slower then 0.1 V/ms. A decoupling cap should be connected to the VCC PAD which is no smaller than 10nF.

(B)Device Reset

To prevent inadvertent write operations or any other spurious events from occurring during a power-up sequence, this device includes a Power-on Reset (POR) circuit. Upon power-up, the device will not respond to any commands until the VCC level crosses the internal voltage threshold (V_{POR}) that brings the device out of Reset and into Standby mode. The system designer must ensure the instructions are not sent to the device until the VCC supply has reached a stable value greater than or equal to the minimum VCC level.

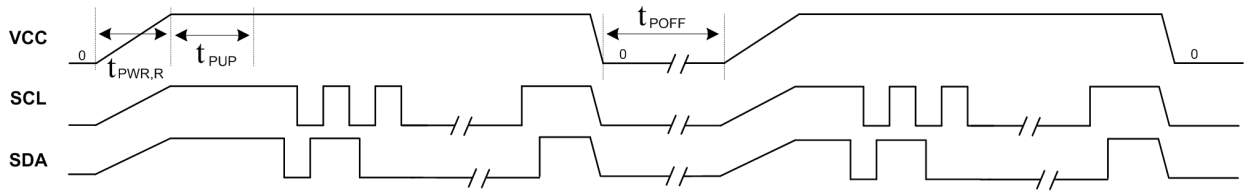


Figure 11: Power on and Power down

If an event occurs in the system where the VCC level supplied to the device drops below the maximum V_{POR} level specified, it is recommended that a full power cycle sequence be performed by first driving the VCC pin to GND, waiting at least the minimum t_{POFF} time and then performing a new power-up sequence in compliance with the requirements defined in this section.

AC CHARACTERISTICS

Symbol	Parameter	1.8 V		2.5V-5.5V		Unit
		Min	Max	Min	Max	
f_{SCL}	Clock frequency, SCL		400		1000	kHz
t_{LOW}	Clock pulse width low	1.3		0.4		μs
t_{HIGH}	Clock pulse width high	0.6		0.4		μs
t_I	Noise suppression time(1)		50		50	ns
t_{AA}	Clock low to data out valid		0.9		0.55	μs
t_{BUF}	Time the bus must be free before a new transmission can start(1)	1.3		0.5		μs
$t_{HD.STA}$	START hold time	0.6		0.25		μs
$t_{SU.STA}$	START set-up time	0.6		0.25		μs
$t_{HD.DAT}$	Data in hold time	0		0		μs
$t_{SU.DAT}$	Data in set-up time	100		100		ns
t_R	Input rise time(1)		0.3		0.3	μs
t_F	Input fall time(1)		300		100	ns
$t_{SU.STO}$	STOP set-up time	0.6		0.25		μs
t_{DH}	Date out hold time	50		50		ns
$t_{PWR,R}$(1)	Vcc slew rate at power up	0.1	50	0.1	50	V/ms
t_{PUP}(1)	Time required after VCC is stable before the device can accept commands	100		100		μs
t_{POFF}(1)	Minimum time at Vcc=0V between power cycles	500		500		ms
t_{WR}	Write cycle time		5		5	ms
Endurance(1)	25°C, Page Mode, 3.3V	1,000,000				Write Cycles

Notes*: 1. This Parameter is expected by characterization but is not fully screened by test.

2. AC Measurement conditions:

R_L (Connects to Vcc): 1.3KΩ

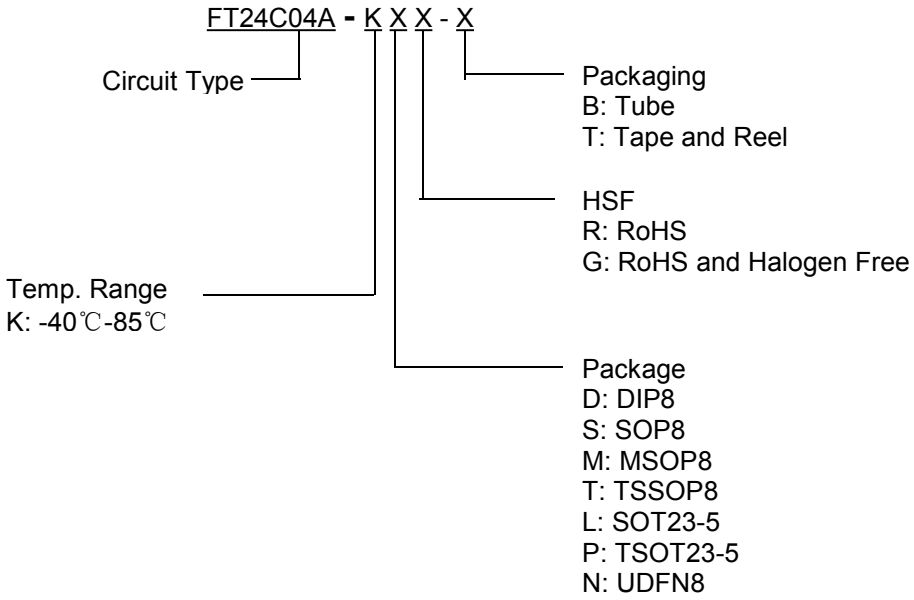
Input Pulse Voltages: 0.3Vcc to 0.7Vcc

Input and output timing reference Voltages: 0.5Vcc

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typical	Max	Units
V_{CC1}	Power supply V_{CC}		1.8		5.5	V
I_{CC1}	Supply read current	V_{CC} @ 5.0V SCL = 400 kHz		0.5	1.0	mA
I_{CC2}	Supply write current	V_{CC} @ 5.0V SCL = 400 kHz		2.0	3.0	mA
I_{SB1}	Supply current	V_{CC} @ 1.8V, V_{IN} = V_{CC} or V_{SS}		< 1.0		μA
I_{SB2}	Supply current	V_{CC} @ 2.5V, V_{IN} = V_{CC} or V_{SS}		< 1.0		μA
I_{SB3}	Supply current	V_{CC} @ 5.0V, V_{IN} = V_{CC} or V_{SS}		< 1.0		μA
I_{IL}	Input leakage current	V_{IN} = V_{CC} or V_{SS}			3.0	μA
I_{LO}	Output leakage current	V_{IN} = V_{CC} or V_{SS}			3.0	μA
V_{IL}	Input low level		-0.6		V_{CC} × 0.3	V
V_{IH}	Input high level		V_{CC} × 0.7		V_{CC} + 0.5	V
V_{OL1}	Output low level	V_{CC} @ 1.8V, I_{OL} = 0.15 mA			0.2	V
V_{OL2}	Output low level	V_{CC} @ 3.0V, I_{OL} = 2.1 mA			0.4	V

ORDER CODE:

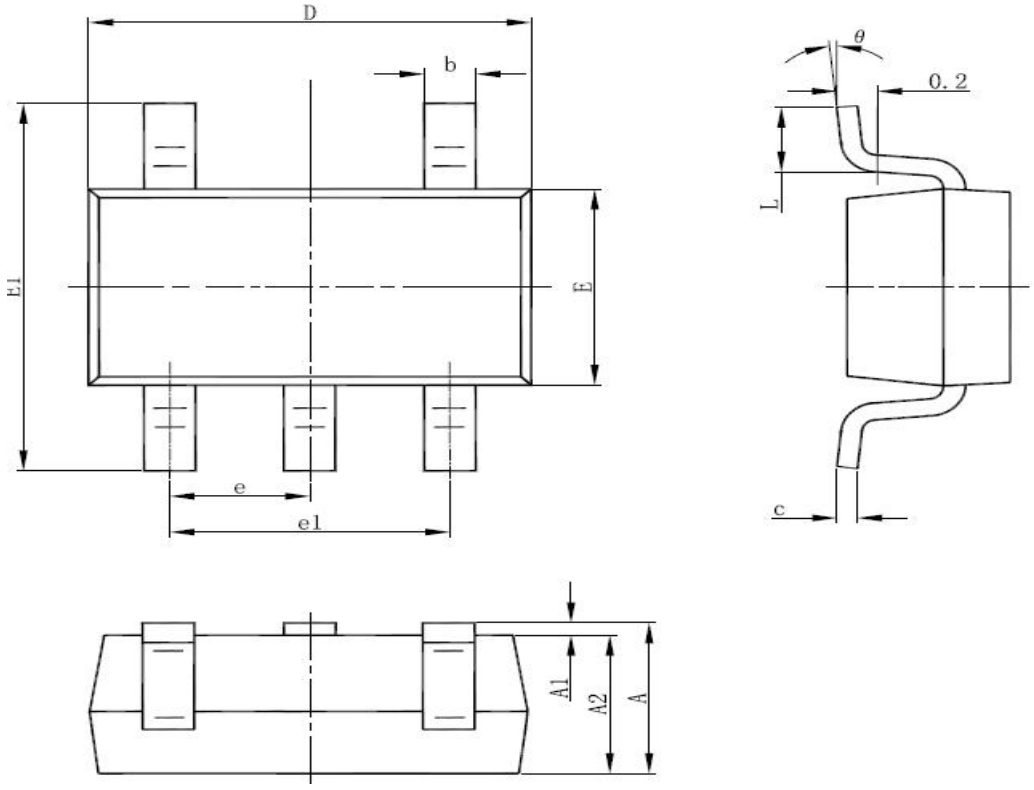


ORDER INFORMATION

Package	Temperature Range	Vcc	HSF	Packaging	Order code
SOT23-5	-40℃-85℃	1.8V-5.5V	RoHS	Tape and Reel	FT24C04A-KLR-T*
			Green	Tape and Reel	FT24C04A-KLG-T*
TSOT23-5	-40℃-85℃	1.8V-5.5V	RoHS	Tape and Reel	FT24C04A-KPR-T*
			Green	Tape and Reel	FT24C04A-KPG-T*
DIP8	-40℃-85℃	1.8V-5.5V	RoHS	Tube	FT24C04A-KDR-B
			Green	Tube	FT24C04A-KDG-B
SOP8	-40℃-85℃	1.8V-5.5V	RoHS	Tube	FT24C04A-KSR-B
				Tape and Reel	FT24C04A-KSR-T
			Green	Tube	FT24C04A-KSG-B
				Tape and Reel	FT24C04A-KSG-T
TSSOP8	-40℃-85℃	1.8V-5.5V	RoHS	Tube	FT24C04A-KTR-B
				Tape and Reel	FT24C04A-KTR-T
			Green	Tube	FT24C04A-KTG-B
				Tape and Reel	FT24C04A-KTG-T
UDFN8	-40℃-85℃	1.8V-5.5V	RoHS	Tape and Reel	FT24C04A-KNR-T
			Green	Tape and Reel	FT24C04A-KNG-T

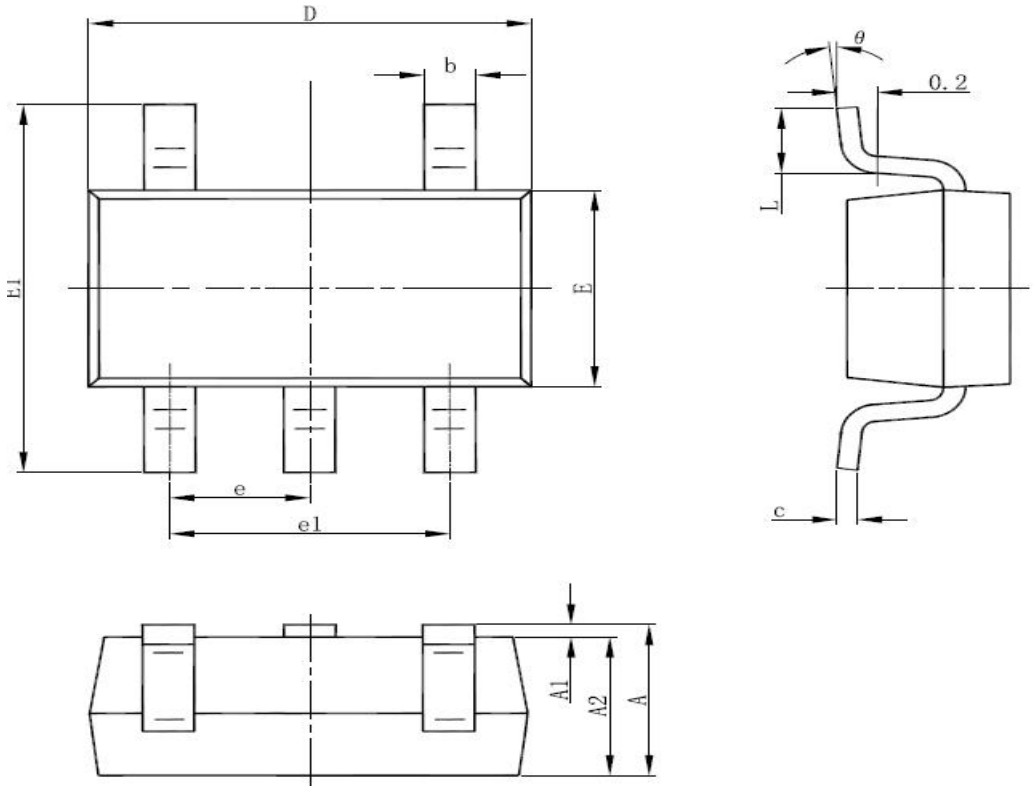
*** KLR/KLG/KPR/KPG : The device address A2 and A1 bits must be set to zero**

SOT-23-5 PACKAGE OUTLINE DIMENSIONS



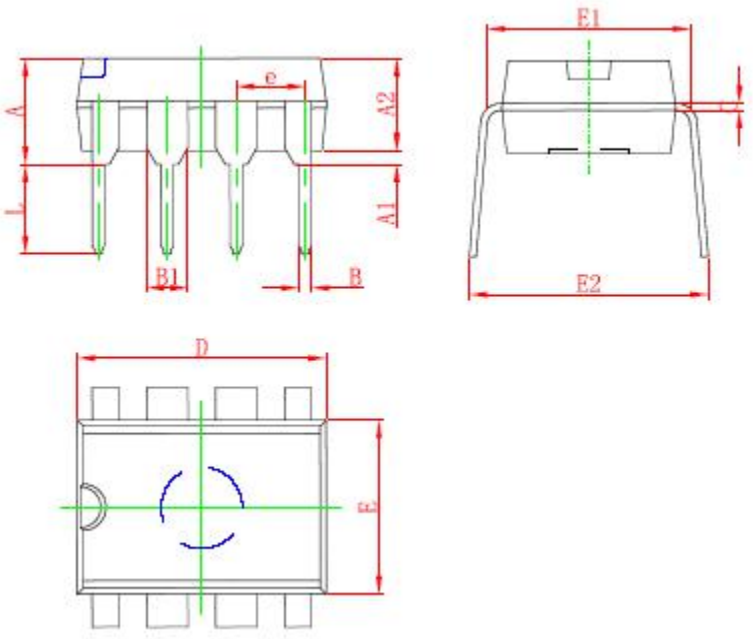
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.95 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	6°

TSOT-23-5 PACKAGE OUTLINE DIMENSIONS



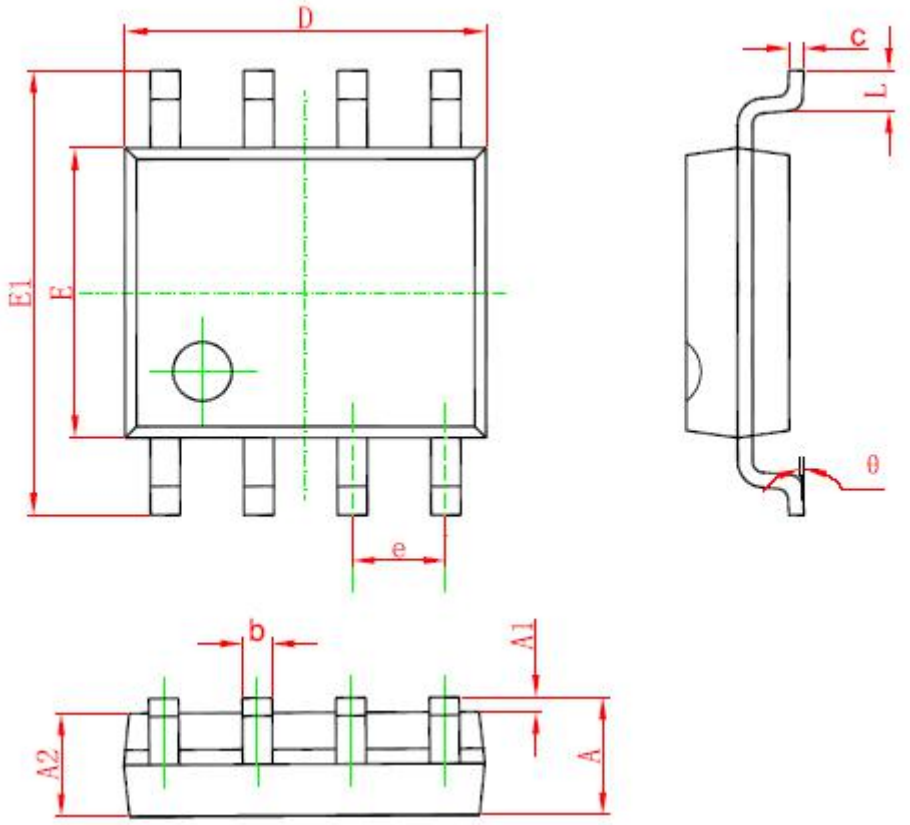
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.900	0.028	0.035
A1	0.000	0.100	0.000	0.004
A2	0.700	0.800	0.028	0.031
b	0.350	0.500	0.014	0.020
c	0.080	0.200	0.003	0.008
D	2.820	3.020	0.111	0.119
E	1.600	1.700	0.063	0.067
E1	2.650	2.950	0.104	0.116
e	0.95 (BSC)		0.037 (BSC)	
e1	1.90 (BSC)		0.075 (BSC)	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

DIP8 PACKAGE OUTLINE DIMENSIONS



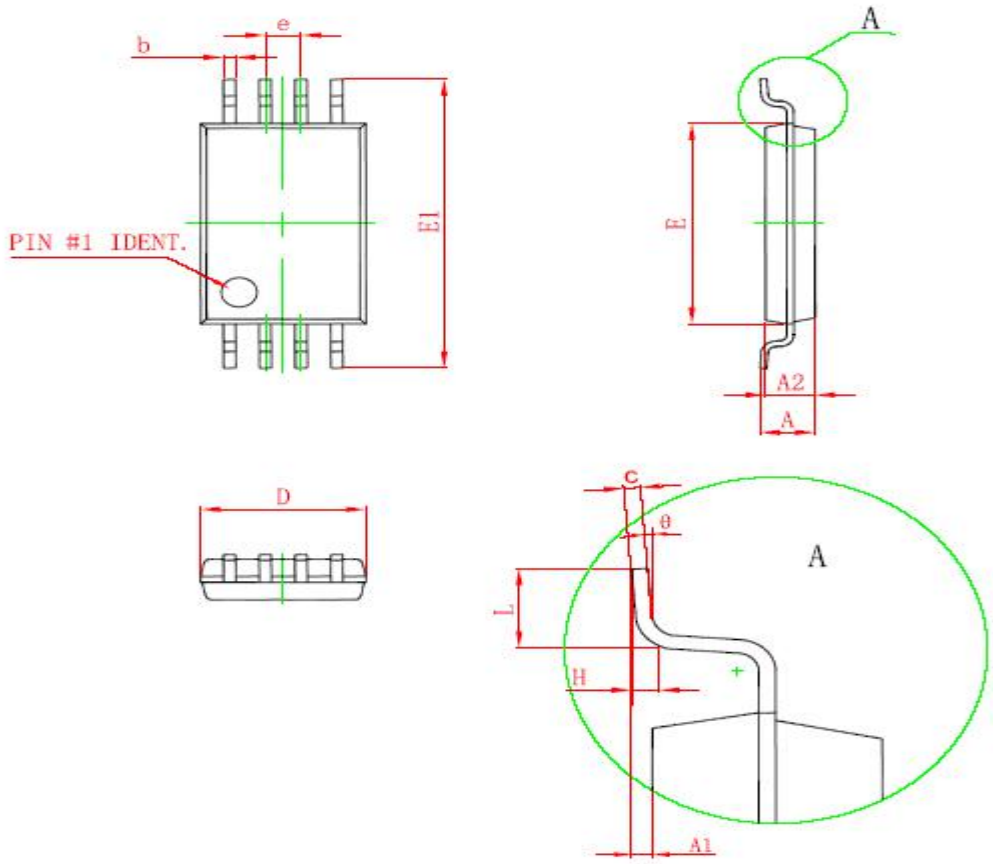
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524（BSC）		0.060（BSC）	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100（BSC）	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

SOP8 PACKAGE OUTLINE DIMENSIONS



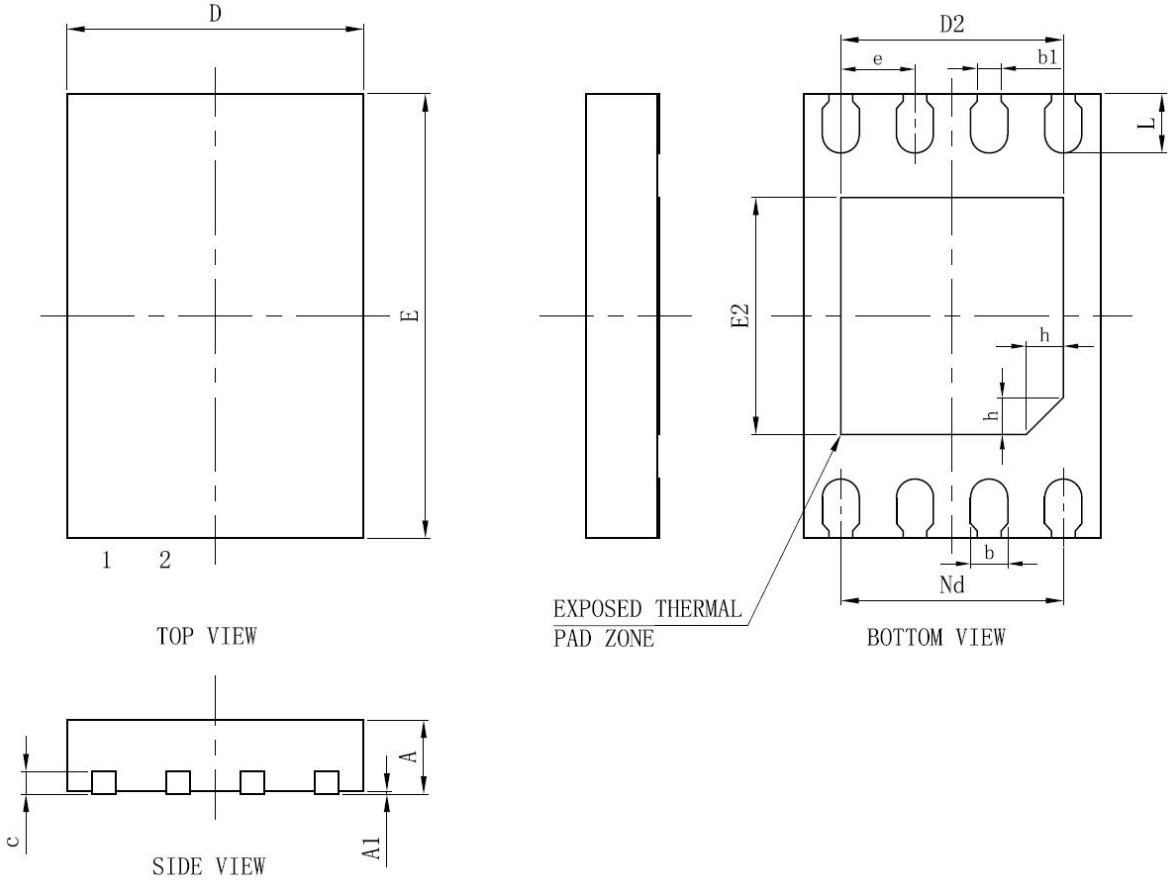
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

TSSOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
θ	1°	7°	1°	7°

UDFN8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.450	0.550	0.017	0.021
A1	0.000	0.050	0.000	0.002
b	0.180	0.300	0.007	0.039
b1	0.160REF		0.006REF	
c	0.100	0.200	0.004	0.008
D	1.900	2.100	0.075	0.083
D2	1.400	1.600	0.055	0.062
e	0.500BSC		0.020BSC	
Nd	1.500BSC		0.059BSC	
E	2.900	3.100	0.114	0.122
E2	1.500	1.700	0.059	0.067
L	0.300	0.500	0.012	0.020
h	0.200	0.300	0.066	0.12

Fremont Micro Devices (SZ) Limited

#1&5-8, 10/F, Changhong Building, Ke-Ji Nan 12 Road, Nanshan District, Shenzhen
Tel: (86 755) 86117811
Fax: (86 755) 86117810

Fremont Micro Devices (Hong Kong) Limited

#16, 16/F, Blk B, Veristrong Industrial Centre, 34-36 Au Pui Wan Street, Fotan, Shatin, Hong Kong
Tel: (852) 27811186
Fax: (852) 27811144

Web Site: http://www.fremontmicro.com/