Project Plan report format – Your first page MUST match this format

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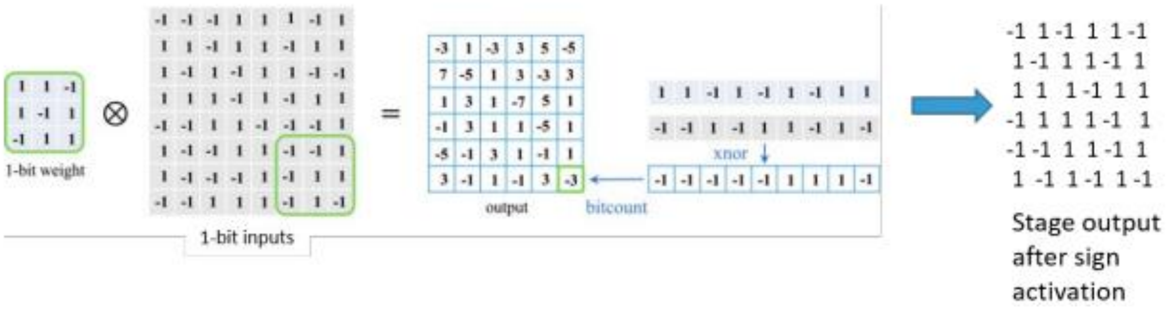
Summary Risk Plan:
The area that I am most unsure of in this design is the controller and state machine. I think I understand pretty well how the convolutional neural network works conceptually and can implement the data manipulation well enough. However, receiving the control signals throw me off. In executing this project, my greatest concerns is getting the timing down properly. I am a bit uncertain in my abilities to optimize designs and so making sure that the signals are asserted at specific clock cycles will be a bit tricky. Also synthesis is still a huge weak point of mine in general and so approaching that in my own design without instruction will be a bit of a challenge.

Schedule:
10/25 – Controller Design Complete
10/29 – Datapath Design Programmed
11/3 – Controller Programmed
11/5 – Connected Datapath and Controller
11/8 – Verification of Design
11/10 – Final Project Turn-in

Verification Plan:
In order to verify that my design functions properly, I plan to create a more exhaustive test bench with hand verified examples of different input matrices and verify them according to a golden output data file. I also plan to perform timing verification and design check using the different synthesis tools we have used in class. I also plan to hand verify a timing diagram and compare with the output waveform.

Brief Description of Mode of operation, including selected algorithms
After reading the documentation, the overall approach that I have decided to use to tackle this problem is to replace the multiply and add portions of the convolution with XNORs and bit counting. This picture from the project specification demonstrates the conceptual approach I will be taking:



1	1	-1
1	-1	1
-1	1	1

-1	-1	-1	1	1	1	-1	1
1	1	-1	1	1	-1	1	1
1	-1	1	-1	1	1	-1	-1
1	1	1	-1	1	-1	1	1
-1	-1	1	1	-1	-1	-1	1
1	-1	-1	1	1	-1	-1	1
1	-1	-1	-1	1	-1	1	1
-1	-1	1	1	1	-1	1	-1

-3	1	-3	3	5	-5
7	-5	1	3	-3	3
1	3	1	-7	5	1
-1	3	1	1	-5	1
-5	-1	3	1	-1	1
3	-1	1	-1	3	-3

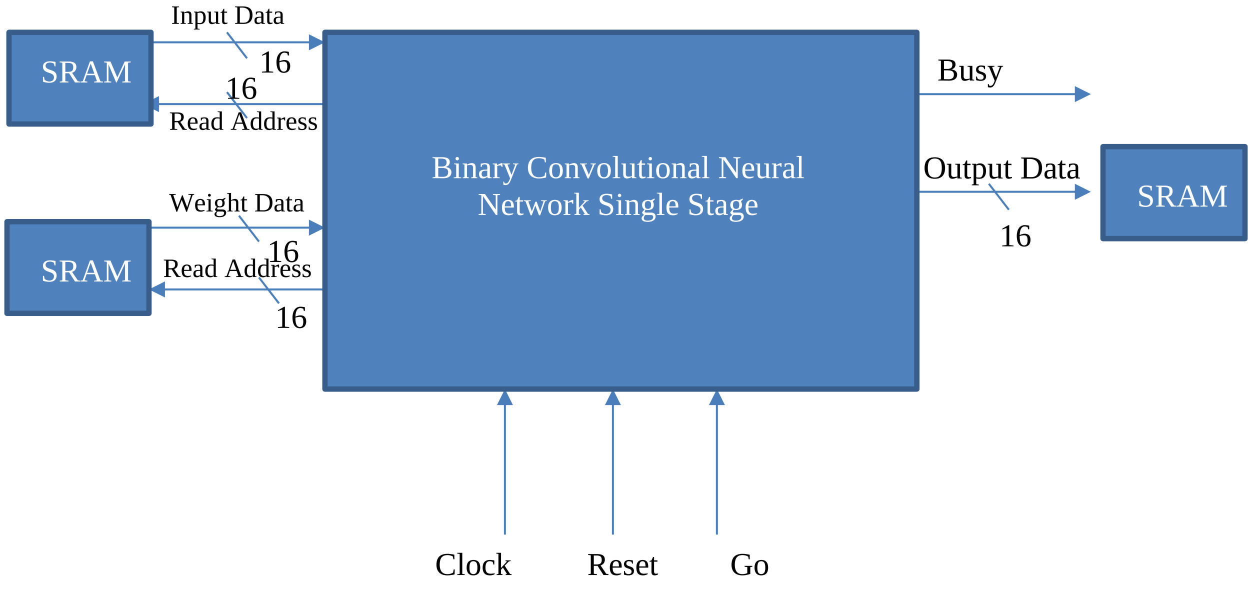
1	1	-1	1	-1	1	-1	1	1
-1	-1	1	-1	1	1	-1	1	-1
-1	-1	-1	-1	-1	1	1	1	-1

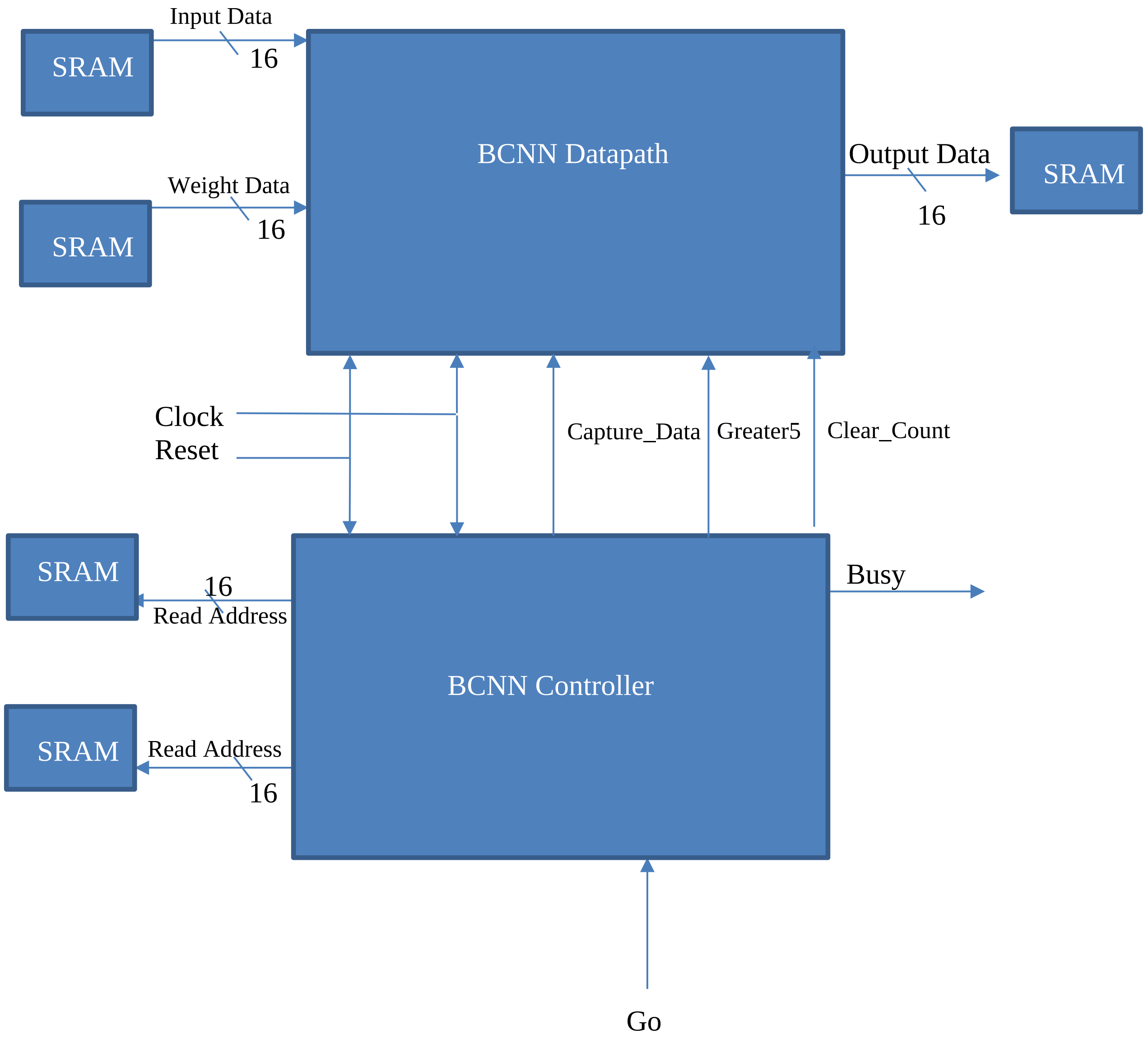
-1	1	-1	1	1	-1
1	-1	1	1	-1	1
1	1	1	-1	1	1
-1	1	1	1	-1	1
-1	-1	1	1	-1	1
1	-1	1	-1	1	-1

Knowing that the input matrix will be of size 4x4, and the weighted matrix will be of size 3x3, we know that the output matrix will ultimately be of size 2x2. This is because the size of the output matrix is equal to the size of the input matrix – size of weight matrix + 1. The way the data is packed, we can treat each matrix as an array of sorts.

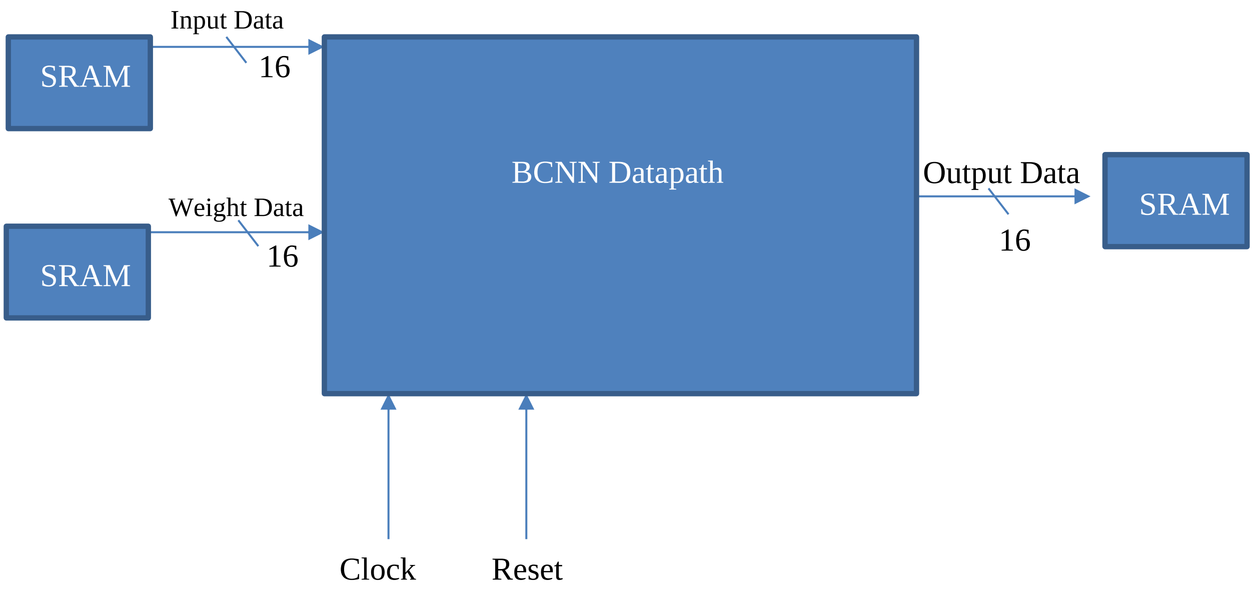
Upon received the signal to process the data, The input will be split into four separate sections representation each overlay that would occur during convolution by hand. Various bits from the input data are concatenated together and then XNOR'd with the least significant 9 bits of the weighted data. This array of bits is then iterated through and at each point where a 1 occurs, it is added to a counter. This way we can measure if our value has more ones or zeroes and can determine the output. If there are 5 or more 1's than we can determine that the output will be a 1.

High level sketch.

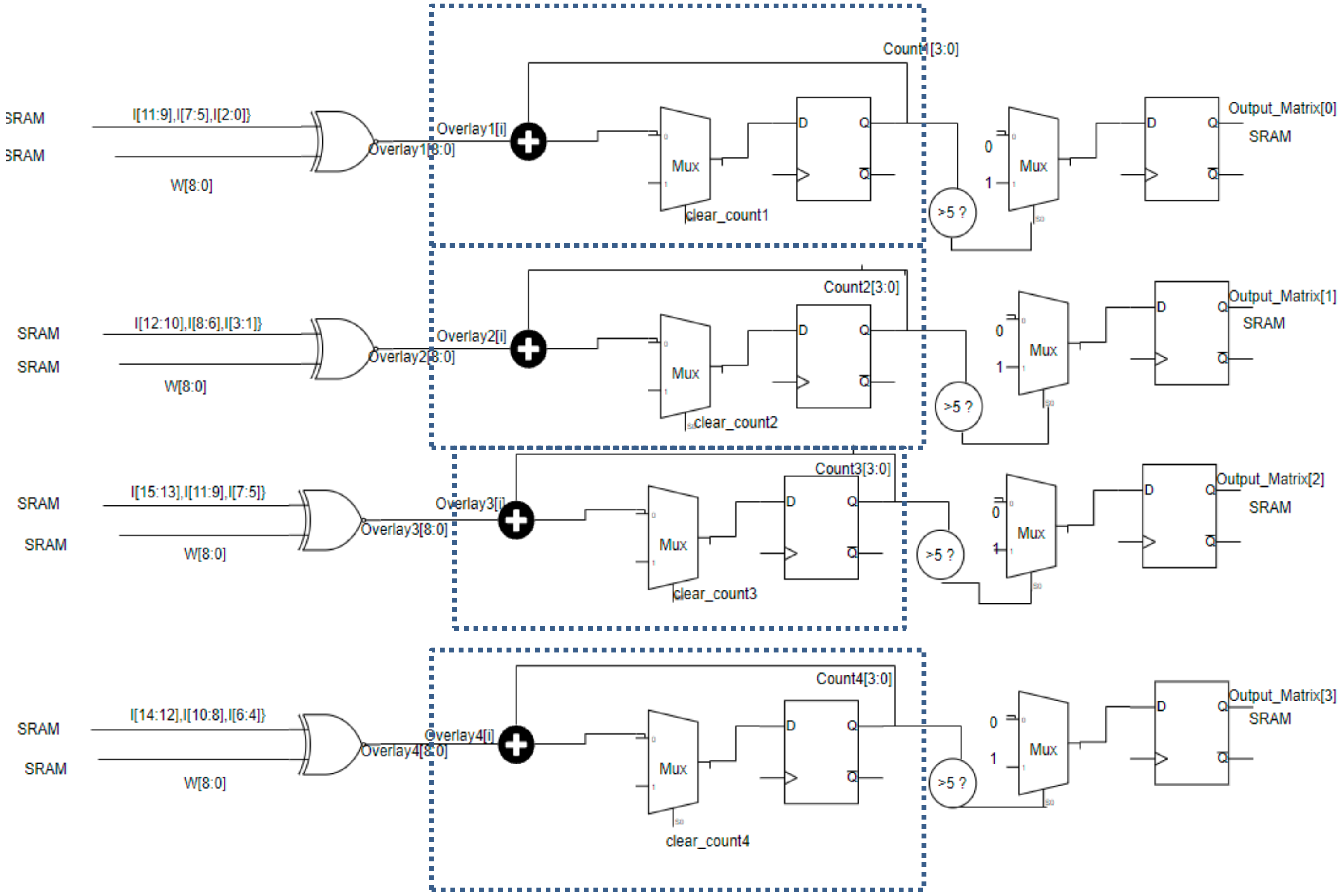




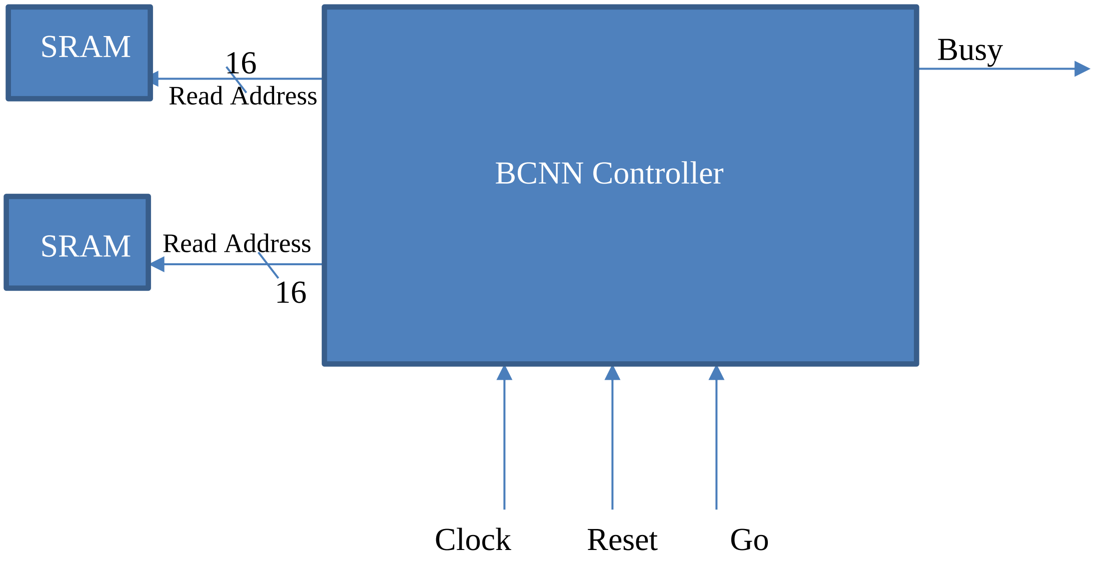
Datapath: The datapath will be taking the two input matrices from the SRAM and manipulating them in a way that will result in the correct output matrix.



The dotted lines are a representation of a for loop



Controller: The controller will manipulate signals given by the testbench and the control signals in the datapath. For this particular controller, it will determine when and what address needs to be read in SRAM in order to deliver the proper inputs to the datapath. Also, it will assert a busy signal when the calculations are being performed so the test bench knows when to halt and not input data too early. There will be a few internal signals that I have designed in order to better communicate with the datapath. In particular, a clear_count signal to clear a count of 1's in order to perform a bit count after the XNOR calculation. A signal will also be asserted when that count is greater than 5, after a for loop has iterated through the array of values. The high level block diagram appears as follows:


SRAM
16
Read Address
SRAM
Read Address
16
BCNN Controller
Busy
Clock
Reset
Go