Preliminary report

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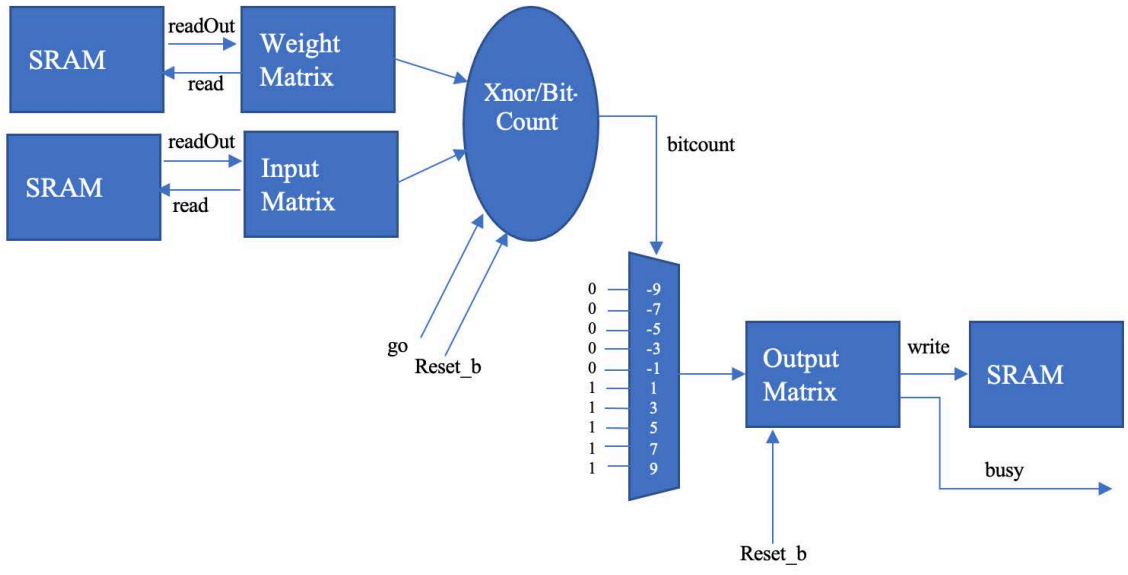
Name: Jon Mark Long **StudentID**: 200256447 **UnityID**: jmlong4	10/24 - datapath design 10/29 - controller design 11/1 - code datapath	11/4 - code controller 11/6 - synthesis 11/10 - timing and adjustments	**Schedule**

Summary Risk Plan: The biggest risk is my inexperience which makes project planning and estimation of timeline difficult. It's hard to know how difficult something will be when you haven't done it often. Another risk is hitting a roadblock that I am not technically proficient enough to solve with out help. I plan to work early so that I am not running into deadlines and have plenty of time to seek assistance if I need it

Verification Plan: After a hand design of the project, I will first create a hand drawn timing diagram. Then after I have designed and coded my project I will create a test bench that check and outputs errors when the output does not match the expected output I created in my hand drawn timing diagram. Lastly I'll double check that my design meets all the specifications of the project.

Brief Description of Mode of operation, including selected algorithms: First read in the weights, then the inputs, then do the first xnors, add 1 to bitcount when the xnor = 1 and minus 1 when xnor = 0, then check bitcout for plus or minus 9,7,5,3,1, if it's the plus version, that output bit gets 1, if minus, 0 (I think this will be less logic than a comparison statement). Once the output matrix is complete, write it back to memory making sure to pause reading. I also plan on trying to find patterns to reuse inside the matrix since the internal values are reused 9 times, but the outside border only once. Those patterns and pipelining to read or write to memory every clock cycle will enable an efficient and compact hardware design of this project.

High level sketch.



Weight and Input Matrices hold the info to send to the computation block which executes then outputs a count of the 1's relevant to the current Output Matrix cell. This count then decides whether to send a 0 or 1 to the Output Matrix. When the Matrix is complete it is written to the SRAM.