December 4, 2019

Subject: UMC-to-USJC 40nm Process Transfer - Characterization Summary

SYNOPSIS

In August of 2014, UMC and MIFS (Mie USJC Semiconductor) entered into a partnership to share 40nm technology. Lattice does business with both MIFS and UMC and used this opportunity to create a 40nm second source.

In June of 2018, UMC completed the purchase of MIFS to create a wholly-owned subsidiary, called USJC (United Semiconductor Japan Co., Ltd). The rest of this document will refer to the new entity even though the work originally started with MIFS.

Lattice has completed the transfer of the 40nm Low Power (40LP) process from UMC to USJC on three devices: ECP5U-25F, ECP5U-45F and the LIF-MD6000(Crosslink). This document summarizes the electrical characterization of those devices. Lattice recommends release of the USJC-version of these three devices into full production.

OVERALL TRANSFER PLAN

The process transfer occurred over many months. Here is a graphical overview of the process steps and sequence.

	ECP5-45							ECP4-25, LIF-MD6000		
Mask:	Shuttle Mask	Production Mask						Production Mask		
Lots:	Eng lots	Eng Lots	Production Lots					Production Lots		
Outcome:	Process Optimization via Etest and Wafer Characterization		Wafer Char	Package Assembly	Package Char	Silicon Qual	Package Qual	Wafer Char	Package Assembly	Package Char (MIPI)

The ECP5-45 was first taped out on a multi-die shuttle mask that allowed Lattice and USJC to make incremental process changes to match the performance of UMC processed wafers. The process was checked through wafer sort yield, construction analysis and comparison of parametric scribe measurements. A total of 12 shuttle lots were run before the LFE5U-45F was taped out in a dedicated production mask.

Characterization was performed in two steps. Wafer level characterization was performed for increased sample size. Unit-level characterization was also performed on packaged devices (381caBGA) for those tests that were not conducive to the wafer probe environment or that required specialized bench equipment. Process-skewed wafers from both foundries were tested at the same time for performance comparisons over expected process variations.

Wafer and unit characterizations were also performed by two separate engineering groups, that while coordinated in the planning process, allowed for independent auditing and reporting of the results.

There were no schematic changes of the ECP5-45F associated with the conversion to the MIFS fab**.**

Once the characterization of the ECP5-45 was completed, the product was released on a limited basis to one customer. There have been **no application issues** with this customer in high volume production.

At that point, production masks were taped out for the ECP5-25 and LIF-MD6000 and the characterization process was repeated. Package characterization focused on unique IP blocks of the LIF-MD6000, especially the MIPI block. This report will focus on the ECP5-45 but also summarizes the key aspects of the ECP5-25 and LIF-MD6000, where different.

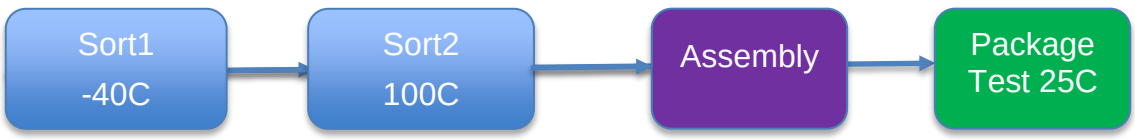
Maskset	Description
ECP5-45-01B	UMC Production Maskset
ECP5-45-02A	USJC Shuttle Maskset
ECP5-45-02B	USJC Production Maskset
ECP5-25-01B	UMC Production Maskset
ECP5-25-02A	USJC Production Maskset
LIF-MD6000-01E	UMC Production Maskset
LIF-MD6000-02A	USJC Production Maskset

E-TEST or WAT SPECIFICATIONS

Wafer Acceptance Testing (WAT, aka E-Test) is the process of making transistor-level parametric measurements on test structures in the wafer scribelines. It is important to note that all 3 products use identical Wafer Acceptance Test (WAT, aka E-Test) specifications and measurement procedures in both the USJC and UMC fabs.

WAFER SORT YIELD SUMMARY

All ECP5 wafers and packaged units for characterization first went through the standard production test flow which is shown graphically below.

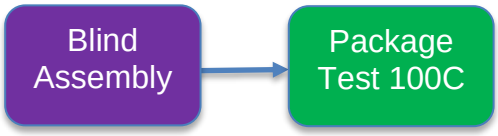


ECP5 Production Test Flow

DEVICE	QTY	Sort1 Yield (-40C)	Sort2 Yield (100C)
FE5UM-45F UMC	73	1.00	1.00
FE5UM-45F USJC	17	1.01	0.99
FE5UM-25F UMC	25	1.00	1.00
FE5UM-25F USJC	1	0.88	0.88

ECP5 Sort Yield Summary (TT Wafers)

The chart above compares normalized ECP5 sort yield for TT wafers from both UMC and USJC. ECP5-45 wafers yielded nearly the same from both foundries. ECP5-25 wafers from USJC suffered from a gross fail area in the center. Corrective action has been performed and this hasn't been seen on subsequent lots from USJC.



Crosslink Production Test Flow

As can be seen by the above diagram, Crosslink does not typically have a wafer sort step (the only exception is Automotive-grade Crosslink). However, for the purposes of this report a sample of typical UMC and USJC wafers were sorted for comparison. The chart below shows normalized yield figures and shows that USJC yield slightly better than UMC but the difference is minimal.

DEVICE	QTY	Sort Yield (25C)
LIF-MD6000 UMC	7	1
LIF-MD6000 USJC	1	1.03

Crosslink Wafer Sort Comparison

SAMPLE SELECTION

ECP5-45

As the first in their family products to transfer from UMC to USJC, the ECP5-45 and the LIF-MD6000 had extensive sample sizes for wafer characterization. After standard production sort1 and sort2, the following samples were run through a wafer characterization program at -40C, 25C and 125C. The wafers were processed intentionally fast, slow and with skews to push the process to its extreme. For instance, “FS” means fast N-channel/slow P-channels – a condition that is unlikely to be replicated in typical production. The die tested were sampled across the entire wafer.

Lot	Split	Fab	Sample Size
4C46916-07	SS	USJC	984
4C46916-09	FS	USJC	903
4C46916-11	SF	USJC	769
4C45843-05	TT	USJC	921
4C45843-06	FF	USJC	364
KLTAF02	TT	UMC	230

ECP5-45 Wafer Characterization Samples

OCRID	SPLIT	FAB	SAMPLE SIZE	NVCM SAMPLE SIZE
4C54297-13	TT	FUJ	314	146
4C54297-14	SS	FUJ	302	150
4C54297-15	FS	FUJ	303	149
4C54297-22	FF	FUJ	296	150
4C54297-23	SF	FUJ	282	150
K0STW-02	SS	UMC	270	NA
K0STW-04	FF	UMC	285	NA

LIF-MD6000 Wafer Characterization Samples

Both products were then characterized at -40C, 25C, 100C and 125C at the wafer-level. By performing characterization at the wafer-level, we can be assured that the DUT junction temperature equals the forced chuck temperature.

The ECP5-25 wafer characterization was performed at the production test temperatures of -40C and 100C listed above.

POR

POR stands for Power-On Reset. In this case it is a Pass/Fail test that makes sure the part has correctly initialized itself after power up and before it reaches the minimum datasheet voltage for correct operation. Each die was ramped from 0V to 1.0V (below the minimum operating voltage for ECP5) and then checked for correct operation. The test was repeated 100 times for each die. There were no fails for any splits across all temperatures.

Correct POR operation is obviously important from an operational perspective but it is also a good indication of process matching since it requires correct functionality of many analog and digital circuits.

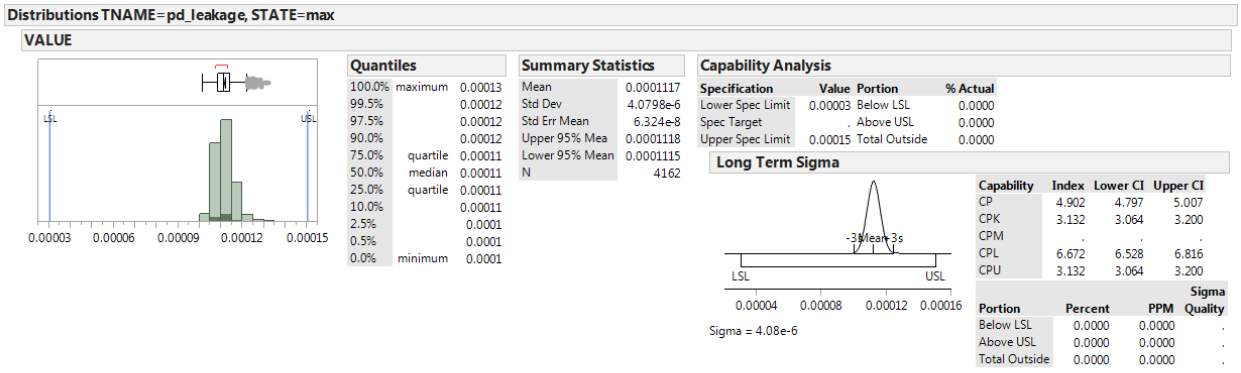
POR RESULTS					
FAB	SPLIT	TEMP	STATE	TNAME	RESULT
FUJ	FF	-40	fail_count	por_cycle_test	PASS
FUJ	FF	-40	first_fail	por_cycle_test	PASS
FUJ	FF	25	fail_count	por_cycle_test	PASS
FUJ	FF	25	first_fail	por_cycle_test	PASS
FUJ	FF	125	fail_count	por_cycle_test	PASS
FUJ	FF	125	first_fail	por_cycle_test	PASS
FUJ	FS	-40	fail_count	por_cycle_test	PASS
FUJ	FS	-40	first_fail	por_cycle_test	PASS
FUJ	FS	25	fail_count	por_cycle_test	PASS
FUJ	FS	25	first_fail	por_cycle_test	PASS
FUJ	FS	125	fail_count	por_cycle_test	PASS
FUJ	FS	125	first_fail	por_cycle_test	PASS
FUJ	SF	-40	fail_count	por_cycle_test	PASS
FUJ	SF	-40	first_fail	por_cycle_test	PASS
FUJ	SF	25	fail_count	por_cycle_test	PASS
FUJ	SF	25	first_fail	por_cycle_test	PASS
FUJ	SF	125	fail_count	por_cycle_test	PASS
FUJ	SF	125	first_fail	por_cycle_test	PASS
FUJ	SS	-40	fail_count	por_cycle_test	PASS
FUJ	SS	-40	first_fail	por_cycle_test	PASS
FUJ	SS	25	fail_count	por_cycle_test	PASS
FUJ	SS	25	first_fail	por_cycle_test	PASS
FUJ	SS	125	fail_count	por_cycle_test	PASS
FUJ	SS	125	first_fail	por_cycle_test	PASS
FUJ	TT	-40	fail_count	por_cycle_test	PASS
FUJ	TT	-40	first_fail	por_cycle_test	PASS
FUJ	TT	25	fail_count	por_cycle_test	PASS
FUJ	TT	25	first_fail	por_cycle_test	PASS
FUJ	TT	125	fail_count	por_cycle_test	PASS
FUJ	TT	125	first_fail	por_cycle_test	PASS
UMC	TT	-40	fail_count	por_cycle_test	PASS
UMC	TT	-40	first_fail	por_cycle_test	PASS
UMC	TT	25	fail_count	por_cycle_test	PASS
UMC	TT	25	first_fail	por_cycle_test	PASS
UMC	TT	100	fail_count	por_cycle_test	PASS
UMC	TT	100	first_fail	por_cycle_test	PASS

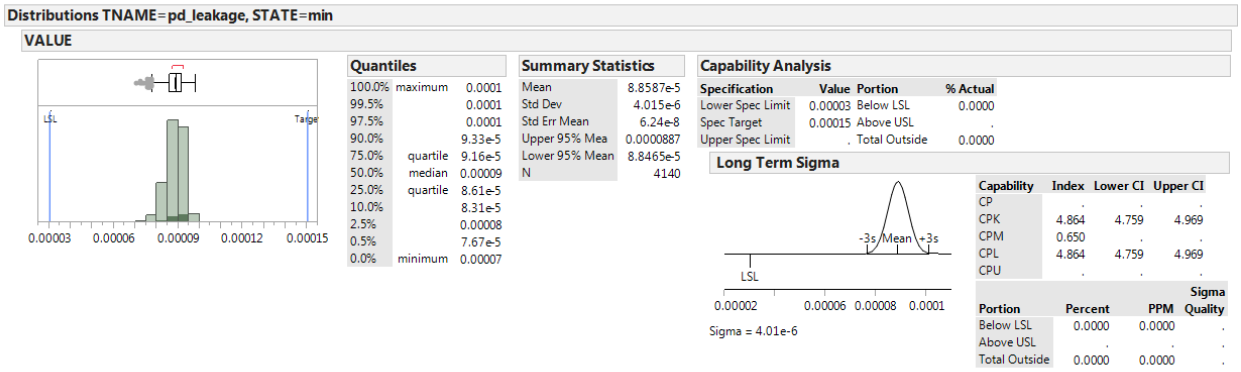
ECP5-45 POR Test Results

[por not performed for ECP5-25 or Crosslink]

IO LEAKAGE

IO leakage was measured in the pulldown, no-pull and pullup configurations (labeled pd_leakage, pin_leakage and pu_leakage on the following graphs). The spec limits are plotted as blue vertical bars for each condition. All splits are plotted together and UMC measurements illustrated by the dark color on the bar graphs. USJC IO leakage is identical with UMC performance as can be seen by the UMC mean centered in the USJC distribution.

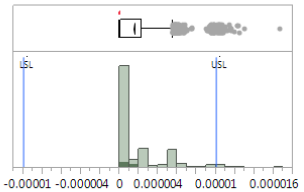




ECP5-45 Pull-down Leakage Test Results

Distributions TNAME=pin_leakage, STATE=max

VALUE



Quantiles

100.0%	maximum	1.66e-5
99.5%		0.00001
97.5%		0.00001
90.0%		5.51e-6
75.0%	quartile	2.25e-6
50.0%	median	5.44e-8
25.0%	quartile	4.56e-8
10.0%		4.37e-8
2.5%		4.25e-8
0.5%		4.13e-8
0.0%	minimum	3.94e-8

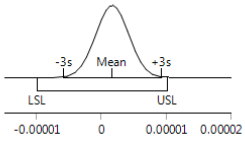
Summary Statistics

Mean	1.5363e-6
Std Dev	2.5097e-6
Std Err Mean	3.8901e-8
Upper 95% Mea	1.6125e-6
Lower 95% Mean	1.46e-6
N	4162

Capability Analysis

Specification	Value	Portion	% Actual
Lower Spec Limit	-0.00001	Below LSL	0.0000
Spec Target	.	Above USL	1.8741
Upper Spec Limit	0.00001	Total Outside	1.8741

Long Term Sigma



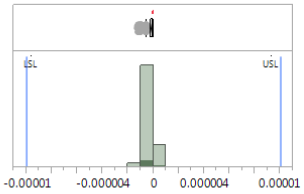
Sigma = 2.51e-6

Capability	Index	Lower CI	Upper CI
CP	1.328	1.300	1.357
CPK	1.124	1.098	1.150
CPM	.	.	.
CPL	1.532	1.498	1.567
CPU	1.124	1.098	1.150

Portion	Percent	PPM	Sigma Quality
Below LSL	0.0002	2.1456	6.097
Above USL	0.0372	372.4975	4.872
Total Outside	0.0375	374.6431	4.871

Distributions TNAME=pin_leakage, STATE=min

VALUE



Quantiles

100.0%	maximum	3.75e-9
99.5%		2.5e-9
97.5%		1.87e-9
90.0%		6.3e-10
75.0%	quartile	-1.3e-9
50.0%	median	-3.7e-9
25.0%	quartile	-2.2e-7
10.0%		-5.2e-7
2.5%		-1e-6
0.5%		-1.2e-6
0.0%	minimum	-1.3e-6

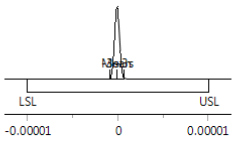
Summary Statistics

Mean	-1.583e-7
Std Dev	2.5854e-7
Std Err Mean	4.0075e-9
Upper 95% Mea	-1.504e-7
Lower 95% Mean	-1.661e-7
N	4162

Capability Analysis

Specification	Value	Portion	% Actual
Lower Spec Limit	-0.00001	Below LSL	0.0000
Spec Target	.	Above USL	0.0000
Upper Spec Limit	0.00001	Total Outside	0.0000

Long Term Sigma



Sigma = 2.59e-7

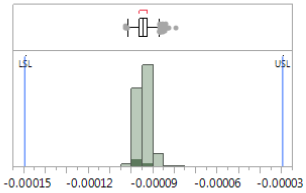
Capability	Index	Lower CI	Upper CI
CP	12.893	12.616	13.170
CPK	12.689	12.416	12.962
CPM	.	.	.
CPL	12.689	12.416	12.961
CPU	13.097	12.815	13.378

Portion	Percent	PPM	Sigma Quality
Below LSL	0.0000	0.0000	.
Above USL	0.0000	0.0000	.
Total Outside	0.0000	0.0000	.

ECP5-45 No-Pull Leakage Test Results

Distributions TNAME=pu_leakage, STATE=max

VALUE



Quantiles

100.0%	maximum	-0.0001
99.5%		-0.0001
97.5%		-0.0001
90.0%		-0.0001
75.0%	quartile	-0.0001
50.0%	median	-0.0001
25.0%	quartile	-0.0001
10.0%		-0.0001
2.5%		-0.0001
0.5%		-0.0001
0.0%	minimum	-0.0001

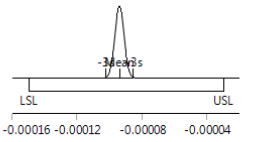
Summary Statistics

Mean	-9.431e-5
Std Dev	2.7665e-6
Std Err Mean	4.2981e-8
Upper 95% Mea	-9.423e-5
Lower 95% Mean	-9.439e-5
N	4143

Capability Analysis

Specification	Value	Portion	% Actual
Lower Spec Limit	-0.00015	Below LSL	0.0000
Spec Target	.	Above USL	0.0000
Upper Spec Limit	-0.00003	Total Outside	0.0000

Long Term Sigma



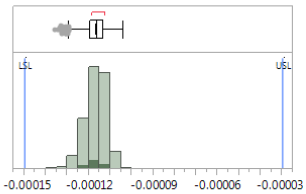
Sigma = 2.77e-6

Capability	Index	Lower CI	Upper CI
CP	7.229	7.074	7.385
CPK	6.710	6.565	6.855
CPM	.	.	.
CPL	6.710	6.565	6.855
CPU	7.749	7.581	7.915

Portion	Percent	PPM	Sigma Quality
Below LSL	0.0000	0.0000	.
Above USL	0.0000	0.0000	.
Total Outside	0.0000	0.0000	.

Distributions TNAME=pu_leakage, STATE=min

VALUE



Quantiles

100.0%	maximum	-0.0001
99.5%		-0.0001
97.5%		-0.0001
90.0%		-0.0001
75.0%	quartile	-0.0001
50.0%	median	-0.0001
25.0%	quartile	-0.0001
10.0%		-0.0001
2.5%		-0.0001
0.5%		-0.0001
0.0%	minimum	-0.0001

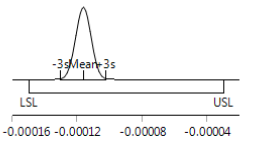
Summary Statistics

Mean	-0.000117
Std Dev	4.6384e-6
Std Err Mean	7.1898e-8
Upper 95% Mea	-0.000116
Lower 95% Mean	-0.000117
N	4162

Capability Analysis

Specification	Value	Portion	% Actual
Lower Spec Limit	-0.00015	Below LSL	0.0000
Spec Target	.	Above USL	0.0000
Upper Spec Limit	-0.00003	Total Outside	0.0000

Long Term Sigma



Sigma = 4.64e-6

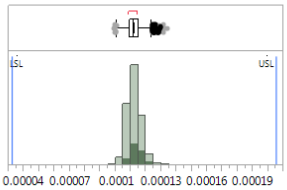
Capability	Index	Lower CI	Upper CI
CP	4.312	4.219	4.404
CPK	2.402	2.349	2.454
CPM	.	.	.
CPL	2.402	2.349	2.454
CPU	6.222	6.088	6.356

Portion	Percent	PPM	Sigma Quality
Below LSL	0.0000	0.0000	8.705
Above USL	0.0000	0.0000	.
Total Outside	0.0000	0.0000	8.705

ECP5-45 Pull-up Leakage Test Results

Distributions FLOW=SORT1, TEMP=-40

pd_leakage_max



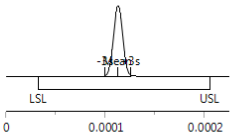
Quantiles		
100.0%	maximum	0.00013
99.5%		0.00013
97.5%		0.00012
90.0%		0.00012
75.0%	quartile	0.00012
50.0%	median	0.00011
25.0%	quartile	0.00011
10.0%		0.00011
2.5%		0.0001
0.5%		0.0001
0.0%	minimum	0.0001

Summary Statistics	
Mean	0.0001124
Std Dev	4.3542e-6
Std Err Mean	3.2148e-8
Upper 95% Mea	0.0001125
Lower 95% Mean	0.0001123
N	18345

Capability Analysis

Specification	Value	Portion	% Actual
Lower Spec Limit	0.000032	Below LSL	0.0000
Spec Target	.	Above USL	0.0000
Upper Spec Limit	0.000205	Total Outside	0.0000

Long Term Sigma



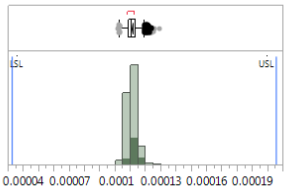
Sigma = 4.35e-6

Capability	Index	Lower CI	Upper CI
CP	6.622	6.554	6.690
CPK	6.156	6.093	6.219
CPM	.	.	.
CPL	6.156	6.092	6.219
CPU	7.088	7.016	7.161

Portion	Percent	PPM	Sigma Quality
Below LSL	0.0000	0.0000	.
Above USL	0.0000	0.0000	.
Total Outside	0.0000	0.0000	.

Distributions FLOW=SORT2, TEMP=100

pd_leakage_max



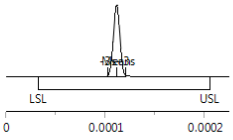
Quantiles		
100.0%	maximum	0.00013
99.5%		0.00012
97.5%		0.00012
90.0%		0.00011
75.0%	quartile	0.00011
50.0%	median	0.00011
25.0%	quartile	0.00011
10.0%		0.00011
2.5%		0.00011
0.5%		0.0001
0.0%	minimum	0.0001

Summary Statistics	
Mean	0.0001109
Std Dev	3.0808e-6
Std Err Mean	2.3808e-8
Upper 95% Mea	0.000111
Lower 95% Mean	0.0001109
N	16746

Capability Analysis

Specification	Value	Portion	% Actual
Lower Spec Limit	0.000032	Below LSL	0.0000
Spec Target	.	Above USL	0.0000
Upper Spec Limit	0.000205	Total Outside	0.0000

Long Term Sigma



Sigma = 3.08e-6

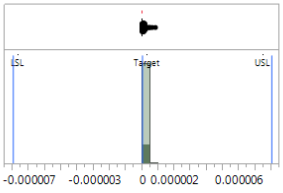
Capability	Index	Lower CI	Upper CI
CP	9.359	9.259	9.459
CPK	8.539	8.448	8.631
CPM	.	.	.
CPL	8.539	8.448	8.631
CPU	10.178	10.069	10.287

Portion	Percent	PPM	Sigma Quality
Below LSL	0.0000	0.0000	.
Above USL	0.0000	0.0000	.
Total Outside	0.0000	0.0000	.

ECP5-25 Pull-down Leakage Test Results

Distributions FLOW=SORT1, TEMP=-40

pin_leakage_max



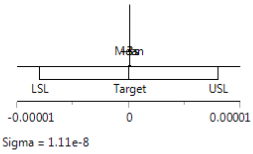
Quantiles		
100.0%	maximum	8.32e-7
99.5%		7.02e-8
97.5%		5.25e-8
90.0%		4.81e-8
75.0%	quartile	4.63e-8
50.0%	median	4.44e-8
25.0%	quartile	4.25e-8
10.0%		4.13e-8
2.5%		4e-8
0.5%		3.88e-8
0.0%	minimum	3.75e-8

Summary Statistics	
Mean	4.4991e-8
Std Dev	1.1092e-8
Std Err Mean	8.189e-11
Upper 95% Mea	4.5152e-8
Lower 95% Mean	4.4831e-8
N	18345

Capability Analysis

Specification	Value	Portion	% Actual
Lower Spec Limit	-8e-6	Below LSL	0.0000
Spec Target	0	Above USL	0.0000
Upper Spec Limit	0.000008	Total Outside	0.0000

Long Term Sigma



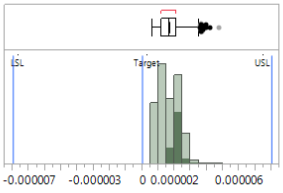
Sigma = 1.11e-8

Capability	Index	Lower CI	Upper CI
CP	240.41	237.95	242.87
CPK	239.06	236.61	241.51
CPM	57.548	57.351	57.744
CPL	241.76	239.29	244.24
CPU	239.06	236.61	241.50

Portion	Percent	PPM	Sigma Quality
Below LSL	0.0000	0.0000	.
Above USL	0.0000	0.0000	.
Total Outside	0.0000	0.0000	.

Distributions FLOW=SORT2, TEMP=100

pin_leakage_max



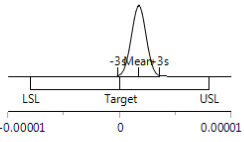
Quantiles		
100.0%	maximum	4.76e-6
99.5%		3.13e-6
97.5%		2.82e-6
90.0%		2.49e-6
75.0%	quartile	2.13e-6
50.0%	median	1.69e-6
25.0%	quartile	1.19e-6
10.0%		7.73e-7
2.5%		6.99e-7
0.5%		6.64e-7
0.0%	minimum	6.16e-7

Summary Statistics	
Mean	1.661e-6
Std Dev	6.2572e-7
Std Err Mean	4.8353e-9
Upper 95% Mea	1.6705e-6
Lower 95% Mean	1.6516e-6
N	16746

Capability Analysis

Specification	Value	Portion	% Actual
Lower Spec Limit	-8e-6	Below LSL	0.0000
Spec Target	0	Above USL	0.0000
Upper Spec Limit	0.000008	Total Outside	0.0000

Long Term Sigma



Sigma = 6.26e-7

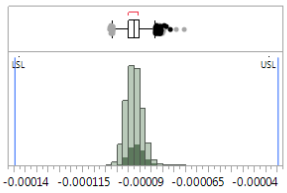
Capability	Index	Lower CI	Upper CI
CP	4.262	4.216	4.307
CPK	3.377	3.340	3.413
CPM	1.502	1.495	1.510
CPL	5.147	5.091	5.202
CPU	3.377	3.340	3.413

Portion	Percent	PPM	Sigma Quality
Below LSL	0.0000	0.0000	.
Above USL	0.0000	0.0000	.
Total Outside	0.0000	0.0000	.

ECP5-25 No-Pull Leakage Test Results

Distributions FLOW=SORT1, TEMP=-40

pu_leakage_max



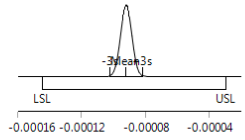
Quantiles		
100.0%	maximum	-0.0001
99.5%		-0.0001
97.5%		-0.0001
90.0%		-0.0001
75.0%	quartile	-0.0001
50.0%	median	-0.0001
25.0%	quartile	-0.0001
10.0%		-0.0001
2.5%		-0.0001
0.5%		-0.0001
0.0%	minimum	-0.0001

Summary Statistics	
Mean	-9.254e-5
Std Dev	3.4162e-6
Std Err Mean	2.5223e-8
Upper 95% Mea	-9.249e-5
Lower 95% Mean	-9.259e-5
N	18345

Capability Analysis

Specification	Value	Portion	% Actual
Lower Spec Limit	-0.00015	Below LSL	0.0000
Spec Target	.	Above USL	0.0000
Upper Spec Limit	-0.00003	Total Outside	0.0000

Long Term Sigma



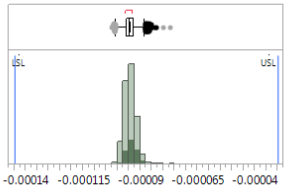
Sigma = 3.42e-6

Capability	Index	Lower CI	Upper CI
CP	5.610	5.553	5.668
CPK	5.119	5.066	5.171
CPM	.	.	.
CPL	5.119	5.066	5.171
CPU	6.102	6.040	6.165

Portion	Percent	PPM	Sigma Quality
Below LSL	0.0000	0.0000	.
Above USL	0.0000	0.0000	.
Total Outside	0.0000	0.0000	.

Distributions FLOW=SORT2, TEMP=100

pu_leakage_max



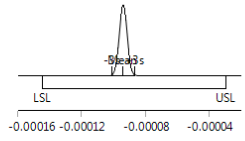
Quantiles		
100.0%	maximum	-0.0001
99.5%		-0.0001
97.5%		-0.0001
90.0%		-0.0001
75.0%	quartile	-0.0001
50.0%	median	-0.0001
25.0%	quartile	-0.0001
10.0%		-0.0001
2.5%		-0.0001
0.5%		-0.0001
0.0%	minimum	-0.0001

Summary Statistics	
Mean	-9.439e-5
Std Dev	2.3829e-6
Std Err Mean	1.8414e-8
Upper 95% Mea	-9.436e-5
Lower 95% Mean	-9.443e-5
N	16746

Capability Analysis

Specification	Value	Portion	% Actual
Lower Spec Limit	-0.00015	Below LSL	0.0000
Spec Target	.	Above USL	0.0000
Upper Spec Limit	-0.00003	Total Outside	0.0000

Long Term Sigma



Sigma = 2.38e-6

Capability	Index	Lower CI	Upper CI
CP	8.043	7.957	8.130
CPK	7.079	7.003	7.155
CPM	.	.	.
CPL	7.079	7.003	7.155
CPU	9.008	8.911	9.104

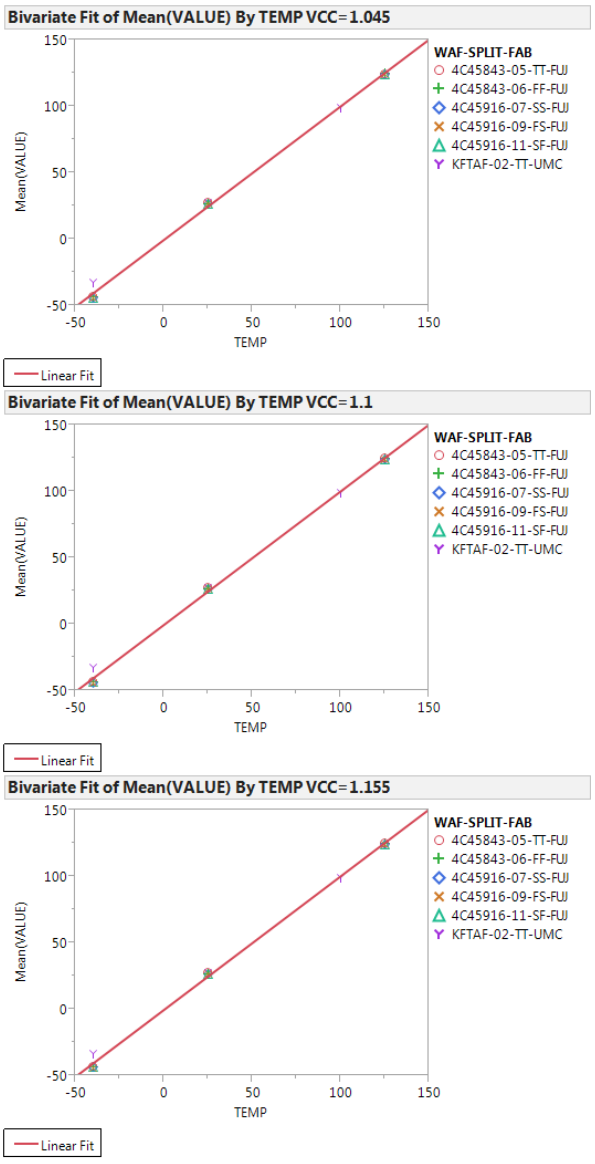
Portion	Percent	PPM	Sigma Quality
Below LSL	0.0000	0.0000	.
Above USL	0.0000	0.0000	.
Total Outside	0.0000	0.0000	.

ECP5-25 Pull-down Leakage Test Results

DTR

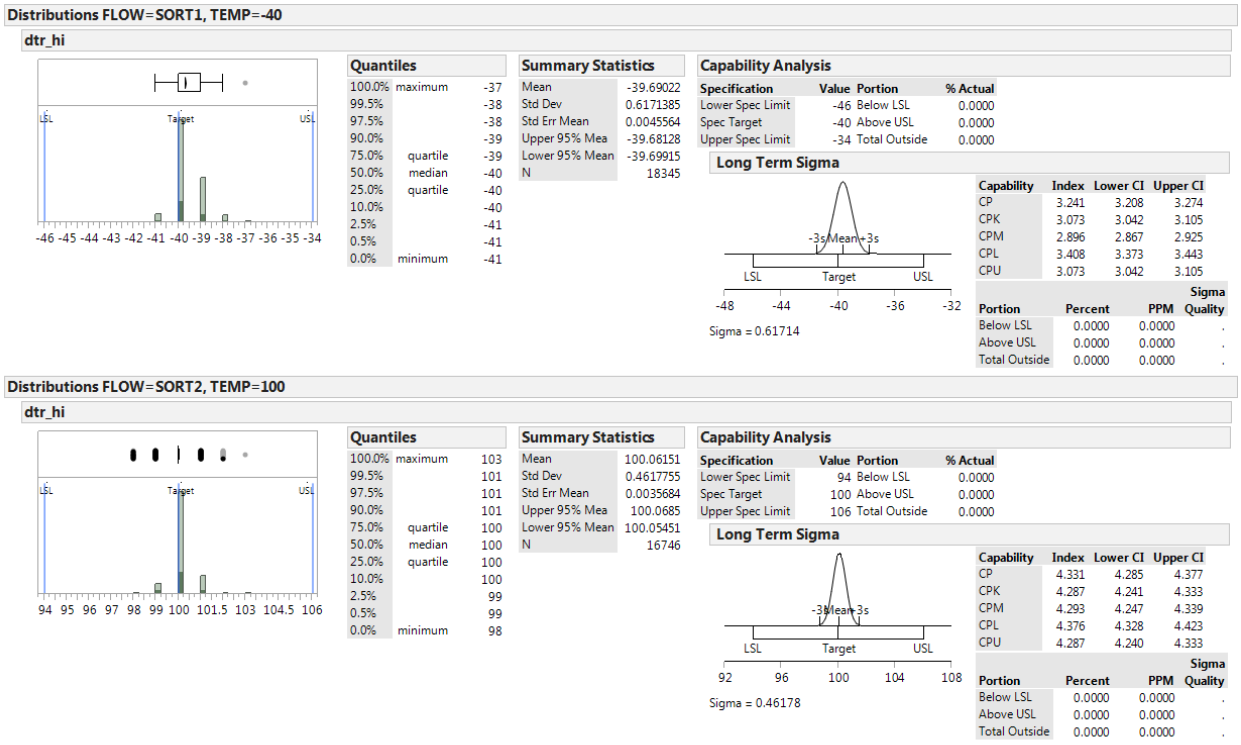
DTR stands for Digital Temperature Readout. While this is not a user accessible function, it does use a variety of circuits that are both analog (bandgap) and digital in nature which makes it a good parameter to measure relative performance.

The DTR readout is consistent across PVT and matches the UMC fabricated material.



ECP5-45 DTR Correlation Across Voltage & Process

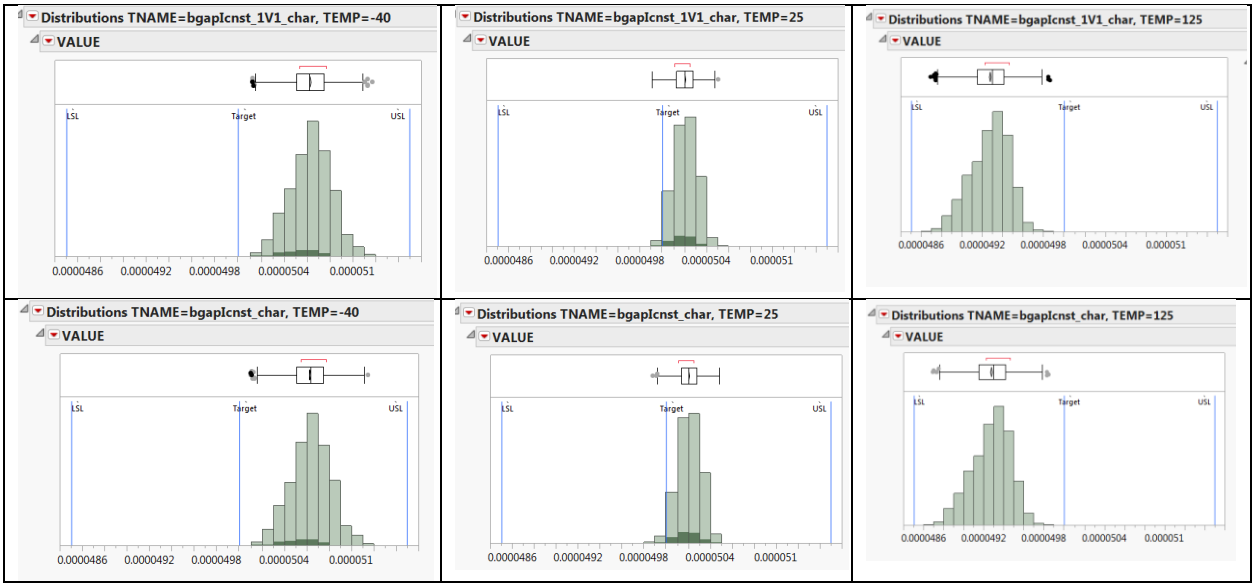
The DTR of the ECP5-45 is also tightly correlated between UMC (dark shaded) and USJC fabs.



ECP5-45 DTR Correlation at Process at -40C and 100C

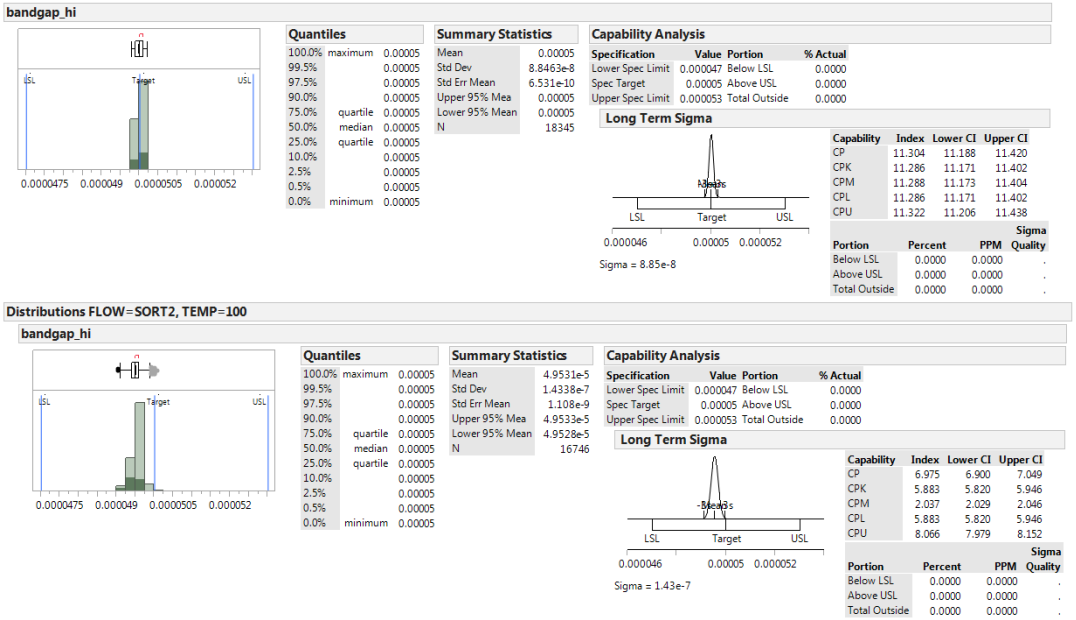
BANDGAP

The Bandgap voltage is not a directly measureable customer feature but is integral to the operation of the ECP5. USJC bandgap measurements are all well within specs and straddle the nominal UMC distributions. Operation is very closely correlated between the two foundries. Below are the bandgap measurements for all ECP5-45 samples across temperature.



ECP5-45 Bandgap Measurements

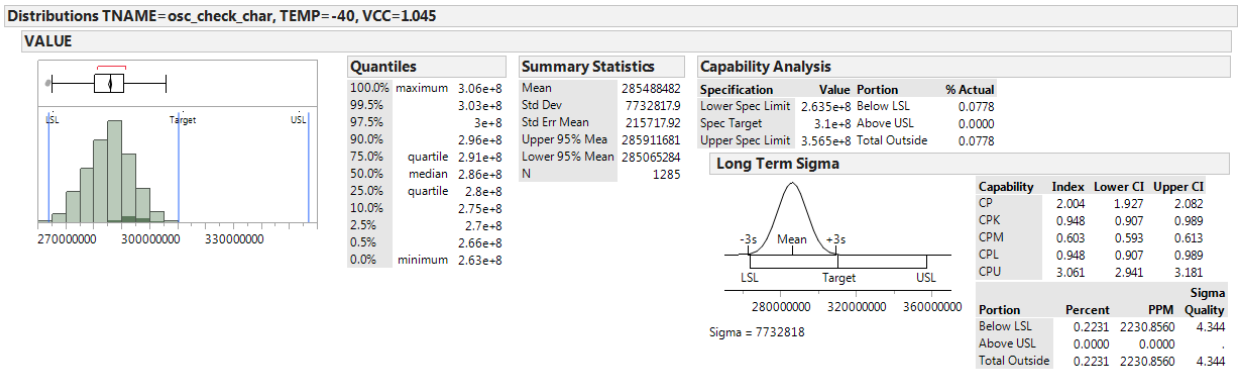
The same bandgap data for the ECP5-25 shows similar performance very little differences between fabs. This is the 100C data with UMC measurements are the darker shaded distribution.

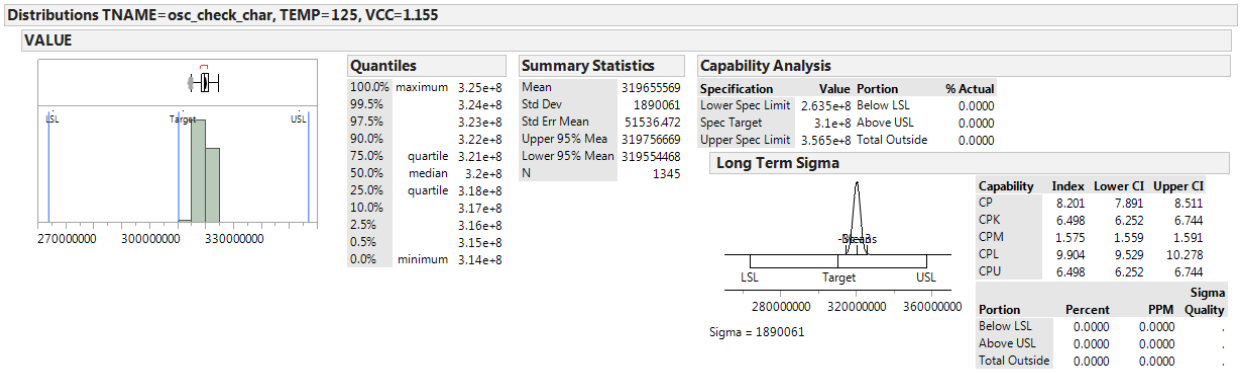


ECP5-25 Bandgap Measurements

USER OSCILLATOR

The user oscillator was measured across PVT with the most extreme conditions (low temp/low Vcc and high temp/high Vcc) plotted below. UMC performance is again shown as the darker bands in the bar graphs. UMC oscillator speed is a bit higher than USJC material but this is because of the slightly higher IONN values for UMC at a given transistor Vt. USJC material has good margin to spec – there was a single failure at the SS process corner at -40C. As noted in the name, this oscillator is a user function and fully tested for in production.



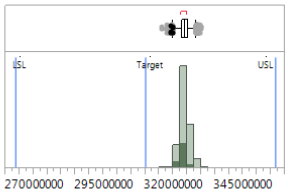


ECP5-45 User Oscillator

The ECP5-25 user oscillator correlation between fabs is excellent.

Distributions FLOW=SORT1, TEMP=-40

osc_hi



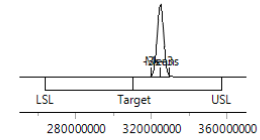
Quantiles		
100.0%	maximum	3.3e+8
99.5%		3.29e+8
97.5%		3.28e+8
90.0%		3.27e+8
75.0%	quartile	3.25e+8
50.0%	median	3.24e+8
25.0%	quartile	3.23e+8
10.0%		3.22e+8
2.5%		3.21e+8
0.5%		3.2e+8
0.0%	minimum	3.16e+8

Summary Statistics	
Mean	324240220
Std Dev	1637526.8
Std Err Mean	12090.091
Upper 95% Mea	324263917
Lower 95% Mean	324216522
N	18345

Capability Analysis

Specification	Value	Portion	% Actual
Lower Spec Limit	2.635e+8	Below LSL	0.0000
Spec Target	3.1e+8	Above USL	0.0000
Upper Spec Limit	3.565e+8	Total Outside	0.0000

Long Term Sigma



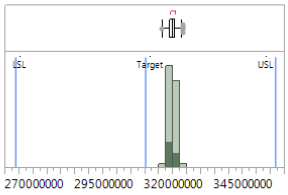
Sigma = 1637527

Capability	Index	Lower CI	Upper CI
CP	9.465	9.369	9.562
CPK	6.567	6.499	6.634
CPM	1.081	.	1.083
CPL	12.364	12.237	12.491
CPU	6.567	6.499	6.634

Portion	Percent	PPM	Sigma Quality
Below LSL	0.0000	0.0000	.
Above USL	0.0000	0.0000	.
Total Outside	0.0000	0.0000	.

Distributions FLOW=SORT2, TEMP=100

osc_hi



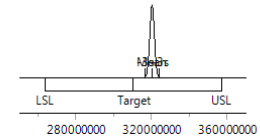
Quantiles		
100.0%	maximum	3.24e+8
99.5%		3.23e+8
97.5%		3.22e+8
90.0%		3.21e+8
75.0%	quartile	3.21e+8
50.0%	median	3.2e+8
25.0%	quartile	3.19e+8
10.0%		3.18e+8
2.5%		3.18e+8
0.5%		3.17e+8
0.0%	minimum	3.16e+8

Summary Statistics	
Mean	319855588
Std Dev	1190334.5
Std Err Mean	9198.425
Upper 95% Mea	319873617
Lower 95% Mean	319837558
N	16746

Capability Analysis

Specification	Value	Portion	% Actual
Lower Spec Limit	2.635e+8	Below LSL	0.0000
Spec Target	3.1e+8	Above USL	0.0000
Upper Spec Limit	3.565e+8	Total Outside	0.0000

Long Term Sigma



Sigma = 1190334

Capability	Index	Lower CI	Upper CI
CP	13.022	12.882	13.161
CPK	10.262	10.152	10.372
CPM	1.561	.	1.564
CPL	15.781	15.612	15.950
CPU	10.262	10.152	10.372

Portion	Percent	PPM	Sigma Quality
Below LSL	0.0000	0.0000	.
Above USL	0.0000	0.0000	.
Total Outside	0.0000	0.0000	.

ECP5-25 User Oscillator

NVCM Characterization (Crosslink)

The Non-Volatile Configuration Memory (NVCM) is another key block in the Crosslink product. NVCM was characterized over PVT to the schedule shown below. The programming times were comparable between the two fabs. Blank and programmed cell read margin was identical across datasheet conditions. No differences over data sheet conditions were observed.

	UMC	USJC
Wafer / Sample Size	**KRAPJ-01-TT (51u)** **KRAPJ-03-FF (58u)** **KRAPJ-05-SS (48u)**	**4C54297-13-TT (126u)** **4C54297-22-FF (137u)** **4C54297-14-SS (139u)** **4C54297-15-FS (140u)** **4C54297-23-SF (122u)**
Temp (°C)	**Program: 0 & 40** **Read: -40, 25, 100, 125**	
Voltages (V)	**Vcc: 1.14, 1.20, 1.26** **VccAux: 2.375, 2.500, 2.625**	

Crosslink NVCM Characterization Sample/Conditions

	UMC		FUJITSU	
0C	**Ave. Programming Time (ms)**	**# of Pulses**	**Ave. Programming Time (ms)**	**# of Pulses**
	133.46	1	130.938	1
	1968.53	15	1929.697	15
40C	131.28	1	132.728	1
	1940	15	1918.717	15

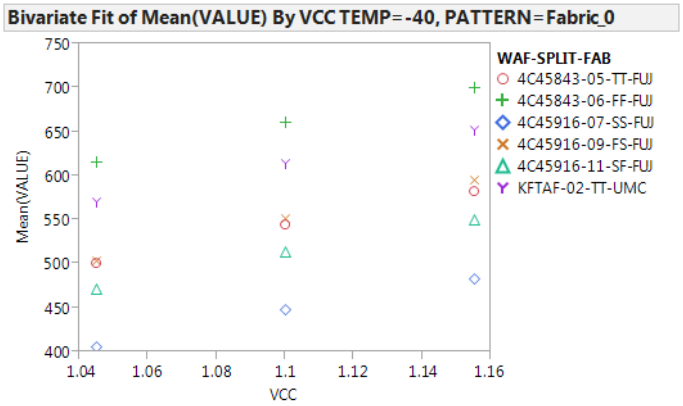
Crosslink NVCM Pulse Width Timing

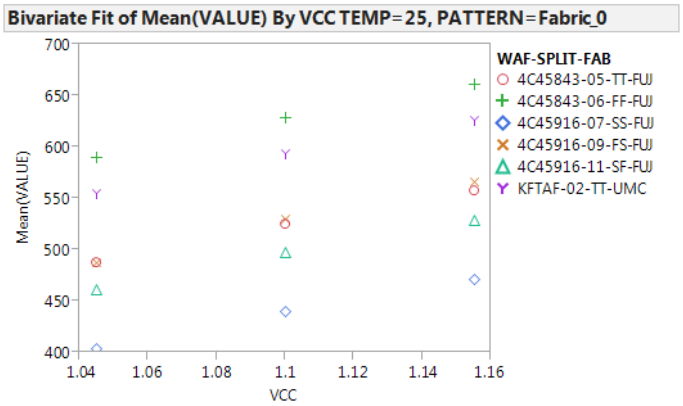
AC PERFORMANCE

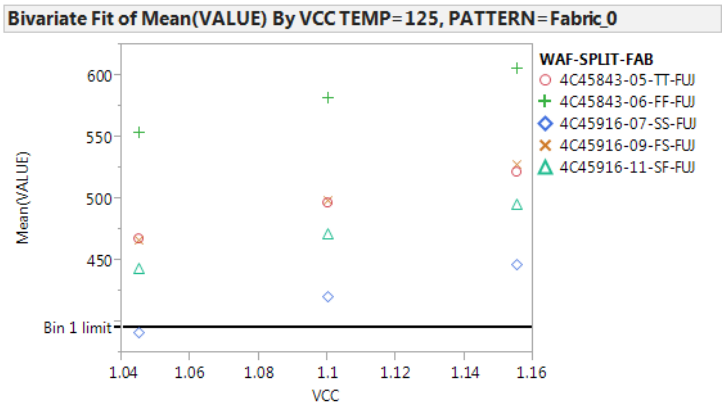
Manufacturing speed testing is done using BIST approach called a Tpdcounter. The idea is to create a ring oscillator that goes through as much of the FPGA fabric as possible and then feed the result of that oscillator into a counter. The count after a specified period of time (microseconds) is known as the Tpdcount. There are several advantages to this methodology:

1. Since the measurement is made over microseconds instead of making individual nanosecond propagation time measurements, tester accuracy and repeatability go up by the same factors.
2. A properly designed Tpdcount pattern can be correlated to almost any datasheet timing parameter.

The Tpdcount values of USJC material follow the same trend and slope with respect to Vcc and temperature as shown by the graphs below.



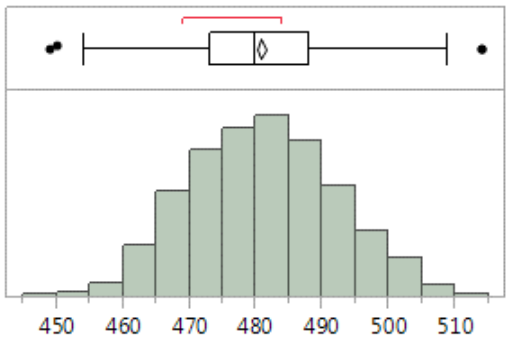




Like the internal oscillator, USJC Tpdcounts are about 6% slower than UMC when comparing nominal processed wafers. This is again attributed to the slightly higher IONN. The graphs below compare nominal UMC to USJC material at 100C/1.045V.

Distributions TEMP=100, WAF-SPLIT-FAB=4C45843-05-TT-FUJ, VCC=1.045, PATTERN=Fabric_0

VALUE

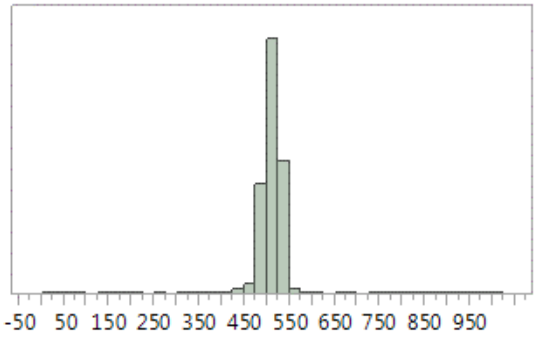


Quantiles		
100.0%	maximum	514
99.5%		509
97.5%		502
90.0%		495
75.0%	quartile	488
50.0%	median	480
25.0%	quartile	473
10.0%		467
2.5%		461
0.5%		454
0.0%	minimum	449

Summary Statistics	
Mean	480.76688
Std Dev	10.911538
Std Err Mean	0.3894495
Upper 95% Mea	481.53137
Lower 95% Mean	480.00239
N	785

Distributions TEMP=100, UMC Production, VCC=1.045

Tpd_Fabric_0_Lo

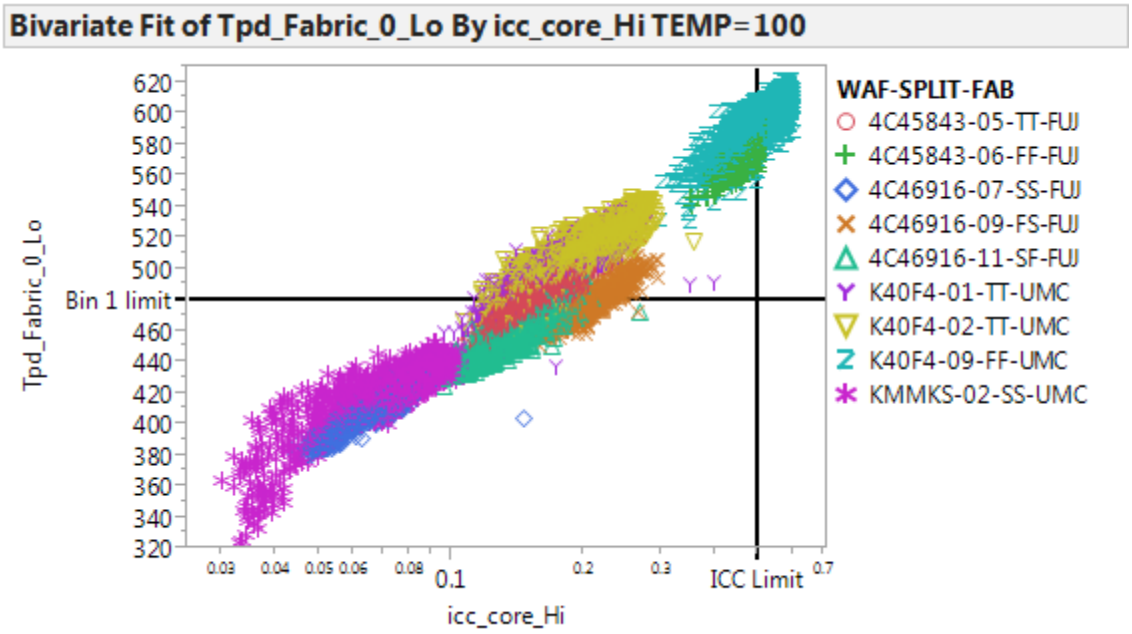


Quantiles		
100.0%	maximum	1023
99.5%		552
97.5%		544
90.0%		535
75.0%	quartile	525
50.0%	median	512
25.0%	quartile	500
10.0%		490
2.5%		474
0.5%		445
0.0%	minimum	0

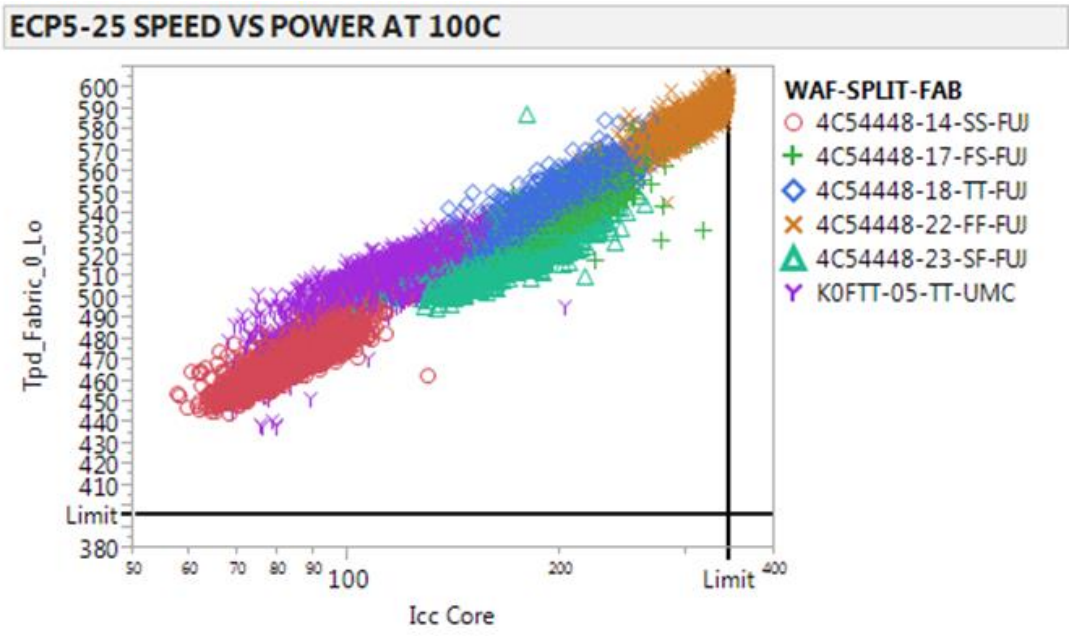
Summary Statistics	
Mean	511.85477
Std Dev	21.961815
Std Err Mean	0.033221
Upper 95% Mea	511.91988
Lower 95% Mean	511.78966
N	437031

Power

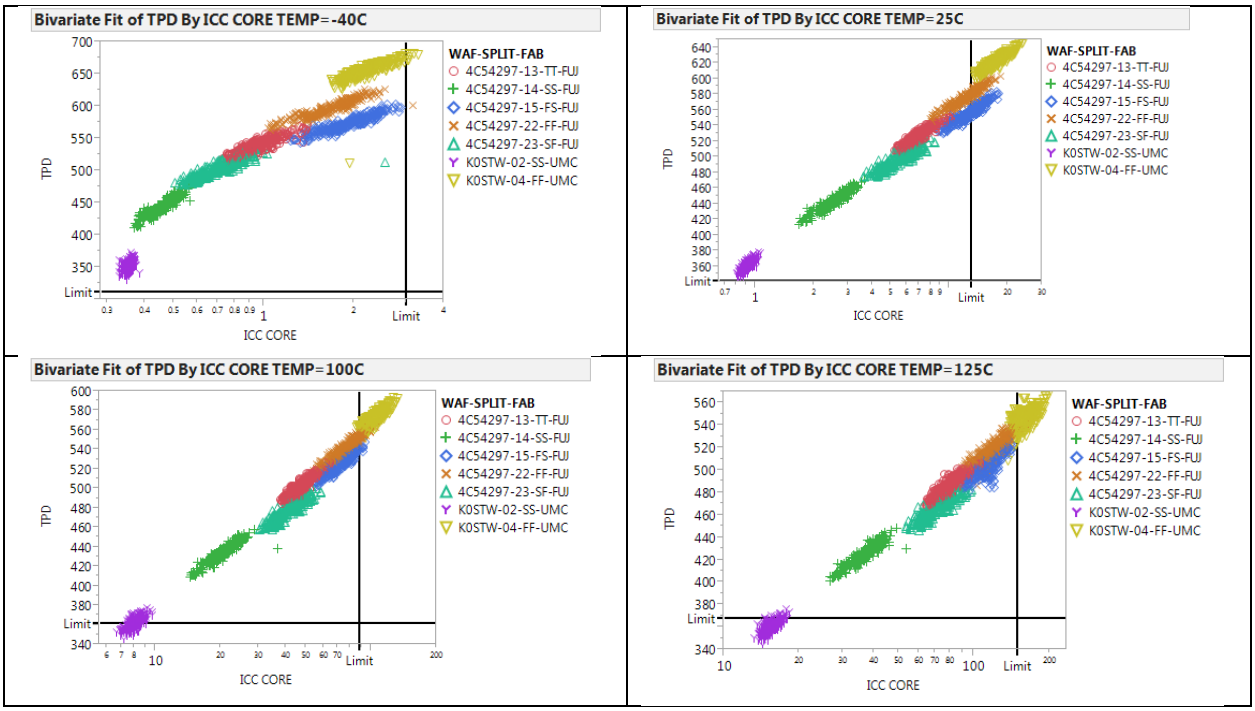
Speed vs power curves are plotted below for all three products. They all generate speed/power curves that follow the same trend across the two foundries.



ECP5-45 Speed vs Power (UMC and USJC)



ECP5-25 Speed vs Power (UMC and USJC)



LIF-MD6000 Speed vs Power (UMC and USJC)

PACKAGE CHAR DATA

As previously mentioned, a separate characterization effort was performed on the ECP5-45 at the package level (in 381caBGA package). This characterization also covered the temperature range from -40C to 125C and also used the same USJC process splits.

The sample size for this characterization was 30 units per process split which is sufficient to calculate Cpk and Design Index (DI) statistics. The Cpk target is 1.5 which translates to a PPM of 7. The Cpk statistic weighs all splits equally but that isn't reality. If the Cpk is less than 1.5, then the DI statistic which weighs the probability of the various splits is used with a goal of being greater than 1.0. Note that in the cases where **all** values pass the datasheet parameter, the Cpk and DI is listed as "N/A".

POR

POR data in the package characterization performs a complementary function in that POR was measured for all the supply voltages except Vcc (which was previously tested in the wafer char as mentioned above). All DI values are greater than 1.0

Power-On-Reset Voltage Levels					Spec			Silicon Data - UMC					Silicon Data - Fujitsu				
Symbol	Parameter			Unit	Min	Typ	Max	Min	Typ	Max	Cpk	DI	Min	Typ	Max	Cpk	DI
V_{PORUP}	All Devices	Power-On-Reset ramp-up trip point (Monitoring VCC, VCCAUX, and VCCIO8)	V_{CC}	V	0.90	—	1.02	Tested					Tested				
			V_{CCAUX}	V	2.00	—	2.20	2.08	2.11	2.15	1.82	1.12	2.07	2.11	2.18	1.15	1.06
			V_{CCIO8}	V	0.95	—	1.05	0.99	1.00	1.02	2.49	1.50	0.98	1.01	1.04	1.43	1.52
V_{PORDN}	All Devices	Power-On-Reset ramp-down trip point (Monitoring VCC, and VCCAUX)	V_{CC}	V	0.77	—	0.87	0.81	0.83	0.86	1.45	1.19	0.81	0.84	0.86	1.03	1.13
			V_{CCAUX}	V	1.80	—	2.00	1.85	1.90	1.94	2.14	1.09	1.87	1.91	1.96	1.38	1.05

MIPI

Two key IP blocks on the LIF-MD6000 are the hard and soft MIPI. A detailed characterization was performed on packaged units on the bench across Vcc (min, nom and max spec), Temp (-40, 25 and 100C) and Process (SS, TT, FF splits). Sample size was 6 units per split for USJC and 30 units per split for UMC. The data below is an abbreviated summary.

While the USJC material had better performance on several parameters, there were enough differences to warrant datasheet changes. (Note that MIPI performance is the only area between all three affected devices where a significant performance difference was noted). Please see PCN 10A-19 for more details. Both UMC and USJC devices are guaranteed to meet the new datasheet specification.

Hard D-PHY

Parameter	Spec	Min	Avg	Max	Sigma	CPK
RX Parameters						
USJC Setup Time	133.3 ps	-6 ps	22.9 ps	56.4 ps	10.9 ps	3.36
UMC Setup Time	133.3 ps	-12 ps	19.5 ps	222 ps	27.7 ps	1.37
USJC Hold Time	133.3 ps	38.1 ps	59.0 ps	93.3 ps	9.9 ps	2.49
UMC Hold Time	133.3 ps	47.6 ps	93.9 ps	256.6 ps	27.4 ps	0.48
TX Parameters						
USJC tDVB Tx	0.2 UI	-0.06 UI	0.01 UI	0.09 UI	0.03 UI	2.13
UMC tDVB Tx	0.2 UI	-0.06 UI	-0.02 UI	0.03 UI	0.03 UI	2.32
USJC tDVA	0.2 UI	-0.11 UI	-0.04 UI	0.02 UI	0.03 UI	1.73
UMC tDVA	0.2 UI	-0.02 UI	0.04 UI	0.07 UI	0.03 UI	2.16

Soft D-PHY

Parameter	Spec	Min	Avg	Max	Sigma	CPK
RX Vid=70mV						
Fujitsu Setup Time	333.3 ps	-23 ps	54 ps	151 ps	40 ps	2.30
UMC Setup Time	333.3 ps	-127 ps	50 ps	198 ps	52 ps	1.82
Fujitsu Hold Time	333.3 ps	94 ps	146 ps	267 ps	36 ps	1.74
UMC Hold Time	333.3 ps	-38 ps	106 ps	244 ps	44 ps	1.71
RX Vid=140mV, .15UI						
Fujitsu Setup Time	172.4 ps	-3 ps	46 ps	100 ps	25 ps	1.70
UMC Setup Time	172.4 ps	-28 ps	50 ps	119 ps	26 ps	1.56

Fujitsu Hold Time	172.4 ps	54 ps	82 ps	135 ps	17 ps	1.76
UMC Hold Time	172.4 ps	-20 ps	54 ps	120 ps	25 ps	1.60
RX Vid=140mV, 0.2UI						
Fujitsu Setup Time	186.9 ps	-17 ps	36 ps	87 ps	24 ps	2.14
UMC Setup Time	186.9 ps	-87 ps	38 ps	98 ps	28 ps	1.78
Fujitsu Hold Time	186.9 ps	50 ps	78 ps	112 ps	14 ps	2.63
UMC Hold Time	186.9 ps	-22 ps	54 ps	120 ps	25 ps	1.78

IO DC Characteristics

ECP5-45 IO DC characteristics have very large Cpk values indicating plenty of margin to datasheet specifications for both UMC and USJC material.

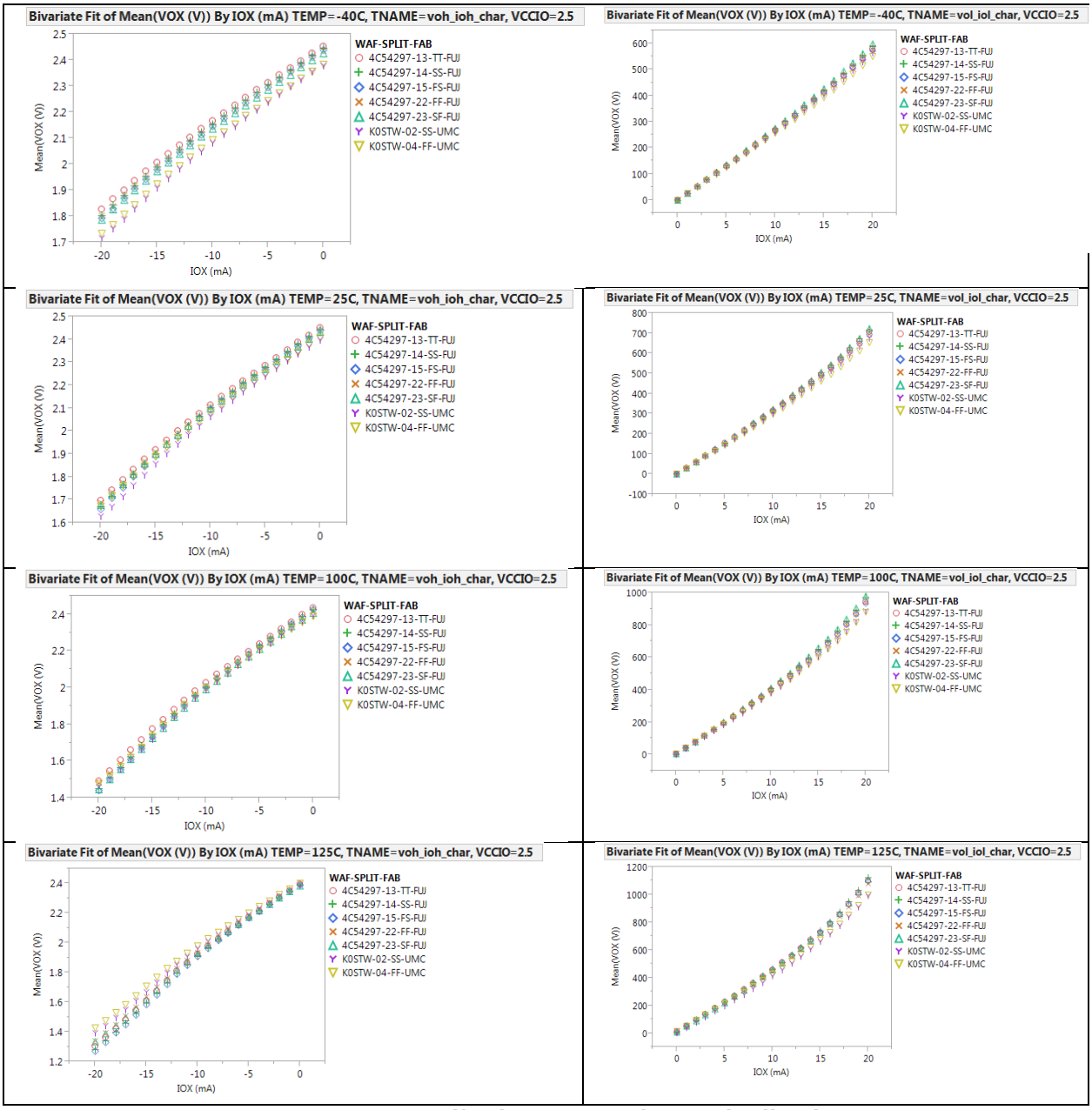
Vil/Vih Specifcations			Spec			Silicon Data - UMC					Silicon Data - Fujitsu				
Parameter	Input/Output Standard	Unit	Min	Typ	Max	Min	Typ	Max	Cpk	DI	Min	Typ	Max	Cpk	DI
vil_{LVC33}	LVCMOS33	V	-0.3	—	0.8	1.23	1.24	1.25	27.49	24.11	1.23	1.24	1.25	27.49	24.11
vil_{LVC15}	LVCMOS15	V	-0.3	—	$0.35*V_{CCIO}$	0.77	0.78	0.79	7.63	6.85	0.77	0.78	0.79	7.63	6.85
vil_{LVC12}	LVCMOS12	V	-0.3	—	$0.35*V_{CCIO}$	0.63	0.66	0.66	10.84	10.00	0.63	0.66	0.66	10.84	10.00
vih_{LVC33}	LVCMOS33	V	2.0	—	3.465	1.60	1.61	1.62	29.43	16.70	1.60	1.61	1.62	29.43	16.70
vih_{LVC15}	LVCMOS15	V	$0.65*V_{CCIO}$	—	3.465	0.80	0.81	0.82	12.61	10.49	0.80	0.81	0.82	12.61	10.49
vih_{LVC12}	LVCMOS12	V	$0.65*V_{CCIO}$	—	3.465	0.61	0.62	0.62	4.67	3.23	0.61	0.62	0.62	4.67	3.23
vih_{SSTI5_I}	SSTL15 _I (DDR3 Memory)	V	$V_{REF}+0.1$	—	3.465	0.80	0.81	0.82	4.86	4.01	0.80	0.81	0.82	4.86	4.01

ECP5-45 VIl/VIH - UMC and USJC(Fujitsu)

Vol/Voh Specifications				Spec			Silicon Data - UMC					Silicon Data - Fujitsu				
Parameter	Input/Output Standard	I_{OL} (mA)	Unit	Min	Typ	Max	Min	Typ	Max	Cpk	DI	Min	Typ	Max	Cpk	DI
vol_{LVC33_16ma}	LVCMOS33	16	V	—	—	0.4	0.30	0.32	0.35	2.11	1.79	0.27	0.31	0.34	2.54	2.24
vol_{LVC33_12ma}	LVCMOS33	12	V	—	—	0.4	0.27	0.30	0.33	2.88	2.45	0.25	0.28	0.31	3.09	2.55
vol_{LVC33_8ma}	LVCMOS33	8	V	—	—	0.4	0.13	0.17	0.20	3.08	2.89	0.17	0.19	0.21	8.88	7.44
vol_{LVC33_4ma}	LVCMOS33	4	V	—	—	0.4	0.18	0.20	0.21	10.18	7.67	0.15	0.17	0.19	10.20	8.69
voh_{LVC33_16ma}	LVCMOS33	-16	V	$V_{CCIO}-0.4$	—	—	3.16	3.18	3.20	3.21	2.63	3.00	3.02	3.03	3.05	2.39
voh_{LVC33_12ma}	LVCMOS33	-12	V	$V_{CCIO}-0.4$	—	—	3.15	3.17	3.20	2.65	2.25	3.16	3.19	3.22	2.65	2.41
voh_{LVC33_8ma}	LVCMOS33	-8	V	$V_{CCIO}-0.4$	—	—	3.18	3.19	3.21	2.64	2.18	3.18	3.20	3.24	3.05	2.75
voh_{LVC33_4ma}	LVCMOS33	-4	V	$V_{CCIO}-0.4$	—	—	3.13	3.18	3.20	1.20	1.08	3.13	3.19	3.21	1.60	1.44
voh_{LVC12_8ma}	LVCMOS12	-8	V	$V_{CCIO}-0.4$	—	—	1.02	1.05	1.06	7.80	4.96	0.84	0.85	0.86	9.90	2.29
voh_{LVC12_4ma}	LVCMOS12	-4	V	$V_{CCIO}-0.4$	—	—	1.04	1.05	1.07	5.12	3.86	1.05	1.07	1.08	7.49	4.47

ECP5-45 Vol/Voh - UMC and USJC(Fujitsu)

LIF-MD6000 IO characteristics are also very well matched between UMC and USJC product across PVT.



LIF-MD6000 Vol/Voh - UMC and USJC(Fujitsu)

IO Fmax

Cpk values for IO Fmax characteristics are also very large, indicating plenty of margin to datasheet specifications for both UMC and USJC material. Note that the Output frequency parameters passed datasheet limits for all devices, which is indicated by the “N/A”.

Serial Output Timing and Levels			Spec	Silicon Data - UMC					Silicon Data - Fujitsu				
Buffer	Description	Unit	Max	Min	Typ	Max	Cpk	DI	Min	Typ	Max	Cpk	DI
Maximum Input Frequency[1]													
LVDS25	LVDS, VCCIO = 2.5V	MHz	400.0	478	480	481	60.32	54.20	479	480	481	53.74	48.40
MLVDS25	MLDS, Emulated, VCCIO = 2.5V	MHz	400.0	239.5	240.0	240.5	86.38	77.83	239.5	240.0	240.4	84.34	77.83
BLVDS25	BLVDS, Emulated, VCCIO = 2.5V	MHz	400.0	239.5	240.0	240.5	86.38	77.83	239.5	240.0	240.4	84.34	77.83
MIPID-PHY (HS MODE)	MIPI Video	MHz	400.0	478.4	479.9	481.1	60.32	54.20	478.5	479.9	481.3	53.74	48.40
MIPID-PHY (LP MODE)	MIPI Video	MHz	400.0	478.2	479.9	481.3	3.96	3.03	478.5	479.9	481.6	55.01	49.64
SLVS	Mini LVDS	MHz	400.0	478.4	479.9	481.1	60.32	54.20	478.5	479.9	481.3	53.74	48.40
Mini LVDS	Mini LVDS	MHz	400.0	478.4	479.9	481.1	60.32	54.20	478.5	479.9	481.3	53.74	48.40
LVPECL33	LVPECL, Emulated, Vccio = 3.3V	MHz	400.0	239.5	240.0	240.5	85.75	77.24	239.6	240.0	240.5	87.24	77.24
SSTL18 (all supported classes)	SSTL_18 class I, II, Vccio = 1.8V	MHz	400.0	478.3	479.9	481.4	57.02	51.33	478.5	479.9	481.4	53.79	53.79
SSTL15 (all supported classes)	SSTL_15 class I, II, Vccio = 1.5V	MHz	400.0	478.3	479.9	481.4	55.35	49.78	478.5	479.9	481.2	52.36	52.36
SSTL135 (all supported classes)	SSTL_135 class I, II, Vccio = 1.35V	MHz	400.0	460.3	479.9	501.9	15.86	14.50	477.7	479.9	481.7	51.88	51.88
HSUL12 (all supported classes)	HSUL_12 class I, II, Vccio = 1.2V	MHz	400.0	470.0	479.9	502.9	37.00	19.93	478.4	479.9	481.4	53.32	53.32
LVTTL33	LVTTL, Vccio = 3.3V	MHz	200.0	239.5	240.0	240.5	85.75	77.24	239.6	240.0	240.5	87.24	77.24
LVCMOS33	LVCMOS, Vccio = 3.3V	MHz	200.0	239.5	240.0	240.5	85.75	77.24	239.6	240.0	240.5	87.24	77.24
LVCMOS25	LVCMOS, Vccio = 2.5V	MHz	200.0	239.5	240.0	240.5	86.38	77.83	239.5	240.0	240.4	84.34	77.83
LVCMOS18	LVCMOS, Vccio = 1.8V	MHz	200.0	239.5	240.0	240.4	93.64	84.25	239.5	240.0	240.5	85.14	84.25
LVCMOS15	LVCMOS, Vccio = 1.5V	MHz	200.0	239.5	240.0	240.4	87.03	78.36	239.5	240.0	240.4	88.79	78.36
LVCMOS12	LVCMOS, Vccio = 1.2V	MHz	200.0	239.6	240.0	240.5	87.67	79.02	239.5	240.0	240.4	84.25	79.02
Maximum Outpu Frequency[2]													
LVDS25E	LVDS, Emulated, Vccio = 2.5V	MHz	300.0	—	—	360.0	N/A	N/A	—	—	360.0	N/A	N/A
MLVDS25	MLVDS, Emulated, Vccio = 2.5V	MHz	300.0	—	—	360.0	N/A	N/A	—	—	360.0	N/A	N/A
BLVDS25	BLVDS, Emulated, VCCIO = 2.5V	MHz	300.0	—	—	360.0	N/A	N/A	—	—	360.0	N/A	N/A
LVPECL33	LVPECL, Emulated, Vccio = 3.3V	MHz	300.0	—	—	360.0	N/A	N/A	—	—	360.0	N/A	N/A
LVDS25	LVDS, Vccio = 2.5V	MHz	400.0	—	—	480.0	N/A	N/A	—	—	480.0	N/A	N/A
SSTL18 (all supported classes)	SSTL_18 class I, II, Vccio = 1.8V	MHz	400.0	—	—	480.0	N/A	N/A	—	—	480.0	N/A	N/A
SSTL15 (all supported classes)	SSTL_15 class I, II, Vccio = 1.5V	MHz	400.0	—	—	480.0	N/A	N/A	—	—	480.0	N/A	N/A
SSTL135 (all supported classes)	SSTL_135 class I, II, Vccio = 1.35V	MHz	400.0	—	—	480.0	N/A	N/A	—	—	480.0	N/A	N/A
HSUL12 (all supported classes)	HSUL_12 class I, II, Vccio = 1.2V	MHz	400.0	—	—	480.0	N/A	N/A	—	—	480.0	N/A	N/A
LVTTL33	LVTTL, Vccio = 3.3V	MHz	150.0	—	—	180.0	N/A	N/A	—	—	180.0	N/A	N/A
LVCMO33 (for all drives)	LVCMOS, Vccio = 3.3V	MHz	150.0	—	—	180.0	N/A	N/A	—	—	180.0	N/A	N/A
LVCMOS25 (for all drives)	LVCMOS, Vccio = 2.5V	MHz	150.0	—	—	180.0	N/A	N/A	—	—	180.0	N/A	N/A
LVCMOS18 (for all drives)	LVCMOS, Vccio = 1.8V	MHz	150.0	—	—	180.0	N/A	N/A	—	—	180.0	N/A	N/A
LVCMOS15 (for all drives)	LVCMOS, Vccio = 1.5V	MHz	150.0	—	—	180.0	N/A	N/A	—	—	180.0	N/A	N/A
LVCMOS12 (for all drives)	LVCMOS, Vccio = 1.2V	MHz	150.0	—	—	180.0	N/A	N/A	—	—	180.0	N/A	N/A
LVCMOS12 (for all drives)	LVCMOS, Vccio = 1.2V	MHz	150.0	—	—	180.0	N/A	N/A	—	—	180.0	N/A	N/A

Note 1: CPK\DI was calculated for Input Frequency at Fmax + 20% guard bands

Note 2: CPK\DI was calculated for AC level output voltages that guarantees the transition point for the receiving chip

GDDR Timing

The characterization of the EPC5-45F played a dual role – the stated characterization of the USJC fab and the UMC Automotive qual of the same device. GDDR characterization exposed a GDDR timing parameter ($t_{SU\_GDDRX2\_aligned}$) that did not meet the Cpk goal of 1.5 or the DI goal of 1.0. That parameter will be adjusted in the Automotive version of the ECP5 datasheet. Note that the USJC-processed material had acceptable performance for this parameter at Automotive conditions.

Parameter	Description	Spec			Silicon Data - UMC					Silicon Data - Fujitsu				
		-6		Unit	Min	Mean	Max	Cpk	DI	Min	Mean	Max	Cpk	DI
		Min	Max											
Generic DDR Input														
Generic DDRX1 Inputs with Clock and Data Centered at Pin														
$t_{SU\_GDDRX1\_centered}$	Data Setup Before CLK Input	0.52	—	ns	0.20	0.24	0.27	1.48	1.3	0.06	0.09	0.12	4.17	3.5
$t_{HD\_GDDRX1\_centered}$	Data Hold After CLK Input	0.52	—	ns	-0.03	0.00	0.04	3.37	3	0.11	0.18	0.24	3.32	2.5
$f_{DATA\_GDDRX1\_centered}$	GDDRX1 Data Rate[1]	—	500	Mb/s	—	—	1300	N/A	N/A	—	—	1300	N/A	N/A
$f_{MAX\_GDDRX1\_centered}$	GDDRX1 CLK Frequency (SCLK)[1]	—	250	MHz	—	—	650	N/A	N/A	—	—	650	N/A	N/A
Generic DDRX1 Inputs with Clock and Data Aligned at Pin (GDDRX1_RX.SCLK.Aligned)														
$t_{SU\_GDDRX1\_aligned}$	Data Setup from CLK Input	—	-0.55	ns+1/2 UI	-0.26	-0.23	-0.20	4.71	1.5	-0.06	-0.05	-0.04	3.89	3.5
$t_{HD\_GDDRX1\_aligned}$	Data Hold from CLK Input	0.55	—	ns+1/2 UI	-0.03	-0.01	0.01	3.58	3.2	0.12	0.19	0.25	2.69	2.2
$f_{DATA\_GDDRX1\_aligned}$	GDDRX1 Data Rate[1]	—	500	Mb/s	—	—	1300	N/A	N/A	—	—	1300	N/A	N/A
$f_{MAX\_GDDRX1\_aligned}$	GDDRX1 CLK Frequency (SCLK)[1]	—	250	MHz	—	—	650	N/A	N/A	—	—	650	N/A	N/A
Generic DDRX2 Inputs with Clock and Data Centered at Pin (GDDRX2_RX.ECLK.Centered)														
$t_{SU\_GDDRX2\_centered}$	Data Setup before CLK Input[2]	0.471	—	ns	0.23	0.25	0.26	3.51	3.10	0.21	0.22	0.23	6.76	5.68
$t_{HD\_GDDRX2\_centered}$	Data Hold after CLK Input[2]	0.471	—	ns	-0.03	0.07	0.04	3.10	2.80	0.01	0.07	0.13	1.57	1.42
$f_{DATA\_GDDRX2\_centered}$	GDDRX2 Data Rate[3]	—	624	Mb/s	—	—	750	N/A	N/A	—	—	750	N/A	N/A
$f_{MAX\_GDDRX2\_centered}$	GDDRX2 CLK Frequency (ECLK)[3]	—	312	MHz	—	—	375	N/A	N/A	—	—	375	N/A	N/A
Generic DDRX2 Inputs with Clock and Data Aligned at Pin (GDDRX2_RX.ECLK.Aligned)														
$t_{SU\_GDDRX2\_aligned}$	Data Setup before CLK Input	—	–0.495	ns+1/2 UI	-0.24	-0.21	-0.15	1.09	0.98	-0.23	-0.18	-0.13	1.25	1.12
$t_{HD\_GDDRX2\_aligned}$	Data Hold after CLK Input	0.495	—	ns+1/2 UI	0.01	0.07	0.14	1.66	1.43	0.04	0.09	0.18	1.72	1.55
$f_{DATA\_GDDRX2\_aligned}$	GDDRX2 Data Rate[4]	—	624	Mb/s	—	—	750	N/A	N/A	—	—	750	N/A	N/A
$f_{MAX\_GDDRX2\_aligned}$	GDDRX2 CLK Frequency (ECLK)[4]	—	312	MHz	—	—	375	N/A	N/A	—	—	375	N/A	N/A
Video DDRX7:1 Inputs With Clock and Data Aligned at Pin (GDDRX71_RX.ECLK)														
$t_{SU\_LVDS71\_i}$	Data Setup from CLK Input (bit i)[5]	—	–0.41	ns+1/2 UI	-0.08	-0.12	-0.04	1.65	1.48	-0.15	-0.12	-0.06	1.64	1.47
$t_{HD\_LVDS71\_i}$	Data Hold from CLK Input (bit i)[5]	0.41	—	ns+1/2 UI	0.04	-0.01	0.08	1.58	1.42	-0.03	0.01	0.08	1.82	1.56
f_{DATA_LVDS71}	DDR71 Data Rate[6]	—	525	Mb/s	—	—	700	N/A	N/A	—	—	700	N/A	N/A
f_{MAX_LVDS71}	DDR71 CLK Frequency (ECLK)[6]	—	262.5	MHz	—	—	350	N/A	N/A	—	—	350	N/A	N/A

1. Generic DDRX1 modes were tested for error-free operation at 750, 1000, and 1300 Mb/s. No devices failed at any condition.

2. Generic DDRX2 centered modes show a bimodal distribution of setup/hold time requirements. There is an approximate 100 ps difference in mean between the two curves. On any given unit, this 100 ps difference in measurement can be seen intermittently at any set of conditions. Cpk/DI analysis is performed on the worst-case of the two distributions, independent of the better distribution. See Appendix A to see which data is used in this analysis. This bimodality is setup and word-alignment related, a given unit at a given condition would show results in both distributions.

3. The Cpk of DDRX2 Aligned setup-time is below the target of 1.5 on UMC material. This is worst on TT material at 125C because of a high standard deviation, though the mean is worse on FF material. Other conditions meet the Cpk requirement.

4. Generic DDRX2 modes were tested for error-free operation at 750, 1000, and 1300 Mb/s. No devices failed at 750 Mb/s, ~50% of devices/conditions failed at 1000 Mb/s, ~75% of devices/conditions failed at 1300Mb/s.

5. Video DDRX71 showed a bimodal distribution for setup and hold time. See Appendix A to see which data is used in this analysis. This bimodality is BIST-related, and the erroneous values are excluded from Cpk/DI analysis. See appendix for distributions which data was excluded.

6. Video DDRX71 was tested for error-free operation at 490, 560, 630, and 700 Mb/s. No devices failed at any condition

sysCONFIG Timing

The sysCONFIG port is the primary method of providing FPGA configuration data to the device. There is plenty of spec margin to both UMC and USJC material as the minimum Cpk was 2.24.

Config Port Timing Specifications			Spec			Silicon Data - UMC					Silicon Data - Fujitsu				
Symbol	Parameter	Unit	Min	Typ	Max	Min	Typ	Max	Cpk	DI	Min	Typ	Max	Cpk	DI
Master CCLK															
—	Frequency (tested at 310MHz setting)	%	-20	—	20	277.5	307.3	326.8	2.73	1.70	270.0	306.0	328.0	2.52	1.54
Slave Parallel															
t_{CORD}	CCLK to DOUT for Read Data	ns	—	—	12	6.6	6.8	7.0	19.37	4.54	7.4	7.6	7.9	11.93	3.45
t_{SUCBDI}	Data Setup Time to CCLK	ns	1.5	—	—	-0.3	-0.2	0.0	7.94	5.84	-0.5	-0.4	-0.3	11.09	7.96
t_{HCBDI}	Data Hold Time to CCLK	ns	1.5	—	—	0.9	1.1	1.2	2.89	1.78	1.0	1.1	1.3	2.28	1.53
t_{SUCS}	CSN, CSN1 Setup Time to CCLK	ns	2.5	—	—	0.5	0.7	1.2	7.35	6.04	0.6	0.8	0.9	9.75	6.30
t_{HCS}	CSN, CSN1 Hold Time to CCLK	ns	1.5	—	—	0.9	1.1	1.2	2.85	1.78	1.0	1.1	1.3	2.24	1.52
t_{SUWD}	WRITEN Setup Time to CCLK	ns	45	—	—	41.1	41.7	42.0	4.40	2.50	41.4	41.9	42.4	3.73	2.24
t_{HCWD}	WRITEN Hold Time to CCLK	ns	2	—	—	0.9	1.1	1.2	5.98	3.21	1.0	1.1	1.3	5.50	2.94
t_{DCB}	CCLK to BUSY Delay Time	ns	—	—	12	5.6	5.8	6.0	22.84	5.85	5.3	5.5	5.8	20.15	4.97
Slave Parallel															
f_{MAX}	TCK Clock Frequency	MHz	—	—	25	72.4	76.8	78.8	11.96	2.68	78.3	81.4	86.1	8.58	2.61

ECP5-45 sysCONFIG Timings - UMC and USJC(Fujitsu)

ETest/WAT Limits

The goal for this project was to create a functionally equivalent device from the USJC foundry. The process monitors (aka ETest or Wafer Acceptance Testing) are identical between USJC and UMC. The USJC and UMC 40nm Low Power process uses same WAT limits and sampling plan (9 sites, 100% wafer testing)

CONCLUSION

The ECP5U-25F, the ECP5U-45F and the LIF-MD6000 which were originally single sourced from UMC have been successfully second sourced at USJC. Performance of all three of these devices is indistinguishable for any customer using the device within recommended datasheet conditions.

Lattice recommends release of the USJC-versions of the ECP5U-25F, the ECP5U-45F and the LIF-MD6000 into full production at this time.