Stratix III DSP WYSIWYG Description

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1 Introduction

This document describes the WYSIWYG primitive for the Stratix III DSP (or MAC) block. The Stratix III DSP is similar to the Stratix II DSP, but some features are removed (like dynamic scan chains), some are enhanced (like rounding/saturation), and some new ones are added (like output chain adder).

As in previous architectures, the Stratix III DSP is instantiated using two basic primitives: the MAC_MULT and the MAC_OUT. Every function instantiation must have one MAC_OUT primitive and one or more MAC_MULT primitives, depending on the operation mode.

2 Stratix III DSP Multiplier

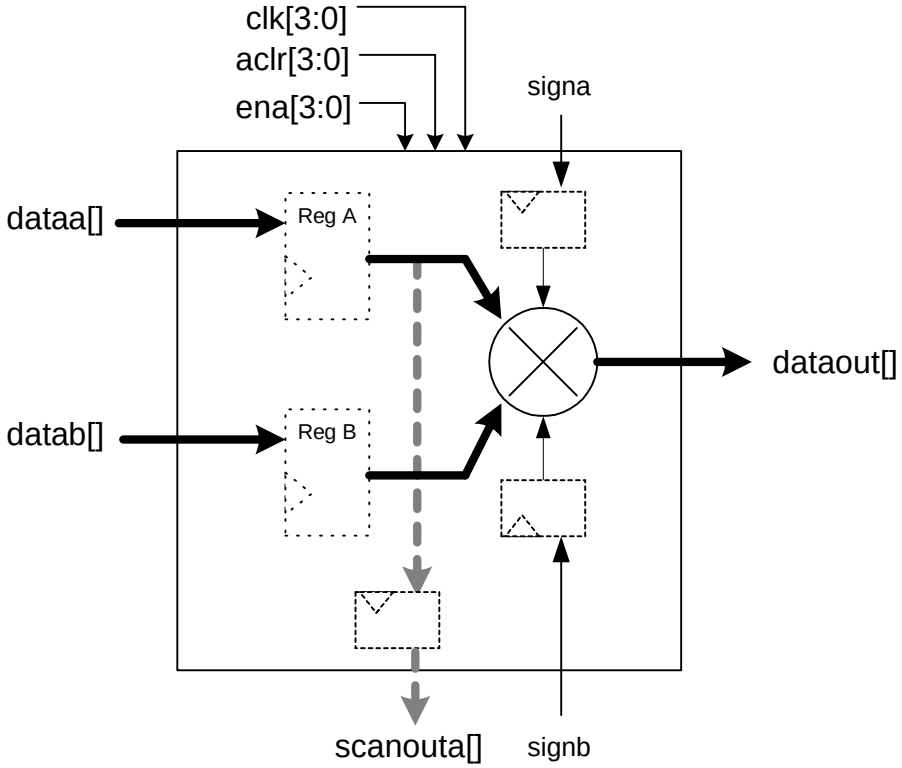


Figure 1: The Stratix III DSP Multiplier WYSIWYG

2.1 Stratix III DSP Multiplier WYSIWYG Primitive

```
STRATIX III_MAC_MULT<InstanceName>
(
      // Input Ports
      .SIGNA( <Sign representation of A> ),
      .SIGNB( <Sign representation of B> ),
      .DATAA( <Data A> ),
      .DATAB( <Data B> ),
      .CLK( <Clock> ),
      .ACLR( <Asynchronous clear> ),
      .ENA( <Clock enable> ),

      // Output Ports
      .DATAOUT( <Data output> ),
      .SCANOUTA( <Output of input register A> ),

      // Observable ports
      .OBSERVABLEDATAAREGOUT( <Observable bus for data port A> ),
      .OBSERVABLEDATABREGOUT( <Observable bus for data port B> ),
      .OBSERVABLESIGNAREGOUT( <Observable port for port A sign register> ),
      .OBSERVABLESIGNBREGOUT( <Observable port for port B sign register> )
);

// Parameters
defparam <InstanceName>.dataa_width = <Data A width>;
defparam <InstanceName>.datab_width = <Data B width>;
defparam <InstanceName>.dataa_clock = <Data A clock>;
defparam <InstanceName>.datab_clock = <Data B clock>;
defparam <InstanceName>.signa_clock = <Sign A clock>;
defparam <InstanceName>.signb_clock = <Sign B clock>;
defparam <InstanceName>.scanouta_clock = <Scanout A clock>;
defparam <InstanceName>.dataa_clear = <Data A clear>;
defparam <InstanceName>.datab_clear = <Data B clear>;
defparam <InstanceName>.signa_clear = <Sign A clear>;
defparam <InstanceName>.signb_clear = <Sign B clear>;
defparam <InstanceName>.scanouta_clear = <Scanout A clear>;
defparam <InstanceName>.signa_internally_grounded = <Sets Sign A to GND>;
defparam <InstanceName>.signb_internally_grounded = <Sets sign B to GND>;
```

2.1.1 Input Ports:

SIGNA - Sign representation of A	
Size (bits)	1
Float Level	High
Programmable Invert	Present
Default Value	VCC
Description	Specifies signed representation of multiplier data A input. Specifying a value of VCC means the data is signed and a value of GND means the data is unsigned. The signal can be registered by specifying signa_clock/clear parameters.
SIGNB - Sign representation of B	
Size (bits)	1
Float Level	High
Programmable Invert	Present
Default Value	VCC
Description	Specifies signed representation of multiplier data B input. Specifying a value of VCC means the data is signed and a value of GND means the data is unsigned. The signal can be registered by specifying signb_clock/clear parameters.
DATAA - Data A	
Size (bits)	18
Float Level	High
Programmable Invert	Present
Default Value	0x3FFFF
Description	Data A input bus of multiplier. Width is specified using dataa_width parameter. Can be registered using dataa_clock/clear parameters.
DATAB - Data B	
Size (bits)	18
Float Level	High
Programmable Invert	Present
Default Value	0x3FFFF
Description	Data B input bus of multiplier. Width is specified using datab_width parameter. Can be registered using datab_clock/clear parameters.
CLK - Clock	
Size (bits)	4
Float Level	High

Programmable Invert	Present
Default Value	0x0
Description	Clock bus for the MAC_MULT.

ACLR - Asynchronous clear

Size (bits)	4
Float Level	High
Programmable Invert	Present
Default Value	0x0
Description	Asynchronous clear bus for the MAC_MULT.

ENA - Clock enable

Size (bits)	4
Float Level	High
Programmable Invert	Present
Default Value	0xF
Description	Clock enable bus for the MAC_MULT.

2.1.2 Output Ports:

DATAOUT - Data output

Size (bits)	36
Description	Data output bus of multiplier. Width is sum of dataa and datab widths. This output can only feed one of the data inputs of the MAC_OUT WYSIWYG using dedicated routing.

SCANOUTA - Output of input register A

Size (bits)	18
Description	Output of input register A, which can feed data A input of another MAC_MULT WYSIWYG. Several of these connections can be cascaded together to form a shift register on the multiplier's data A inputs.

2.1.3 Parameters:

dataa_width - Data A width

Type	Integer
Possible Values	Possible values are 0 and above.
Default Value	1
Required	Must be specified
Description	Specifies the width of data port A.

datab_width - Data B width

Type	Integer
Possible Values	Possible values are 0 and above.
Default Value	1
Required	Must be specified
Description	Specifies the width of data port B.

dataa_clock - Data A clock

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for data port A register. Parameter specifies which index of the clock bus and clock enable bus controls this register. Specify 'none' to bypass register. A single parameter specifies both clock and clock enable index as these control signals are paired (e.g. to specify same clock but different enable, two separate clock and clock-enable indices are required, where the two clock indices are driven by the same clock signal).

datab_clock - Data B clock

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for data port B register. Similar to dataa_clock.

signa_clock - Sign A clock

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for port A sign register.

signb_clock - Sign B clock

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for port B sign register.

scanouta_clock - Scanout A clock

Type	String
Default	"NONE"

Value	
Required	Specification is optional
Description	Specifies the clock and clock enable for scanout port A register.

dataa_clear - Data A clear

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for data port A register. Parameter specifies which index of asynchronous clear bus controls this register. Specify 'none' to bypass register.

datab_clear - Data B clear

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for data port B register. Similar to dataa_clear.

signa_clear - Sign A clear

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for port A sign register.

signb_clear - Sign B clear

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for port B sign register.

scanouta_clear - Scanout A clear

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for scanout port A register.

signa_internally_grounded - Sets Sign A to GND

Type	String
Default	"FALSE"

Value	
Required	Specification is optional
Description	Configures sign A port to ground. This is used only in 36_BIT_MULTIPLY, SHIFT, and DOUBLE modes to ensure proper operation.

signb_internally_grounded - Sets sign B to GND

Type	String
Default Value	"FALSE"
Required	Specification is optional
Description	Configures sign A port to ground. This is used only in 36_BIT_MULTIPLY, SHIFT, and DOUBLE modes to ensure proper operation.

Note: all 'clock' and 'clear' parameters can have values of "none", 0, 1, 2, or 3.

2.1.4 Observable Ports:

OBSERVABLEDATAAREGOUT - Observable bus for data port A

Size (bits)	18
Description	Assigns a name to the observable bus for data port A. This observable bus is only created if the data bus input registers are used.

OBSERVABLEDATABREGOUT - Observable bus for data port B

Size (bits)	18
Description	Assigns a name to the observable bus for data port B. This observable bus is only created if the data bus input registers are used.

OBSERVABLESIGNAREGOUT - Observable port for port A sign register

Size (bits)	1
Description	Assigns a name to the observable port for port A sign register. This observable port is only created if the corresponding port input register is used. **This feature has not been implemented yet.**

OBSERVABLESIGNBREGOUT - Observable port for port B sign register

Size (bits)	1
Description	Assigns a name to the observable port for port B sign register. This observable port is only created if the corresponding port input register is used. **This feature has not been implemented yet.**

3 Stratix III DSP Output

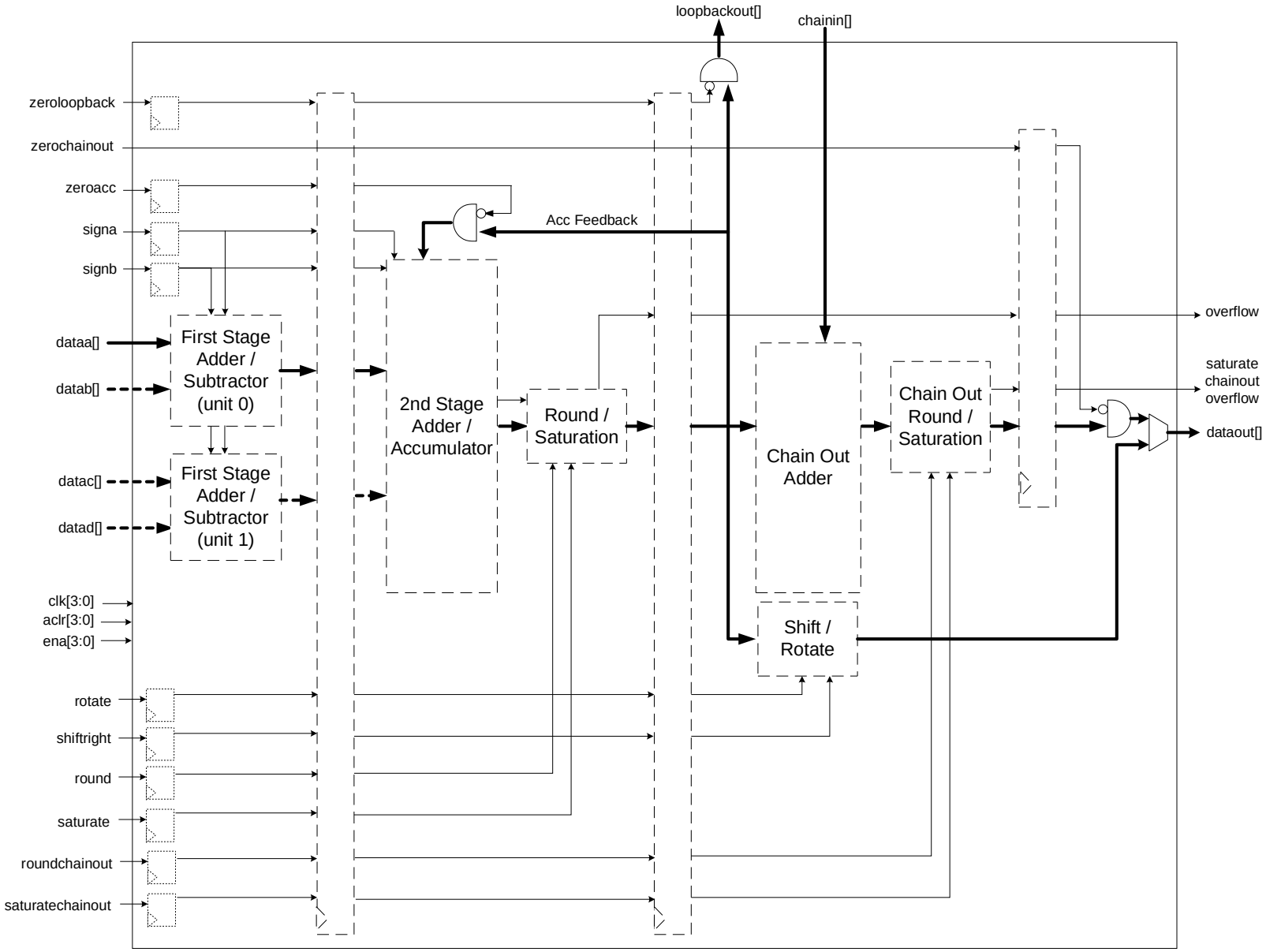


Figure 2: Stratix III DSP Output WYSIWYG

3.1 Stratix III DSP Output WYSIWYG Primitive

```
STRATIX III_MAC_OUT<InstanceName>
(
      // Input Ports
      .SIGNA( <Sign representation of A> ),
      .SIGNB( <Sign representation of B> ),
      .ZEROACC( <Zero accumulator port.> ),
      .ZEROCHAINOUT( <Zero chain out port> ),
      .ZEROLOOPBACK( <Zero loopback port> ),
      .ROTATE( <Rotate port> ),
      .SHIFTRIGHT( <Shift right port> ),
      .ROUND( <Round port> ),
      .ROUNDCHAINOUT( <Saturation for the chain out adder> ),
      .SATURATE( <Saturate port> ),
      .SATURATECHAINOUT( <SATURATECHAINOUTValue> ),
      .DATAA( <Data input A> ),
      .DATAB( <Data input B> ),
      .DATAC( <Data input C> ),
      .DATAD( <Data input D> ),
      .CHAININ( <Adder chain input> ),
      .CLK( <Clock> ),
      .ACLR( <Asynchronous clear> ),
      .ENA( <Clock enable> ),

      // Output Ports
      .OVERFLOW( <Overflow output> ),
      .SATURATECHAINOUTOVERFLOW( <Saturate chain out overflow output> ),
      .DATAOUT( <Data output> ),
      .LOOPBACKOUT( <Loopback output> ),

      // Observable Ports
      .OBSERVABLEFIRSTADDER0REGOUT( <Observable bus for data after the top first-
      level-adder> ),
      .OBSERVABLEFIRSTADDER1REGOUT( <Observable bus for data after the bottom first-
      level-adder> ),
      .OBSERVABLESECONDADDERREGOUT( <Observable bus for data after the second-level-
      adder> ),
      .OBSERVABLEZEROACCREGOUT( <Observable port for the zero accumulator register>
      ),
```

```
.OBSERVABLEZEROLOOPBACKREGOUT( <Observable port for the zero loopback register> ),
.OBSERVABLEROTATEREGOUT( <Observable port for the rotate register> ),
.OBSERVABLESHIFTRIGHTREGOUT( <Observable port for the shift right register> ),
.OBSERVABLEZEROCHAINOUTOUTPUTREGOUT( <Observable port for the zero chain out output register> ),
.OBSERVABLEZEROLOOPBACKOUTPUTREGOUT( <Observable port for the zero loopback output register> ),
.OBSERVABLEROTATEOUTPUTREGOUT( <Observable port for the rotate output register> ),
.OBSERVABLESHIFTRIGHTOUTPUTREGOUT( <Observable port for the shift right output register> ),
.OBSERVABLEROUNDREGOUT( <Observable port for the round register> ),
.OBSERVABLEROUNDCHAINOUTREGOUT( <Observable port for the round register of the chain out adder> ),
.OBSERVABLESATURATEREGOUT( <Observable port for the saturate register> ),
.OBSERVABLESATURATECHAINOUTREGOUT( <Observable port for the saturate register of the chain out adder> ),
.OBSERVABLESIGNAREGOUT( <Observable port for the port A sign register> ),
.OBSERVABLESIGNBREGOUT( <Observable port for the port B sign register> ),
.OBSERVABLEZEROACCPIPELINEREGOUT( <Observable port for the zero accumulator pipeline register> ),
.OBSERVABLEZEROLOOPBACKPIPELINEREGOUT( <Observable port for the zero loopback pipeline register> ),
.OBSERVABLEROTATEPIPELINEREGOUT( <Observable port for the rotate pipeline register> ),
.OBSERVABLESHIFTRIGHTPIPELINEREGOUT( <Observable port for the shift right pipeline register> ),
.OBSERVABLEROUNDPIPELINEREGOUT( <Observable port for the round pipeline register> ),
.OBSERVABLEROUNDCHAINOUTPIPELINEREGOUT( <Observable port for the round pipeline register of the chain out adder> ),
.OBSERVABLESATURATEPIPELINEREGOUT( <Observable port for the saturate pipeline register> ),
.OBSERVABLESATURATECHAINOUTPIPELINEREGOUT( <Observable port for the saturate pipeline register of the chain out adder> ),
.OBSERVABLESIGNAPIPELINEREGOUT( <Observable port for the port A sign pipeline register> ),
.OBSERVABLESIGNBPIPELINEREGOUT( <Observable port for the port B sign pipeline register> ),
.OBSERVABLEROUNDCHAINOUTOUTPUTREGOUT( <Observable port for the round output register of the chain out adder> ),
```

```
      .OBSERVABLESATURATECHAINOUTOUTPUTREGOUT( <Observable port for the saturate
      output register of the chain out adder> ),

      // Hidden Output Ports
      .DFTOUT( <DFT signal> )
);

// Parameters
defparam <InstanceName>.dataa_width = <Data A width>;
defparam <InstanceName>.datab_width = <Data B width>;
defparam <InstanceName>.datac_width = <Data C width>;
defparam <InstanceName>.datad_width = <Data D width>;
defparam <InstanceName>.chainin_width = <Adder chain input width>;
defparam <InstanceName>.first_adder0_clock = <Top pipeline register after the
first-level-adder clock>;
defparam <InstanceName>.first_adder1_clock = <Bottom pipeline register after the
first-level-adder clock>;
defparam <InstanceName>.second_adder_clock = <Output register after the second-
level-adder in chain-out modes clock>;
defparam <InstanceName>.output_clock = <Output clock>;
defparam <InstanceName>.signa_clock = <Sign A clock>;
defparam <InstanceName>.signb_clock = <Sign B clock>;
defparam <InstanceName>.round_clock = <Round clock>;
defparam <InstanceName>.roundchainout_clock = <Round clock of the chain out
adder>;
defparam <InstanceName>.saturate_clock = <Saturate clock>;
defparam <InstanceName>.saturatechainout_clock = <Saturate clock of the chain out
adder>;
defparam <InstanceName>.zeroacc_clock = <Zero accumulator clock>;
defparam <InstanceName>.zeroloopback_clock = <Zero loopback clock>;
defparam <InstanceName>.rotate_clock = <Rotate clock>;
defparam <InstanceName>.shiftright_clock = <Shift right clock>;
defparam <InstanceName>.roundchainout_output_clock = <Round output register
clock of the chain out adder>;
defparam <InstanceName>.saturatechainout_output_clock = <Saturate output
register clock of the chain out adder>;
defparam <InstanceName>.zerochainout_output_clock = <Zero chain out output
clock>;
defparam <InstanceName>.zeroloopback_output_clock = <Zero loopback output
clock>;
defparam <InstanceName>.rotate_output_clock = <Rotate output clock>;
defparam <InstanceName>.shiftright_output_clock = <Shift right output clock>;
defparam <InstanceName>.signa_pipeline_clock = <Sign A pipeline clock>;
```

```
defparam <InstanceName>.signb_pipeline_clock = <Sign B pipeline clock>;
defparam <InstanceName>.round_pipeline_clock = <Round pipeline clock>;
defparam <InstanceName>.roundchainout_pipeline_clock = <Round pipeline clock of the chain out adder>;
defparam <InstanceName>.saturate_pipeline_clock = <Saturate pipeline clock>;
defparam <InstanceName>.saturatechainout_pipeline_clock = <Saturate pipeline clock of the chain out adder>;
defparam <InstanceName>.zeroacc_pipeline_clock = <Zero accumulator pipeline clock>;
defparam <InstanceName>.zeroloopback_pipeline_clock = <Zero loopback pipeline clock>;
defparam <InstanceName>.rotate_pipeline_clock = <Rotate pipeline clock>;
defparam <InstanceName>.shiftright_pipeline_clock = <Shift right pipeline clock>;
defparam <InstanceName>.first_adder0_clear = <Top pipeline register after the first-level-adder clear>;
defparam <InstanceName>.first_adder1_clear = <Bottom pipeline register after the first-level-adder clear>;
defparam <InstanceName>.second_adder_clear = <Output register after the second-level-adder in chain-out modes clear>;
defparam <InstanceName>.output_clear = <Output clear>;
defparam <InstanceName>.signa_clear = <Sign A clear>;
defparam <InstanceName>.signb_clear = <Sign B clear>;
defparam <InstanceName>.round_clear = <Round clear>;
defparam <InstanceName>.roundchainout_clear = <Round clear of the chain out adder>;
defparam <InstanceName>.saturate_clear = <Saturate clear>;
defparam <InstanceName>.saturatechainout_clear = <Saturate clear of the chain out adder>;
defparam <InstanceName>.zeroacc_clear = <Zero accumulator clear>;
defparam <InstanceName>.zeroloopback_clear = <Zero loopback clear>;
defparam <InstanceName>.rotate_clear = <Rotate clear>;
defparam <InstanceName>.shiftright_clear = <Shift right clear>;
defparam <InstanceName>.roundchainout_output_clear = <Round output register clear of the chain out adder>;
defparam <InstanceName>.saturatechainout_output_clear = <Saturate output register clear of the chain out adder>;
defparam <InstanceName>.zerochainout_output_clear = <Zero chain out output clear>;
defparam <InstanceName>.zeroloopback_output_clear = <Zero loopback output clear>;
defparam <InstanceName>.rotate_output_clear = <Rotate output clear>;
defparam <InstanceName>.shiftright_output_clear = <Shift right output clear>;
```

```
defparam <InstanceName>.signa_pipeline_clear = <Sign A pipeline clear>;
defparam <InstanceName>.signb_pipeline_clear = <Sign B pipeline clear>;
defparam <InstanceName>.round_pipeline_clear = <Round pipeline clear>;
defparam <InstanceName>.roundchainout_pipeline_clear = <Round pipeline clear of
the chain out adder>;
defparam <InstanceName>.saturate_pipeline_clear = <Saturate pipeline clear>;
defparam <InstanceName>.saturatechainout_pipeline_clear = <Saturate pipeline
clear of the chain out adder>;
defparam <InstanceName>.zeroacc_pipeline_clear = <Zero accumulator pipeline
clear>;
defparam <InstanceName>.zeroloopback_pipeline_clear = <Zero loopback pipeline
clear>;
defparam <InstanceName>.rotate_pipeline_clear = <Rotate pipeline clear>;
defparam <InstanceName>.shiftright_pipeline_clear = <Shift right pipeline clear>;
defparam <InstanceName>.first_adder0_mode = <Top first-level-adder mode>;
defparam <InstanceName>.first_adder1_mode = <Bottom first-level-adder mode>;
defparam <InstanceName>.acc_adder_operation = <Second-level-adder in
accumulator mode operation>;
defparam <InstanceName>.round_mode = <Rounding mode>;
defparam <InstanceName>.round_chain_out_mode = <Chain out rounding mode>;
defparam <InstanceName>.round_width = <Rounding width>;
defparam <InstanceName>.round_chain_out_width = <Chain out rounding width>;
defparam <InstanceName>.saturate_mode = <Saturation mode>;
defparam <InstanceName>.saturate_chain_out_mode = <Chain out saturation mode>;
defparam <InstanceName>.saturate_width = <Chain out saturation width>;
defparam <InstanceName>.saturate_chain_out_width =
<saturate_chain_out_widthValue>;
defparam <InstanceName>.operation_mode = <Operation mode>;
```

3.1.1 Input Ports:

SIGNA - Sign representation of A

Size (bits)	1
Float Level	High
Programmable Invert	Present
Default Value	VCC
Description	Specifies signed representation of multiplier data A input. Specifying a value of VCC means the data is signed and a value of GND means the data is unsigned. The signal can be registered by specifying signa_clock/clear parameters.

SIGNB - Sign representation of B

Size (bits)	1
Float Level	High
Programmable Invert	Present
Default Value	VCC
Description	Specifies signed representation of multiplier data B input. Specifying a value of VCC means the data is signed and a value of GND means the data is unsigned. The signal can be registered by specifying signb_clock/clear parameters.

ZEROACC - Zero accumulator port.

Size (bits)	1
Float Level	High
Programmable Invert	Present
Default Value	GND
Description	Clears the accumulator feedback path to zero. This is also equivalent to synchronously loading the accumulator with the result of second-level-adder. This allows clearing the accumulator and beginning a new accumulation in the same cycle.

ZEROCHAINOUT - Zero chain out port

Size (bits)	1
Float Level	High
Programmable Invert	Present
Default Value	GND
Description	Clears the output of the chain-out adder. This is used to reset the output adder chain to zero.

ZEROLOOPBACK - Zero loopback port

Size (bits)	1
Float Level	High
Programmable Invert	Present
Default Value	GND
Description	Clears the loopback path from the first-level adder into the multiplier.

ROTATE - Rotate port

Size (bits)	1
Float Level	High
Programmable Invert	Present
Default Value	GND
Description	Enable/disable rotation when in the 'shift' mode. When this signal is used, the shiftright

	signal should be GND. A value of GND means do not rotate, while a value of VCC means perform the rotation. Only 32-bit data inputs are supported, with an assumption that the input data is padded with 4 0s on the LSBs to make 36-bit inputs. In this mode, the result is always at the same position of the output (starting at bit 8).
SHIFTRIGHT - Shift right port	
Size (bits)	1
Float Level	High
Programmable Invert	Present
Default Value	GND
Description	Select between left shift and right shift when in the 'shift' operation mode. A value of GND means shift left, and a value of VCC means shift right. Only 32-bit data inputs are supported, with an assumption that the input data is padded with 4 0s on the LSBs to make 36-bit inputs. In this mode, the result is always at the same position of the output (starting at bit 8).
ROUND - Round port	
Size (bits)	1
Float Level	High
Programmable Invert	Present
Default Value	GND
Description	Enable/disable rounding after the second-level adder. A value of VCC enables rounding, while GND disables rounding.
ROUNDCHAINOUT - Rounding for the chain out adder	
Size (bits)	1
Float Level	High
Programmable Invert	Present
Default Value	GND
Description	Enable/disable rounding after the chain out adder. A value of VCC enables rounding, while GND disables rounding.
SATURATE - Saturate port	
Size (bits)	1
Float Level	High
Programmable Invert	Present
Default Value	GND
Description	Enable/disable saturation after the second-level adder. A value of VCC enables saturation, while GND disables saturation.
SATURATECHAINOUT - Saturation for the chain out adder	
Size (bits)	1

Float Level	High
Programmable Invert	Present
Default Value	GND
Description	Enable/disable saturation after the chain out adder. A value of VCC enables saturation, while GND disables saturation.
DATAA - Data input A	
Size (bits)	36
Float Level	High
Programmable Invert	None
Default Value	0xFFFFFFFFF
Description	Data input for port A.
DATAB - Data input B	
Size (bits)	36
Float Level	High
Programmable Invert	None
Default Value	0xFFFFFFFFF
Description	Data input for port B.
DATAC - Data input C	
Size (bits)	36
Float Level	High
Programmable Invert	None
Default Value	0xFFFFFFFFF
Description	Data input for port C.
DATAD - Data input D	
Size (bits)	36
Float Level	High
Programmable Invert	None
Default Value	0xFFFFFFFFF
Description	Data input for port D.
CHAININ - Adder chain input	
Size (bits)	44
Float Level	High

Programmable Invert	None
Default Value	0x00000000000
Description	Adder chain-in input for previous half-block. Used only in chain-out modes.
CLK - Clock	
Size (bits)	4
Float Level	High
Programmable Invert	Present
Default Value	0x0
Description	Clock bus for the MAC_OUT.
ACLR - Asynchronous clear	
Size (bits)	4
Float Level	High
Programmable Invert	Present
Default Value	0x0
Description	Asynchronous clear bus for the MAC_OUT.
ENA - Clock enable	
Size (bits)	4
Float Level	High
Programmable Invert	Present
Default Value	0xF
Description	Clock enable bus for the MAC_OUT.

3.1.2 Output Ports:

OVERFLOW - Overflow output	
Size (bits)	1
Description	Saturation or accumulator overflow output of second-level-adder. In accumulator mode, output is accumulator overflow when 'saturate' is not asserted, and is saturation overflow when 'saturate' is asserted.
SATURATECHAINOUTOVERFLOW - Saturate chain out overflow output	
Size (bits)	1
Description	Saturation overflow output of chain out saturation block.
DATAOUT - Data output	

Size (bits)	72
Description	Data output bus which contains the result of the MAC_OUT function.

LOOPBACKOUT - Loopback output

Size (bits)	18
Description	Internal loopback output from first-level adder's output to MAC_MULT's Data B input port, using dedicated routing. Used only in loopback mode.

3.1.3 Parameters:

dataa_width - Data A width

Type	Integer
Possible Values	Possible values are 0 and above.
Default Value	1
Required	Must be specified
Description	Specifies the width of data port A.

datab_width - Data B width

Type	Integer
Possible Values	Possible values are 0 and above.
Default Value	1
Required	Must be specified
Description	Specifies the width of data port B.

datac_width - Data C width

Type	Integer
Possible Values	Possible values are 0 and above.
Default Value	1
Required	Must be specified
Description	Specifies the width of data port C.

datad_width - Data D width

Type	Integer
Possible Values	Possible values are 0 and above.
Default Value	1
Required	Must be specified

Description	Specifies the width of data port D.
chainin_width - Adder chain input width	
Type	Integer
Possible Values	Possible values are 0 and above.
Default Value	1
Required	Specification is optional
Description	Specifies the width of the adder chain input port. The adder chain input feeds the chain-out adder and is fed by the data output of the MAC_OUT from the previous DSP half-block. Only be used in chain-out modes.
first_adder0_clock - Top pipeline register after the first-level-adder clock	
Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable of the top pipeline register after the first-level-adder.
first_adder1_clock - Bottom pipeline register after the first-level-adder clock	
Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable of the bottom pipeline register after the first-level-adder.
second_adder_clock - Output register after the second-level-adder in chain-out modes clock	
Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable of the output register after the second-level-adder in chain-out modes. Not used in non chain-out modes.
output_clock - Output clock	
Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for the output port register.
signa_clock - Sign A clock	
Type	String

Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for port A sign register.

signb_clock - Sign B clock

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for port B sign register.

round_clock - Round clock

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for the round port register.

roundchainout_clock - Round clock of the chain out adder

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for the round port input register of the chain out adder.

saturate_clock - Saturate clock

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for the saturate port input register.

saturatechainout_clock - Saturate clock of the chain out adder

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for the saturate port input register of the chain out adder.

zeroacc_clock - Zero accumulator clock

Type	String

Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for the zero accumulator port input register.

zeroloopback_clock - Zero loopback clock

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for the zero loopback port input register.

rotate_clock - Rotate clock

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for the rotate port input register.

shiftright_clock - Shift right clock

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for the shift right port input register.

roundchainout_output_clock - Round output register clock of the chain out adder

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for the round output register of the chain out adder.

saturatechainout_output_clock - Saturate output register clock of the chain out adder

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for the saturate output register of the chain out adder.

zerochainout_output_clock - Zero chain out output clock

Type	String
Default	"NONE"

Value	
Required	Specification is optional
Description	Specifies the clock and clock enable for the zero chain out port output register.

zeroloopback_output_clock - Zero loopback output clock

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for the zero loopback port output register.

rotate_output_clock - Rotate output clock

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for the rotate port output register.

shiftright_output_clock - Shift right output clock

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for the shift right port output register.

signa_pipeline_clock - Sign A pipeline clock

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for port A sign pipeline register.

signb_pipeline_clock - Sign B pipeline clock

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for port B sign pipeline register.

round_pipeline_clock - Round pipeline clock

Type	String
Default Value	"NONE"

Required	Specification is optional
Description	Specifies the clock and clock enable for the round port pipeline register.

roundchainout_pipeline_clock - Round pipeline clock of the chain out adder

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for the round pipeline register of the chain out adder.

saturate_pipeline_clock - Saturate pipeline clock

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for the saturate port pipeline register.

saturatechainout_pipeline_clock - Saturate pipeline clock of the chain out adder

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for the saturate pipeline register of the chain out adder.

zeroacc_pipeline_clock - Zero accumulator pipeline clock

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for the zero accumulator port pipeline register.

zeroloopback_pipeline_clock - Zero loopback pipeline clock

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for the zero loopback port pipeline register.

rotate_pipeline_clock - Rotate pipeline clock

Type	String
Default Value	"NONE"
Required	Specification is optional

Description	Specifies the clock and clock enable for the rotate port pipeline register.
shiftright_pipeline_clock - Shift right pipeline clock	
Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clock and clock enable for the shift right port pipeline register.
first_adder0_clear - Top pipeline register after the first-level-adder clear	
Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear of the top pipeline register after the first-level-adder.
first_adder1_clear - Bottom pipeline register after the first-level-adder clear	
Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear of the bottom pipeline register after the first-level-adder.
second_adder_clear - Output register after the second-level-adder in chain-out modes clear	
Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear of the output register after the second-level-adder in chain-out modes. Not used in non chain-out modes.
output_clear - Output clear	
Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for the output port register.
signa_clear - Sign A clear	
Type	String
Default Value	"NONE"
Required	Specification is optional

Description	Specifies the clear for port A sign register.
signb_clear - Sign B clear	
Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for port B sign register.
round_clear - Round clear	
Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for the round port register.
roundchainout_clear - Round clear of the chain out adder	
Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for the round port input register of the chain out adder.
saturate_clear - Saturate clear	
Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for the saturate port input register.
saturatechainout_clear - Saturate clear of the chain out adder	
Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for the saturate port input register of the chain out adder.
zeroacc_clear - Zero accumulator clear	
Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for the zero accumulator port input register.

zeroloopback_clear - Zero loopback clear

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for the zero loopback port input register.

rotate_clear - Rotate clear

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for the rotate port input register.

shiftright_clear - Shift right clear

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for the shift right port input register.

roundchainout_output_clear - Round output register clear of the chain out adder

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for the round output register of the chain out adder.

saturatechainout_output_clear - Saturate output register clear of the chain out adder

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for the saturate output register of the chain out adder.

zerochainout_output_clear - Zero chain out output clear

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for the zero chain out port output register.

zeroloopback_output_clear - Zero loopback output clear

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for the zero loopback port output register.

rotate_output_clear - Rotate output clear

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for the rotate port output register.

shiftright_output_clear - Shift right output clear

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for the shift right port output register.

signa_pipeline_clear - Sign A pipeline clear

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for port A sign pipeline register.

signb_pipeline_clear - Sign B pipeline clear

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for port B sign pipeline register.

round_pipeline_clear - Round pipeline clear

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for the round port pipeline register.

roundchainout_pipeline_clear - Round pipeline clear of the chain out adder

Type	String

Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for the round pipeline register of the chain out adder.

saturate_pipeline_clear - Saturate pipeline clear

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for the saturate port pipeline register.

saturatechainout_pipeline_clear - Saturate pipeline clear of the chain out adder

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for the saturate pipeline register of the chain out adder.

zeroacc_pipeline_clear - Zero accumulator pipeline clear

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for the zero accumulator port pipeline register.

zeroloopback_pipeline_clear - Zero loopback pipeline clear

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for the zero loopback port pipeline register.

rotate_pipeline_clear - Rotate pipeline clear

Type	String
Default Value	"NONE"
Required	Specification is optional
Description	Specifies the clear for the rotate port pipeline register.

shiftright_pipeline_clear - Shift right pipeline clear

Type	String
Default	"NONE"

Value	
Required	Specification is optional
Description	Specifies the clear for the shift right port pipeline register.

first_adder0_mode - Top first-level-adder mode

Type	String
Possible Values	Possible values are: "Add", "Subtract". An alias for "Subtract" is "Sub".
Default Value	"Add"
Required	Specification is optional
Description	Specifies whether the top first-level-adder does addition or subtraction.

first_adder1_mode - Bottom first-level-adder mode

Type	String
Possible Values	Possible values are: "Add", "Subtract". An alias for "Subtract" is "Sub".
Default Value	"Add"
Required	Specification is optional
Description	Specifies whether the bottom first-level-adder does addition or subtraction.

acc_adder_operation - Second-level-adder in accumulator mode operation

Type	String
Possible Values	Possible values are: "Add", "Subtract". An alias for "Subtract" is "Sub".
Default Value	"Add"
Required	Specification is optional
Description	Specifies whether the second-level-adder does addition or subtraction in accumulator mode.

round_mode - Rounding mode

Type	String
Possible Values	Possible values are: "Nearest_Integer", "Nearest_Even".
Default Value	"Nearest_Integer"
Required	Specification is optional
Description	Selects whether the rounding mode is nearest integer (i.e. biased) or nearest even (i.e. unbiased).

round_chain_out_mode - Chain out rounding mode

Type	String

Possible Values	Possible values are: "Nearest_Integer", "Nearest_Even".
Default Value	"Nearest_Integer"
Required	Specification is optional
Description	Selects whether the rounding mode of the chain out adder is nearest integer (i.e. biased) or nearest even (i.e. unbiased). The chain-out and second-level rounding and saturation blocks must be configured the same.

round_width - Rounding width

Type	Integer
Possible Values	Possible values are 0 and above.
Default Value	15
Required	Specification is optional
Description	Specifies the width of fractional data to round to.

round_chain_out_width - Chain out rounding width

Type	Integer
Possible Values	Possible values are 0 and above.
Default Value	15
Required	Specification is optional
Description	Specifies the width of fractional data of the chain out adder to round to. The chain-out and second-level rounding and saturation blocks must be configured the same.

saturate_mode - Saturation mode

Type	String
Possible Values	Possible values are: "Asymmetric", "Symmetric".
Default Value	"Asymmetric"
Required	Specification is optional
Description	Selects whether the saturation mode is asymmetric or symmetric.

saturate_chain_out_mode - Chain out saturation mode

Type	String
Possible Values	Possible values are: "Asymmetric", "Symmetric".
Default Value	"Asymmetric"
Required	Specification is optional

Description	Selects whether the saturation mode of the chain out adder is asymmetric or symmetric. The chain-out and second-level rounding and saturation blocks must be configured the same.
saturate_width - Saturation width	
Type	Integer
Possible Values	Possible values are 0 and above.
Default Value	1
Required	Specification is optional
Description	Specifies the width of fractional data to saturate to.
saturate_chain_out_width - Chain out saturation width	
Type	Integer
Possible Values	Possible values are 0 and above.
Default Value	1
Required	Specification is optional
Description	Specifies the width of fractional data of the chain out adder to saturate to. The chain-out and second-level rounding and saturation blocks must be configured the same.
operation_mode - Operation mode	
Type	String
Possible Values	Possible values are: "Output_only", "One_level_adder", "Loopback", "Accumulator", "Two_level_adder", "Accumulator_chain_out", "Two_level_adder_chain_out", "36_bit_multiply", "Shift", "Double".
Default Value	"Output_only"
Required	Must be specified
Description	Selects the operation mode of the MAC_OUT atom. Based on the operation mode, different ports and parameters can be used.

Note: all ‘clock’ and ‘clear’ parameters can have values of “none”, 0, 1, 2, or 3.

3.1.4 Observable Ports:

OBSERVABLEFIRSTADDER0REGOUT - Observable bus for data after the top first-level-adder	
Size (bits)	37
Description	Assigns a name to the observable bus for data after the top first-level-adder. This observable bus is only created if the corresponding data pipeline registers are used. **This feature has not been implemented yet.**
OBSERVABLEFIRSTADDER1REGOUT - Observable bus for data after the bottom first-level-adder	
Size (bits)	37

Description	Assigns a name to the observable bus for data after the bottom first-level-adder. This observable bus is only created if the corresponding data pipeline registers are used. **This feature has not been implemented yet.**

OBSERVABLESECONDADDERREGOUT - Observable bus for data after the second-level-adder

Size (bits)	44
Description	Assigns a name to the observable bus for data after the second-level-adder. This observable bus is only created if the corresponding data second-stage pipeline registers are used. **This feature has not been implemented yet.**

OBSERVABLEZEROACCREGOUT - Observable port for the zero accumulator register

Size (bits)	1
Description	Assigns a name to the observable port for the zero accumulator register. This observable port is only created if the corresponding port input register is used. **This feature has not been implemented yet.**

OBSERVABLEZEROLOOPBACKREGOUT - Observable port for the zero loopback register

Size (bits)	1
Description	Assigns a name to the observable port for the zero loopback register. This observable port is only created if the corresponding port input register is used. **This feature has not been implemented yet.**

OBSERVABLEROTATEREGOUT - Observable port for the rotate register

Size (bits)	1
Description	Assigns a name to the observable port for the rotate register. This observable port is only created if the corresponding port input register is used. **This feature has not been implemented yet.**

OBSERVABLESHIFTRIGHTREGOUT - Observable port for the shift right register

Size (bits)	1
Description	Assigns a name to the observable port for the shift right register. This observable port is only created if the corresponding port input register is used. **This feature has not been implemented yet.**

OBSERVABLEZEROCHAINOUTOUTPUTREGOUT - Observable port for the zero chain out output register

Size (bits)	1
Description	Assigns a name to the observable port for the zero chain out output register. This observable port is only created if the corresponding port output register is used. **This feature has not been implemented yet.**

OBSERVABLEZEROLOOPBACKOUTPUTREGOUT - Observable port for the zero loopback output register

Size (bits)	1
Description	Assigns a name to the observable port for the zero loopback output register. This observable port is only created if the corresponding port output register is used. **This feature has not been implemented yet.**

OBSERVABLEROTATEOUTPUTREGOUT - Observable port for the rotate output register

Size (bits)	1
Description	Assigns a name to the observable port for the rotate output register. This observable port is only created if the corresponding port output register is used. **This feature has not been implemented yet.**

OBSERVABLESHIFTRIGHTOUTPUTREGOUT - Observable port for the shift right output register

Size (bits)	1
Description	Assigns a name to the observable port for the shift right output register. This observable port is only created if the corresponding port output register is used. **This feature has not been implemented yet.**

OBSERVABLEROUNDREGOUT - Observable port for the round register

Size (bits)	1
Description	Assigns a name to the observable port for the round register. This observable port is only created if the corresponding port input register is used. **This feature has not been implemented yet.**

OBSERVABLEROUNDCHAINOUTREGOUT - Observable port for the round register of the chain out adder

Size (bits)	1
Description	Assigns a name to the observable port for the round register of the chain out adder. This observable port is only created if the corresponding port input register is used. **This feature has not been implemented yet.**

OBSERVABLESATURATEREGOUT - Observable port for the saturate register

Size (bits)	1
Description	Assigns a name to the observable port for the saturate register. This observable port is only created if the corresponding port input register is used. **This feature has not been implemented yet.**

OBSERVABLESATURATECHAINOUTREGOUT - Observable port for the saturate register of the chain out adder

Size (bits)	1
Description	Assigns a name to the observable port for the saturate register of the chain out adder. This observable port is only created if the corresponding port input register is used. **This feature has not been implemented yet.**

OBSERVABLESIGNAREGOUT - Observable port for the port A sign register

Size (bits)	1
Description	Assigns a name to the observable port for the port A sign register. This observable port is only created if the corresponding port input register is used. **This feature has not been implemented yet.**

OBSERVABLESIGNBREGOUT - Observable port for the port B sign register

Size (bits)	1
Description	Assigns a name to the observable port for the port B sign register. This observable port is only created if the corresponding port input register is used. **This feature has not been implemented yet.**

OBSERVABLEZEROACCPIPELINEREGOUT - Observable port for the zero accumulator pipeline register

Size (bits)	1
Description	Assigns a name to the observable port for the zero accumulator pipeline register. This observable port is only created if the corresponding port pipeline register is used. **This feature has not been implemented yet.**

OBSERVABLEZEROLOOPBACKPIPELINEREGOUT - Observable port for the zero loopback pipeline register

Size (bits)	1
Description	Assigns a name to the observable port for the zero loopback pipeline register. This observable port is only created if the corresponding port pipeline register is used. **This feature has not been implemented yet.**

OBSERVABLEROTATEPIPELINEREGOUT - Observable port for the rotate pipeline register

Size (bits)	1
Description	Assigns a name to the observable port for the rotate pipeline register. This observable port is only created if the corresponding port pipeline register is used. **This feature has not been implemented yet.**

OBSERVABLESHIFTRIGHTPIPELINEREGOUT - Observable port for the shift right pipeline register

Size (bits)	1
Description	Assigns a name to the observable port for the shift right pipeline register. This observable port is only created if the corresponding port pipeline register is used. **This feature has not been implemented yet.**

OBSERVABLEROUNDPIPELINEREGOUT - Observable port for the round pipeline register

Size (bits)	1
Description	Assigns a name to the observable port for the round pipeline register. This observable port is only created if the corresponding port pipeline register is used. **This feature has not been implemented yet.**

OBSERVABLEROUNDCHAINOUTPIPELINEREGOUT - Observable port for the round pipeline register of the chain out adder

Size (bits)	1
Description	Assigns a name to the observable port for the round pipeline register of the chain out adder. This observable port is only created if the corresponding port pipeline register is used. **This feature has not been implemented yet.**

OBSERVABLESATURATEPIPELINEREGOUT - Observable port for the saturate pipeline register

Size (bits)	1
Description	Assigns a name to the observable port for the saturate pipeline register. This observable port is only created if the corresponding port pipeline register is used. **This feature has not been implemented yet.**

OBSERVABLESATURATECHAINOUTPIPELINEREGOUT - Observable port for the saturate pipeline register of the chain out adder

Size (bits)	1
Description	Assigns a name to the observable port for the saturate pipeline register of the chain out adder. This observable port is only created if the corresponding port pipeline register is used. **This feature has not been implemented yet.**

OBSERVABLESIGNAPIPELINEREGOUT - Observable port for the port A sign pipeline register

Size (bits)	1
Description	Assigns a name to the observable port for the port A sign pipeline register. This observable port is only created if the corresponding port pipeline register is used. **This feature has not been implemented yet.**

OBSERVABLESIGNBPIPELINEREGOUT - Observable port for the port B sign pipeline register

Size (bits)	1

Description	Assigns a name to the observable port for the port B sign pipeline register. This observable port is only created if the corresponding port pipeline register is used. **This feature has not been implemented yet.**
OBSERVABLEROUNDCHAINOUTOUTPUTREGOUT - Observable port for the round output register of the chain out adder	
Size (bits)	1
Description	Assigns a name to the observable port for the round output register of the chain out adder. This observable port is only created if the corresponding port output register is used. **This feature has not been implemented yet.**
OBSERVABLESATURATECHAINOUTOUTPUTREGOUT - Observable port for the saturate output register of the chain out adder	
Size (bits)	1
Description	Assigns a name to the observable port for the saturate output register of the chain out adder. This observable port is only created if the corresponding port output register is used. **This feature has not been implemented yet.**

3.1.5 Hidden Output ports:

DFTOUT - DFT signal	
Size (bits)	1
Description	For testing purposes only.

Table 1: Output Widths for MAC Output Cell

Operation Mode	Max Output Width for dataout port
Output Only	width_a
One Level Adder	width_a *(note: not width_a +1)*
Loopback	width_a *(note: not width_a +1)*
Accumulator	width_a + 8
Accumulator + Chainout	width_a + 8
Two Level Adder	width_a + 2
Two Level Adder + Chainout	width_a + 8
36_Bit_Multiply	width_a + width_b
Shift	width_a + width_b
Double	width_a + 19 *(note: due to one 18-bit shift)*

4 Modes of Operation

This section describes each of the possible modes of operation for a MAC slice.

4.1 Multiplier Only Mode

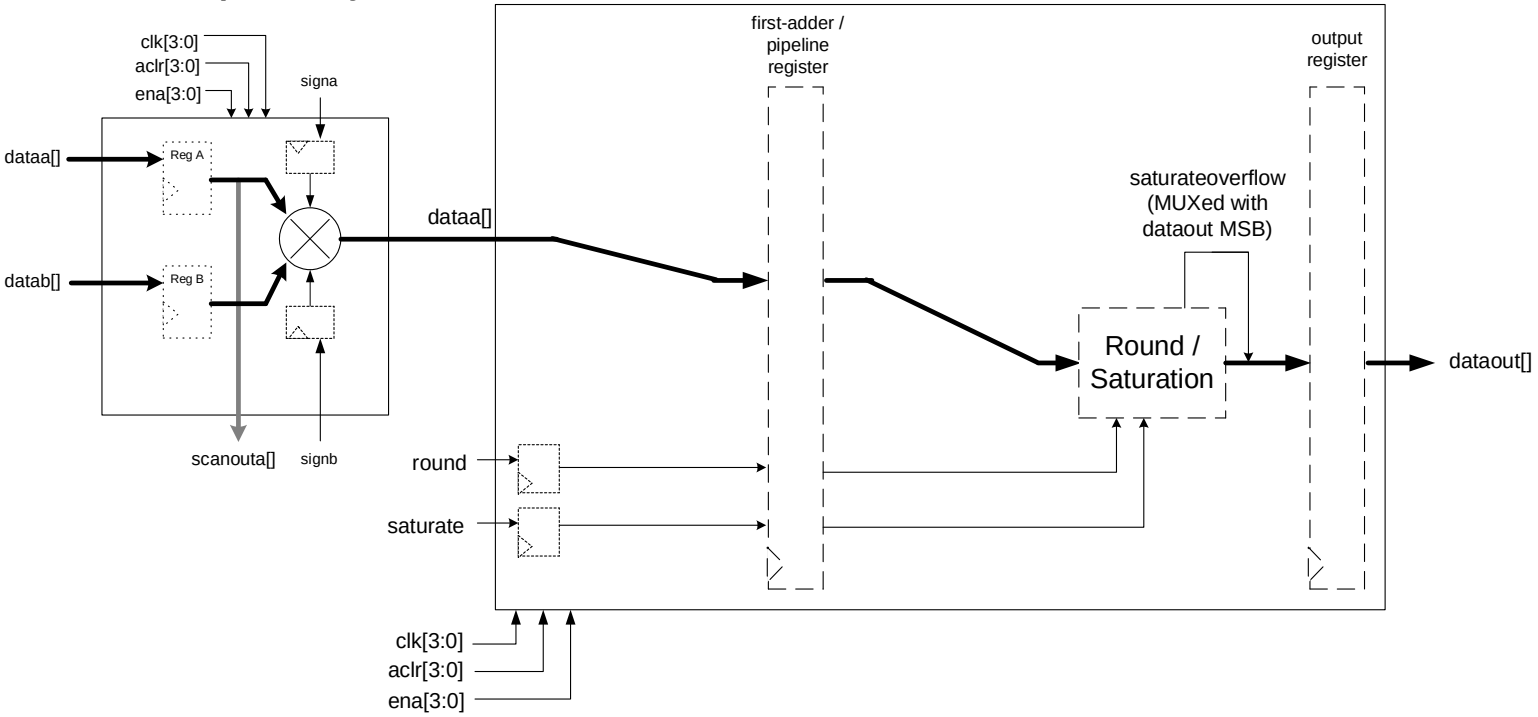


Figure 3: Multiplier Only Mode

4.2 Multiply-One-Level-Adder Mode

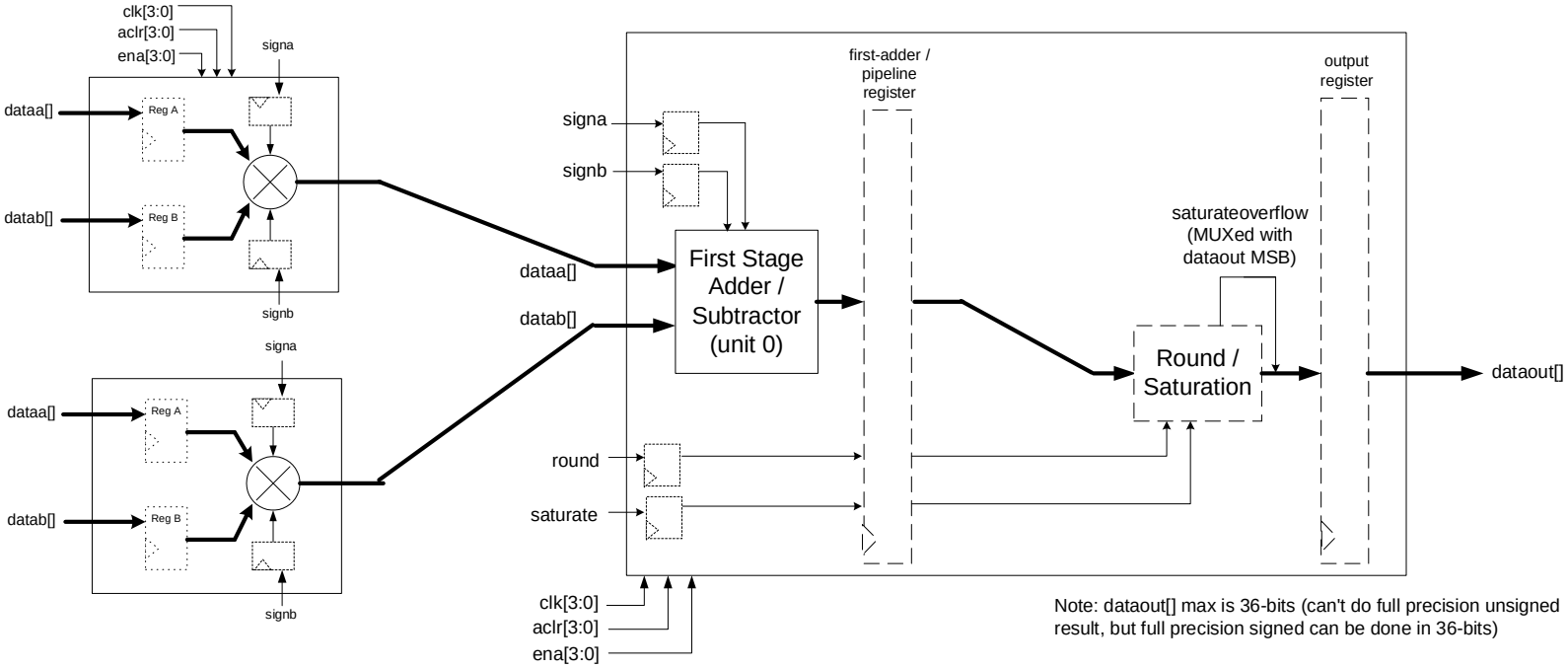


Figure 4: Multiply-One-Level-Adder Mode

4.3 Multiply-Loopback Mode

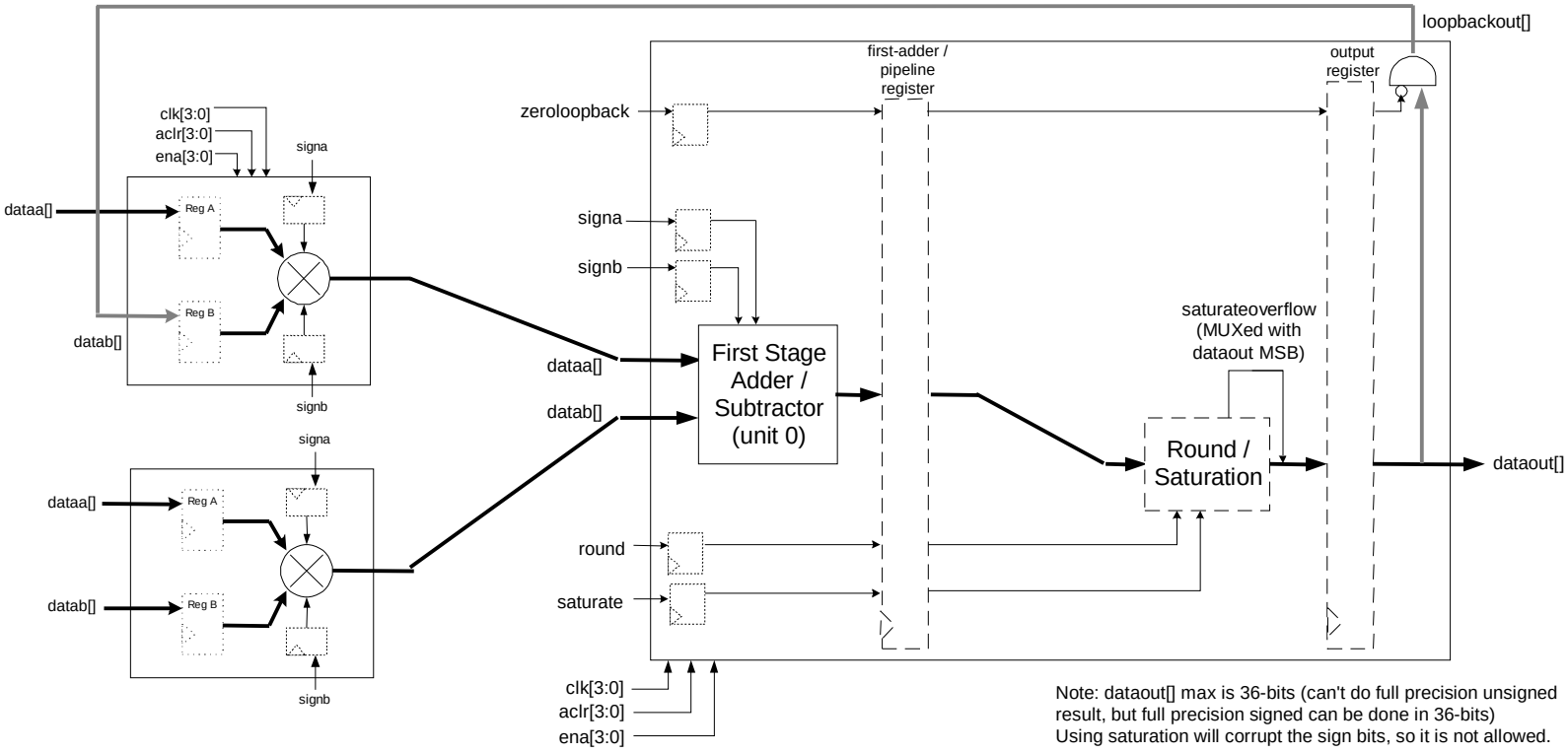


Figure 5: Multiplier Loopback Mode

4.4 Multiply-Accumulator Mode

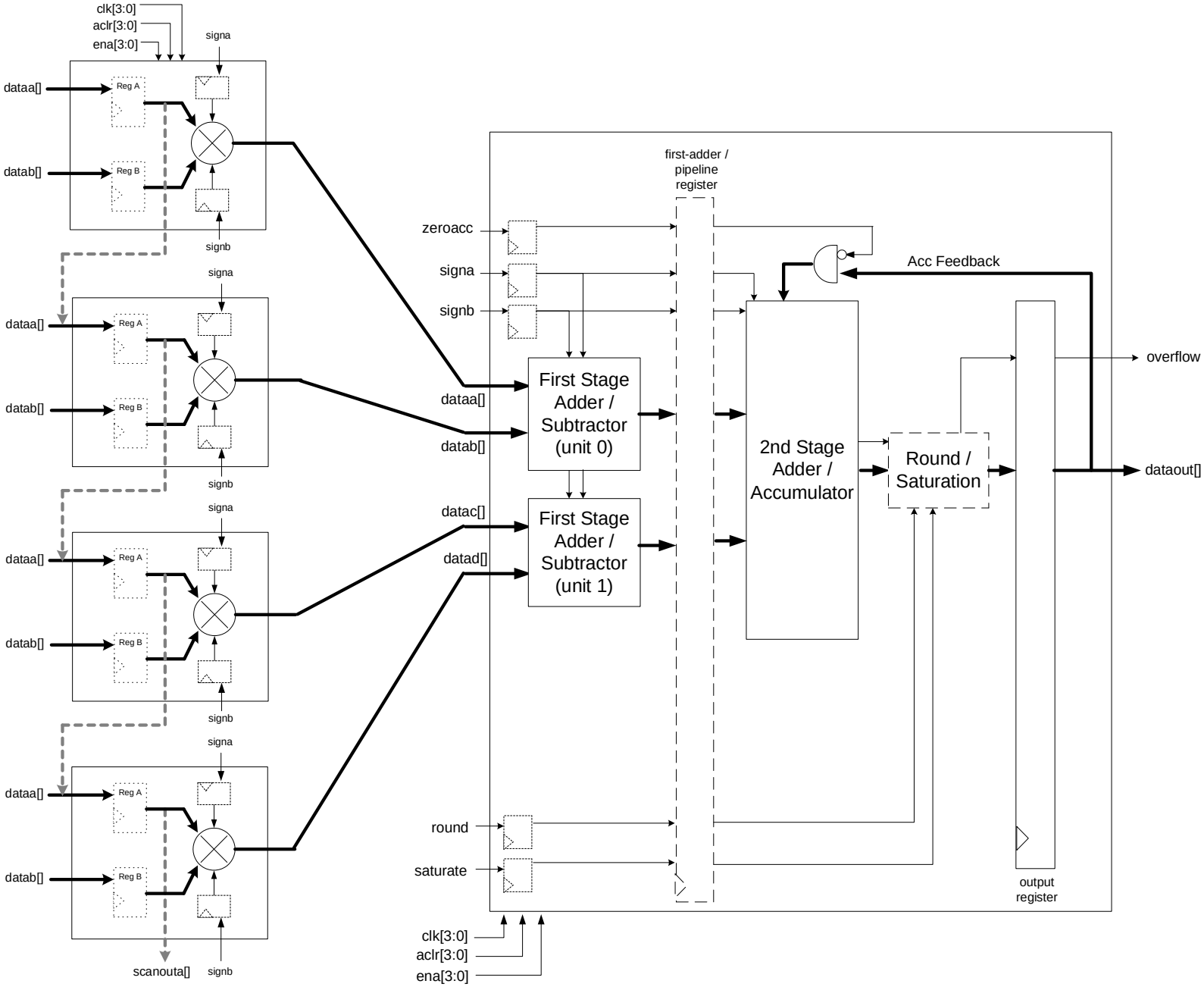
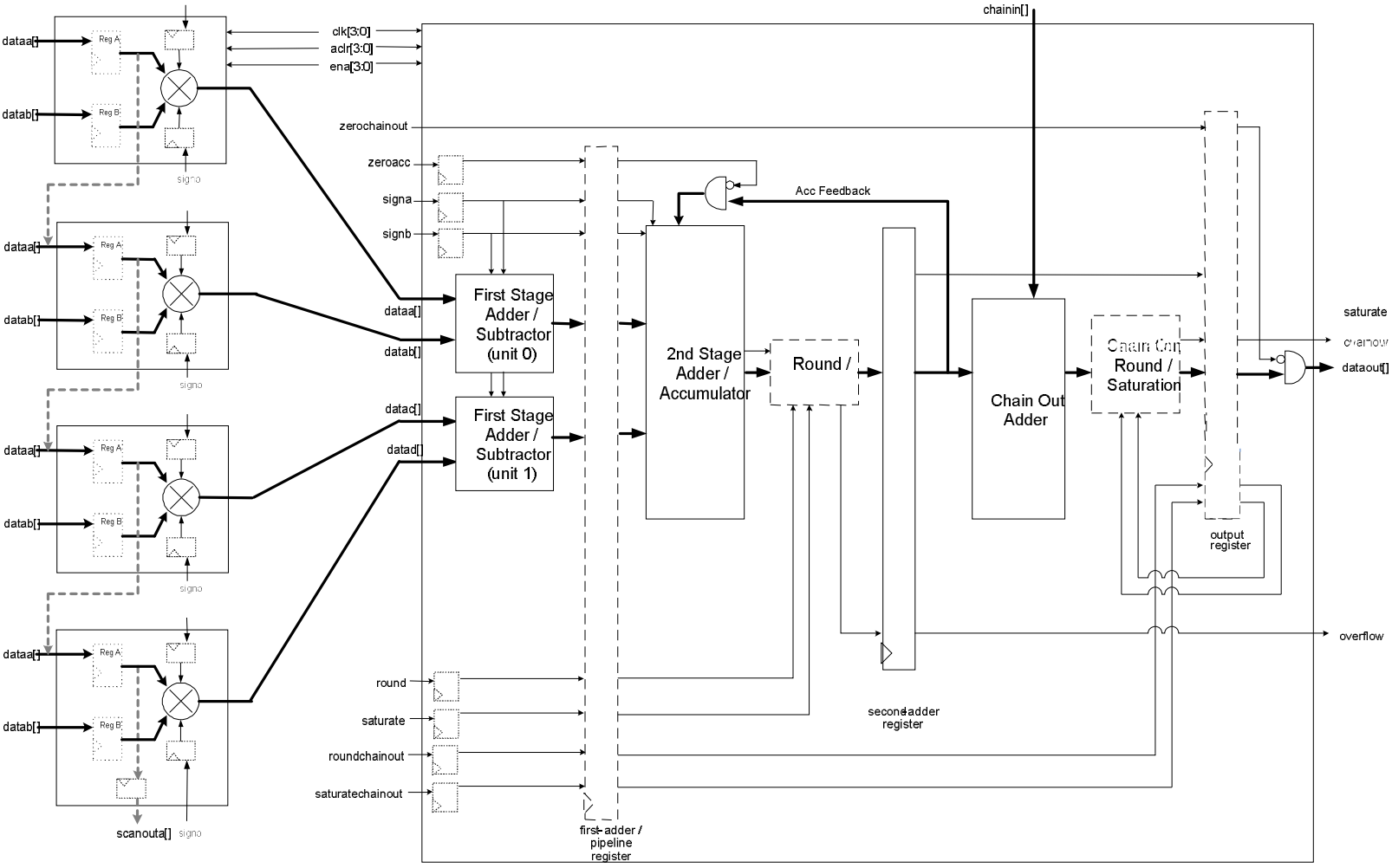


Figure 6: Multiply-Accumulator Mode

4.5 Multiply-Accumulator Chainout Mode



Note: Round must be connected to GND to avoid corrupting the data going into the chain out adder.
Round_chain_out must be connected to GND for the same reason, unless it's the last MAC_OUT in the adder chain.
Saturation must be toggled on in each stage to ensure that the proper overflows are detected.
Asymmetric saturation or full-width symmetric saturation must be used to avoid corrupting the data to be passed on.
The second adder register and the output register should be registered the same to sync the data coming out of the second adder with the rounding/saturation signals.

Figure 7: Multiply Accumulator Chainout Mode

4.6 Multiply-Two-Level-Adder Mode

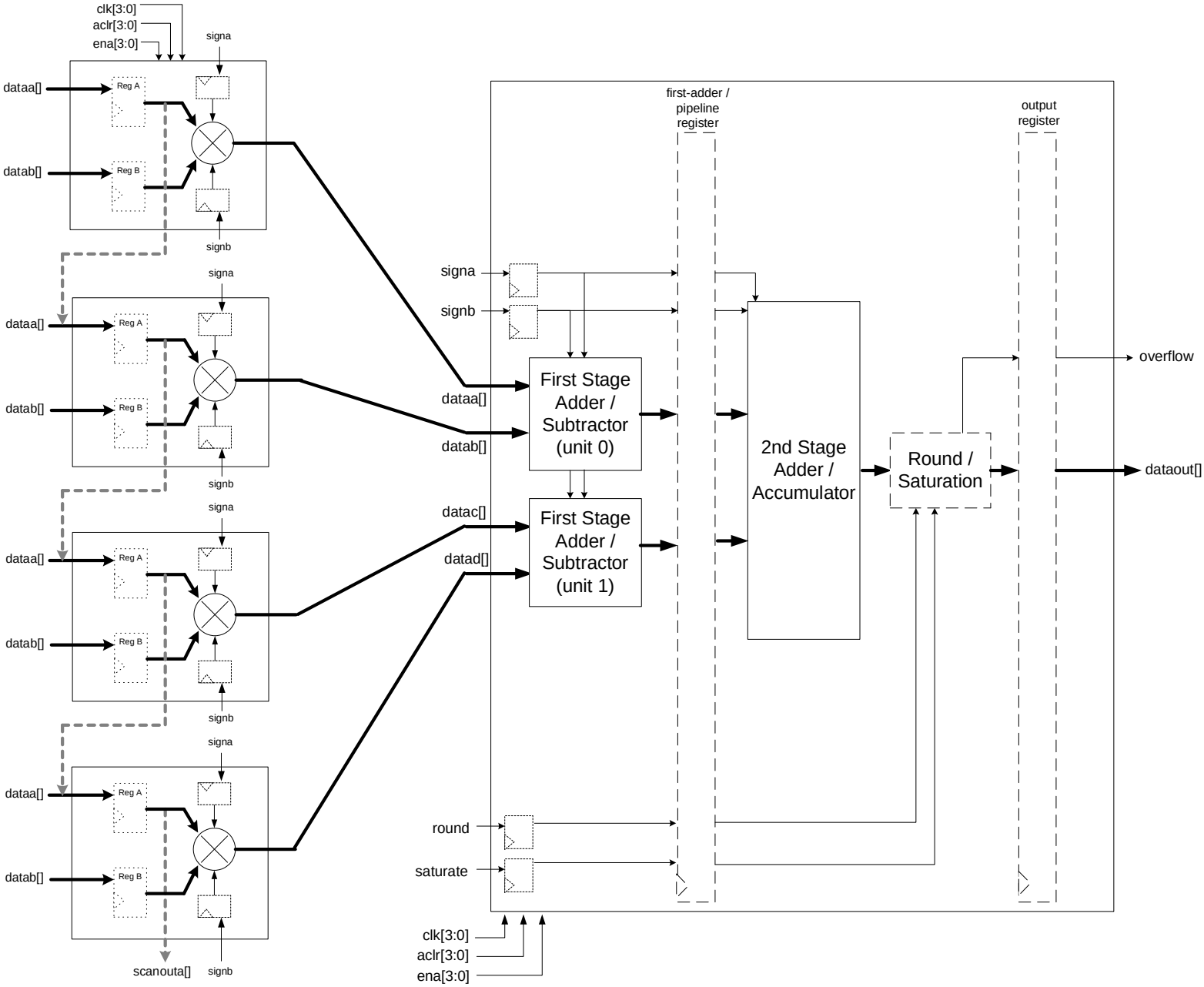
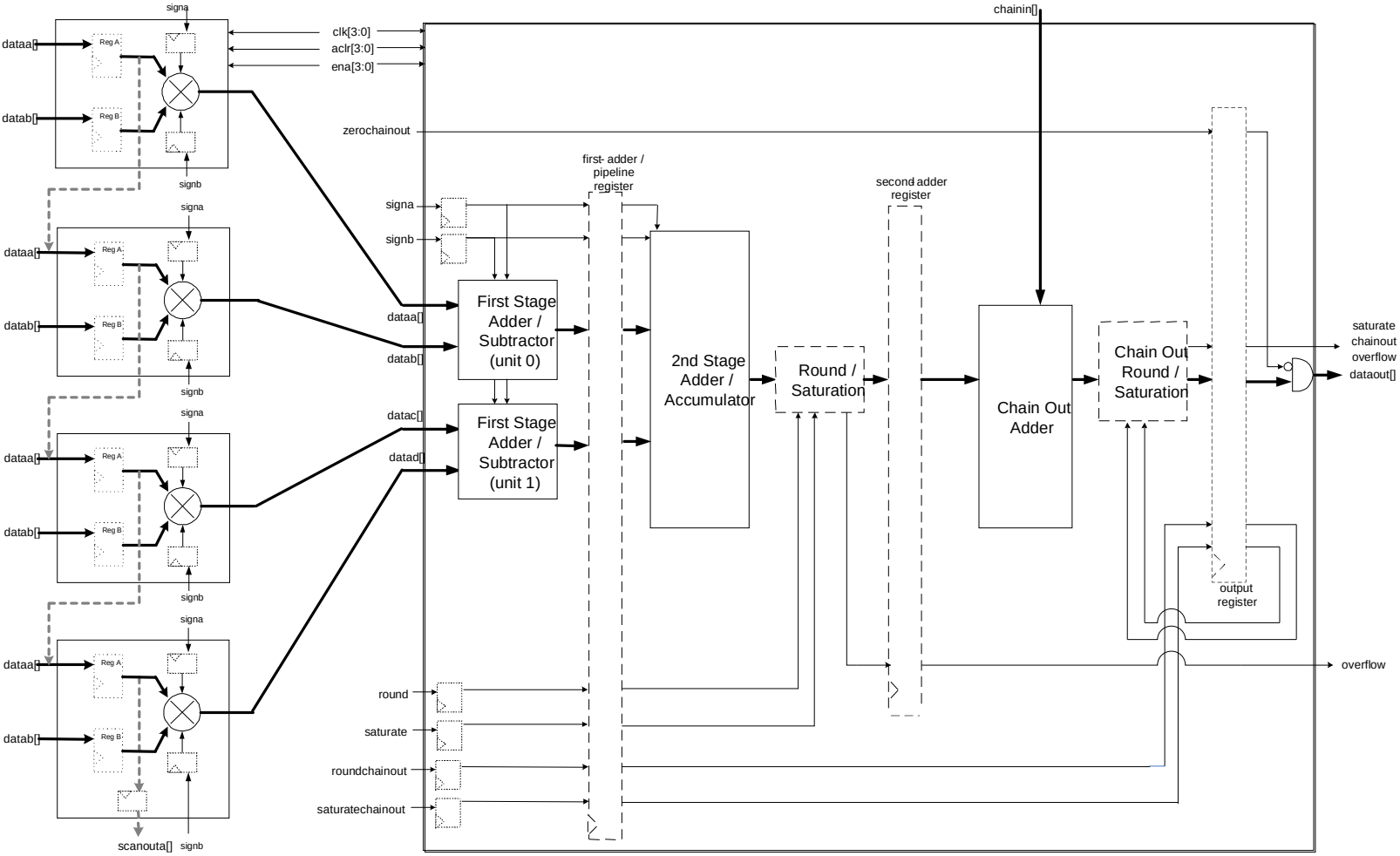


Figure 8: Multiply-Two-Level-Adder Mode

4.7 Multiply Two-Level-Adder Chainout Mode



Note: Round must be connected to GND to avoid corrupting the data going into the chain out adder.
Round_chain_out must be connected to GND for the same reason, unless it's the last MAC_OUT in the adder chain.
Saturation must be toggled on in each stage to ensure that the proper overflows are detected.
Asymmetric saturation or full-width symmetric saturation must be used to avoid corrupting the data to be passed on.
The second adder register and the output register should be registered the same to sync the data coming out of the second adder with the rounding/saturation signals.

Figure 9: Multiply Two-Level-Adder Chainout Mode

4.8 36-bit Multiplier Mode

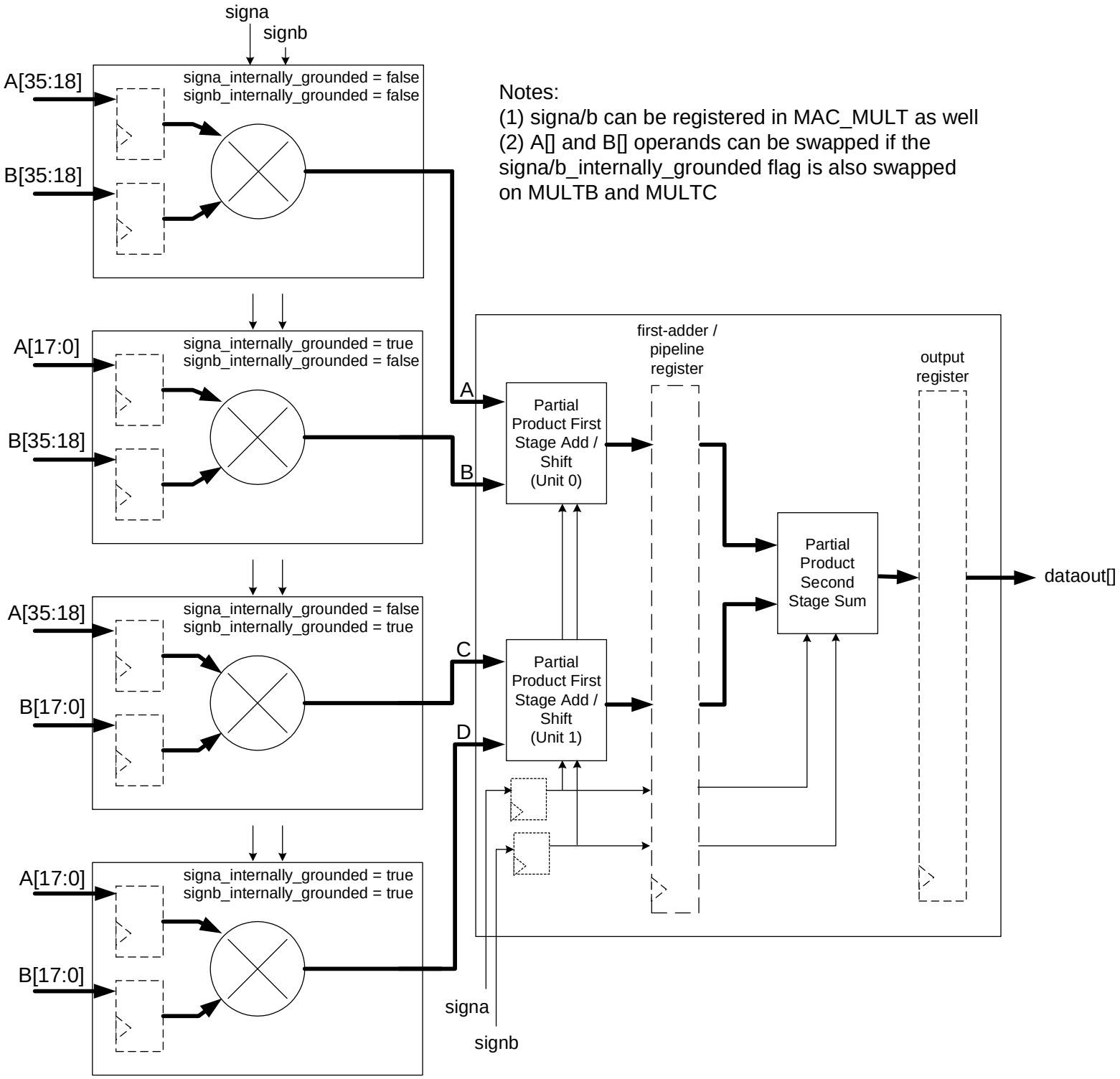


Figure 10: 36-bit Multiplier Mode

4.9 Shift Mode

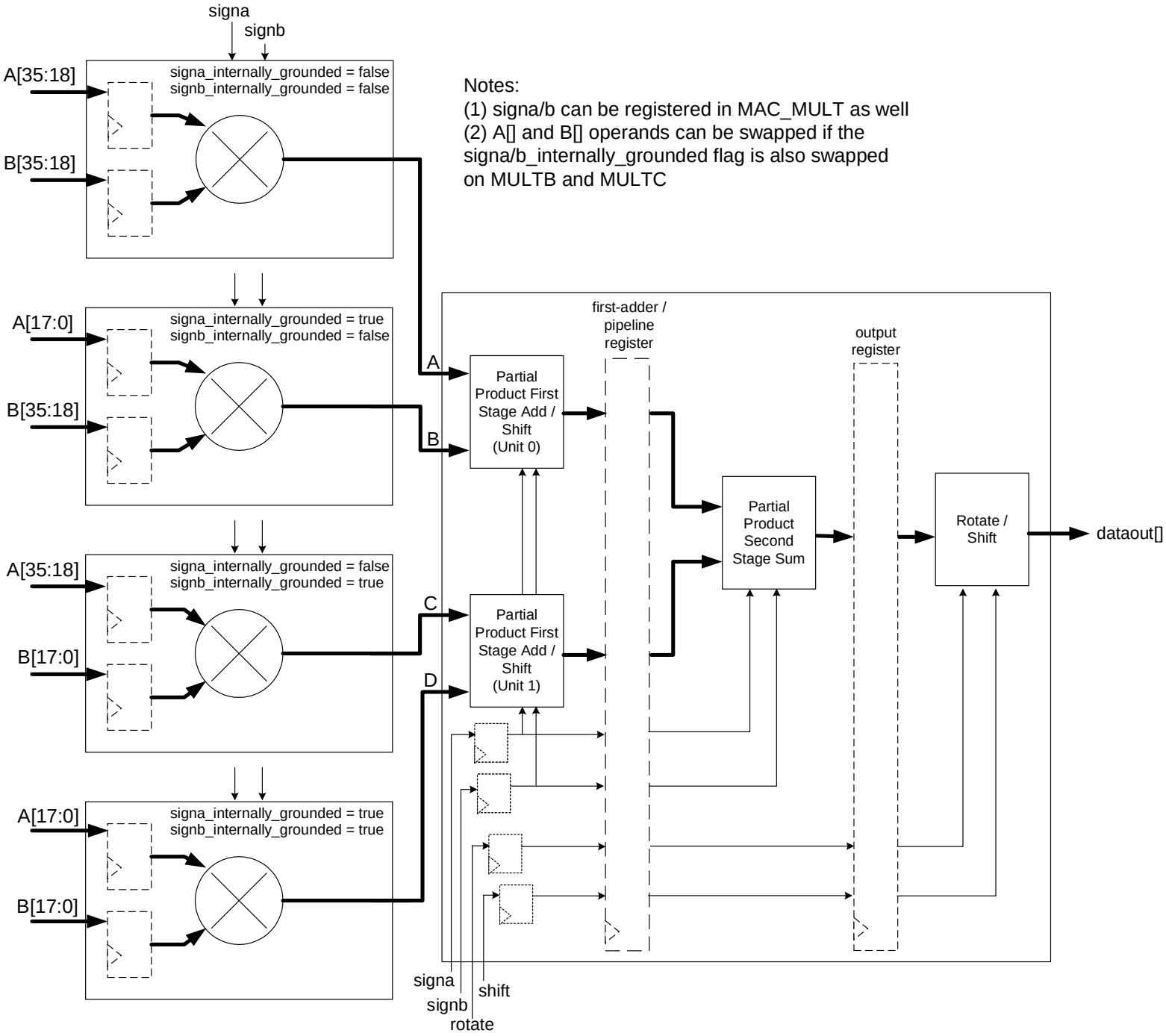


Figure 11: Shift Mode

4.10 Double Mode (Partial 54x54 Multiplier)

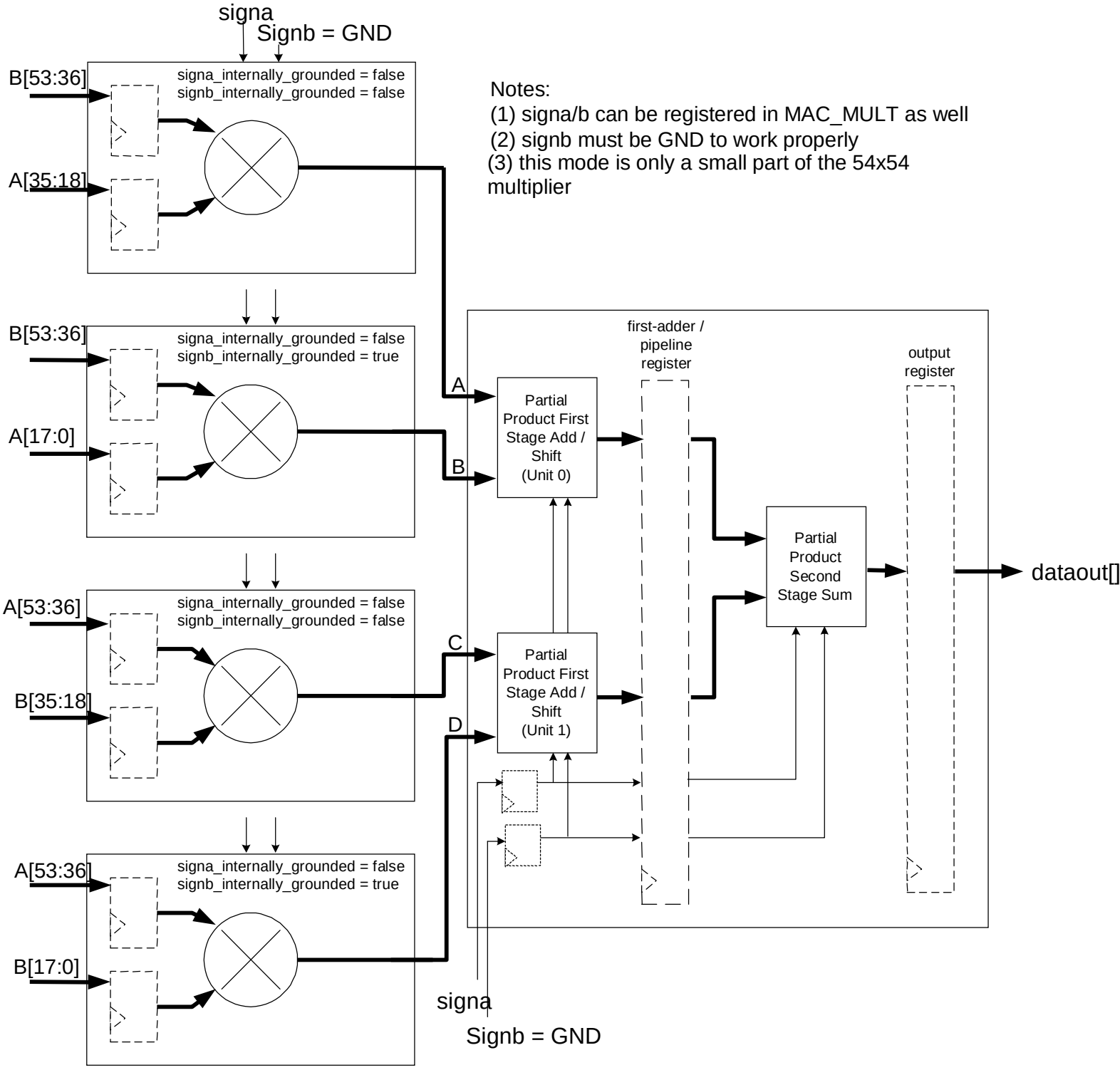


Figure 12: Double Mode

4.11 Double Mode (Complex 36x18 Multiplier – Real Part)

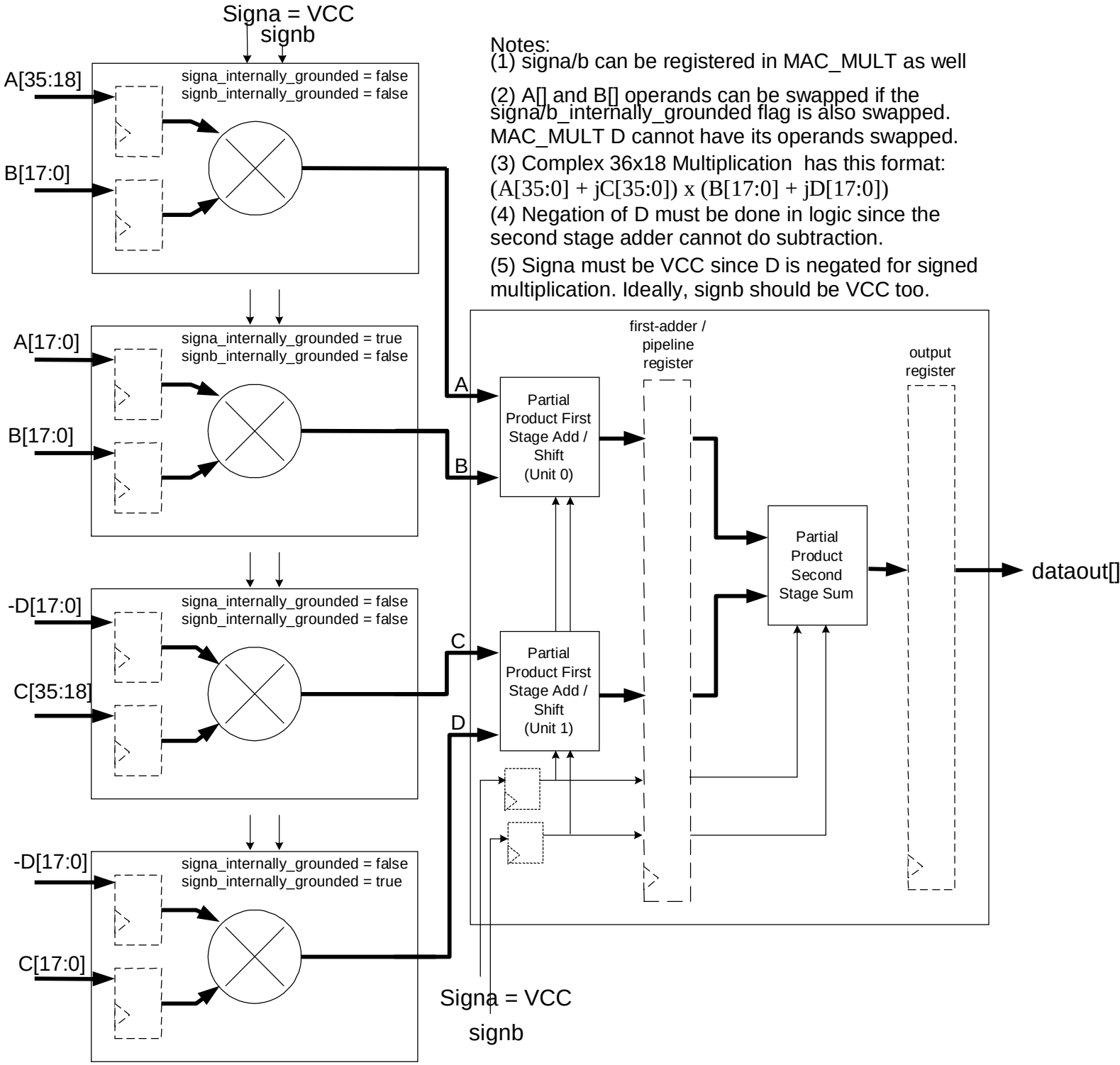


Figure 13: Double Mode for Complex 36x18 Multiplier (Real Part)

4.12 Double Mode (Complex 36x18 Multiplier – Imaginary Part)

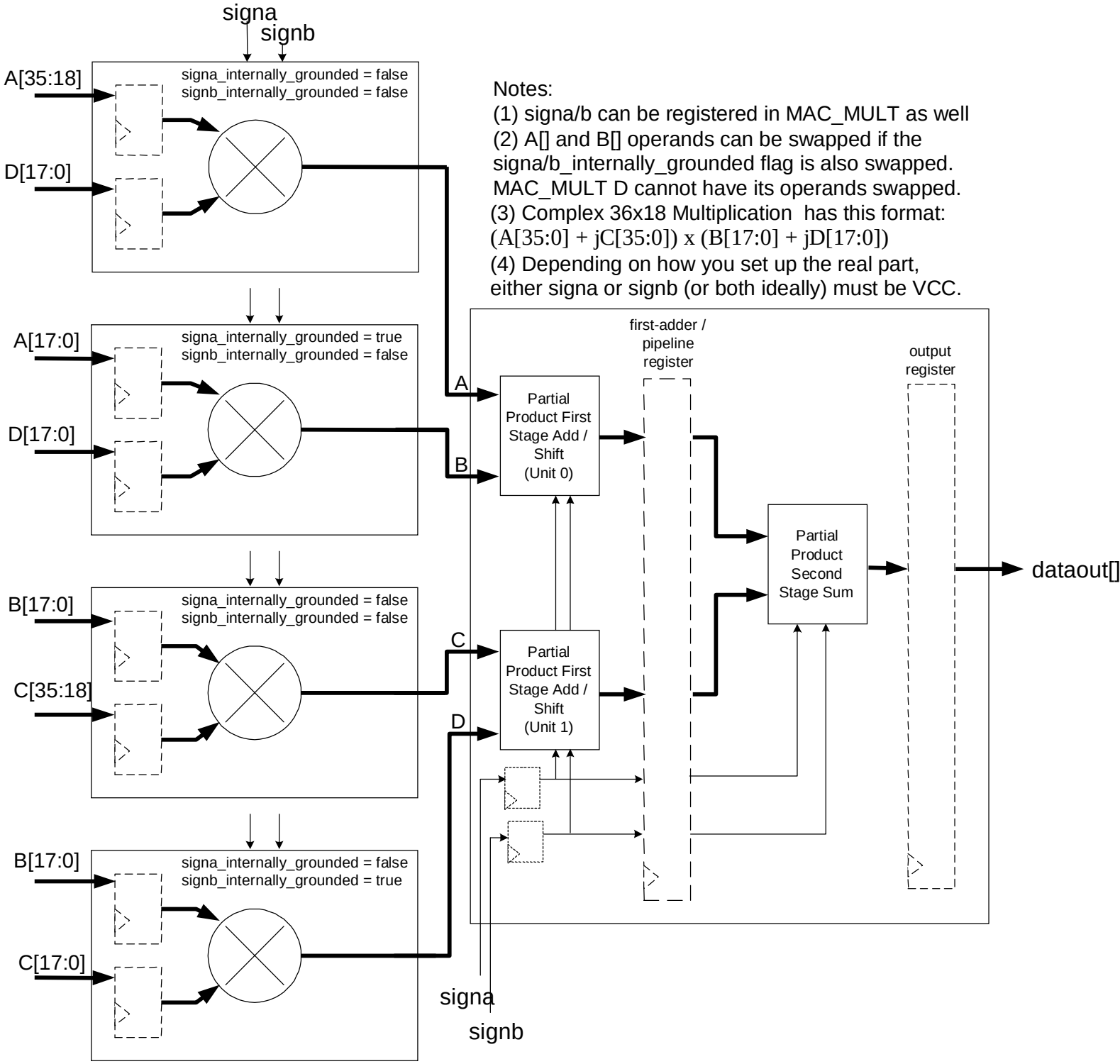


Figure 14: Double Mode for Complex 36x18 Multiplier (Imaginary Part)

4.13 Double Mode (Sum of 2 36x18 Multipliers)

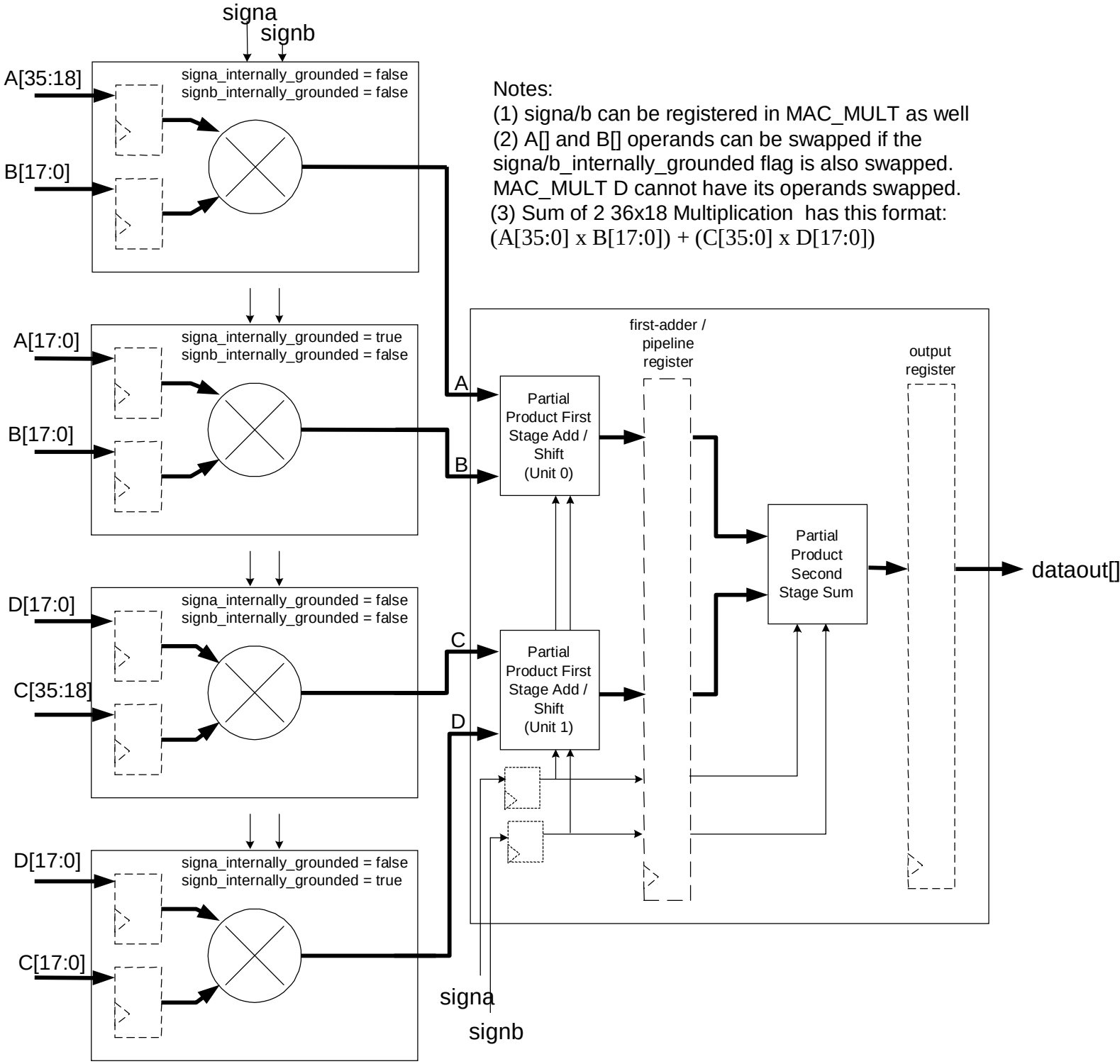


Figure 15: Double Mode for Sum of 2 36x18 Multipliers