Cyclone™ II Family Functional Description

Version 1.1

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1. Document Overview

The purpose of this document is to give a general overview of the Cyclone II family with a focus on specific differences between the Stratix® II, Cyclone and Cyclone II families. It is a brief description and it is not intended to have a detailed description of any of the features. This is intended as a starter document before reading all the other documents. Each feature will have its specific functional description in the future. Familiarity with the Stratix II and Cyclone architectures is key to understanding this document.

2. Family Overview

The Cyclone II family is the next generation low-cost FPGA. It is backwards compatible with the Cyclone family. Any design that is compiled for the Cyclone architecture can be recompiled for the Cyclone II architecture without changing the functionality of the design. The family has the following blocks: Logic Cell, M4K memory blocks, embedded multiplier (MULT) blocks, which are a strict subset of Stratix II DSP blocks, I/O cells without DDIO capabilities, CLKCTRL blocks and PLLs. The I/O cell is identical to the one in the Cyclone family. The M4K memory blocks and CLKCTRL blocks are identical to the ones in the Stratix II architecture. The PLL is based on the Stratix II Fast PLL, but is not a subset or superset. The biggest change from the Cyclone family is the LAB, the Logic Element and the PLLs.

3. Cyclone II Routing Structure

The Cyclone II architecture has R4/C4 and R24/C16 routing architecture with reduced number of wires compared to the Stratix II architecture.

Cyclone II devices have 8 or 16 global clock networks with 2 or 4 PLLs, while Cyclone devices have one or two PLLs and 8 global clock networks.

The DQS memory interface is implemented very similarly to the Cyclone interface, with dedicated DQS pins, which feature programmable delays and can drive the global clock networks.

4. Coordinate System and Floorplan

The Cyclone II floorplan is very similar to the Cyclone floorplan. It is a flat X, Y grid of blocks. A block is an I/O block, M4K memory block, LAB, MULT block, PLL or a configuration related interface. The coordinate system for Cyclone II devices is also derived from Stratix devices. The origin of all blocks and coordinates is the bottom left hand corner of the block. It is all based on an (X,Y) grid of LABs with the origin in the bottom left hand corner of the device. It is a pure mathematical based grid system with the (0,0) origin in the corner. Some blocks (e.g. the PLL) are more than 1 LAB wide or 1 LAB long. Figure 1 below shows an example floorplan of a Cyclone II device. This is just for illustrative purposes and does not represent a particular device.

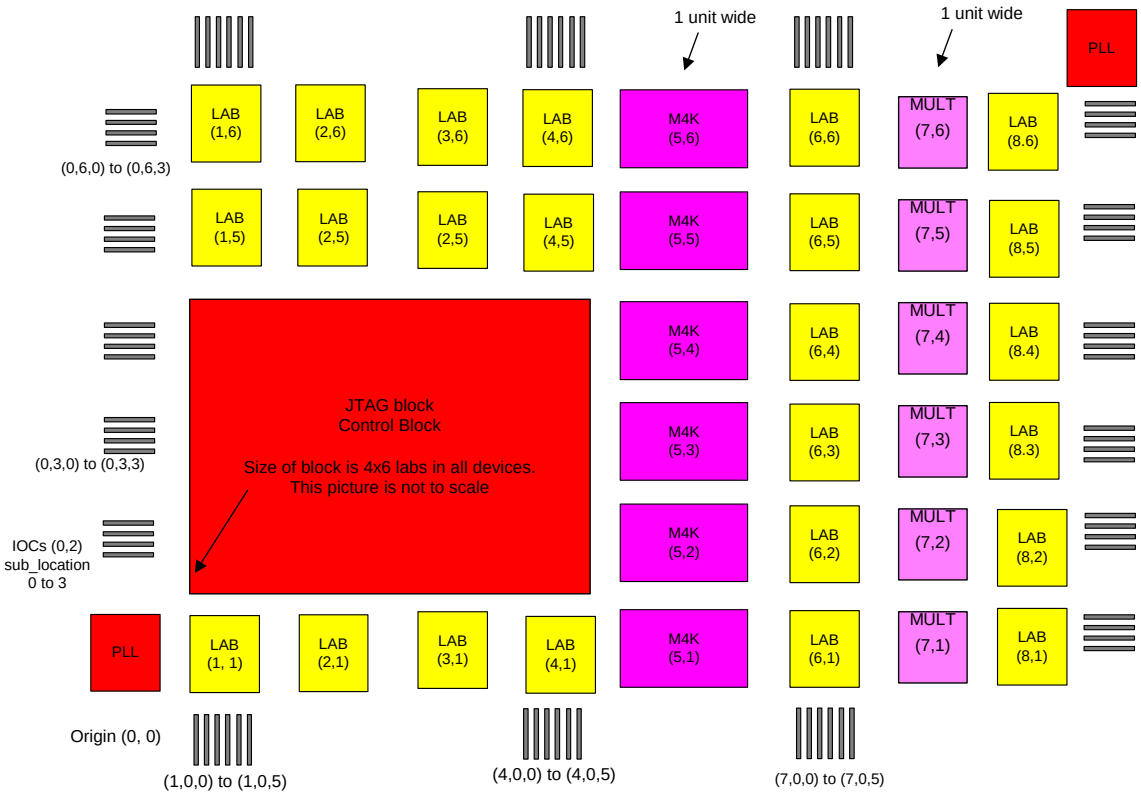

Figure 1 Floorplan and Coordinate System

4.1 LAB Details

The LAB in Cyclone II devices is completely different than the LAB in Cyclone devices. It consists of 16 LE_COMB blocks and 16 LE_FF blocks. LE_COMB blocks are 1 combinational element each while LE_FF blocks are 1 flipflop (register) element each. Each group of 1 LE_COMBs and 1 LE_FFs are organized into 1 LE (Cyclone II LE). Thus, each LAB has 16 LEs. Even numbered sub-locations (indices) in the LAB are combinational elements (LE_COMBs) while odd numbered sub-locations are registered (LE_FFs) elements. For details of the content of LE_FF and LE_COMB elements, please refer to the Cyclone II WYSIWYG document. Figure 2 shows the coordinate system for the cells inside a LAB.

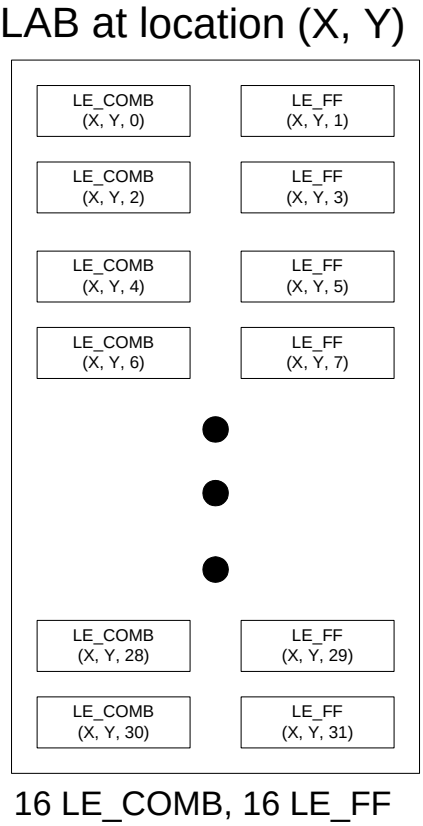

Figure 2 LAB Coordinate System

4.2 MULT Block Details

A MULT block is 1 LABs wide by 1 LABs long. Each MULT block consists of 2 embedded multiplier blocks and 1 MULT output block. The (X,Y) coordinates of the embedded multipliers follow the LAB numbering scheme and an index to decide if it is the first or the second in that LAB row. For details of the contents of each block please refer to the MULT block functional description. Figure 3 shows the coordinates for a MULT block.

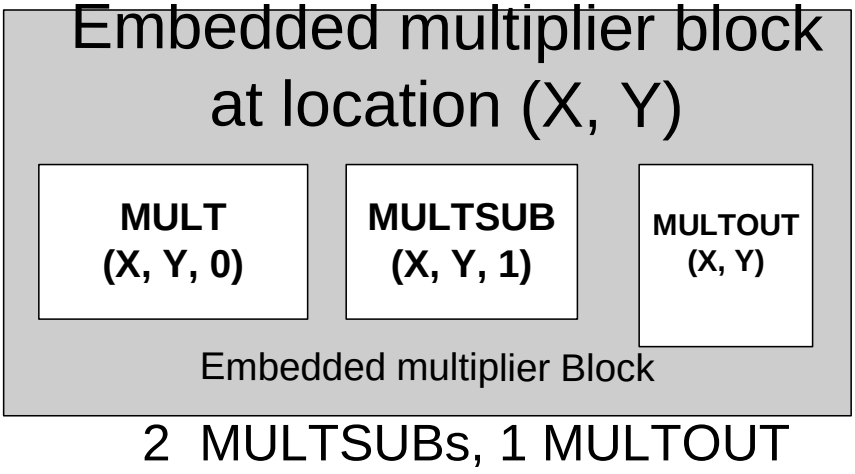

Figure 3. Embedded Multiplier Block Coordinate Details

4.3 Assignment Strings

The following are examples of location strings for objects in a Cyclone II floorplan.

LAB_X1_Y4 is a LAB block at location (1,4)

MULTSUB_X24_Y2_N1 is the second Embedded Multiplier block at location (24,2). You do know where the MULT block coordinates are with just this coordinate as the block is just one row long. The MULTOUT block has the same coordinates as the MULT block.

IOC_X0_Y3_N1 is the second pin in IO block whose bottom left corner is location (0,3)

To identify a block, you need the coordinate of the bottom left hand corner of the block. To identify an element inside the block, you need the sub-location (or index) within a block. The format of a location in Cyclone II devices is always:
<Location Name>_X<X coordinate>_Y<Y coordinate> or

<Location Name>_X<X coordinate>_Y<Y coordinate>_N<Sub-location>

PLLs and CLKCTRLs support special assignments of the kind PLL_1, PLL_2, CLKCTRL_0, etc., which the Quartus® II software internally translates to the X Y location.

5. Family Plan

Having described at a very high-level the blocks of the Cyclone II architecture, we are ready to define the family plan.

Table 1 Cyclone II Family Plan

Final

	LE	RAM	Embedded Memory	I/O	CLK	PLL
2C5	4,608	26	13	144	8	2
2C8	8,256	36	18	176	8	2
2C20	18,752	52	26	304	16	4
2C35	33,216	105	35	470	16	4
2C50	50,528	129	86	444	16	4
2C70	68416	250	150	614	16	4

The pin count is the maximum I/O count which may not be achieved in all of the packages

6. Device Packages

See the EDA toolkit for the exact device ordering codes.

7. Extra Terminology and Reading Order

We have made every effort to get a consistent naming convention between all the documents. LE_COMB and LCELL_COMB refer to the exact same element or block. Similarly, LE_FF and LCELL_FF are the same.

In some cases, due to translation from internal engineering terminology, we refer to the LE_COMB as the BLE_COMB or the LE_FF as BLE_FF. BLE stands for Basic LE. This terminology is incorrect and should not be used.

The documents should be read in the following order:

1) Cyclone II Family FD
2) Lcell WYSIWYG Description for the Cyclone II Architecture
3) MULT WYSIWYG Descripton for the Cyclone II Architecture
4) Cyclone II EDA Functional Description

8. Conclusion

This is a very high-level document to get people started on the Cyclone II architecutre. This is the first document to read and then you can pick which block to learn in detail by reading the specific functional description of each block.