Cyclone™ II Memory Block EDA Functional Description

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1 Overview

This document is intended for EDA tool developers working with Cyclone II memory architecture. It is a companion to the "Cyclone II Family FD" and the "Cyclone II RAM WYSIWYG Description", and should be used in conjunction with them. This document provides information about the Cyclone II memory architecture to allow EDA vendors to infer these blocks optimally.

2 Cyclone II Memory Block Description

The Cyclone II memory block (also referred to as the RAM Block) is a block that provides storage resources. As in Cyclone family, there is only 1 type of memory block known as M4K, as in the Stratix® II architecture. It is a true dual-port RAM and can store up to 4608 (512x9) bits data. It supports various operation modes like ROM, single-port, simple dual-port and true dual-port. The following picture shows the high-level functional block of Cyclone II memory block.

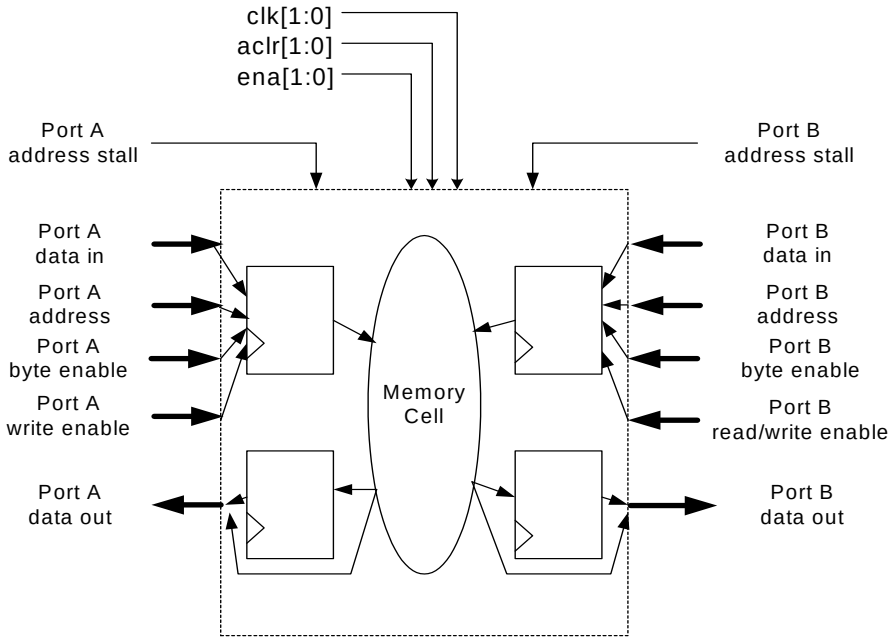


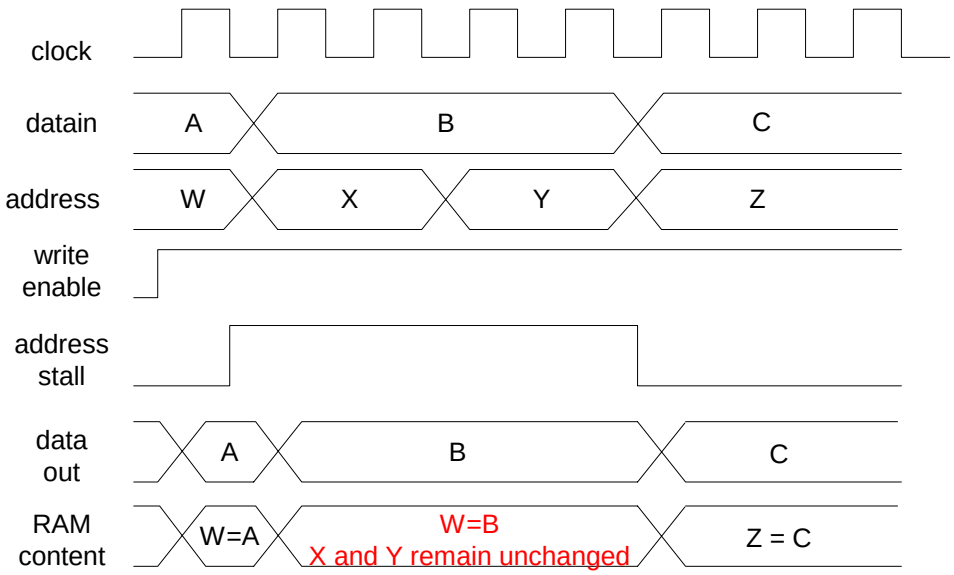
Figure 1: CycloneII RAM

From the feature aspect, it is identical to the M4K block of the Stratix II family. So it is almost a superset of the Cyclone RAM block with the exception of asynchronous clear on the input registers, which is only available in Cyclone and Stratix families. The block is optimized for cost as opposed to speed in the Stratix II device family, so it's smaller but slower.

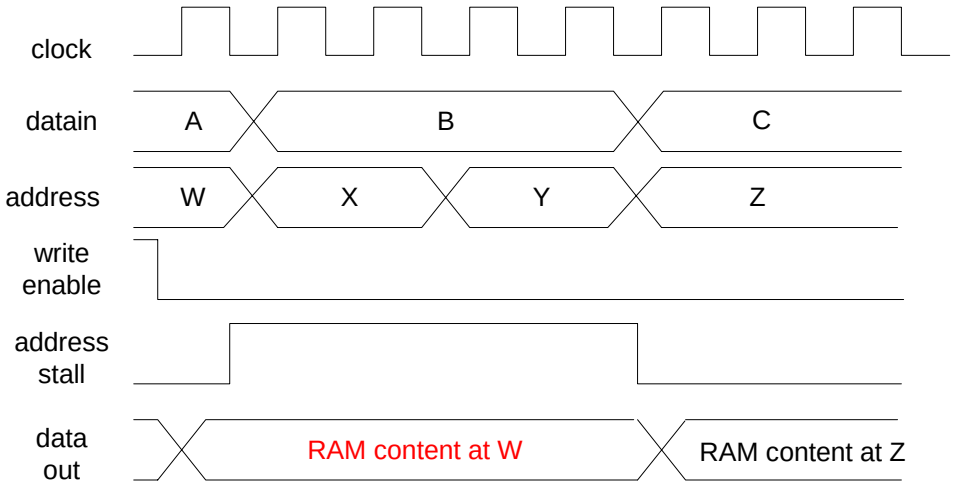
Since the Cyclone II RAM block is derived from the Stratix II M4K block, it also inherits all improvements of the M4K block as compared to the Cyclone architecture. The following describe the new functionality in the Cyclone II RAM block as compared to the Cyclone family.

2.1 Address-Stall

Address-stall feature has been added to the Cyclone II memory block. Address stall is a feature that can hold the previous address value for as long as the stall signal is enabled. This feature is added to improve the efficiency in cache-miss applications. It actually behaves like an additional clock-enable on the clock input of the address registers. The following waveforms show its behavior during a read/write cycle.



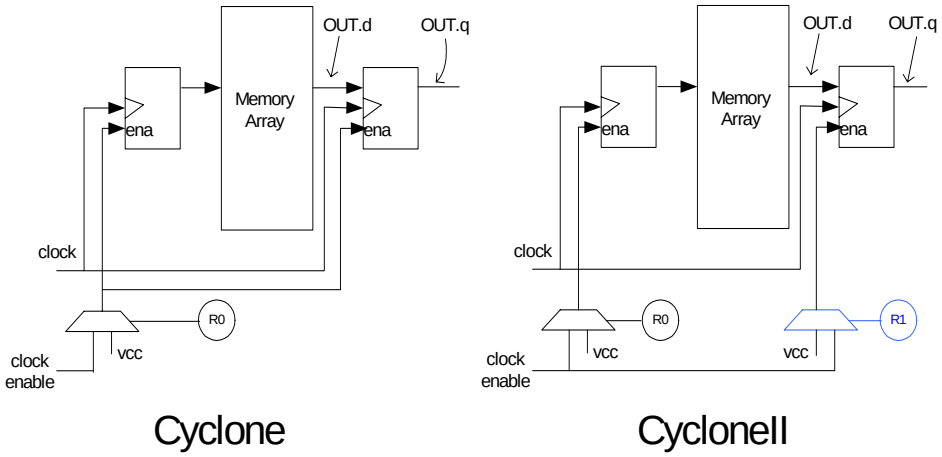
Address Stall during write cycle
assuming output is unregistered

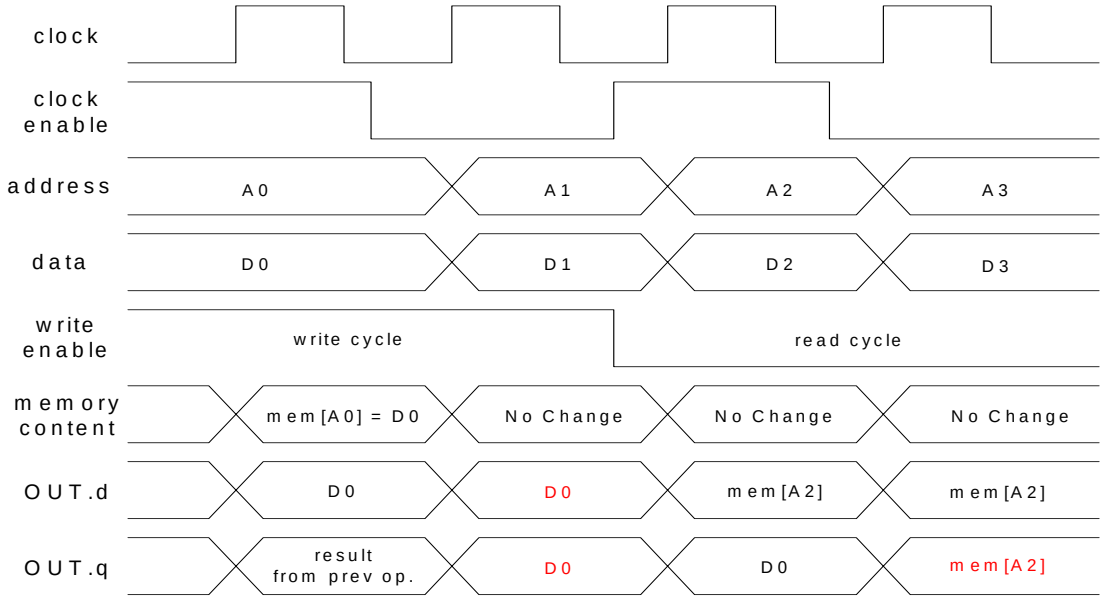


Address Stall during read cycle
assuming output is unregistered

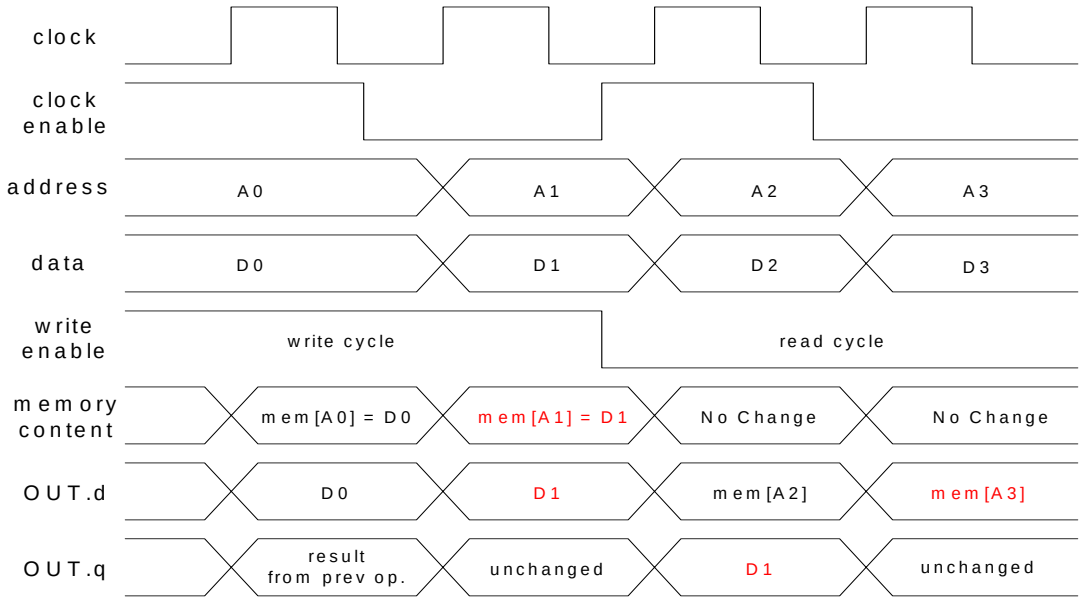
2.2 Improved clock-enable control

The Cyclone II memory blocks have more flexible clock-enable control as compared to the Cyclone memory blocks. In the Cyclone architecture, once the clock is paired with clock-enable, all registers fed by the clock will get the clock-enable. This has been causing problems in our DCFIFO (dual-clock FIFO) megafunction implementation. The DCFIFO megafunction requires two clocks, one for read and one for write. However, it also requires gating the read clock on the output registers with clock-enable while leaves the read clock not-gated on read input registers. This is something the Cyclone and Stratix hardware does not support. This incurs some area overhead on the DCFIFO implementation in the Cyclone and Stratix architectures. In the Cyclone II device family, this should no longer be a problem with the additional flexibility of independent control of clock-enable on input registers vs. output registers. The following waveforms describe the behavior in details.


OUT.d
OUT.q
Memory Array
ena
ena
clock
R0
vcc
clock enable
Cyclone
OUT.d
OUT.q
Memory Array
ena
ena
clock
R0
R1
vcc
vcc
clock enable
CycloneII



Example: Single-Port RAM with registered outputs
CLOCK_ENABE_INPUT_A = NORMAL
CLOCK_ENABLE_OUTPUT_A = BYPASS



Example: Single-Port RAM with registered outputs
port_a_disable_ce_on_input_registers = on,
port_a_disable_ce_on_output_registers = off

3 Instantiating RAM Blocks

The RAM blocks can be instantiated by either instantiating the RAM_BLOCK WYSIWYGs directly, or by instantiating RAM-related megafunctions. As with Cyclone devices, we recommend instantiating the altsyncram megafunction instead of the WYSIWYGs directly due to the complexity of RAMs.

Since the Cyclone II RAM is functionally equivalent to the Stratix II RAM, the same megafunctions used to support the Stratix II, Stratix, and Cyclone RAM blocks have been updated to support the Cyclone II RAM blocks. These megafunctions are backwards compatible with the Cyclone family. As a result, a megafunction instantiated for Cyclone RAM blocks can also be compiled for Cyclone II RAM blocks (with the exception of asynchronous clear used on input registers).

Please refer to the Stratix II Megafunction Library FD for details of the ALTSYNCRAM megafunction.

4 Inferring RAM Blocks

As in the Cyclone, Stratix, and Stratix II device families, synthesis tools can infer RAM blocks from the HDL source. Since the Cyclone II RAM block is functionally identical to the Stratix II M4K block, refer to the "Stratix II Memory Block EDA FD" for details on how to infer the RAM of each operation modes from HDL source.