PLacer Delay Model (PLDM) Specifications

Version 0.2

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1. Overview

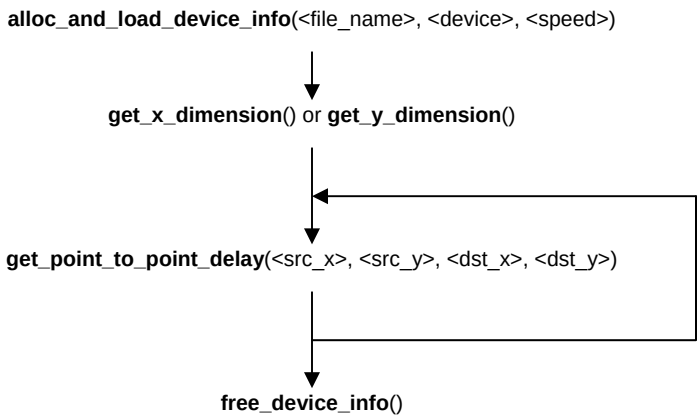
This document describes the interface that PLDM provides for 3rd party EDA vendors and academics to estimate inter-block routing delays on Altera® devices. More information can be obtained by looking at pldm_delay_estimate.[ch] found in the <DIR> directory.

PLDM enables 3rd party synthesis tools to access the Quartus® II development tool's exact placer delay model used inside the fitter. EDA tools can use the delay data when resynthesizing and optimizing the design to meet user constraints in the final place and routed design.

2. How to use PLDM

PLDM consists of two main parts, the source/reader files (<DIR>/pldm_delay_estimate.c|h) and the ASCII data files (<DIR>/family_name.ref).

This is a typical flow when using PLDM:



Note, Altera chip information must first be loaded from a file before get_point_to_point_delay() can be called. For example device EP1S10B672C7 would be loaded by calling alloc_and_load_device_info("stratix.ref", "EP1S10", "7"). Also note that the data file is package independent, but still depends on the speed grade.

2.1 Memory Usage

Memory usage is approximately 80K for an EP1S10 and 500K for an EP1S80.

2.2 Load Time

Load time for alloc_and_load_device_info() ranges from approximately 10ms for a EP1S10 and 60ms for a EP1S80.

2.3 Access Time

Access time for get_point_to_point_delay() is approximately 0ms for both a EP1S10 and a EP1S80.

2.4 Device Dimension Information

The dimensions returned are a strict upper bound on the coordinate system. The x-dimension ranges from [0, x - 1] and the y-dimension ranges from [0, y - 1], where 'x' and 'y' are the horizontal and vertical dimensions of the chip respectively. The origin of the coordinate system is the bottom left corner of the chip. These coordinates are the same as the ones used in the Quartus floorplan. For a more detailed description of the coordinate system please see the document "Altera XML Architecture Description File Detailed Design" found in the <DIR> directory.

2.5 Routing Delay Information

An estimate of the routing delay between two points <src_x, src_y> and <dst_x, dst_y> in pico seconds can be obtained from the get_point_to_point_delay function. It returns an optimistic best-case estimate for block-to-block delays. It takes into account the following:

1) Local lines used between LEs in the same LAB (ie. src_x==dst_x and src_y==dst_y), but not quick feedback or lut cascade
2) Output buffer delays at the source and input lab line delays at the destination, but not delays inside the blocks
3) Nearest neighbour connections between adjacent LABs

Delays given are estimates of the best-case route. The following are reasons why they may be inaccurate:

1) It ignores non-linear effects, which final timing signoff does properly
2) Congestion may force the router to use a slower route for the signal. There is no way of knowing which lines/wires the router will take to make a successful fit, especially in times of congestion
3) It uses LAB output buffer delays for all blocks except I/Os. This will be slightly incorrect for MACs and RAMs.
4) Assumes regular routing, which is wrong for global signals such as clock nets

Returns delay if successful and PLDM_DELAY_ERROR if any of the following should occur:

1) Device coordinates do not belong to chip (ie. negative or greater than dimensions)

It is also the caller's responsibility to ensure that the points in question are valid (ie. not an empty corner of the chip, not inside an MRAM or DSP, etc.)