# WYSIWYG Device Primitives User Guide for the MAX II Family

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# Table of Contents:

# 1. Overview

The WYSIWYG cells that are the same as MAX II will just refer the reader to that document so that they cannot get out of sync.

# 2. The MAX II Logic Cell

The MAX II logic cell is identical to Stratix. See the *WYSIWYG Device Primitives User Guide for the Stratix Family* for its description.

# 3. MAX II I/O Element

The MAX II I/O element is a subset of the Cyclone I/O, and a new atom will be created to protect the other Stratix families. The main differences are:

- There will be no I/O register related ports since there are no I/O registers
- There will be no delay chains

## 3.1 I/O Primitive

```
maxii_io <I/O name>
(
      .datain(<output source>),
      .oe(<oe source>),
      .padio(<pad I/O source/output>),

      .combout(<combinatorial output>)
);
defparam <I/O name>.operation_mode = <operation mode>;
defparam <I/O name>.open_drain_output = <open drain mode>;
defparam <I/O name>.bus_hold = <bus hold mode>;
```

## 3.2 I/O Input Ports

<*I/O name*> is the unique identifier for the I/O element. This is any identifier name which is legal for the given description language (e.g. Verilog, VHDL, AHDL, etc.). *This field is required.*

.**datain (**<*output source*>**)** is the data input to the I/O element.

**.oe(**<*oe source*>**)** is the output enable signal for the I/O element. This should not be specified when the I/O element is in "input" mode. It defaults to VCC (permanently enabled) in output mode, and it should not be specifically set to VCC.

## 3.3 I/O Output Ports

**.combout(**<*combinational output*>**)** is the combinatorial output of the I/O element. It always feeds directly from the padio.

## 3.4 I/O Bidirectional Ports

**.padio(**<*pad I/O source/output*>**)** represents the physical pad of the I/O element. A bi-directional port, this signal should be connected directly to module inputs and outputs. Logic feeding out between these ports and the top-level module outputs is illegal.

Example 1 demonstrates how the .padio signal is used to connect up to input, output and bidir signals.

Example 1 – MAX II .padio Example

```
module foo ( input_signal, output_signal, bidir_signal )
      input input_signal;
      output output_signal;
      inout bidir_signal;
      maxii_io input_io (.padio(input_signal), ...);
            defparam input_io.operation_mode = "input";
            ...
      maxii_io bidir_io (.padio(bidir_signal), ...)
            defparam bidir_io.operation_mode = "bidir";
            ...
      maxii_io output_io (.padio(output_signal), ...)
            defparam output_io.operation_mode = "output";
            ...
end module
```

## 3.5 I/O Modes

<*operation_mode*> is one of *{input, output, bidir}*. Determines the directionality of the I/O element. *This field is required.*

<*open_drain_mode*> is one of *{true, false}*. This field is optional and defaults to *false*. This field can only be set to *true* when the I/O is in output or bidir mode but not input mode.

<*bus_hold_mode*> is one of *{true, false}*. This field is optional and defaults to *false*.

## 3.6 I/O Polarities and Default Values

Table 1 – Polarity of I/O Inputs

| *Signal* | *Polarity* | *Programmable Inversion* |
|---|---|---|
| .datain | -- | Yes |
| .oe | Active high | Yes |

If not explicitly set in the device primitive instantiation, signals default to unconnected on the I/O element. Output enable will default to GND when the I/O element is in "input" mode, and VCC when it is in "output" mode. It should be left unconnected in "input" mode, and it should not be set to VCC in "output" mode.

All MAX II I/O element inputs have programmable inversion, and hence can be provided in either polarity.

## 4. MAX II JTAG Support

The MAX II architecture provides the same access to the JTAG pins and scan chain as the Stratix architecture. See the *Stratix JTAG Feature Functional Description* for more information.

## 5. MAX II User Flash Memory

There will be a separate document to describe the MAX II user flash memory.