MAX II EDA Functional Description

Version 1.1

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1. Overview

This document is intended for EDA tool developers working with the MAX II architecture. It is a companion to the *WYSIWYG Device Primitive User Guide for the MAX II Family* and should be used in conjunction with that document. This document provides information about the MAX II architecture to allow EDA vendors to synthesize designs to the architecture while avoiding fitting problems.

2. MAX II WYSIWYGs vs. Cyclone

Basically, the MAX II device contains the Cyclone logic cell, a simplified version of Cyclone I/O cell with I/O registers and delay chains removed, and the user flash memory. Compared to the Cyclone architecture:

- The MAX II logic cell is identical to the Cylcone logic cell, which in turn is as the same as the Stratix logic cell. See the *Stratix EDA Functional Description* for the legality rules governing which ports can be connected on a logic cell. The Quartus II development software considers stratix_lcell, cyclone_lcell and maxii_lcell synonyms
- The MAX II LAB is identical to the Cyclone LAB, which in turn is as the same as the Stratix LAB. See the *Stratix EDA Functional Description* for signal limit rules on carry chains that guarantee it is possible to form legal LABs from the synthesized circuit.
- The MAX II I/O has a subset of the Cyclone IO functionality. Since the MAX II I/O does not have any I/O registers, any I/O register related ports do not exist on the MAX II IO WYSIWYG. The MAX II I/O does not support any delay chains, or any differential I/O standards. The MAX II device does support the following I/O features:
    - Simple I/O standards – LVTTL/LVCMOS at 3.3, 2.5, 1.8, and 1.5V; 3.3V PCI
    - Drive strength – high/low
    - Slew rate – slow/fast
    - Bus hold
    - Weak pull up
    - Open Drain
- The user flash memory is the only new block for Max II. Please refer to the *User Non-Volatile Memory WYSIWYG Description for the MAX II Familyi* for details on that block. Only black box support is required for UNVM, which means that 3rd party synthesis does not need to infer this block. The following rules should be obeyed by synthesis tools for the user flash memory:
    - The **.drdin** port is not required, but must be connected when the signal at **.drshft** port is high
    - The **.drdclk** port must be connected
    - The **.drshft** port must be connected
    - The **.ardin** port must be connected
    - The **.ardclk** port must be connected
    - The **.arshft** port must be connected

  - The **.oscena** port must be connected when the **.osc** output port is used
  - The **.drdout** port must be connected
  - The parameter **address_width** can have one of the following values: 7, 8, or 9
- The MAX II device does not have any DSP blocks. Consequently, synthesis must not generate any MAC_MULT or MAC_OUT WYSIWYGs when targeting the MAX II family. Instantiating lpm_mult blocks is fine, so long as DEDICATED_MULTIPLIER_CIRCUITRY=YES is not set in the lpm instantiation – the multiplier will be built out of logic cells. The altmult_accum and altmult_add megafunctions cannot be used with MAX II devices, since they currently do not support logic cell based implementations.
- The MAX II device does not have any RAM blocks.
- The MAX II device does not support any PLL blocks.

Synthesis output targeted to Cyclone will be accepted and compiled by the Quartus II software, provided the netlist does not try to use features not present in the MAX II architecture.

3. The MAX II Routing Structure and Delays

The MAX II device has a segmented routing structure which, at a high-level, is similar to that of Cyclone devices. Consequently, the rules for floorplanning designs for Cyclone devices largely hold true for MAX II as well. Manhattan distance is still a reasonable predictor of routing delay.

Each horizontal routing channel in a MAX II device contains 64 R4 lines that span four LABs horizontally. Similarly, each vertical channel contains 56 C4 lines that span 4 LABs vertically. The R4 and C4 lines can be driven by logic cell (LE) outputs and each other, and can drive LAB lines (which connect to LE inputs) and other R4 and C4 lines.

There is only one new type of connection in the MAX II architecture. In addition to the R4 and C4 lines mentioned above, each MAX II I/O cell has a *bypass path* connection directly from the logic cells in the adjacent LAB. This connection is added to improve T_{PD} and T_{CO} timing.

The speed of connections in MAX II devices, from fastest to slowest is:

- Source and destination in the same LAB
  - A connection from the combinational output of a logic cell to the **.datad** input of the logic cell immediately below it (and in the same LAB) is made via the *LUT cascade* and is extra-fast. So there is a very fast path from **.combout** of LE #0 to the **.datad** of LE #1 and so on. The fitter will automatically try to exploit this extra-fast connections
  - Other connections within the LAB are made with local lines. The delay of a local line is approximately 2x that of the LUT cascade.
- Destination in the LAB immediately to the left or right of the source. These connections are made via an LE to LAB line connection. The delay is approximately 1.5x that of a local line connection.
- Delay for larger distances is proportional to the Manhattan distance between the source and destination. Ceil (manhattan_distance/4) is a good estimate of the number of routing wires that will be used.

4. Coordinate System and Location Assignments

The MAX II devices use the same coordinate system and location assignment strings as Cyclone devices, which in turn is the same as Stratix devices. See the *Stratix EDA Functional Description* for the details of this coordinate system and assignment strings.

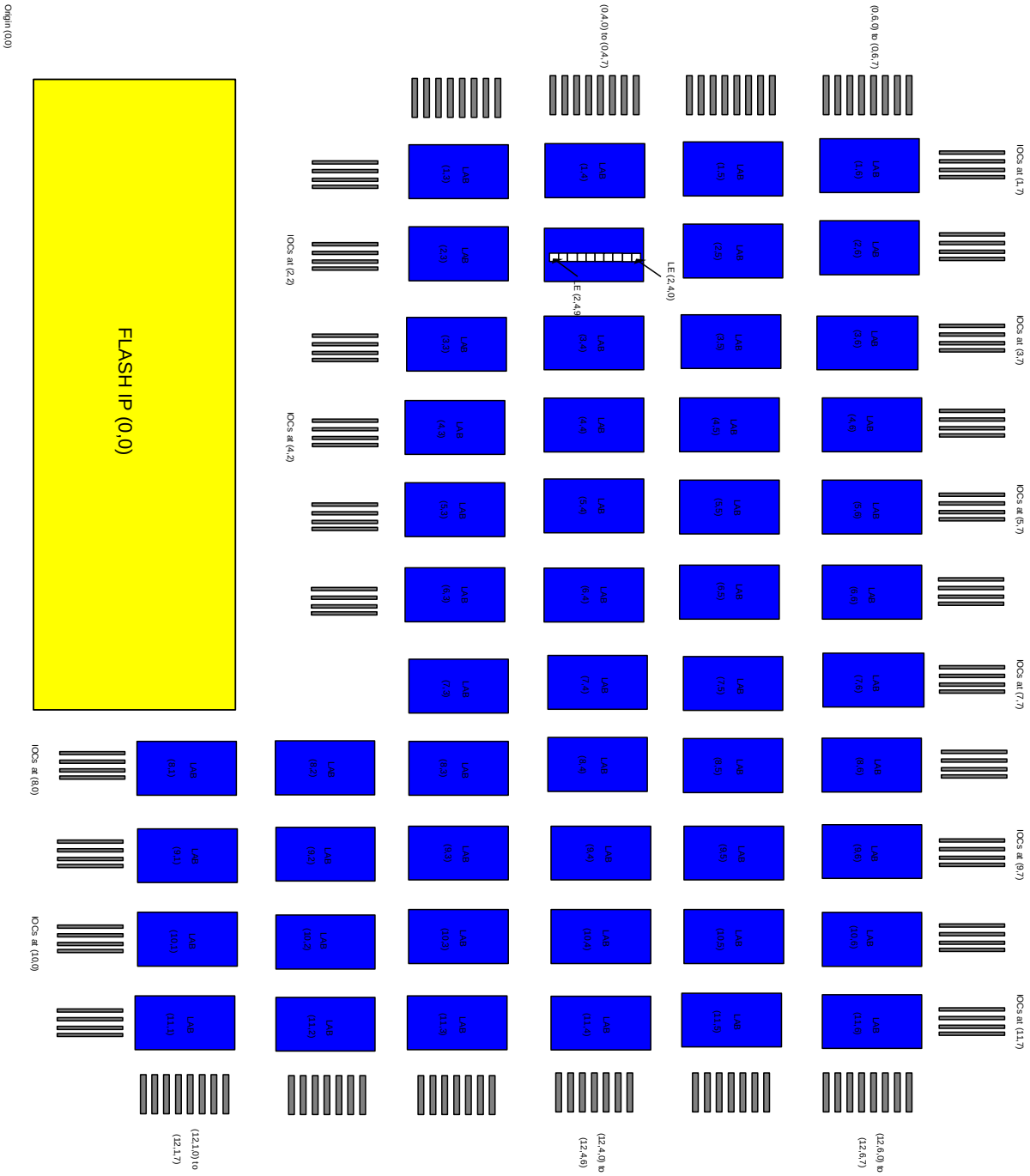

Figure 1: MAX II Coordinate System.