Stratix DLL WYSIWYG Description

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Table of Contents:

1 Overview

This describes the new Stratix DLL (Delay Locked Loop) WYSIWYG and a new input port on the Stratix I/O WYSIWYG. These components are required to correctly register data inputs when reading from DDR SDRAM.

Normally when reading from DDR SDRAM, a DQS clock is sent edge-aligned with the DQ data input. To register the data at the optimum time, the clock must be phase shifted to center-align with the data (usually a shift of 72° or 90°). The DLL circuit uses a reference clock at the same frequency as the input DQS clocks to compute the amount of delay required at each DQS pin to perform the phase shift. The DLL feeds the required delay to its connected DQS I/Os.

2 Delay Locked Loop Representation

The DLL (delay locked loop) represents the specialized phase shift reference circuit for controlling the phase shifting of the DQS clocks used to register the DQ inputs. Currently, each device in the family has two DLLs – one for the top edge DQS pins and one for the bottom edge DQS pins. This is a change from the current method of specifying the circuit via ESF assignments to the DQS pins (on the variables DQS_SHIFT, DQS_FREQUENCY, DQS_SYSTEM_CLOCK). Note that the ESF variables will remain for backward compatibility.

2.1 DLL Primitive

```
stratix_dll <dll_name>
(
        .clk(<input port>),

        .delayctrlout(<output port>)
);
defparam <dll_name>.input_frequency = <frequency of the clk input>;
defparam <dll_name>.phase_shift = <desired phase shift>;
defparam <dll_name>.sim_valid_lock = <number of half-cycles needed
      to lock>;
defparam <dll_name>.sim_invalid_lock = <number of half-cycles to
      keep lock>;
```

2.2 DLL Input Signals

<*dll name*>**:** is the unique identifier for the delay locked loop. This is any identifier name which is legal for the given description language (e.g. Verilog, VHDL, AHDL, etc.). *This field is required.*

.clk(<*input port*>**)** is the reference clock matching in frequency to the DQS clock used to determine the delay required to perform the phase shift. This input is required.

2.3 DLL Output Signals

.delayctrlout(<*output port*>**)** is the control signal used by all the DQS pins fed by this DLL to delay their input clock by the amount specified in the phase_shift parameter. This is, in affect, a lock signal. Note that this signal can only feed the delayctrlin input of DQS pins.

2.4 DLL Modes

<*phase_shift*> is one of *{0, 72, 90}*. Determines the phase shift applied to the DQS clocks. *This field is required.*

<*input_frequency*> is the frequency of the clock connected to the clk input port. This parameter should be checked to ensure it falls within a legal range. This parameter is only used for simulation.

<*sim_valid_lock*> is the number of half-cycles needed from the clk input before the DLL locks onto the signal. This parameter is included so that the user doesn't have to add simulation vectors for the actual number of half-cycles needed for a lock (512 in Stratix). The default value is 1 (same as for the PLL). This parameter is only used for simulation.

<*sim_invalid_lock*> is the number of half-cycles on the clk input that the DLL can keep a lock. The default value is 5 (same as for the PLL). This parameter is only used for simulation.

3 Updated I/O Representation

The I/O atom is the basically the same as before, but with an added delay control input port so that DQS pins can read the phase shift delay from the DLL and perform the phase shift locally within the I/O.

3.1 Updated I/O Primitive

```
stratix_io <I/O name>
(
        {same original ports},
        .delayctrlin(<input port]>),
        .dqsundelayedout(<combinational output(only when DQS I/O)>)
);
{same original parameters}…
defparam <I/O name>.sim_dll_phase_shift = <phase from the DLL>;
defparam <I/O name>. sim_dqs_input_frequency = <input frequency>;
```

3.2 New I/O Input Signal

.delayctrlin(<*input port*>**)** can only be fed by the DLL delayctrlout port to delay the incoming signal by the amount specified in the DLL's phase_shift. This port is optional. If unconnected, the DLL will not control the input delay on this pin. This port is only valid on DQS pins.

.dqsundelayedout(<combinational output (only when DQS I/O)>**)** is the combinational output of the I/O element. It can only be used when the I/O element is a DQS I/O. It provides the combinational output without the DQS phase-shift.

3.3 New I/O Modes

<*dll_phase_shift*> should be copied from the phase_shift parameter of the DLL connected to the delayctrlin port. . This parameter is only used for simulation. Valid values are {0, 72, 90, unused}.

<*input_frequency*> should be the frequency of the DQS input. This should either match the input_frequency of the DLL connected to the delayctrlin port, or be set to unused if the port is unconnected. This parameter is only used for simulation.

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