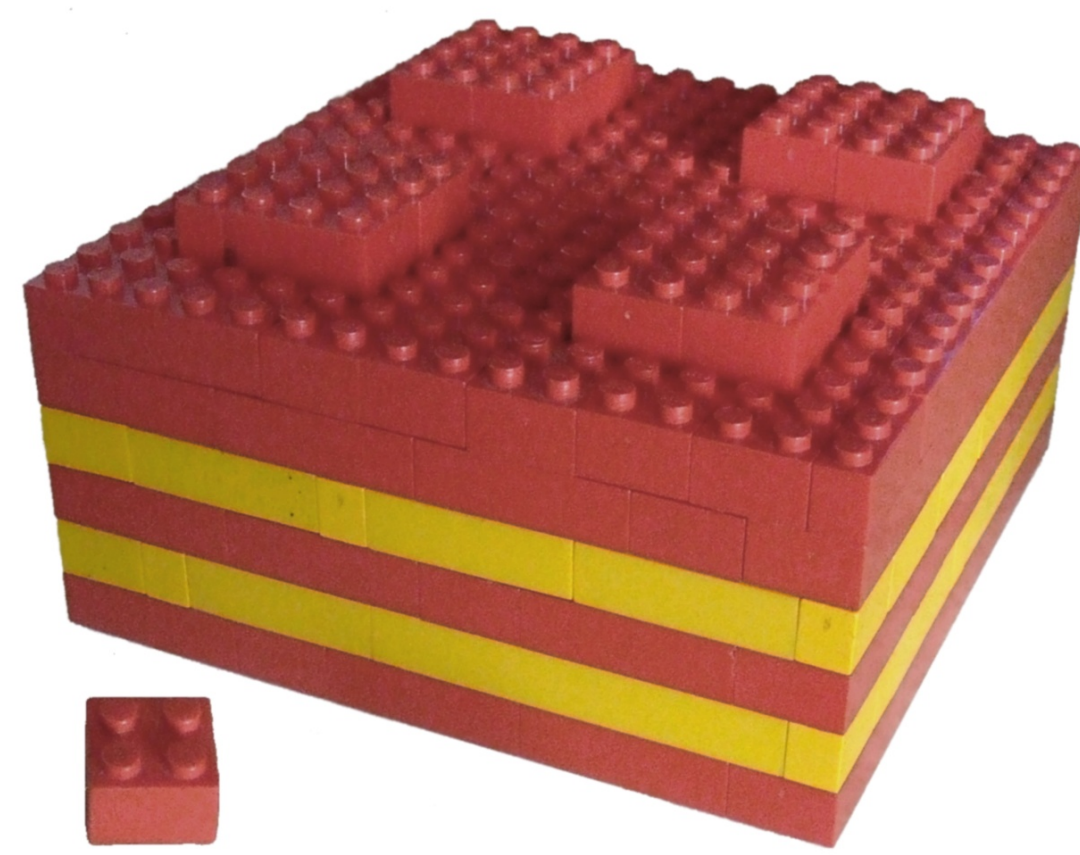


## Goal:

To implement an FPGA on an FPGA.

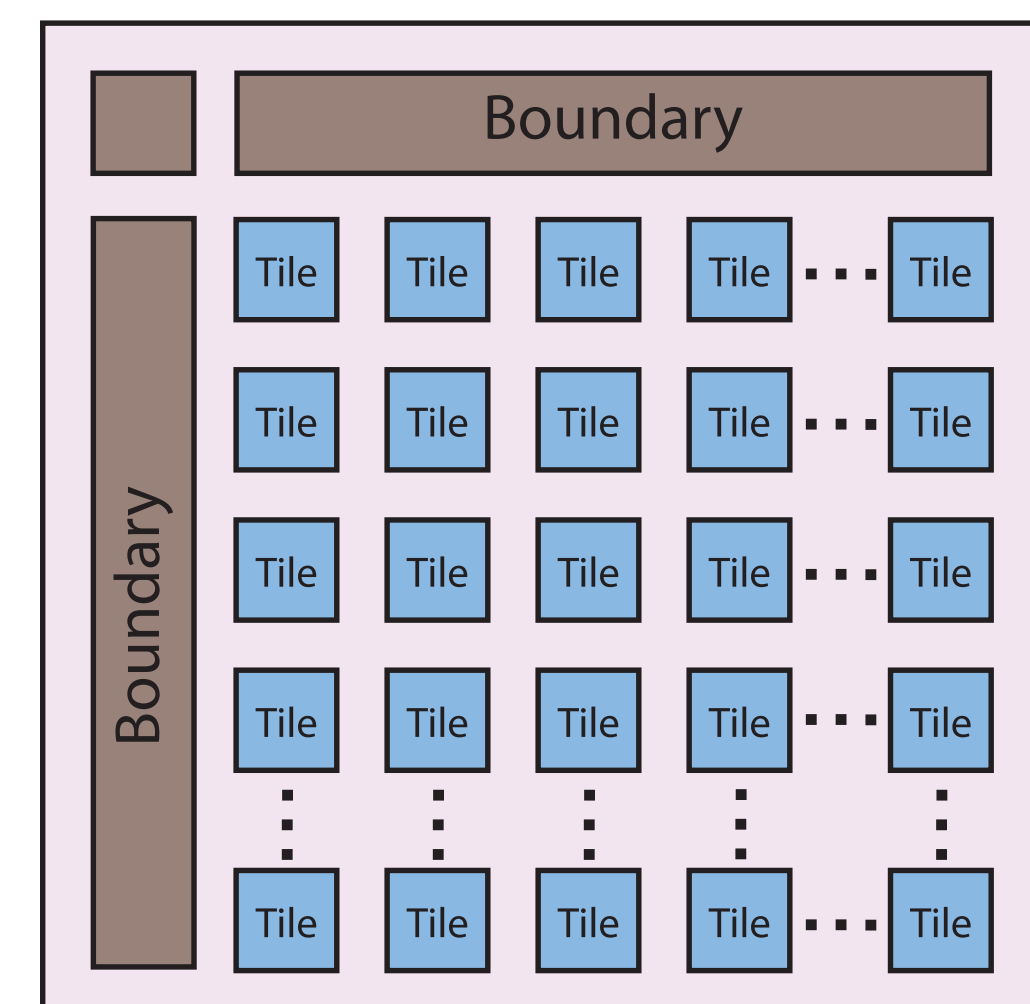


*It's like building a lego block out of lego!*

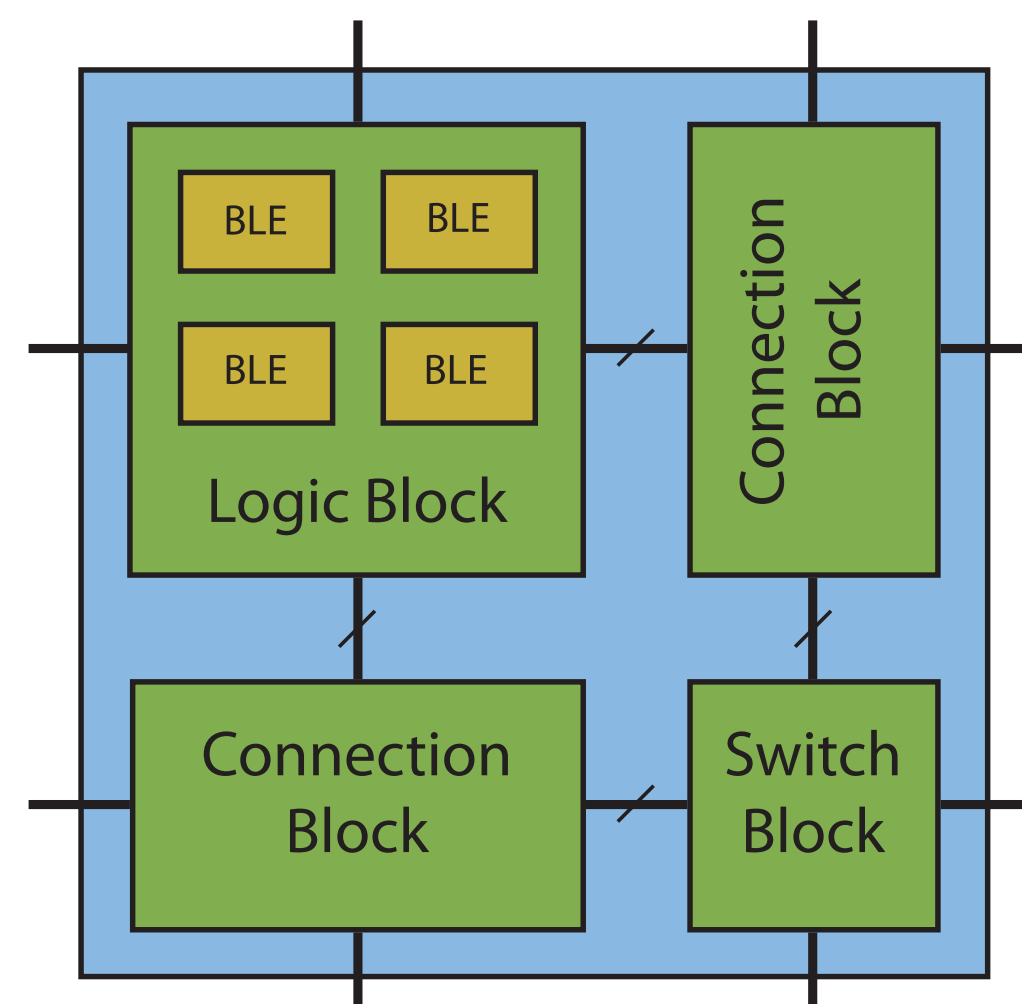
## Why bother?

- Build FPGA prototypes to test new designs
- Abstraction layer for bitstream compatibility
- Works with open-source FPGA tools like VPR
- Can now test output from VPR in hardware

## Overlay FPGA Hierarchy

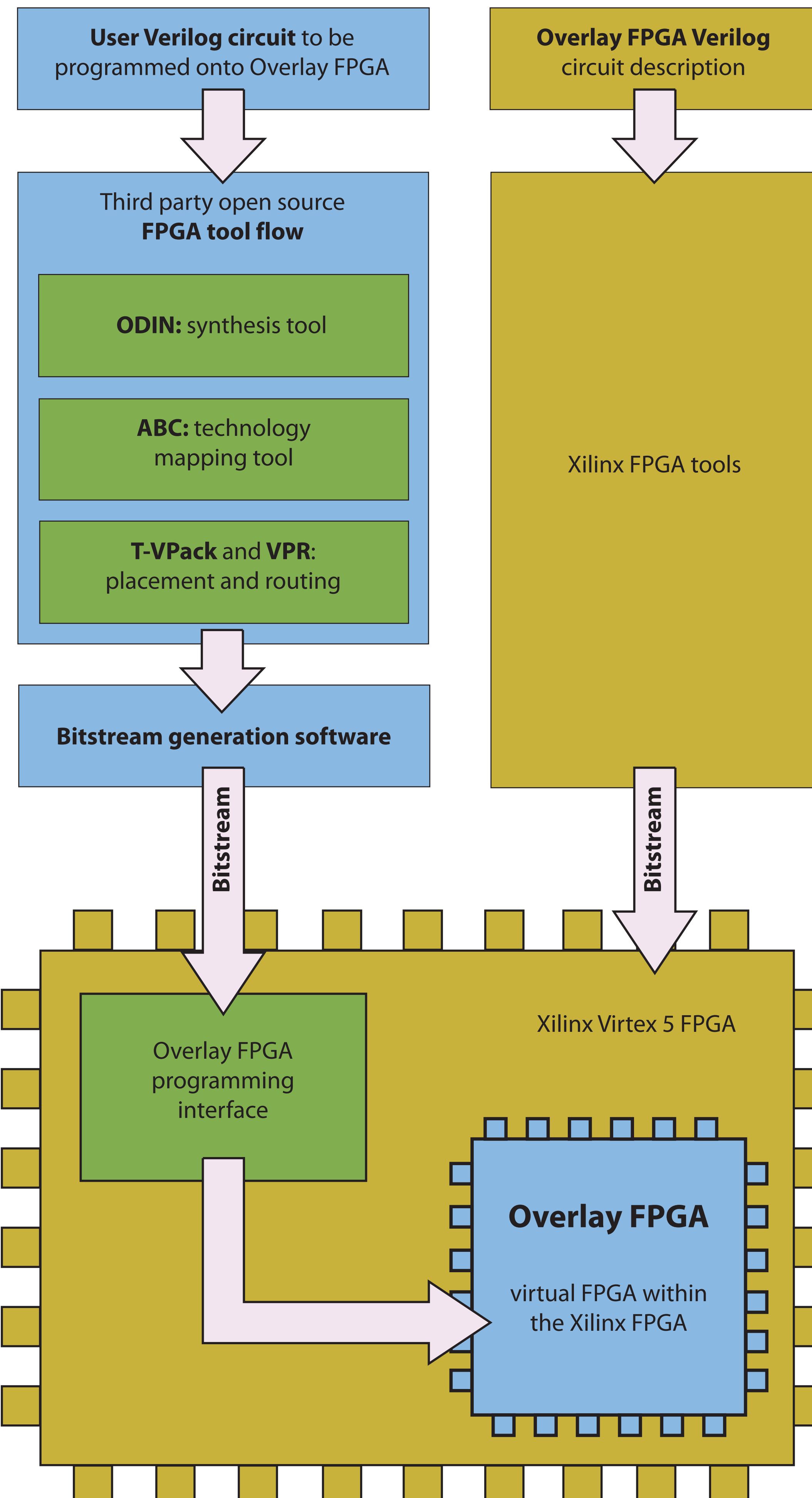
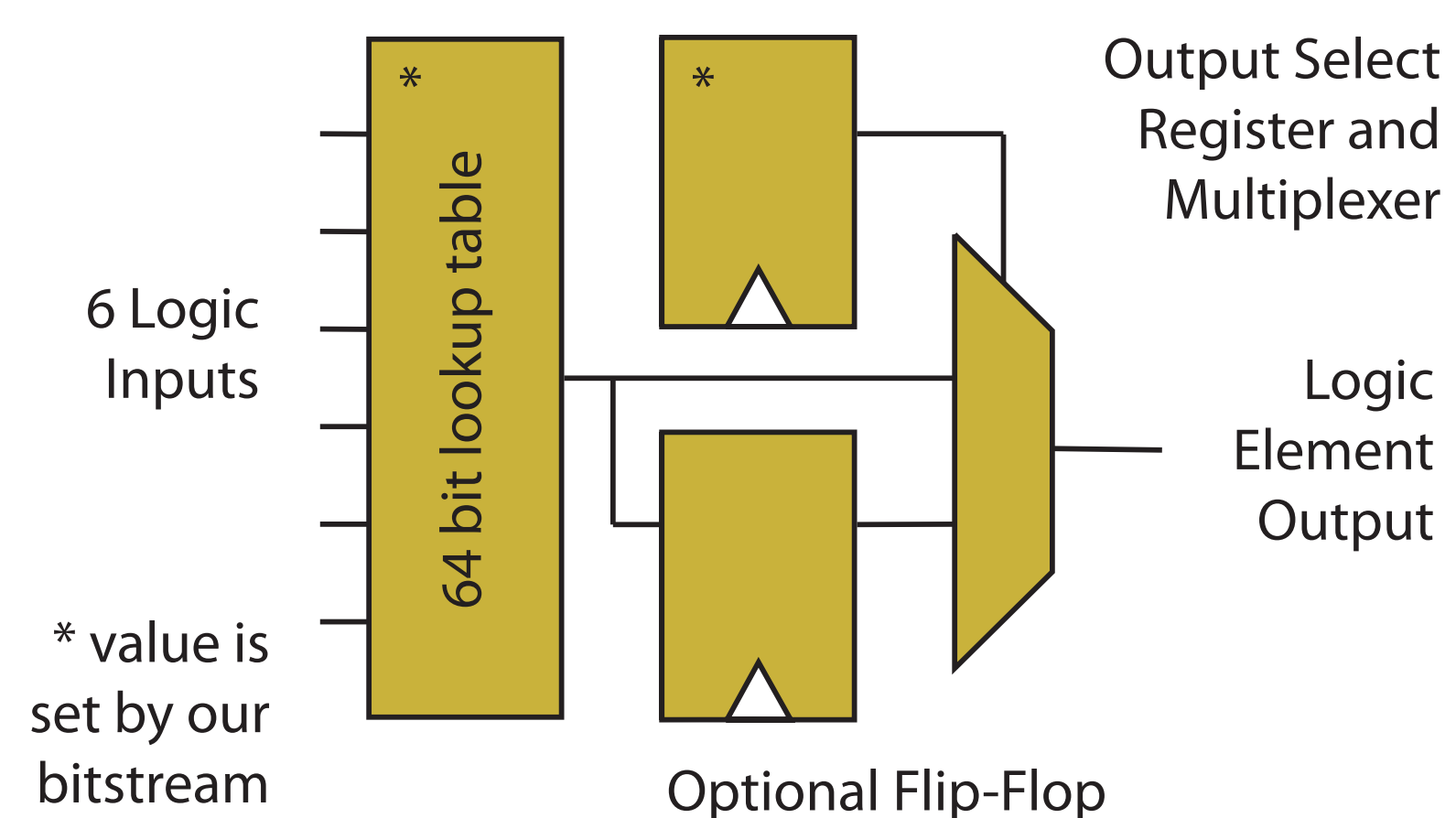


The overlay is an array of tiles



Individual tile composition

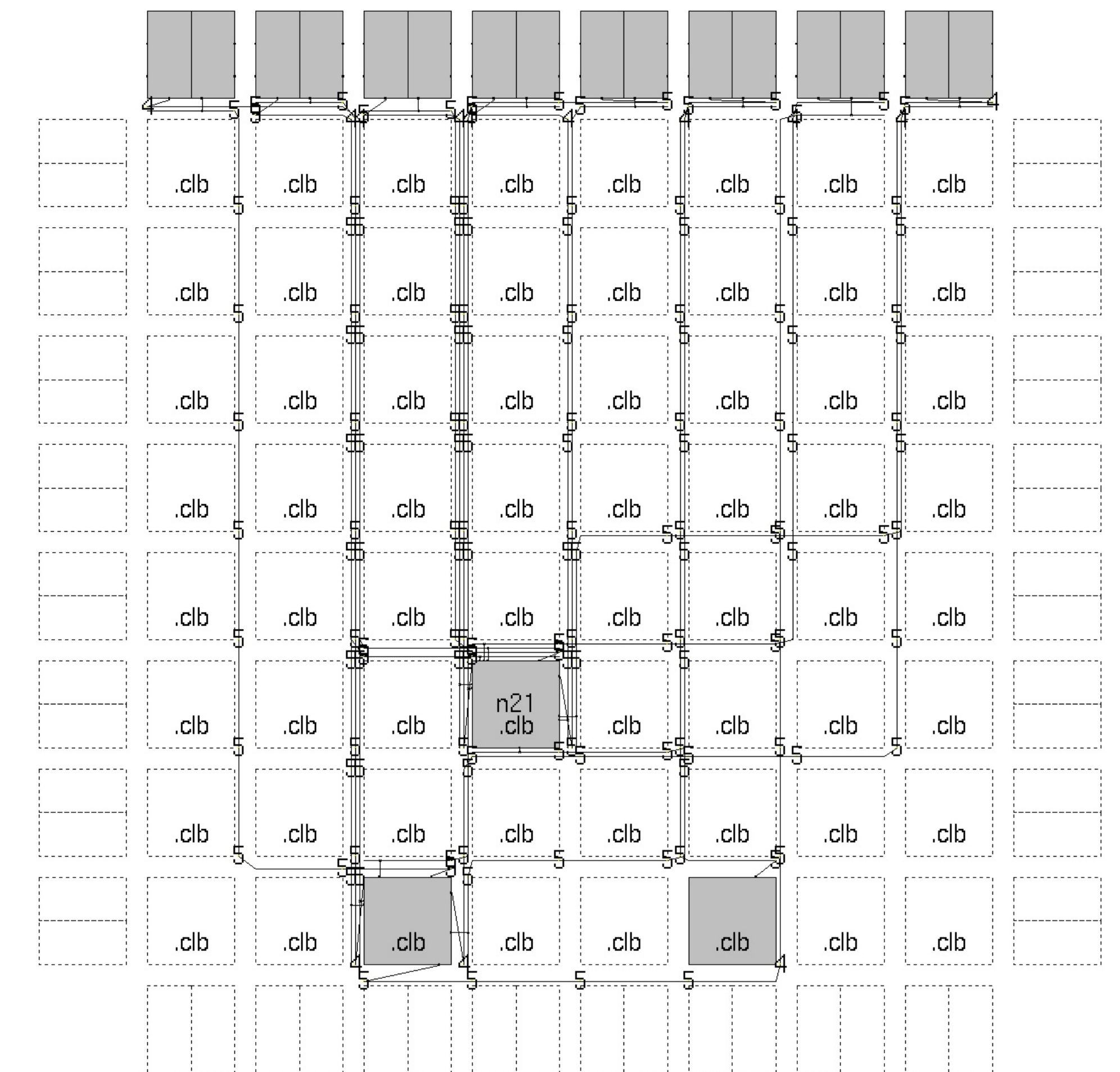
## Basic Logic Element (BLE)



## Challenges:

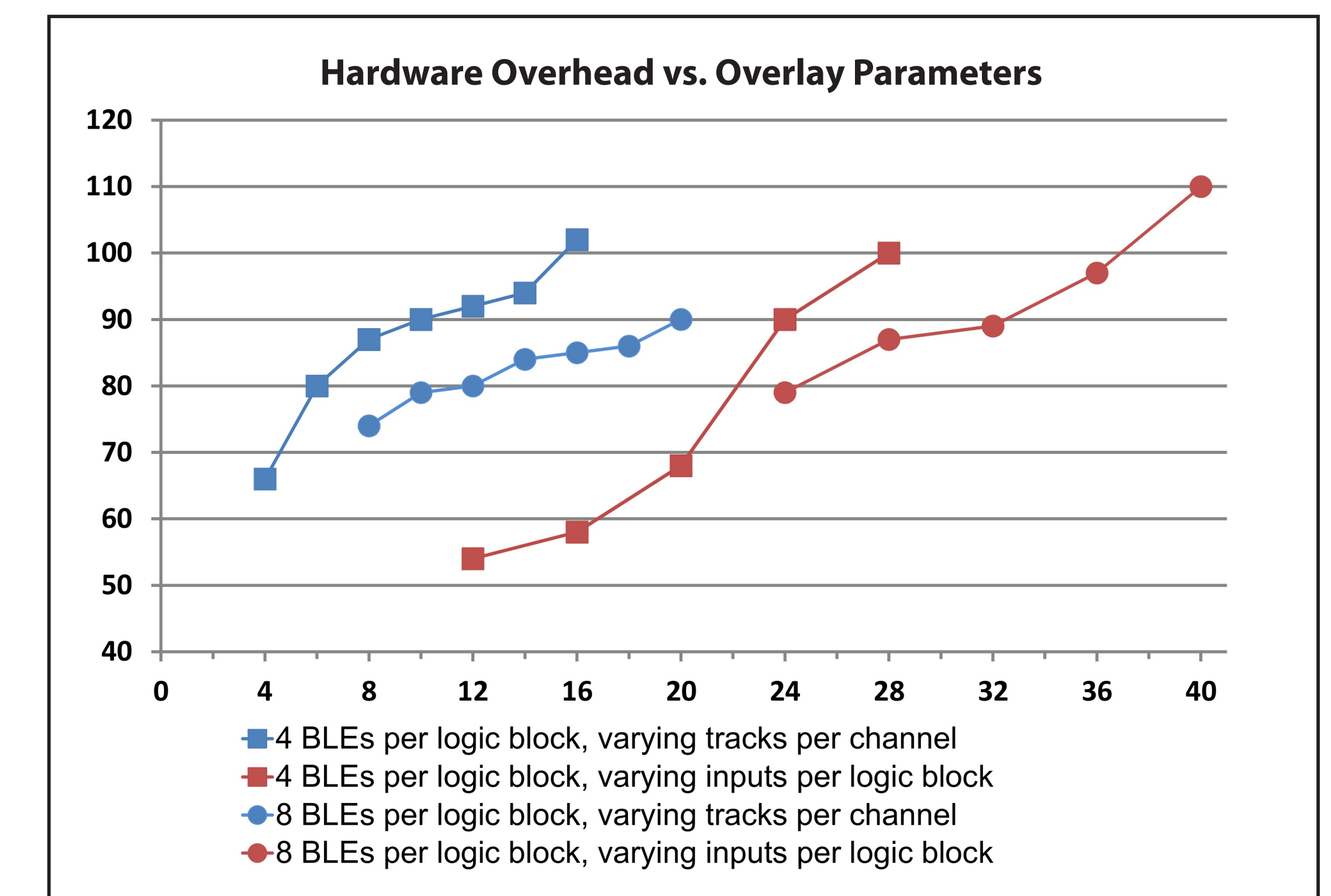
- Learning and implementing an FPGA architecture
- Hardware programming specification
- Consistency with our bitstream software
- Working around issues in third party tools

## Placement and routing of 4-bit adder circuit in VPR



Versatile Place and Route (VPR) version 5.0.2 was used  
64 Tiles with 4 BLEs per tile, 4 tracks per channel  
Logic Blocks are shown in grey as ".clb"  
Inputs and Outputs are they grey boxes at the top  
Routing connections shown as lines between logic blocks

## Implementation Overhead



Overhead = Virtex 5 lookup tables used / Overlay logic elements  
Uses 24 inputs to logic block and track width of 10 when not varying