ECE496Y Project Proposal Document Evaluation Form

| ent | Project Title: | Virtual FPGA fabrics: Implementation of a virtual FPGA architecture | | | | | | | | |
|-----|---|---|----------------|----------------|--|------------------------------------|---|--|--|--|
| hud | Project ID: | 2011017 | Supervisor: | Jason Anderson | | | | | | |
| Ś | Section #: 7 | | Administrator: | Ross Gillett | | | | | | |
| | Estimate # contact hours per month with supervisor: 4 | | | | | Suggest optimal # hours per month: | 4 | | | |

| Administrator's Project Proposal Event (Provide a rating for each section) | valuation | Excellent | Good | Adequate | Marginal | Poor | Comments |
|--|----------------------|-----------|--------|----------|----------|------|----------------------------|
| Project Description | | | | | | | |
| Background and Motivation (design problem, past | work, references) | | | | | | |
| Project Goal and Requirements (Verifiable? Link problem?) | to original | Ш | | | | | |
| Validation and Acceptance Tests (Link to goal and | nd requirements?) | | | | | | |
| Technical Design | | | | | | | |
| Possible Solutions and Design Alternatives (| key trade-offs) | | | | | | |
| System-level overview (system block diagram) | | | | | | | |
| Module-level descriptions (inputs/outputs, functional | al description) | | | | | | |
| Assessment of Proposed Design (strengths, limitat | ions, trade-offs) | | | | | | |
| Work Plan | | | | | ! | | |
| Work breakdown structure (tasks verifiable? Complidivision of work) | lete, clear and fair | | | | | | |
| Gantt chart (task described and numbered, logical s | cheduling) | | | | | | |
| Financial plan (Justification for funding? Contingency | y plan?) | | | | | | |
| Feasibility Assessment (skill & resources, risk mitig | ation plan) | | | | | | |
| Overall | | | | ! | ! | | |
| Presentation (grammar, spelling, writing style, figure | s) | | | | | | |
| Content (Exec. summary, organization, logical coher | ence, substance) | | | | | | |
| Other problems (Late, student-supervisor agreemen | t unsigned, supervis | or cont | act ti | me t | too lo | w) | |
| ☐ Ethics review (if gathering personal information of | or testing on human | or anim | al su | ıbjec | ets) | | |
| Administrator's grade only (/10) | Document sectio | | | | | | Administrator's signature: |
| (*Supervisor's grade on <u>next</u> page) | | | | | | | |
| Administrator's comments (also see comments in repo | ort) | | | | | | |
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ECE496Y Design Review Meeting Evaluation Form

| ant | Project Title: | Virtual FPGA fabrics: Implementation of a virtual FPGA architecture | | | | | | | |
|-----|----------------|---|--------------------|----------------|---------------|-----------------------|---|--|--|
| 2 | Project ID: | 2011017 | Supervisor: | Jason Anderson | | | | | |
| Ü. | Section #: 7 | | Administrator: | Ross Gillett | | | | | |
| | Estimate # cor | ntact hours | per month with sur | pervisor: 4 | Suggest optim | al # hours per month: | 4 | | |

| | 7 0 7 | 4 - | |
|--|--------------------------------------|--------------|----------------------------|
| Administrator's Evaluation | Good | <u> </u> | Comments to Group |
| | lent Good Adequate Marginal | Poor/unclear | |
| | Excellent Ade | oor | |
| Group Evaluation | Exc | | |
| Project Description (background, goals, requirements, acceptance tests) | | | |
| Technical Design (alternatives, trade- offs, system overview, testing) | | | |
| Work Plan (scheduling, risks, resources) | | | |
| December Review Target Received | | | |
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| Additional deliverables for December Review: | | | |
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| Individual Evaluations (roles and | contributions) | <u>C</u> | Comments to Individuals |
| Student 1: | | | |
| | | | |
| Mark: /10 | | | |
| Student 2: | | | |
| | | | |
| Mark: /10 | | | |
| Student 3: | | | |
| Student 6. | | | |
| | | | |
| Mark: /10 | | | |
| Student 4: | | | |
| | | | |
| Mark: /10 | | | |
| Section average (/10): | ☐ Ethics review | А | Administrator's Signature: |
| | recommended | | - |

Note to Supervisors:

Your evaluation was done online. There is no need to return anything else to the administrator. Please return this report to your students.

The Edward S. Rogers Sr. Department of Electrical and Computer Engineering

University of Toronto ECE496Y Design Project Course

Group Project Proposal (final draft)

Title: Virtual FPGA fabrics: Implementation of a virtual FPGA architecture

| Project I.D.#: | 2011017 | | | | | | |
|--------------------------------------|------------------|----------------------|--|--|--|--|--|
| Team members: | Name: | Email: | | | | | |
| (Select one member to | Neil Isaac * | n.isaac@utoronto.ca | | | | | |
| be the main contact. Mark with '*') | Keyi Shi | keyi.shi@utoronto.ca | | | | | |
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| | | | | | | | |
| Supervisor: | Jason Anderson | | | | | | |
| Section #: | 7 | | | | | | |
| Administrator: Gillett | | | | | | | |
| Date: | October 18, 2011 | | | | | | |