LCELL WYSIWYG Description for Cyclone III

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Table of Contents:

1. Overview

It's assumed that the reader is familiar with the Cyclone II LCELL WYSIWYGs described

This is a summary of the LCELL WYSIWYG and atom support for Cyclone III. The Cyclone III logic cell is identical to the Cyclone II logic cell in terms of functionality so it is modeled similarly. The only difference is in Cyclone III, we are modeling IO registers separately from the rest of the IO cell, similar to what we have been doing with lcell registers, thus registers used in LAB and I/O blocks are modeled with a common primitive. This Cyclone III register primitive is documented separately.

Section 2 describes the combinational WYSIWYG block.

Section 3 describes the register WYSIWYG block.

Section 4 describes how they are connected in a logic cell.

2. Combinational Logic Cell Primitive

```
cuda_lcell_comb <lcell_name>
(
      .dataa(<data_a source>),
      .datab(<data_b source>),
      .datac(<data_c source>),
      .datad(<data_d source>),
      .cin(<carry in source>),

      .combout(<combinational output>),
      .cout(<carry output>)
);
defparam <lcell_name>.lut_mask = <lut mask>;
defparam <lcell_name>.sum_lutc_input = <sum lut input choice>;
```

2.1 Combinational Logic Cell Input Ports

Same as in the Cyclone II case.

2.2 Combinational Logic Cell Output Ports

Same as in the Cyclone II case.

2.3 Combinational Logic Cell Modes

Same as in the Cyclone II case.

2.4 Combinational Logic Cell Block Diagram

Same as in the Cyclone II case.

2.5 Combinational Logic Cell Usage

Same as in the Cyclone II case.

2.6 Interpreting the LUT Mask

Same as in the Cyclone II case.

2.7 Combinational Logic Cell Polarities and Default Values

Same as in the Cyclone II case.

3. LAB Register Primitive

See the Cyclone III register primitive documentation for more details on the primitive itself.

3.1 Register Logic Cell Control Signal Choices

Same as in the Cyclone II case.

4. Cyclone III Logic Cell Description

Same as in the Cyclone II case.