

ZC706 Evaluation Board for the Zynq-7000 XC7Z045 All Programmable SoC *User Guide*

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Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|------------|---------|---|
| 10/08/2012 | 1.0 | Initial Xilinx release. |
| 11/21/2012 | 1.1 | Added additional user LED in ZC706 Evaluation Board Features section, Table 1-1 , User I/O section, Figure 1-25 , and Table 1-28 . In Table 1-1 , added fan sink information and updated notes for 10/100/1000 Ethernet PHY, user pushbuttons, user DIP switch, and FPGA PROG pushbutton. Added Encryption Key Backup Circuit section. Updated second paragraph in DDR3 SODIMM Memory (PL) section. Updated second paragraph in SD Card Interface section. Updated Table 1-11 . Added U53 information to first paragraph in HDMI Video Output section. Added fourth bullet to Real Time Clock (RTC) section. Updated Figure 1-23 . Added pin A17 to Table 1-28 . Updated Figure 1-32 . Replaced UCF file in Appendix C . Added additional reference to References in Appendix F . |

| Date | Version | Revision |
|------------|---------|--|
| 04/24/2013 | 1.2 | <p>Chapter 1, ZC706 Evaluation Board Features: Table 1-1 feature descriptions are now linked to their respective sections in the book. Figure 1-2, Figure 1-33, and Figure 1-34 were replaced. Table 1-2 was removed because it was a duplicate of Table 1-11. Table 1-2: Switch SW11 Configuration Option Settings was added. FMC Connector JTAG Bypass, page 33 was updated. Default lane size information below Figure 1-17 was changed. Figure 1-18 PCI Express Lane Size Select Jumper J19 was added. The names of pins 18 and 19 changed in Table 1-17. The address of I²C bus PMBUS_DATA/CLOCK changed in Table 1-25. Reference designator DS35 was added to Table 1-27. Callout numbers in the User I/O, page 57 section are now linked to Table 1-1. SW13 information was added to the section User Pushbuttons, page 59. In Table 1-33, J5 pin H22 changed to XC7Z045 (U1) pin AH26 and H23 changed to AH27. The section ZC706 Board Power System, page 72 was added. Voltage levels were changed in VADJ Voltage Control, page 79. Table 1-37 was modified and Table 1-38 was added.</p> <p>Appendix A, Default Switch and Jumper Settings: The SW11 selection in Table A-1 changed.</p> <p>Appendix G, Regulatory and Compliance Information: A link to the master answer record was added.</p> |

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ZC706 Evaluation Board Features

Overview

The ZC706 evaluation board for the XC7Z045 All Programmable SoC (AP SoC) provides a hardware environment for developing and evaluating designs targeting the Zynq™-7000 XC7Z045-2FFG900C All Programmable SoC. The ZC706 evaluation board provides features common to many embedded processing systems, including DDR3 SODIMM and component memory, a four-lane PCI Express™ interface, an Ethernet PHY, general purpose I/O, and two UART interfaces. Other features can be supported using VITA-57 FPGA mezzanine cards (FMC) attached to the low pin count (LPC) FMC and high pin count (HPC) FMC connectors.

ZC706 Evaluation Board Features

The ZC706 evaluation board features are listed in here. Detailed information for each feature is provided in [Feature Descriptions](#) starting on [page 13](#).

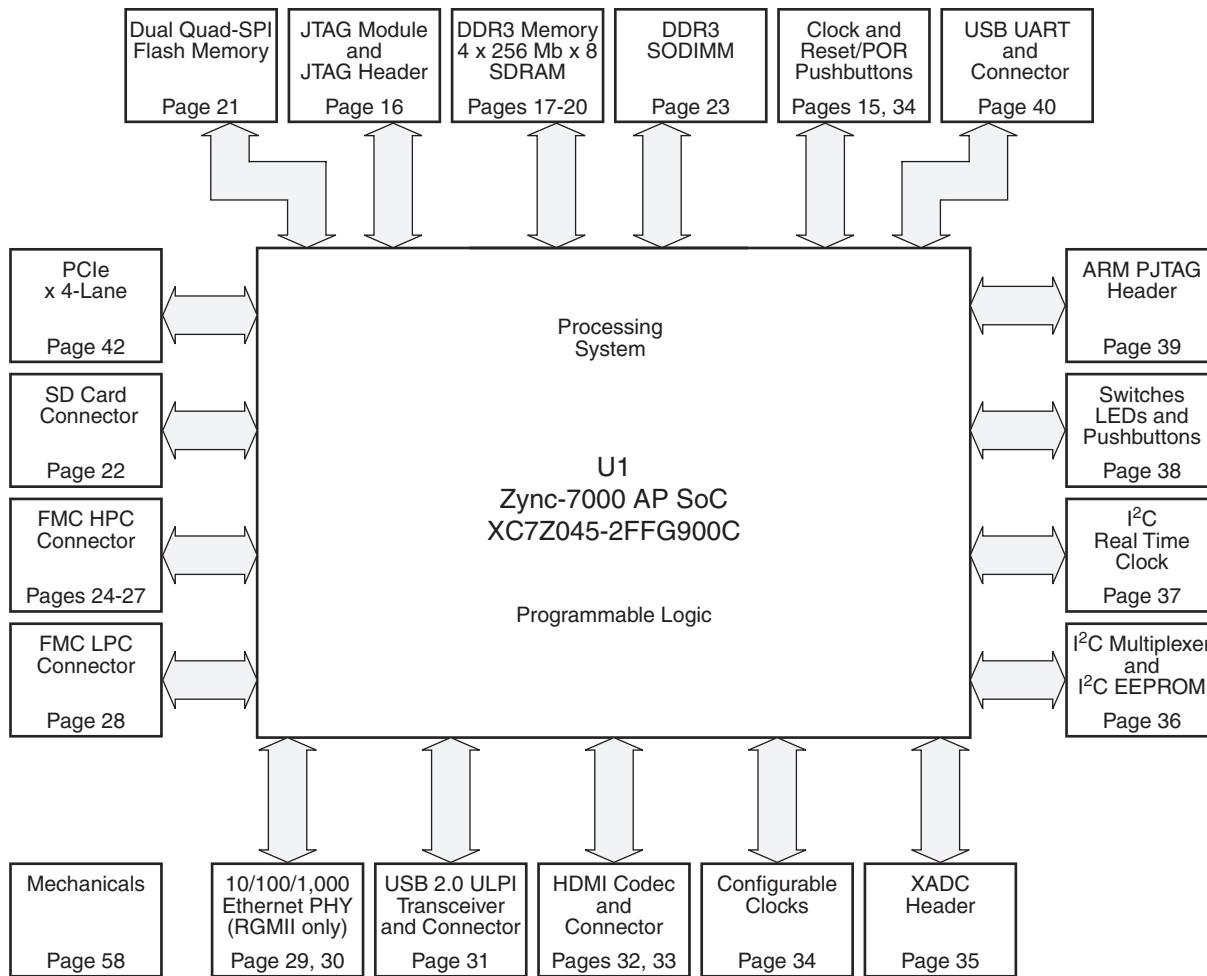
- Zynq-7000 XC7Z045-2FFG900C AP SoC
- 1 GB DDR3 memory SODIMM on the programmable logic (PL) side
- 1 GB DDR3 component memory (four [256 Mb x 8] devices) on the processing system (PS) side
- Two 128 Mb Quad-SPI (QSPI) flash memory (Dual Quad-SPI)
- USB 2.0 ULPI (UTMI+ low pin interface) transceiver with micro-B USB connector
- Secure Digital (SD) connector
- USB JTAG interface via Digilent module with micro-B USB connector
- Clock sources:
 - Fixed 200 MHz LVDS oscillator (differential)
 - I²C programmable LVDS oscillator (differential)
 - Fixed 33.33 MHz LVCMOS oscillator (single-ended)
 - SMA connectors (differential)
 - SMA connectors for GTX transceiver clocking (differential)

- GTX transceivers
 - FMC HPC connector (eight GTX transceivers)
 - FMC LPC connector (one GTX transceiver)
 - SMA connectors (one pair each for TX, RX and REFCLK)
 - PCI Express (four lanes)
 - Small form-factor pluggable plus (SFP+) connector
 - Ethernet PHY RGMII interface
- PCI Express endpoint connectivity
 - Gen1 4-lane (x4)
 - Gen2 4-lane (x4)
- SFP+ Connector
- Ethernet PHY RGMII interface with RJ-45 connector
- USB-to-UART bridge with mini-B USB connector
- HDMI codec with HDMI connector
- I²C bus
- I²C bus multiplexed to:
 - Si570 user clock
 - ADV7511 HDMI codec
 - M24C08 EEPROM (1 kB)
 - 1-to-16 TCA6416APWR port expander
 - DDR3 SODIMM
 - RTC-8564JE real time clock
 - FMC HPC connector
 - FMC LPC connector
 - PMBUS data/clock
- Status LEDs:
 - Ethernet status
 - TI Power Good
 - Linear Power Good
 - PS DDR3 Component V_{tt} Good
 - PL DDR3 SODIMM V_{tt} Good

- FMC Power Good
- 12V Input Power On
- FPGA INIT
- FPGA DONE
- User I/O:
 - Four (PL) user LEDs
 - Three (PL) user pushbuttons
 - One (PL) user DIP switch (4-pole)
 - Two Dual row Pmod GPIO headers
- AP SoC PS Reset Pushbuttons:
 - SRST_B PS reset button
 - POR_B PS reset button
- VITA 57.1 FMC HPC connector
- VITA 57.1 FMC LPC connector
- Power on/off slide switch
- Program_B pushbutton
- Power management with PMBus voltage and current monitoring via TI power controller
- Dual 12-bit 1 MSPS XADC analog-to-digital front end
- Configuration options:
 - Dual Quad-SPI flash memory
 - USB JTAG configuration port (Digilent module)
 - Platform cable header JTAG configuration port
 - 20-pin PL PJTAG header

Block Diagram

The ZC706 evaluation board block diagram is shown in [Figure 1-1](#).



Note: Page numbers reference the page number of schematic 0381513.

UG954_c1_01_1002012

Figure 1-1: ZC706 Evaluation Board Block Diagram

Board Layout

[Figure 1-2](#) shows the ZC706 evaluation board. Each numbered feature that is referenced in [Figure 1-2](#) is described in [Table 1-1](#) with a link to detailed information provided under [Feature Descriptions](#) starting on [page 13](#).

Note: The image in [Figure 1-2](#) is for reference only and might not reflect the current revision of the board.



CAUTION! The ZC706 evaluation board can be damaged by electrostatic discharge (ESD). Follow ESD prevention measures when handling the board.

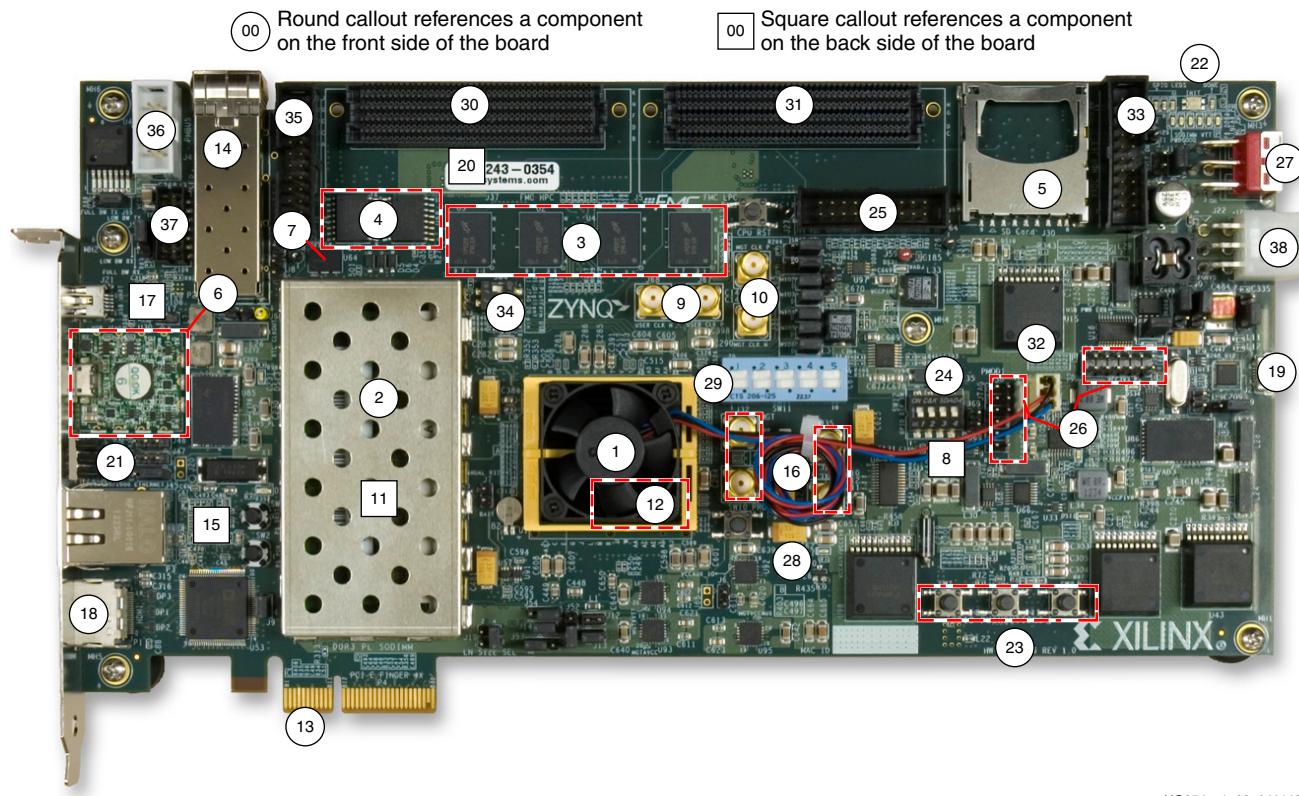


Figure 1-2: ZC706 Evaluation Board Component Locations

Table 1-1: ZC706 Evaluation Board Component Descriptions

| Callout | Feature | Notes | Schematic 0381513 Page Number |
|---------|---|--|-------------------------------------|
| 1 | Zynq-7000 XC7Z045 AP SoC, page 13 Zynq-7000 All Programmable SoC with fan sink | XC7Z045T-2FFG900C with Radian INC3001-7_1.5BU_LI98 fan sink | |
| 2 | DDR3 SODIMM Memory (PL), page 18 DDR3 SODIMM Memory Socket(J1) | Micron MT8JTF12864HZ-1G6G1 | 23 |
| 3 | DDR3 Component Memory (PS), page 22 DDR3 Memory 1GB (4x256M U2-U5) | Micron MT41J256M8HX-15E | 17-20 |
| 4 | Quad-SPI Flash Memory, page 25 Dual Quad-SPI Flash (128Mb) (U58-U59) | Spansion S25FL128SAGMFIR01 | 21 |
| 5 | SD Card Interface, page 29 SD Card Interface Connector (J30) | Molex 67840-8001 | 22 |
| 6 | USB 2.0 ULPI Transceiver, page 26 USB JTAG Interface w/Micro-B Connector (U30) | Digilent USB JTAG Module | 16 |
| 7 | System Clock, page 34 System Clock, 2.5V LVDS (U64) | SiTime SIT9102-243N25E200.0000 | 34 |

Table 1-1: ZC706 Evaluation Board Component Descriptions (Cont'd)

| Callout | Feature | Notes | Schematic 0381513 Page Number |
|---------|---|---|-------------------------------------|
| 8 | Programmable User Clock, page 35 I ² C Prog. User Clock 3.3V LVDS (U37, bottom of board) | Silicon Labs SI570BAB0000544DG, default 156.250 MHz | 34 |
| 9 | User SMA Clock Source, page 36 User Differential SMA Clock P/N (J67/J68) | Rosenberger 32K10K-400L5 | 44 |
| 10 | GTX SMA Clock (SMA_MGT_REFCLK_P and SMA_MGT_REFCLK_N), page 37 GTX Differential SMA Clock P/N (J36/J31) | Rosenberger 32K10K-400L5 | 44 |
| 11 | Jitter Attenuated Clock, page 38 Jitter Attenuated Clock (U60, bottom of board) | Silicon Labs SI5324C-C-GM | 43 |
| 12 | GTX Transceivers, page 39 GTX Transceivers | Embedded within AP SoC U1 | 8 |
| 13 | PCI Express Endpoint Connectivity, page 43 PCI Express Connector (P4) | 4-lane card edge connector | 42 |
| 14 | SFP/SFP+ Module Connector, page 45 SFP/SFP+ Module Connector (P2) | Molex 74441-0010 | 41 |
| 15 | 10/100/1,000 Mb/s Tri-Speed Ethernet PHY (PL), page 47 RGMII only 10/100/1000 Mb/s Ethernet PHY w/RJ45 (U51, P3) | Marvell 88E1116RA0-NNC1C000 | 29 |
| 16 | GTX Differential SMA TX and RX P/N (J35/J34 and J32/J33) | Rosenberger 32K10K-400L5 | 44 |
| 17 | USB-to-UART Bridge, page 49 USB-to-UART Bridge with Mini-B Connector (U52, J21) | Silicon Labs CP2103GM bridge | 40 |
| 18 | HDMI Video Output, page 50 HDMI Controller (U53), HDMI Video Connector (P1) | Analog Devices ADV7511KSTZ-P, Molex 500254-1927, | 32, 33 |
| 19 | USB 2.0 ULPI Transceiver, page 26 USB 2.0 ULPI Controller w/ Micro-B Connector (U12, J2) | SMSC USB3320C-EZK | 31 |
| 20 | I²C Bus, page 53 I ² C Bus MUX (U65, bottom of board) | TI PCA9548ARGER | 36 |
| 21 | Ethernet PHY User LEDs, page 57 Ethernet PHY Status LEDs (DS28-DS30) | EPHY status LED, GREEN single-stack | 29 |
| 22 | User LEDs, page 58 User LEDs (DS8-DS10, DS35) | GPIO LEDs, GREEN 0603 | 38 |
| 23 | User Pushbuttons, page 59 User pushbuttons, active-High (SW7, 9, 8) | E-Switch TL3301EF100QG in Left, Center, Right pattern | 38 |

Table 1-1: ZC706 Evaluation Board Component Descriptions (Cont'd)

| Callout | Feature | Notes | Schematic 0381513 Page Number |
|---------|---|--|-------------------------------------|
| 24 | GPIO DIP Switch, page 60 GPIO DIP Switch (SW12) | 4-pole C&K SDA04H1SBD | 38 |
| 25 | ARM PJTAG Header (J64) | 2x10 0.1inch male header, Samtec TST-110-01-G-D | 39 |
| 26 | User PMOD GPIO Headers, page 60 PMOD Headers (J57, J58) | 2x6 0.1 inch male header | 37, 39 |
| 27 | Power On/Off Slide Switch, page 62 Power On/Off Switch (SW1) | C&K 1201M2S3AQE2 | 48 |
| 28 | Program_B Pushbutton, page 63 FPGA PROG pushbutton (SW10) | E-Switch TL3301EF100QG | 38 |
| 29 | AP SoC MIO Config. DIP Switch (SW11) | 5-pole DPDT CTS 206-125 | 15 |
| 30 | HPC Connector J37, page 65 FMC HPC connector (J37) | Samtec ASP_134486_01 | 24-27 |
| 31 | LPC Connector J5, page 70 FMC LPC connector (J5) | Samtec ASP_134603_01 | 28 |
| 32 | Power Management, page 77 Power Management System (top and bottom of board) | TI UCD90120ARGC in conjunction w/various regulators | 48-57 |
| 33 | XADC Analog-to-Digital Converter, page 83 XADC Connector (J63) | 2x10 0.1inch male header, Samtec TST-110-01-G-D | 35 |
| 34 | Programmable Logic JTAG Select Switch, page 31 JTAG Configuration DIP Switch (SW4) | 2-pole C&K SDA02H1SBD | 16 |
| 35 | JTAG Flying Lead Header (J62) | 2x10 0.1inch male header, Samtec TST-110-01-G-D | 16 |
| 36 | 2x5 shrouded PMBus connector J4 | ASSMAN HW10G-0202 | 48 |
| 37 | 2x7 2mm shrouded JTAG cable connector J3 | MOLEX 87832-1420 | 16 |
| 38 | 12V power input 2x6 connector J22 | MOLEX-39-30-1060 | 48 |

Feature Descriptions

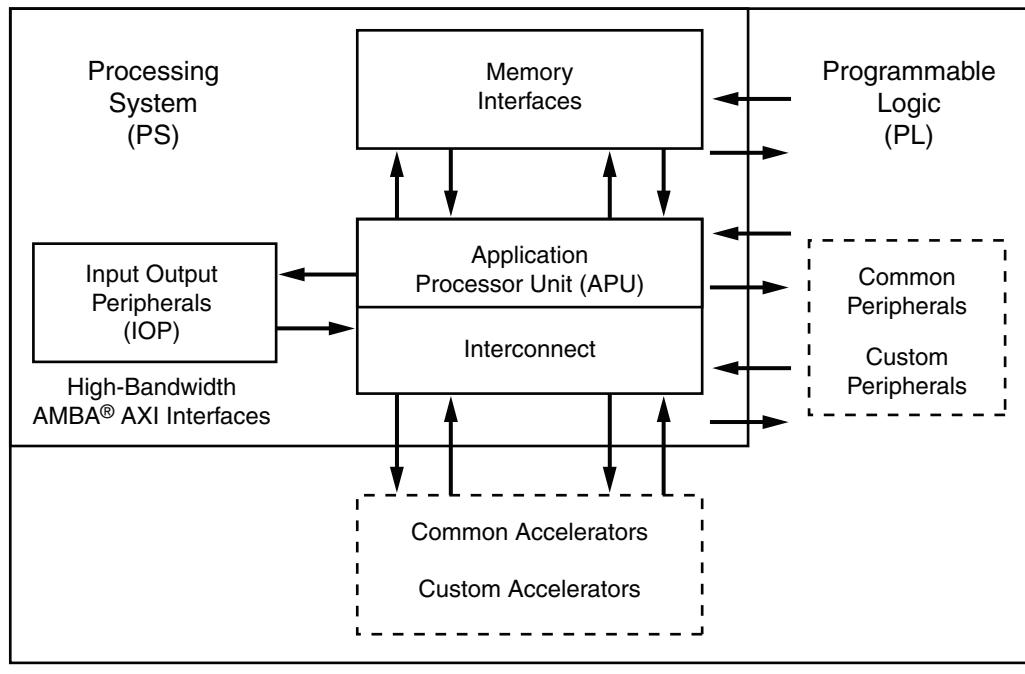
Detailed information for each feature shown in [Figure 1-2](#) and listed in [Table 1-1](#) is provided in this section.

Zynq-7000 XC7Z045 AP SoC

[[Figure 1-2](#), callout 1]

The ZC706 evaluation board is populated with the Zynq-7000 XC7Z045-2FFG900C AP SoC.

The XC7Z045 AP SoC consists of an integrated processing system (PS) and programmable logic (PL), on a single die. The high-level block diagram is shown in [Figure 1-3](#).

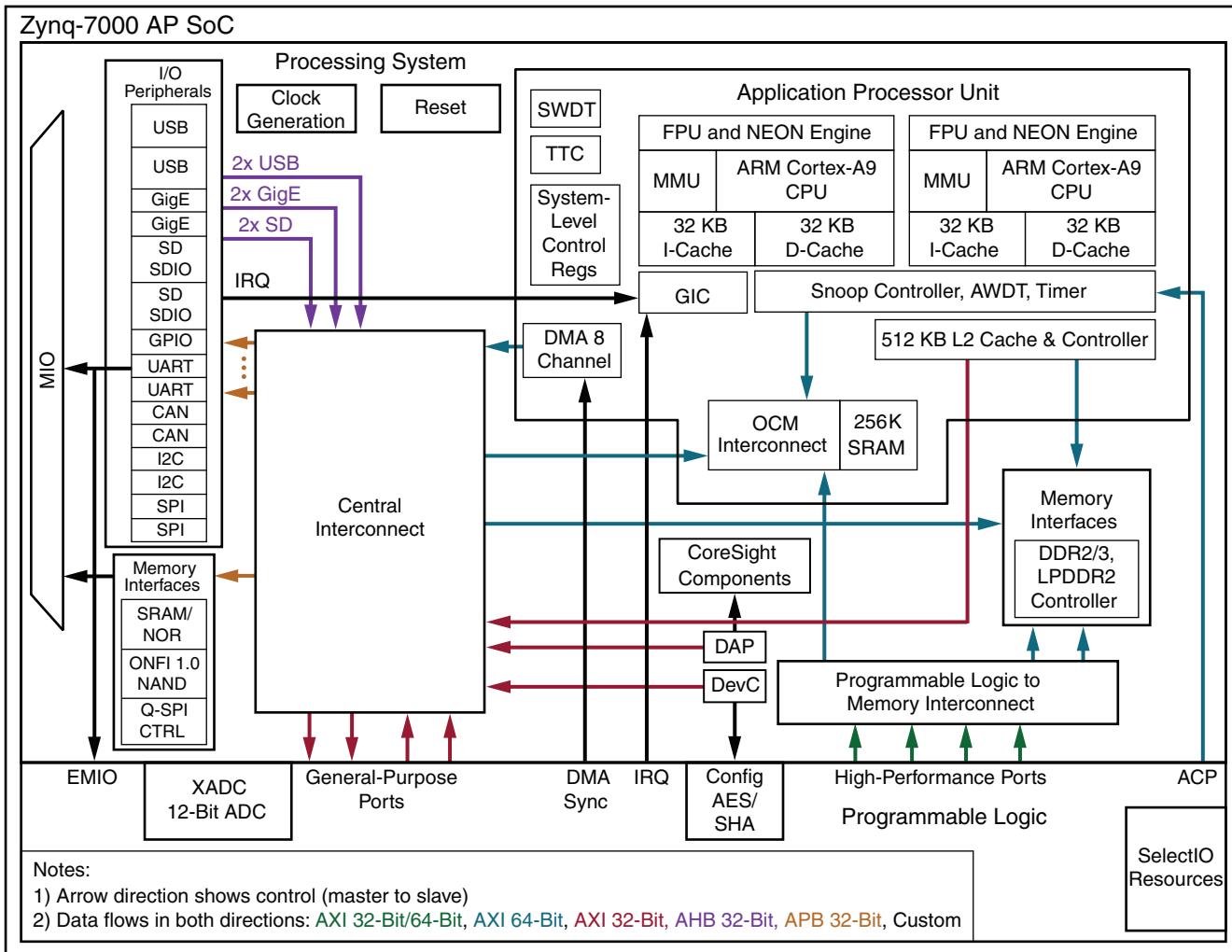


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Figure 1-3: High-Level Block Diagram

The PS integrates two ARM® Cortex™-A9 MPCore™ application processors, AMBA® interconnect, internal memories, external memory interfaces, and peripherals including USB, Ethernet, SPI, SD/SDIO, I²C, CAN, UART, and GPIO. The PS runs independently of the PL and boots at power-up or reset.

A system level block diagram is shown in [Figure 1-4](#).



UG954_c1_04_100112

Figure 1-4: Zynq-7000 Block Diagram

For additional information on Zynq-7000 SoC devices, see [DS190](#), [Zynq-7000 All Programmable SoC Overview](#), and [UG585](#), [Zynq-7000 All Programmable SoC Technical Reference Manual](#).

Device Configuration

the Zynq-7000 XC7Z045 AP SoC uses a multi-stage boot process that supports both a non-secure and a secure boot. The PS is the master of the boot and configuration process. For a secure boot, the PL must be powered on to enable the use of the security block located within the PL, which provides 256-bit AES and SHA decryption/authentication.

The ZC706 evaluation board supports these configuration options:

- PS Configuration: Quad-SPI flash memory
- PS Configuration: Processor System Boot from SD Card (J30)

- PL Configuration: USB JTAG configuration port (Digilent module U30)
- PL Configuration: Platform cable header J3 and flying lead header J62 JTAG configuration ports



TIP: *Designs using serial configuration based on Quad-SPI flash memory can take advantage of low-cost commodity SPI flash memory.*

The JTAG configuration option is selected by setting SW11 (PS) as shown in [Table 1-2](#) and SW4 (PL) as described in [Programmable Logic JTAG Programming Options, page 31](#). SW11 is callout [29](#) in [Figure 1-2](#).

Table 1-2: Switch SW11 Configuration Option Settings

| Boot Mode | SW11.1 | SW11.2 | SW11.3 | SW11.4 | SW11.5 |
|--------------------------|--------|--------|--------|--------|--------|
| JTAG mode ⁽¹⁾ | 0 | 0 | 0 | 0 | 0 |
| Independent JTAG mode | 1 | 0 | 0 | 0 | 0 |
| QSPI mode | 0 | 0 | 0 | 1 | 0 |
| SD mode | 0 | 0 | 1 | 1 | 0 |
| MIO configuration pin | MIO2 | MIO3 | MIO4 | MIO5 | MIO6 |

Notes:

1. Default switch setting

For more information about Zynq®-7000 AP SoC configuration settings, see [UG585, Zynq-7000 All Programmable SoC Technical Reference Manual](#).

Encryption Key Backup Circuit

The XC7Z045 AP SoC U1 implements bitstream encryption key technology. The ZC706 board provides the encryption key backup battery circuit shown in [Figure 1-5](#). The Seiko TS518FE rechargeable 1.5V lithium button-type battery B2 is soldered to the board with the positive output connected to the XC7Z045 AP SoC U1 VCCBATT pin P9. The battery supply current IBATT specification is 150 nA max when board power is off. B2 is charged from the VCCAUX 1.8V rail through a series diode with a typical forward voltage drop of 0.38V and 4.7 KΩ current limit resistor. The nominal charging voltage is 1.42V.

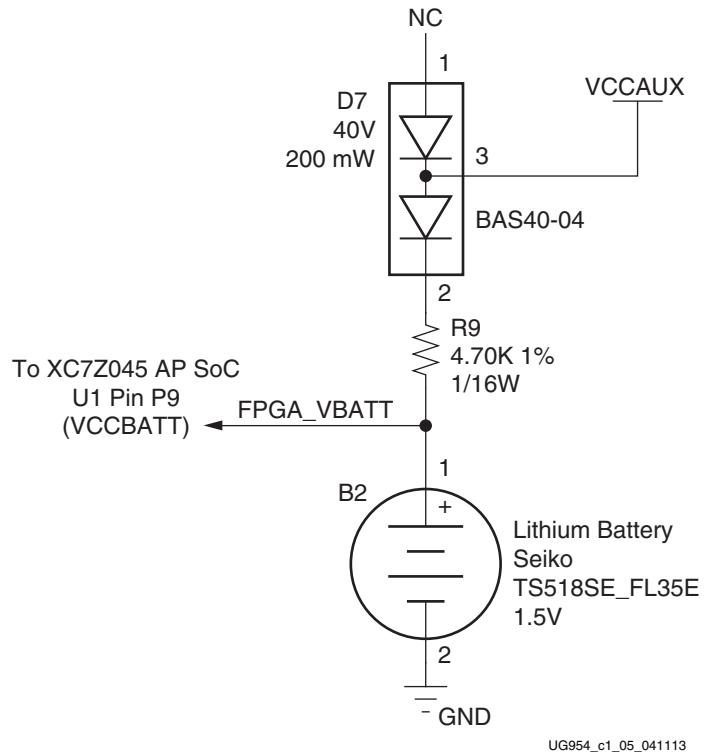


Figure 1-5: Encryption Key Backup Circuit

I/O Voltage Rails

There are eleven I/O banks available on the XC7Z045 AP SoC. The voltages applied to the XC7Z045 AP SoC I/O banks used by the ZC706 evaluation board are listed in [Table 1-3](#).

Table 1-3: I/O Voltage Rails

| XC7Z045 (U1) Bank | Net Name | Voltage | Connected To |
|-------------------|-------------|---------|---|
| PL Bank 0 | VCC3V3_FPGA | 3.3V | AP SoC Configuration Bank 0 |
| PL Bank 9 | VADJ_FPGA | 2.5V | PMOD, USER_SMA_CLOCK, SM_FAN, REC_CLOCK, SFP_TX_DISABLE |
| PL Bank 10 | | | FMC_LPC, PL_JTAG, GPIO |
| PL Bank 11 | | | FMC_HPC, GPIO_LED, HDMI |
| PL Bank 12 | | | FMC_LPC, HDMI |
| PL Bank 13 | | | FMC_HPC, HDMI |
| PL Bank 33 | | | PL_DDR3_D[31:0] |
| PL Bank 34 | VCC1V5_PL | 1.5V | PL_DDR3_A, SYSCLK |
| PL Bank 35 | | | PL_DDR3_D[63:32], XADC |

Table 1-3: I/O Voltage Rails (Cont'd)

| XC7Z045 (U1) Bank | Net Name | Voltage | Connected To |
|-------------------|----------|---------|-----------------------|
| PS Bank 500 | VCCP1V8 | 1.8V | QSPI0,QSPI1 |
| PS Bank 501 | | | PHY_IF,SDIO_IF,USB_IF |
| PS Bank 502 | | | PS_DDR3_IF |

Notes:

1. The ZC706 evaluation board is shipped with V_{ADJ} set to 2.5V.

DDR3 SODIMM Memory (PL)

[Figure 1-2, callout 2]

The memory module at J1 is a 1 GB DDR3 small outline dual-inline memory module (SODIMM). It provides volatile synchronous dynamic random access memory (SDRAM) for storing user code and data.

- Part number: MT8JTF12864HZ-1G6G1 (Micron Technology)
- Supply voltage: 1.5V
- Data path width: 64 bits
- Data rate: Up to 1,600 MT/s

The DDR3 interface is implemented across the PL-side I/O banks. Bank 33 and bank 35 have a dedicated DCI VRP/N resistor connection. An external 0.75V reference VTTREF_SODIMM is provided for data interface banks. Any interface connected to these banks that requires the VTTREF voltage must use this FPGA voltage reference. The connections between the DDR3 memory and the AP SoC are listed in Table 1-4.

Table 1-4: DDR3 SODIMM Socket J1 Connections to the XC7Z045 AP SoC

| XC7Z045 (U1) Pin | Net Name | SODIMM Memory | |
|------------------|------------|---------------|----------|
| | | Pin Number | Pin Name |
| E10 | PL_DDR3_A0 | 98 | A0 |
| B9 | PL_DDR3_A1 | 97 | A1 |
| E11 | PL_DDR3_A2 | 96 | A2 |
| A9 | PL_DDR3_A3 | 95 | A3 |
| D11 | PL_DDR3_A4 | 92 | A4 |
| B6 | PL_DDR3_A5 | 91 | A5 |
| F9 | PL_DDR3_A6 | 90 | A6 |
| E8 | PL_DDR3_A7 | 86 | A7 |
| B10 | PL_DDR3_A8 | 89 | A8 |
| J8 | PL_DDR3_A9 | 85 | A9 |

Table 1-4: DDR3 SODIMM Socket J1 Connections to the XC7Z045 AP SoC (Cont'd)

| XC7Z045 (U1) Pin | Net Name | SODIMM Memory | |
|------------------|-------------|---------------|----------|
| | | Pin Number | Pin Name |
| D6 | PL_DDR3_A10 | 107 | A10/AP |
| B7 | PL_DDR3_A11 | 84 | A11 |
| H12 | PL_DDR3_A12 | 83 | A12_BC_N |
| A10 | PL_DDR3_A13 | 119 | A13 |
| G11 | PL_DDR3_A14 | 80 | A14 |
| C6 | PL_DDR3_A15 | 78 | A15 |
| F8 | PL_DDR3_BA0 | 109 | BA0 |
| H7 | PL_DDR3_BA1 | 108 | BA1 |
| A7 | PL_DDR3_BA2 | 79 | BA2 |
| L1 | PL_DDR3_D0 | 5 | DQ0 |
| L2 | PL_DDR3_D1 | 7 | DQ1 |
| K5 | PL_DDR3_D2 | 15 | DQ2 |
| J4 | PL_DDR3_D3 | 17 | DQ3 |
| K1 | PL_DDR3_D4 | 4 | DQ4 |
| L3 | PL_DDR3_D5 | 6 | DQ5 |
| J5 | PL_DDR3_D6 | 16 | DQ6 |
| K6 | PL_DDR3_D7 | 18 | DQ7 |
| G6 | PL_DDR3_D8 | 21 | DQ8 |
| H4 | PL_DDR3_D9 | 23 | DQ9 |
| H6 | PL_DDR3_D10 | 33 | DQ10 |
| H3 | PL_DDR3_D11 | 35 | DQ11 |
| G1 | PL_DDR3_D12 | 22 | DQ12 |
| H2 | PL_DDR3_D13 | 24 | DQ13 |
| G5 | PL_DDR3_D14 | 34 | DQ14 |
| G4 | PL_DDR3_D15 | 36 | DQ15 |
| E2 | PL_DDR3_D16 | 39 | DQ16 |
| E3 | PL_DDR3_D17 | 41 | DQ17 |
| D4 | PL_DDR3_D18 | 51 | DQ18 |
| E5 | PL_DDR3_D19 | 53 | DQ19 |
| F4 | PL_DDR3_D20 | 40 | DQ20 |
| F3 | PL_DDR3_D21 | 42 | DQ21 |
| D1 | PL_DDR3_D22 | 50 | DQ22 |
| D3 | PL_DDR3_D23 | 52 | DQ23 |
| A2 | PL_DDR3_D24 | 57 | DQ24 |
| B2 | PL_DDR3_D25 | 59 | DQ25 |

Table 1-4: DDR3 SODIMM Socket J1 Connections to the XC7Z045 AP SoC (Cont'd)

| XC7Z045 (U1) Pin | Net Name | SODIMM Memory | |
|------------------|-------------|---------------|----------|
| | | Pin Number | Pin Name |
| B4 | PL_DDR3_D26 | 67 | DQ26 |
| B5 | PL_DDR3_D27 | 69 | DQ27 |
| A3 | PL_DDR3_D28 | 56 | DQ28 |
| B1 | PL_DDR3_D29 | 58 | DQ29 |
| C1 | PL_DDR3_D30 | 68 | DQ30 |
| C4 | PL_DDR3_D31 | 70 | DQ31 |
| K10 | PL_DDR3_D32 | 129 | DQ32 |
| L9 | PL_DDR3_D33 | 131 | DQ33 |
| K12 | PL_DDR3_D34 | 141 | DQ34 |
| J9 | PL_DDR3_D35 | 143 | DQ35 |
| K11 | PL_DDR3_D36 | 130 | DQ36 |
| L10 | PL_DDR3_D37 | 132 | DQ37 |
| J10 | PL_DDR3_D38 | 140 | DQ38 |
| L7 | PL_DDR3_D39 | 142 | DQ39 |
| F14 | PL_DDR3_D40 | 147 | DQ40 |
| F15 | PL_DDR3_D41 | 149 | DQ41 |
| F13 | PL_DDR3_D42 | 157 | DQ42 |
| G16 | PL_DDR3_D43 | 159 | DQ43 |
| G15 | PL_DDR3_D44 | 146 | DQ44 |
| E12 | PL_DDR3_D45 | 148 | DQ45 |
| D13 | PL_DDR3_D46 | 158 | DQ46 |
| E13 | PL_DDR3_D47 | 160 | DQ47 |
| D15 | PL_DDR3_D48 | 163 | DQ48 |
| E15 | PL_DDR3_D49 | 165 | DQ49 |
| D16 | PL_DDR3_D50 | 175 | DQ50 |
| E16 | PL_DDR3_D51 | 177 | DQ51 |
| C17 | PL_DDR3_D52 | 164 | DQ52 |
| B16 | PL_DDR3_D53 | 166 | DQ53 |
| D14 | PL_DDR3_D54 | 174 | DQ54 |
| B17 | PL_DDR3_D55 | 176 | DQ55 |
| B12 | PL_DDR3_D56 | 181 | DQ56 |
| C12 | PL_DDR3_D57 | 183 | DQ57 |
| A12 | PL_DDR3_D58 | 191 | DQ58 |
| A14 | PL_DDR3_D59 | 193 | DQ59 |
| A13 | PL_DDR3_D60 | 180 | DQ60 |

Table 1-4: DDR3 SODIMM Socket J1 Connections to the XC7Z045 AP SoC (Cont'd)

| XC7Z045 (U1) Pin | Net Name | SODIMM Memory | |
|------------------|--------------------|---------------|------------|
| | | Pin Number | Pin Name |
| B11 | PL_DDR3_D61 | 182 | DQ61 |
| C14 | PL_DDR3_D62 | 192 | DQ62 |
| B14 | PL_DDR3_D63 | 194 | DQ63 |
| J3 | PL_DDR3_DM0 | 11 | DM0 |
| F2 | PL_DDR3_DM1 | 28 | DM1 |
| E1 | PL_DDR3_DM2 | 46 | DM2 |
| C2 | PL_DDR3_DM3 | 63 | DM3 |
| L12 | PL_DDR3_DM4 | 136 | DM4 |
| G14 | PL_DDR3_DM5 | 153 | DM5 |
| C16 | PL_DDR3_DM6 | 170 | DM6 |
| C11 | PL_DDR3_DM7 | 187 | DM7 |
| K2 | PL_DDR3_DQS0_N | 10 | DQS0_N |
| K3 | PL_DDR3_DQS0_P | 12 | DQS0_P |
| H1 | PL_DDR3_DQS1_N | 27 | DQS1_N |
| J1 | PL_DDR3_DQS1_P | 29 | DQS1_P |
| D5 | PL_DDR3_DQS2_N | 45 | DQS2_N |
| E6 | PL_DDR3_DQS2_P | 47 | DQS2_P |
| A4 | PL_DDR3_DQS3_N | 62 | DQS3_N |
| A5 | PL_DDR3_DQS3_P | 64 | DQS3_P |
| K8 | PL_DDR3_DQS4_N | 135 | DQS4_N |
| L8 | PL_DDR3_DQS4_P | 137 | DQS4_P |
| F12 | PL_DDR3_DQS5_N | 152 | DQS5_N |
| G12 | PL_DDR3_DQS5_P | 154 | DQS5_P |
| E17 | PL_DDR3_DQS6_N | 169 | DQS6_N |
| F17 | PL_DDR3_DQS6_P | 171 | DQS6_P |
| A15 | PL_DDR3_DQS7_N | 186 | DQS7_N |
| B15 | PL_DDR3_DQS7_P | 188 | DQS7_P |
| G7 | PL_DDR3_ODT0 | 116 | ODT0 |
| C9 | PL_DDR3_ODT1 | 120 | ODT1 |
| G17 | PL_DDR3_RESET_B | 30 | RESET_B |
| J11 | PL_DDR3_S0_B | 114 | S0_B |
| H8 | PL_DDR3_S1_B | 121 | S1_B |
| M10 | PL_DDR3_TEMP_EVENT | 198 | 98 EVENT_B |
| F7 | PL_DDR3_WE_B | 113 | WE_B |
| E7 | PL_DDR3_CAS_B | 115 | CAS_B |

Table 1-4: DDR3 SODIMM Socket J1 Connections to the XC7Z045 AP SoC (Cont'd)

| XC7Z045 (U1) Pin | Net Name | SODIMM Memory | |
|------------------|----------------|---------------|----------|
| | | Pin Number | Pin Name |
| H11 | PL_DDR3_RAS_B | 110 | RAS_B |
| D10 | PL_DDR3_CKE0 | 73 | CKE0 |
| C7 | PL_DDR3_CKE1 | 74 | CKE1 |
| F10 | PL_DDR3_CLK0_N | 103 | CK0_N |
| G10 | PL_DDR3_CLK0_P | 101 | CK0_P |
| D8 | PL_DDR3_CLK1_N | 104 | CK1_N |
| D9 | PL_DDR3_CLK1_P | 102 | CK1_P |

The ZC706 DDR3 SODIMM interface adheres to the constraints guidelines documented in the "Dynamic Memory" section of the *Zynq-7000 All Programmable SoC PCB Design and Pin Planning Guide* ([UG933](#)). The ZC706 DDR3 SODIMM interface is a 40Ω impedance implementation.

DDR3 Component Memory (PS)

[Figure 1-2, callout 3]

The 1 GB, 32-bit wide DDR3 component memory system is comprised of four 256 Mb x 8 SDRAMs (Micron MT41J256M8HX-15E) at U2-U5. This memory system is connected to the XC7Z045 AP SoC Processing System (PS) memory interface bank 502. The DDR3 0.75V VTT termination voltage is sourced from linear regulator U27. The connections between the DDR3 component memory and XC7Z045 AP SoC bank 502 are listed in [Table 1-5](#).

Table 1-5: DDR3 Component Memory Connections to the XC7Z045 AP SoC

| XC7Z045 (U1) Pin | Net Name | Component Memory | | |
|------------------|--------------|------------------|----------|-----------|
| | | Pin Number | Pin Name | Ref. Des. |
| E26 | PS_DDR3_DQ0 | B3 | DQ0 | U2 |
| A25 | PS_DDR3_DQ1 | C7 | DQ1 | U2 |
| E27 | PS_DDR3_DQ2 | C2 | DQ2 | U2 |
| E25 | PS_DDR3_DQ3 | C8 | DQ3 | U2 |
| D26 | PS_DDR3_DQ4 | E3 | DQ4 | U2 |
| B25 | PS_DDR3_DQ5 | E8 | DQ5 | U2 |
| D25 | PS_DDR3_DQ6 | D2 | DQ6 | U2 |
| B27 | PS_DDR3_DQ7 | E7 | DQ7 | U2 |
| A27 | PS_DDR3_DQ8 | B3 | DQ8 | U3 |
| A28 | PS_DDR3_DQ9 | C7 | DQ9 | U3 |
| A29 | PS_DDR3_DQ10 | C2 | DQ10 | U3 |
| C28 | PS_DDR3_DQ11 | C8 | DQ11 | U3 |

Table 1-5: DDR3 Component Memory Connections to the XC7Z045 AP SoC (Cont'd)

| XC7Z045 (U1) Pin | Net Name | Component Memory | | |
|------------------|----------------|------------------|----------|----------------|
| | | Pin Number | Pin Name | Ref. Des. |
| D30 | PS_DDR3_DQ12 | E3 | DQ12 | U3 |
| A30 | PS_DDR3_DQ13 | E8 | DQ13 | U3 |
| D29 | PS_DDR3_DQ14 | D2 | DQ14 | U3 |
| D28 | PS_DDR3_DQ15 | E7 | DQ15 | U3 |
| H27 | PS_DDR3_DQ16 | B3 | DQ16 | U4 |
| G27 | PS_DDR3_DQ17 | C7 | DQ17 | U4 |
| H28 | PS_DDR3_DQ18 | C2 | DQ18 | U4 |
| E28 | PS_DDR3_DQ19 | C8 | DQ19 | U4 |
| E30 | PS_DDR3_DQ20 | E3 | DQ20 | U4 |
| F28 | PS_DDR3_DQ21 | E8 | DQ21 | U4 |
| G30 | PS_DDR3_DQ22 | D2 | DQ22 | U4 |
| F30 | PS_DDR3_DQ23 | E7 | DQ23 | U4 |
| K27 | PS_DDR3_DQ24 | B3 | DQ24 | U5 |
| J30 | PS_DDR3_DQ25 | C7 | DQ25 | U5 |
| J28 | PS_DDR3_DQ26 | C2 | DQ26 | U5 |
| J29 | PS_DDR3_DQ27 | C8 | DQ27 | U5 |
| K30 | PS_DDR3_DQ28 | E3 | DQ28 | U5 |
| M29 | PS_DDR3_DQ29 | E8 | DQ29 | U5 |
| L30 | PS_DDR3_DQ30 | D2 | DQ30 | U5 |
| M30 | PS_DDR3_DQ31 | E7 | DQ31 | U5 |
| C27 | PS_DDR3_DM0 | B7 | DM0 | U2 |
| C26 | PS_DDR3_DQS0_P | C3 | DQS0_P | U2 |
| B26 | PS_DDR3_DQS0_N | D3 | DQS0_N | U2 |
| B30 | PS_DDR3_DM1 | B7 | DM1 | U3 |
| C29 | PS_DDR3_DQS1_P | C3 | DQS1_P | U3 |
| B29 | PS_DDR3_DQS1_N | D3 | DQS1_N | U3 |
| H29 | PS_DDR3_DM2 | B7 | DM2 | U4 |
| G29 | PS_DDR3_DQS2_P | C3 | DQS2_P | U4 |
| F29 | PS_DDR3_DQS2_N | D3 | DQS2_N | U4 |
| K28 | PS_DDR3_DM3 | B7 | DM3 | U5 |
| L28 | PS_DDR3_DQS3_P | C3 | DQS3_P | U5 |
| L29 | PS_DDR3_DQS3_N | D3 | DQS3_N | U5 |
| L25 | PS_DDR3_A0 | K3 | A0 | U2, U3, U4, U5 |
| K26 | PS_DDR3_A1 | L7 | A1 | U2, U3, U4, U5 |
| L27 | PS_DDR3_A2 | L3 | A2 | U2, U3, U4, U5 |

Table 1-5: DDR3 Component Memory Connections to the XC7Z045 AP SoC (Cont'd)

| XC7Z045 (U1) Pin | Net Name | Component Memory | | |
|------------------|-----------------|------------------|----------|----------------|
| | | Pin Number | Pin Name | Ref. Des. |
| G25 | PS_DDR3_A3 | K2 | A3 | U2, U3, U4, U5 |
| J26 | PS_DDR3_A4 | L8 | A4 | U2, U3, U4, U5 |
| G24 | PS_DDR3_A5 | L2 | A5 | U2, U3, U4, U5 |
| H26 | PS_DDR3_A6 | M8 | A6 | U2, U3, U4, U5 |
| K22 | PS_DDR3_A7 | M2 | A7 | U2, U3, U4, U5 |
| F27 | PS_DDR3_A8 | N8 | A8 | U2, U3, U4, U5 |
| J23 | PS_DDR3_A9 | M3 | A9 | U2, U3, U4, U5 |
| G26 | PS_DDR3_A10 | H7 | A10 | U2, U3, U4, U5 |
| H24 | PS_DDR3_A11 | M7 | A11 | U2, U3, U4, U5 |
| K23 | PS_DDR3_A12 | K7 | A12 | U2, U3, U4, U5 |
| H23 | PS_DDR3_A13 | N3 | A13 | U2, U3, U4, U5 |
| J24 | PS_DDR3_A14 | N7 | A14 | U2, U3, U4, U5 |
| M27 | PS_DDR3_BA0 | J2 | BA0 | U2, U3, U4, U5 |
| M26 | PS_DDR3_BA1 | K8 | BA1 | U2, U3, U4, U5 |
| M25 | PS_DDR3_BA2 | J3 | BA2 | U2, U3, U4, U5 |
| K25 | PS_DDR3_CLK_P | F7 | CK | U2, U3, U4, U5 |
| J25 | PS_DDR3_CLK_N | G7 | CK_B | U2, U3, U4, U5 |
| M22 | PS_DDR3_CKE | G9 | CKE | U2, U3, U4, U5 |
| N23 | PS_DDR3_WE_B | H3 | WE_B | U2, U3, U4, U5 |
| M24 | PS_DDR3_CAS_B | G3 | CAS_B | U2, U3, U4, U5 |
| N24 | PS_DDR3_RAS_B | F3 | RAS_B | U2, U3, U4, U5 |
| F25 | PS_DDR3_RESET_B | N2 | RESET_B | U2, U3, U4, U5 |
| N22 | PS_DDR3_CS_B | H2 | CS_B | U2, U3, U4, U5 |
| L23 | PS_DDR3_ODT | G1 | ODT | U2, U3, U4, U5 |
| N21 | PS_VRN | | | |
| M21 | PS_VRP | | | |
| L22 | VTTVREF_PS | | | |
| L24 | VTTVREF_PS | | | |

The ZC706 DDR3 component interface adheres to the constraints guidelines documented in the *DDR3 Design Guidelines* section of *Zynq-7000 All Programmable SoC PCB Design and Pin Planning Guide* ([UG933](#)). The ZC706 DDR3 component interface is a 40Ω impedance implementation.

Quad-SPI Flash Memory

[Figure 1-2, callout 4]

The Quad-SPI flash memory located at U58 and U59 provides 2 x 128 Mb of non-volatile storage that can be used for configuration and data storage.

- Part number: S25FL128SAGMFIR01 (Spansion)
- Supply voltage: 1.8V
- Data path width: 4 bits
- Data rate: Various depending on Single/Dual/Quad mode

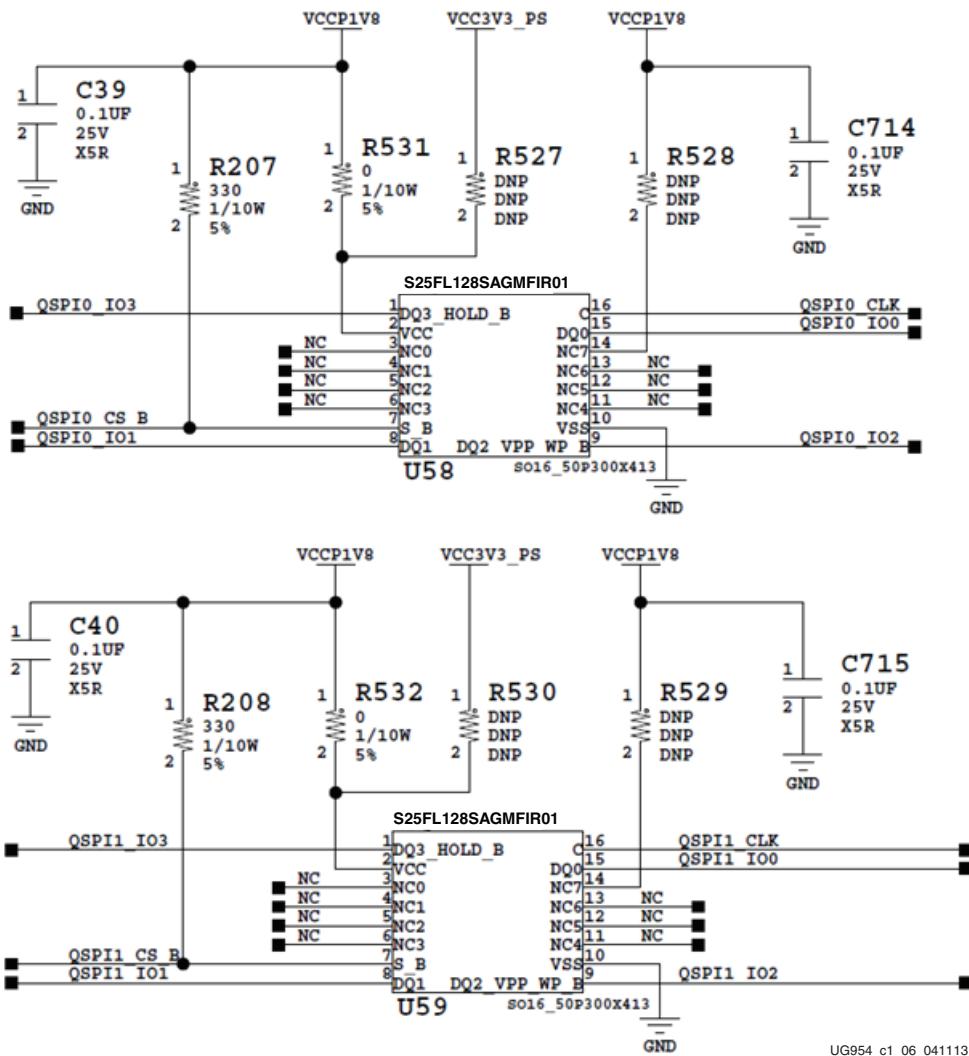
The connections between the SPI flash memory and the XC7Z045 AP SoC are listed in [Table 1-6](#).

Table 1-6: Quad-SPI Flash Memory Connections to the XC7Z045 AP SoC

| XC7Z045 (U1) | | | Schematic Net Name | Quad-SPI Flash Memory | | QSPI Device | MIO Select Header |
|--------------|------|------------|--------------------|-----------------------|------------|-------------|-------------------|
| Pin Name | Bank | Pin Number | | Pin Number | Pin Name | | |
| PS_MIO6 | 500 | D24 | QSPI0_CLK | 16 | C | U58 | J74.2 |
| PS_MIO5 | 500 | C24 | QSPI0_IO3 | 1 | DQ3_HOLD_B | U58 | J73.2 |
| PS_MIO4 | 500 | E23 | QSPI0_IO2 | 9 | WP_B | U58 | J72.2 |
| PS_MIO3 | 500 | C23 | QSPI0_IO1 | 8 | DQ1 | U58 | J71.2 |
| PS_MIO2 | 500 | F23 | QSPI0_IO0 | 15 | DQ0 | U58 | J70.2 |
| PS_MIO1 | 500 | D23 | QSPI0_CS_B | 7 | S_B | U58 | N/A |
| PS_MIO9 | 500 | A24 | QSPI1_CLK | 16 | C | U59 | N/A |
| PS_MIO13 | 500 | F22 | QSPI1_IO3 | 1 | DQ3_HOLD_B | U59 | N/A |
| PS_MIO12 | 500 | E21 | QSPI1_IO2 | 9 | WP_B | U59 | N/A |
| PS_MIO11 | 500 | A23 | QSPI1_IO1 | 8 | DQ1 | U59 | N/A |
| PS_MIO10 | 500 | E22 | QSPI1_IO0 | 15 | DQ0 | U59 | N/A |
| PS_MIO0 | 500 | F24 | QSPI1_CS_B | 7 | S_B | U59 | N/A |

The configuration section of [UG585, Zynq-7000 All Programmable SoC Technical Reference Manual](#) provides details on using the Quad-SPI flash memory.

[Figure 1-6](#) shows the connections of the linear Quad-SPI flash memory on the ZC706 evaluation board. For more details, see the Spansion S25FL128SAGMFIR01 data sheet (www.spansion.com).



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Figure 1-6: 128 Mb Quad-SPI Flash Memory

USB 2.0 ULPI Transceiver

[Figure 1-2, callout 19]

The ZC706 evaluation board uses a Standard Microsystems Corporation USB3320 USB 2.0 ULPI Transceiver at U12 to support a USB connection to the host computer. A USB cable is supplied in the ZC706 evaluation kit (Standard-A connector to host computer, Micro-B connector to ZC706 evaluation board connector J2). The USB3320 is a high-speed USB 2.0 PHY supporting the UTMI+ low pin interface (ULPI) interface standard. The ULPI standard defines the interface between the USB controller IP and the PHY device which drives the physical USB bus. Use of the ULPI standard reduces the interface pin count between the USB controller IP and the PHY device.

The USB3320 is clocked by a 24 MHz crystal. Consult the SMSC USB3320 data sheet at www.smsc.com/ for clocking mode details.

The interface to the USB3320 transceiver is implemented through the IP in the XC7Z045 AP SoC Processor System.

[Table 1-7](#) describes the jumper settings for the USB 2.0 circuit.

Table 1-7: USB Jumper Settings

| Header | Function | Shunt Position |
|--------|--------------------|---|
| J11 | USB PHY reset | Shunt ON = USB PHY reset Shunt OFF ⁽¹⁾ = USB PHY normal operation |
| J10 | Host/OTG or device | Shunt ON ⁽¹⁾ = Host or OTG mode Shunt OFF = Device mode |
| J48 | RVBUS select | Position 1-2 = Device mode (10 KΩ) Position 2-3 ⁽¹⁾ = Host or OTG mode (1 KΩ) |
| J50 | CVBUS select | Position 1-2 = 1 μF to GND Position 2-3 ⁽¹⁾ = 120 μF to GND |
| J49 | Cable ID select | Position 1-2 ⁽¹⁾ = A/B cable detect Position 2-3 = ID not used |
| J51 | USB Micro-B | Position 1-2 ⁽¹⁾ = Shield connected to GND Position 2-3 = Shield floating |

Notes:

1. Default shunt position

The connections between the USB Micro-B connector at J2 and the PHY at U12 are listed in [Table 1-8](#).

Table 1-8: USB Connector Pin Assignments and Signal Definitions Between J2 and U12

| USB Connector J1 | | Net Name | Description | USB3320 (U12) Pin |
|------------------|------|--------------|---|-------------------|
| Pin | Name | | | |
| 1 | VBUS | USB_VBUS_SEL | +5V from host system | 22 |
| 2 | D_N | USB_D_N | Bidirectional differential serial data (N-side) | 19 |
| 3 | D_P | USB_D_P | Bidirectional differential serial data (P-side) | 18 |
| 5 | GND | GND | Signal ground | 33 |

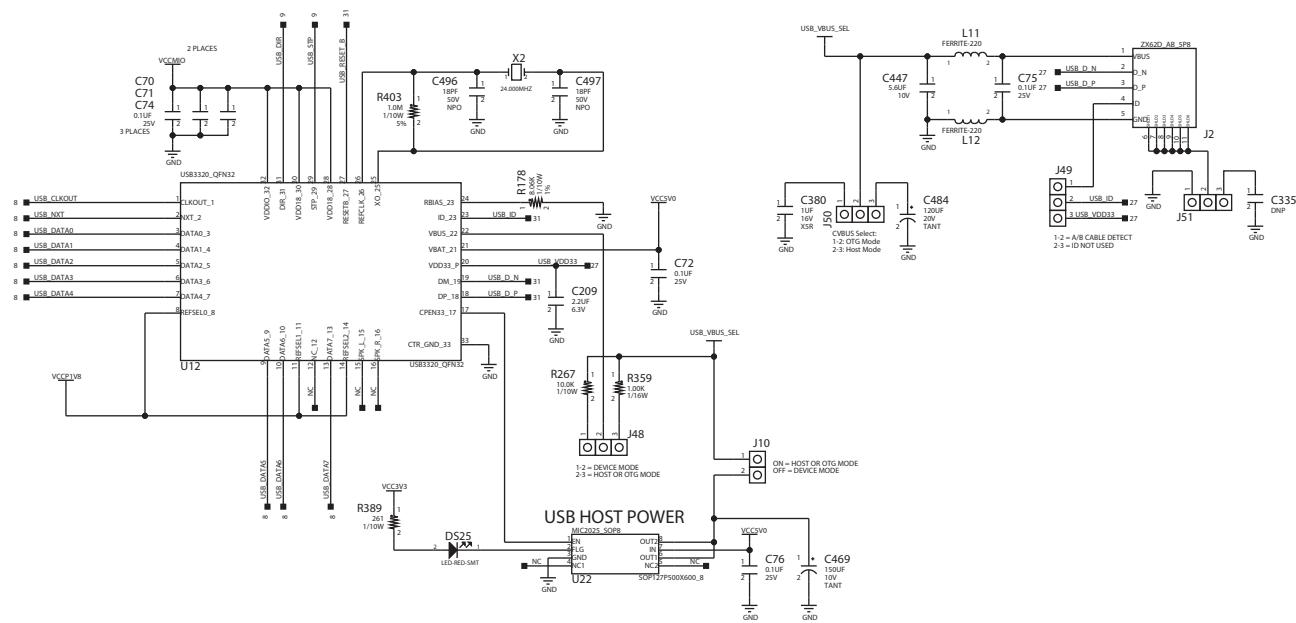
The connections between the USB 2.0 PHY at U12 and the XC7Z045 AP SoC are listed in [Table 1-9](#).

Table 1-9: USB 2.0 ULPI Transceiver Connections to the XC7Z045 AP SoC

| XC7Z045 (U1) | | | Schematic Net Name | USB3320 (U12) Pin |
|--------------|------|------------|--------------------|-----------------------|
| Pin Name | Bank | Pin Number | | |
| PS_MIO36 | 501 | H17 | USB_CLKOUT | 1 |
| PS_MIO31 | 501 | H21 | USB_NXT | 2 |
| PS_MIO32 | 501 | K17 | USB_DATA0 | 3 |
| PS_MIO33 | 501 | G22 | USB_DATA1 | 4 |
| PS_MIO34 | 501 | K18 | USB_DATA2 | 5 |
| PS_MIO35 | 501 | G21 | USB_DATA3 | 6 |
| PS_MIO28 | 501 | L17 | USB_DATA4 | 7 |
| PS_MIO37 | 501 | B21 | USB_DATA5 | 9 |
| PS_MIO38 | 501 | A20 | USB_DATA6 | 10 |
| PS_MIO39 | 501 | F18 | USB_DATA7 | 13 |
| PS_MIO30 | 501 | L18 | USB_STP | 29 |
| PS_MIO29 | 501 | E8 | USB_DIR | 31 |
| PS_MIO7 | 500 | D5 | USB_RESET_B_AND | 27 (via AND gate U13) |

For additional information on the Zynq-7000 AP SoC device USB controllers, see *Zynq-7000 All Programmable SoC Overview* ([DS190](#)) and *Zynq-7000 All Programmable SoC Technical Reference Manual* ([UG585](#)).

[Figure 1-7](#) shows the USB 2.0 ULPI transceiver circuitry. Note that the shield for the USB Micro-B connector (J2) can be tied to GND by a jumper on header J51 pins 1–2 (default). The USB shield can optionally be connected through a capacitor to GND by installing a capacitor (body size 0402) at location C335 and jumping pins 2–3 on header J51.



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Figure 1-7: USB 2.0 ULPI Transceiver

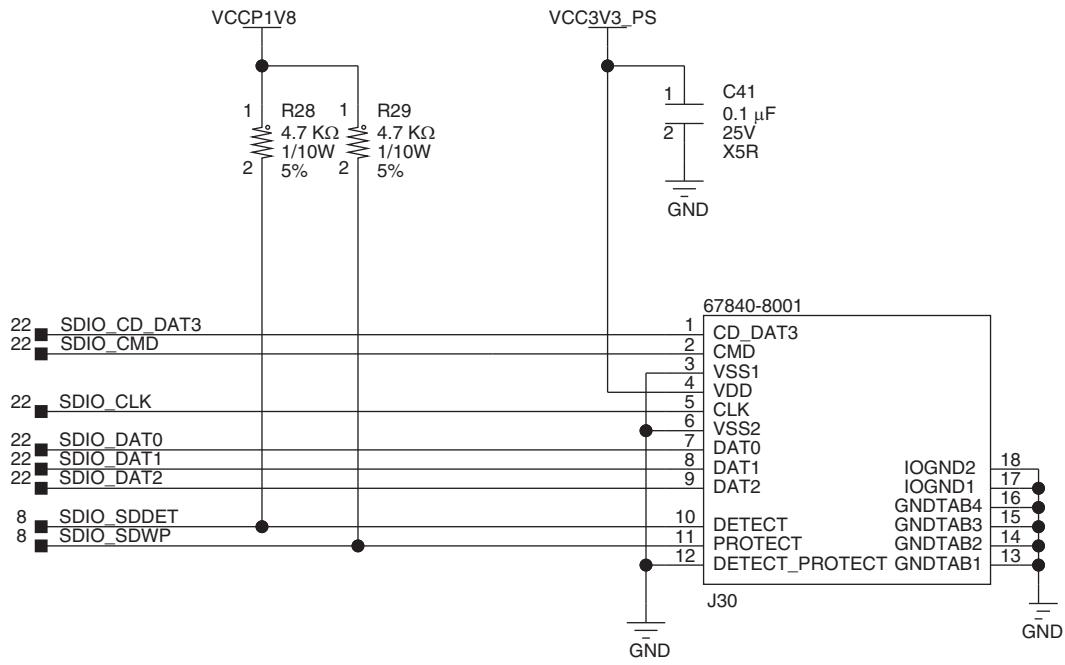
SD Card Interface

[Figure 1-2, callout 5]

The ZC706 evaluation board includes a secure digital input/output (SDIO) interface to provide user-logic access to general purpose non-volatile SDIO memory cards and peripherals. Information for the SD I/O card specification may be found at www.sandisk.com or www.sdcards.org.

The SDIO signals are connected to XC7Z045 AP SoC PS bank 501 which has its VCCMIO set to 1.8V. A MAX13035E high-speed logic-level translator (U11) is used between XC7Z045 AP SoC 1.8V PS bank 501 and the 3.3V SD card connector (J30).

Figure 1-8 shows the connections of the SD card interface on the ZC706 evaluation board.



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Figure 1-8: SD Card Interface

Table 1-10 lists the SD card interface connections to the XC7Z045 AP SoC

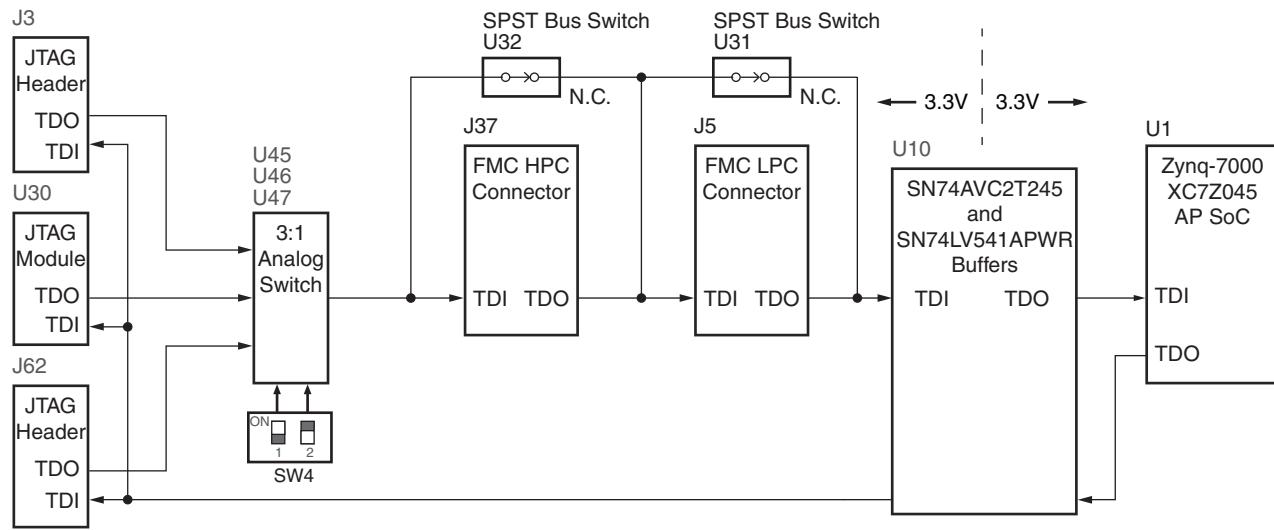
Table 1-10: SDIO Connections to the XC7Z045 AP SoC

| XC7Z045 (U1) Pin | | | Schematic Net Name | Level Shifter (U11) | | SDIO Connector (J30) | |
|------------------|------|------------|--------------------|---------------------|---------------|----------------------|----------|
| Pin Name | Bank | Pin Number | | 1.8V Side Pin | 3.3V Side Pin | Pin Number | Pin Name |
| PS_MIO15 | 500 | C22 | SDIO_SDWP | N/A | N/A | 11 | PROTECT |
| PS_MIO14 | 500 | B22 | SDIO_SDDET | N/A | N/A | 10 | DETECT |
| PS_MIO41 | 501 | J18 | SDIO_CMD_LS | 4 | 20 | 2 | CMD |
| PS_MIO40 | 501 | B20 | SDIO_CLK_LS | 9 | 19 | 5 | CLK |
| PS_MIO44 | 501 | E20 | SDIO_DAT2_LS | 1 | 23 | 9 | DAT2 |
| PS_MIO43 | 501 | E18 | SDIO_DAT1_LS | 7 | 16 | 8 | DAT1 |
| PS_MIO42 | 501 | D20 | SDIO_DAT0_LS | 6 | 18 | 7 | DAT0 |
| PS_MIO45 | 501 | H18 | SDIO_CD_DAT3_LS | 3 | 22 | 1 | CD_DAT3 |

Programmable Logic JTAG Programming Options

[Figure 1-2, callout 6]

The ZC706 evaluation board JTAG chain is shown in Figure 1-9.



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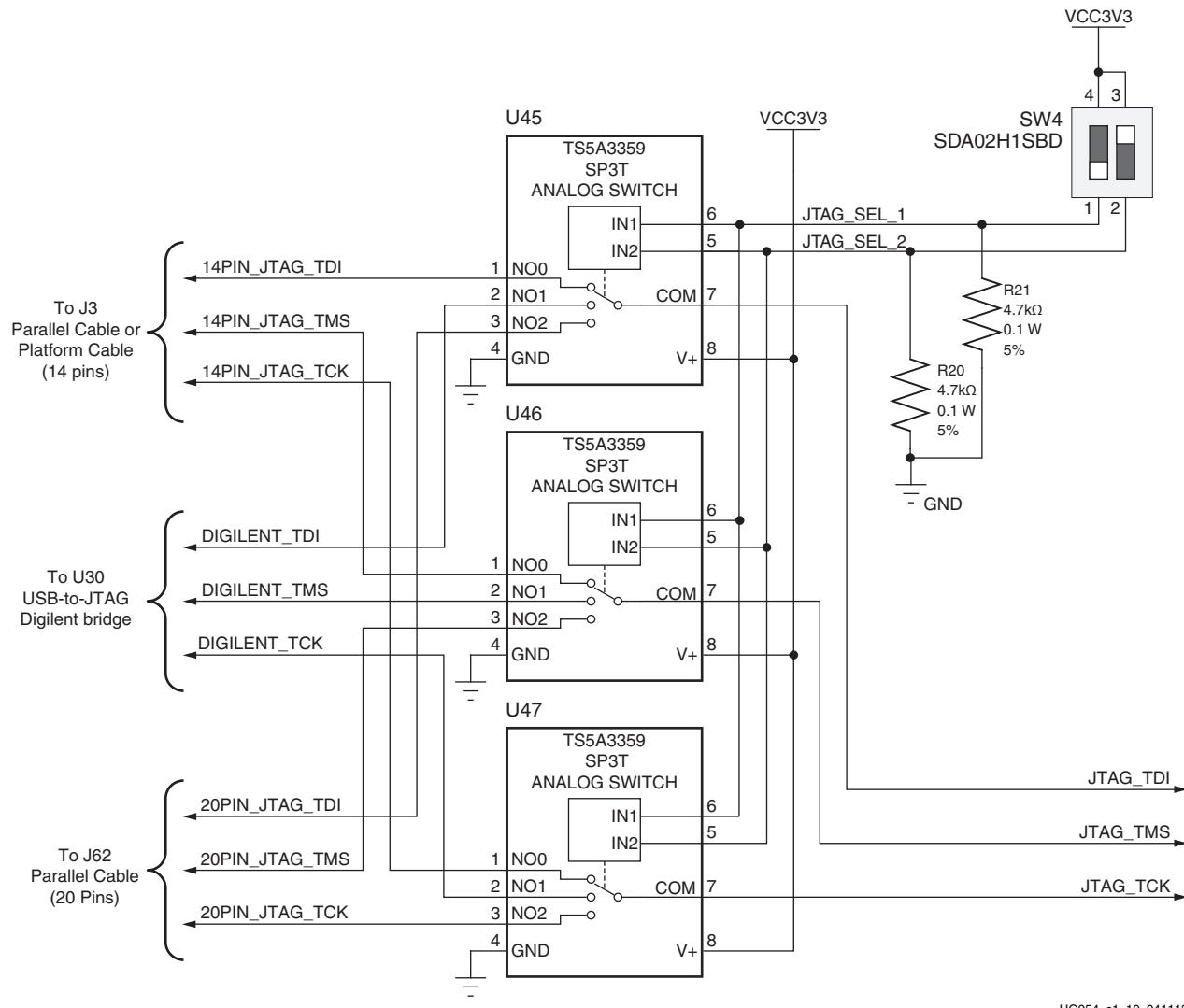
Figure 1-9: JTAG Chain Block Diagram

Programmable Logic JTAG Select Switch

[Figure 1-2, callout 35]

The PL JTAG chain can be programmed by three different methods made available via a 3-to-1 analog switch (U45, U46, and U47) controlled by a 2-position DIP switch at SW4.

Figure 1-10 shows the JTAG analog switches and DIP switch SW4.



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Figure 1-10: PL JTAG Programming Source Analog Switch

DIP switch SW4[1:2] setting 10 selects the 14-pin header J3 for configuration using either a Parallel Cable IV (PC4) or Platform Cable USB II. DIP switch SW4 setting 01 selects the USB-to-JTAG Digilent bridge U30 for configuration over a Standard-A to Micro-B USB cable. DIP switch SW4 setting 11 selects the JTAG 20-pin header at J62. The four JTAG signals TDI, TDO, TCK, and TMS would be connected to J62 via flying leads from a JTAG cable. The 3-to-1 analog switch settings are shown in [Table 1-11](#).

Table 1-11: Switch SW4 Configuration Option Settings

| Configuration Source | DIP Switch SW4 | |
|------------------------------------|------------------------------------|------------------------------------|
| | Switch 1 ⁽¹⁾ JTAG_SEL_1 | Switch 2 ⁽¹⁾ JTAG_SEL_2 |
| None | 0 | 0 |
| Cable Connector J3 ⁽²⁾ | 1 | 0 |
| Digilent USB-to-JTAG interface U30 | 0 | 1 |
| JTAG (flying lead) Header J62 | 1 | 1 |

Notes:

1. 0 = open, 1 = closed
2. Default switch setting

FMC Connector JTAG Bypass

When an FPGA mezzanine card (FMC) is attached to HPC J37 or LPC J5 it is automatically added to the JTAG chain through electronically controlled single-pole single-throw (SPST) switches U32 and U31 respectively. The SPST switches are normally closed and transition to an open state when an FMC is attached. Switch U32 adds an attached FMC to the JTAG chain as determined by the FMC_HPC_PRSNT_M2C_B signal. Switch U31 adds an attached FMC to the JTAG chain as determined by the FMC_LPC_PRSNT_M2C_B signal. The attached FMC card must implement a TDI-to-TDO connection via a device or bypass jumper for the JTAG chain to be completed to the AP SoC U1.

The JTAG connectivity on the ZC706 board allows a host computer to download bitstreams to the FPGA using the Xilinx® iMPACT software. In addition, the JTAG connector allows debug tools such as the ChipScope™ Pro analyzer or a software debugger to access the FPGA. The iMPACT software tool can also indirectly program the linear QSPI flash memory. To accomplish this, the iMPACT software configures the FPGA with a temporary design to access and program the QSPI memory device.

Clock Generation

[Figure 1-2, callouts 7, 8, and 9]

The ZC706 evaluation board provides four clock sources for the XC7Z045 AP SoC. Table 1-12 lists the source devices for each clock.

Table 1-12: ZC706 Evaluation Board Clock Sources

| Clock Name | Clock Source | Description |
|-------------------------|----------------|--|
| System Clock | U64 | SiT9102 2.5V LVDS 200 MHz fixed-frequency oscillator (SiTime). See System Clock, page 34 . |
| User Clock | U37 | Si570 3.3V LVDS I ² C programmable oscillator, 156.250 MHz default (Silicon Labs). See Programmable User Clock, page 35 . |
| User SMA Clock | J67(P), J68(N) | User clock input SMAs, limit input swing voltage to VADJ_FPGA setting (1.8V, 2.5V, 3.3V). See User SMA Clock Source, page 36 . |
| PS Clock | U24 | SIT8103 1.8V single-ended CMOS 33.3333 MHz fixed frequency oscillator (SiTime). See Processing System Clock Source, page 37 . |
| GTX SMA REF Clock | J36(P), J31(N) | User clock input SMAs. See GTX SMA Clock (SMA_MGT_REFCLK_P and SMA_MGT_REFCLK_N), page 37 . |
| Jitter Attenuated Clock | U60 | Si5324C LVDS precision clock multiplier/jitter attenuator (Silicon Labs). See Jitter Attenuated Clock, page 38 . |

Table 1-13 lists the pin-to-pin connections from each clock source to the XC7Z045 AP SoC.

Table 1-13: Clock Connections, Source to XC7Z045 AP SoC

| Clock Source Pin | Net Name | XC7Z045 (U1) Pin |
|------------------|------------------|------------------|
| U64.5 | SYSCLK_N | G9 |
| U64.4 | SYSCLK_P | H9 |
| U37.5 | USRCLK_N | AG14 |
| U37.4 | USRCLK_P | AF14 |
| J67.1 | USER_SMA_CLOCK_P | AD18 |
| J68.1 | USER_SMA_CLOCK_N | AD19 |
| J24.3 | PS_CLK | A22 (Bank 500) |
| J36.1 | SMA_MGT_REFCLK_P | W8 |
| J31.1 | SMA_MGT_REFCLK_N | W7 |
| U60.28 | SI5324_OUT_C_P | AC8 |
| U60.29 | SI5324_OUT_C_N | AC7 |

System Clock

[Figure 1-2, callout 7]

The system clock source is an LVDS 200 MHz oscillator at U64. It is wired to a multi-region clock capable (MRCC) input on programmable logic (PL) bank 34. The signal pair is named SYSCLK_P and SYSCLK_N and each signal is connected to U1 (pins H9 and G9, respectively) on the XC7Z045 AP SoC.

- Oscillator: SiTime SiT9102AI-243N25E200.00000 (200 MHz)
- Frequency jitter: 50 ppm

- LVDS Differential Output

The system clock circuit is shown in [Figure 1-11](#).

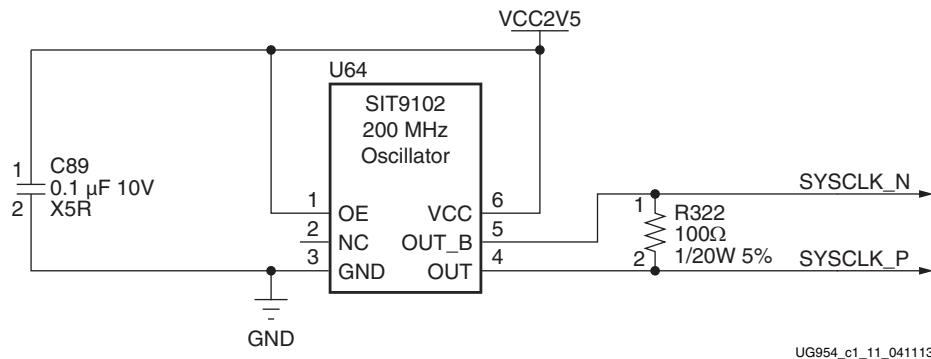


Figure 1-11: System Clock Source

For more details, see the SiTime SiT9102 data sheet at www.sitime.com.

Programmable User Clock

[[Figure 1-2](#), callout 8]

The ZC706 evaluation board has a programmable low-jitter 3.3V LVDS differential oscillator (U37) connected to the MRCC inputs of bank 10. This USRCLK_P and USRCLK_N clock signal pair is connected to XC7Z045 AP SoC U1 pins AF14 and AG14, respectively. On power-up the user clock defaults to an output frequency of 156.250 MHz. User applications can change the output frequency within the range of 10 MHz to 810 MHz through an I²C interface. Power cycling the ZC706 evaluation board reverts the user clock to the default frequency of 156.250 MHz.

- Programmable Oscillator: Silicon Labs Si570BAB0000544DG (10 MHz–810 MHz)
- Frequency jitter: 50 ppm
- LVDS Differential Output

The user clock circuit is shown in [Figure 1-12](#).

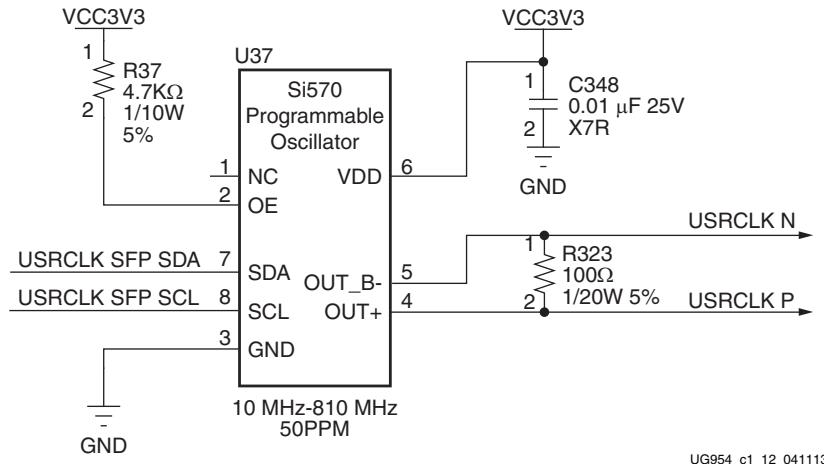


Figure 1-12: User Clock Source

The Silicon Labs Si570 data sheet is available from www.silabs.com.

User SMA Clock Source

The ZC706 board provides a pair of SMAs for differential user clock input into PL Bank 9 (see Figure 1-13). The P-side SMA J67 signal USER_SMA_CLOCK_P is connected to U1 pin AD18, with the N-side SMA J68 signal USER_SMA_CLOCK_N connected to U1 pin AD19. Bank 9 Vcco is VADJ_FPGA, a variable voltage (1.8V, 2.5V, 3.3V) depending on the ZC706 FMC interface banks voltage. The USER_SMA_CLOCK input voltage swing should not exceed the board VADJ_FPGA voltage setting.

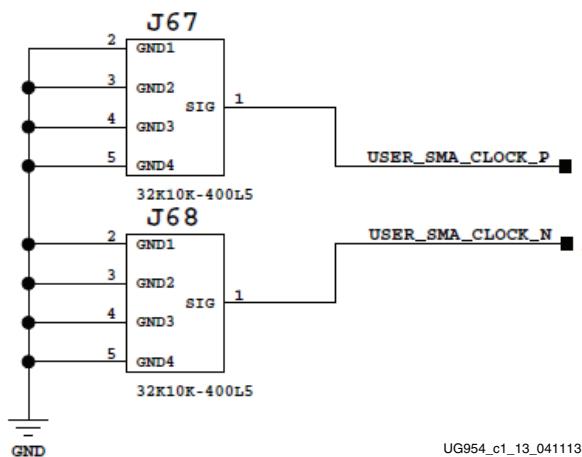


Figure 1-13: User SMA Clock

Processing System Clock Source

The Processing System (PS) clock source is a 1.8V LVC MOS single-ended fixed 33.33333 MHz oscillator at U24. It is wired to PS bank 500, pin A22 (PS_CLK), on the XC7Z045 AP SoC.

- Oscillator: SiTime SiT8103AC-23-18E-33.33333 (33.3 MHz)
- Frequency jitter: 50 ppm
- Single-ended output

The system clock circuit is shown in [Figure 1-14](#).

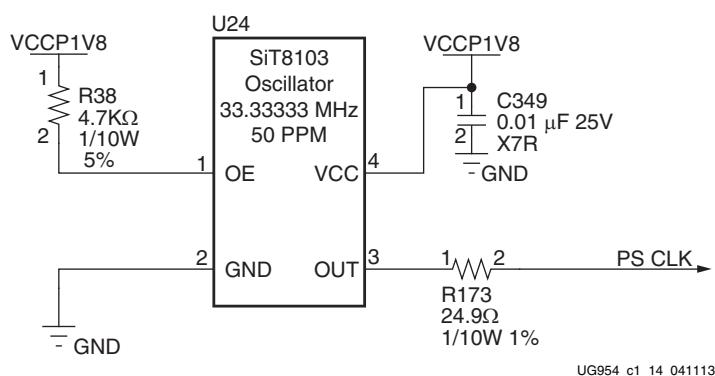


Figure 1-14: Processing System Clock Source

For more details, see the SiTime SiT8103 data sheet at www.sitime.com.

GTX SMA Clock (SMA_MGT_REFCLK_P and SMA_MGT_REFCLK_N)

[[Figure 1-2](#), callout 10]

The ZC706 board includes a pair of SMA connectors for a GTX clock wired to GTX Quad bank 111. This differential clock has signal names SMA_MGT_REFCLK_P and SMA_MGT_REFCLK_N, which are connected to AP SoC U1 pins W8 and W7 respectively.

- External user-provided GTX reference clock on SMA input connectors
- Differential Input

[Figure 1-15](#) shows this AC-coupled clock circuit.

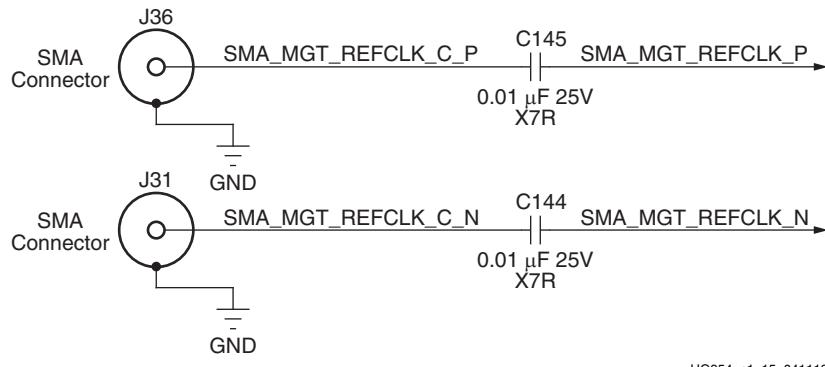


Figure 1-15: GTX SMA Clock Source

Jitter Attenuated Clock

[Figure 1-2, callout 11]

The ZC706 board includes a Silicon Labs Si5324 jitter attenuator U60 on the back side of the board. AP SoC user logic can implement a clock recovery circuit and then output this clock to a differential I/O pair on I/O bank 9 (REC_CLOCK_C_P, AP SoC U1 pin AD20 and REC_CLOCK_C_N, AP SoC U1 pin AE20) for jitter attenuation. The jitter attenuated clock (Si5324_OUT_C_P, Si5324_OUT_C_N) is then routed as a reference clock to GTX Quad 110 inputs MGTREFCLK1P (AP SoC U1 pin AC8) and MGTREFCLK1N (AP SoC U1 pin AC7).

The primary purpose of this clock is to support CPRI/OBSAI applications that perform clock recovery from a user-supplied SFP/SFP+ module and use the jitter attenuated recovered clock to drive the reference clock inputs of a GTX transceiver. The jitter attenuated clock circuit is shown in [Figure 1-16](#).

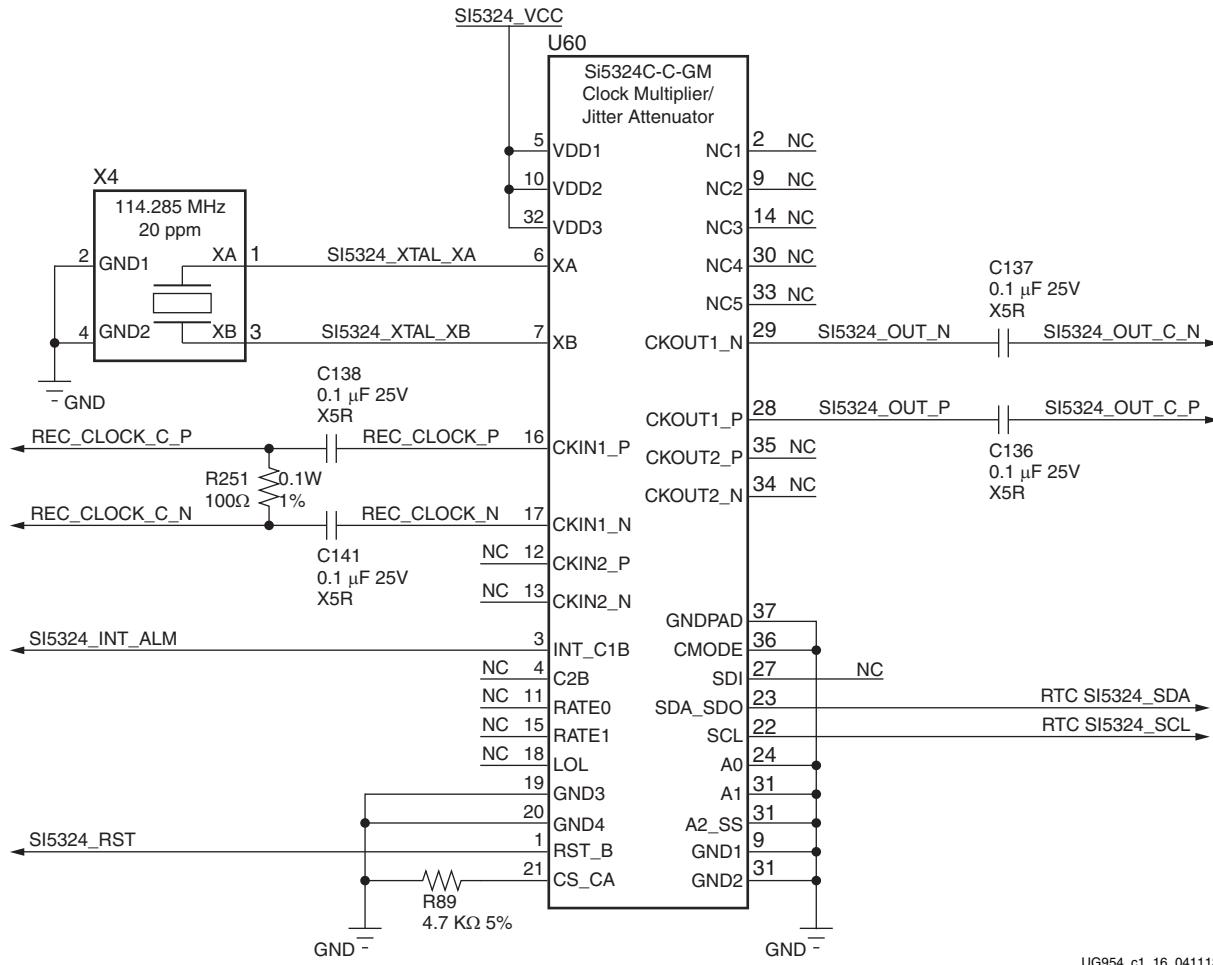


Figure 1-16: Jitter Attenuated Clock

The Silicon Labs Si5324 data sheet is available from www.silabs.com.

GTX Transceivers

[Figure 1-2, callout 12]

The ZC706 board provides access to 16 GTX transceivers:

- Four of the GTX transceivers are wired to the PCI Express x4 endpoint edge connector (P4) fingers
- Eight of the GTX transceivers are wired to the FMC HPC connector (J37)
- One GTX transceiver is wired to the FMC LPC connector (J5)
- One GTX transceiver is wired to SMA connectors (RX: J32, J33 TX: J35, J34)
- One GTX transceiver is wired to the SFP/SFP+ Module connector (P2)

- One GTX transceiver is unused and is wired in a capacitively coupled TX-to-RX loopback configuration

The GTX transceivers in Zynq-7000 series AP SoCs are grouped into four channels described as Quads. The reference clock for a Quad can be sourced from the Quad above or Quad below the GTX Quad of interest. There are four GTX Quads on the ZC706 board with connectivity as shown here:

- Quad 109:
 - MGTREFCLK0 - FMC_HPC_GBTCLK0_M2C clock
 - MGTREFCLK1 - not connected
 - Contains 4 GTX transceivers allocated to FMC_HPC_DP[3:0]_C2M_P/N
- Quad 110:
 - MGTREFCLK0 - FMC_HPC_GBTCLK1_M2C clock
 - MGTREFCLK1 - SI5324_OUT_C_P/N jitter attenuator clock
 - Contains 4 GTX transceivers allocated to FMC_HPC_DP[7:4]_C2M_P/N
- Quad 111:
 - MGTREFCLK0 - FMC_LPC_GBTCLK0_M2C_C_P/N
 - MGTREFCLK1 - SMA_MGT_REFCLK_P/N SMA GTX clock input
 - Contains 1 GTX transceiver allocated to FMC_LPC_DP0_C2M_P/N
 - Contains 1 GTX transceiver allocated to SMA_MGT_TX_P/N and RX_P/N SMA connectors
 - Contains 1 GTX transceiver allocated to SFP_TX and _RX_P/N SFP/SFP+ connector
 - Contains 1 GTX transceiver which is unused and is wired in TX-to-RX loopback configuration
- Quad 112:
 - MGTREFCLK0 - PCIE_CLK_Q0_P/N PCIe edge connector clock
 - MGTREFCLK1 - not connected
 - Contains 4 GTX transceivers allocated to PCIe lanes 0-3

[Table 1-15](#) lists the GTX Banks 109 and 110 interface connections between the AP SoC U1 and FMC HPC connector J37.

Table 1-14: AP SoC GTX Banks 109 and 110 Interface Connections to FMC HPC J37

| Transceiver Bank | AP SoC U1 Pin Number | AP SoC U1 Pin Name | Schematic Net Name | Connected Pin | Connected Device |
|------------------|----------------------|--------------------|--|---------------|------------------|
| GTX_BANK_109 | AK10 | MGTPTXP0_109 | FMC_HPC_DP0_C2M_P | C2 | FMC HPC J37 |
| | AK9 | MGTPTXN0_109 | FMC_HPC_DP0_C2M_N | C3 | |
| | AH10 | MGTPRXP0_109 | FMC_HPC_DP0_M2C_P | C6 | |
| | AH9 | MGTPRXN0_109 | FMC_HPC_DP0_M2C_N | C7 | |
| | AK6 | MGTPTXP1_109 | FMC_HPC_DP1_C2M_P | A22 | |
| | AK5 | MGTPTXN1_109 | FMC_HPC_DP1_C2M_N | A23 | |
| | AJ8 | MGTPRXP1_109 | FMC_HPC_DP1_M2C_P | A2 | |
| | AJ7 | MGTPRXN1_109 | FMC_HPC_DP1_M2C_N | A3 | |
| | AJ4 | MGTPTXP2_109 | FMC_HPC_DP2_C2M_P | A26 | |
| | AJ3 | MGTPTXN2_109 | FMC_HPC_DP2_C2M_N | A27 | |
| | AG8 | MGTPRXP2_109 | FMC_HPC_DP2_M2C_P | A6 | |
| | AG7 | MGTPRXN2_109 | FMC_HPC_DP2_M2C_N | A7 | |
| | AK2 | MGTPTXP3_109 | FMC_HPC_DP3_C2M_P | A30 | |
| | AK1 | MGTPTXN3_109 | FMC_HPC_DP3_C2M_N | A31 | |
| | AE8 | MGTPRXP3_109 | FMC_HPC_DP3_M2C_P | A10 | |
| | AE7 | MGTPRXN3_109 | FMC_HPC_DP3_M2C_N | A11 | |
| | AD10 | MGTREFCLK0P_109 | FMC_HPC_GBTCLK0_M2C_C_P ⁽¹⁾ | D4 | |
| | AD9 | MGTREFCLK0N_109 | FMC_HPC_GBTCLK0_M2C_C_N ⁽¹⁾ | D5 | |
| | AF10 | MGTREFCLK1P_109 | NC | NA | NA |
| | AF9 | MGTREFCLK1N_109 | NC | NA | NA |

Table 1-14: AP SoC GTX Banks 109 and 110 Interface Connections to FMC HPC J37 (Cont'd)

| Transceiver Bank | AP SoC U1 Pin Number | AP SoC U1 Pin Name | Schematic Net Name | Connected Pin | Connected Device |
|------------------|----------------------|--------------------|--------------------------------------|---------------|------------------|
| GTX_BANK_110 | AH2 | MGTPTXP0_110 | FMC_HPC_DP4_C2M_P | A34 | FMC HPC J37 |
| | AH1 | MGTPTXN0_110 | FMC_HPC_DP4_C2M_N | A35 | |
| | AH6 | MGTPRXP0_110 | FMC_HPC_DP4_M2C_P | A14 | |
| | AH5 | MGTPRXN0_110 | FMC_HPC_DP4_M2C_N | A15 | |
| | AF2 | MGTPTXP1_110 | FMC_HPC_DP5_C2M_P | A38 | |
| | AF1 | MGTPTXN1_110 | FMC_HPC_DP5_C2M_N | A39 | |
| | AG4 | MGTPRXP1_110 | FMC_HPC_DP5_M2C_P | A18 | |
| | AG3 | MGTPRXN1_110 | FMC_HPC_DP5_M2C_N | A19 | |
| | AE4 | MGTPTXP2_110 | FMC_HPC_DP6_C2M_P | B36 | |
| | AE3 | MGTPTXN2_110 | FMC_HPC_DP6_C2M_N | B37 | |
| | AF6 | MGTPRXP2_110 | FMC_HPC_DP6_M2C_P | B16 | |
| | AF5 | MGTPRXN2_110 | FMC_HPC_DP6_M2C_N | B17 | |
| | AD2 | MGTPTXP3_110 | FMC_HPC_DP7_C2M_P | B32 | |
| | AD1 | MGTPTXN3_110 | FMC_HPC_DP7_C2M_N | B33 | |
| | AD6 | MGTPRXP3_110 | FMC_HPC_DP7_M2C_P | B12 | |
| | AD5 | MGTPRXN3_110 | FMC_HPC_DP7_M2C_N | B13 | |
| | AA8 | MGTREFCLK0P_110 | FMC_HPC_GBTCLK1_M2C_P ⁽¹⁾ | B20 | |
| | AA7 | MGTREFCLK0N_110 | FMC_HPC_GBTCLK1_M2C_N ⁽¹⁾ | B21 | |
| | AC8 | MGTREFCLK1P_110 | SI5324_OUT_C_P ⁽²⁾ | 28 | SI5324C U60 |
| | AC7 | MGTREFCLK1N_110 | SI5324_OUT_C_N ⁽²⁾ | 29 | |

Notes:

1. AP SoC U1 GTX input clock nets are capacitively coupled to the FMC HPC J37 pins.
2. AP SoC U1 GTX input clock nets are capacitively coupled to the SI5324C Recovery Clock U60 output pins.

Table 1-15 lists the GTX Bank interface connections between the AP SoC U1 and FMC LPC connector J5.

Table 1-15: AP SoC GTX Bank 111 Interface Connections to FMC LPC J5

| Transceiver Bank | AP SoC U1 Pin Number | AP SoC U1 Pin Name | Schematic Net Name | Connected Pin | Connected Device |
|------------------|----------------------|--------------------|--|---------------|------------------------|
| GTX_BANK_111 | AB2 | MGTPTXP0_111 | FMC_LPC_DP0_C2M_P | C2 | FMC LPC J5 |
| | AB1 | MGTPTXN0_111 | FMC_LPC_DP0_C2M_N | C3 | |
| | AC4 | MGTPRXP0_111 | FMC_LPC_DP0_M2C_P | C6 | |
| | AC3 | MGTPRXN0_111 | FMC_LPC_DP0_M2C_N | C7 | |
| | Y2 | MGTPTXP1_111 | SMA_MGT_TX_P | J35.1 | GTX TX/RX SMA |
| | Y1 | MGTPTXN1_111 | SMA_MGT_TX_N | J34.1 | |
| | AB6 | MGTPRXP1_111 | SMA_MGT_RX_P ⁽²⁾ | J32.1 | |
| | AB5 | MGTPRXN1_111 | SMA_MGT_RX_N ⁽²⁾ | J33.1 | |
| | W4 | MGTPTXP2_111 | SFP_TX_P | 18 | SFP+ Conn. P2 |
| | W3 | MGTPTXN2_111 | SFP_TX_N | 19 | |
| | Y6 | MGTPRXP2_111 | SFP_RX_P | 13 | |
| | Y5 | MGTPRXN2_111 | SFP_RX_N | 12 | |
| | V2 | MGTPTXP3_111 | (capacitively coupled to AA4) | U1.AA4 | AP SoC U1 GTX Loopback |
| | V1 | MGTPTXN3_111 | (Cooperatively coupled to AA3) | U1.AA3 | |
| | AA4 | MGTPRXP3_111 | See Pin V2 loopback | U1.V2 | |
| | AA3 | MGTPRXN3_111 | See Pin V1 loopback | U1.V1 | |
| | U8 | MGTREFCLK0P_111 | FMC_LPC_GBTCLK0_M2C_C_P ⁽¹⁾ | D4 | FMC LPC J5 |
| | U7 | MGTREFCLK0N_111 | FMC_LPC_GBTCLK0_M2C_C_N ⁽¹⁾ | D5 | |
| | W8 | MGTREFCLK1P_111 | SMA_MGT_REFCLK_P ⁽²⁾ | J36.1 | GTX REFCLK SMA |
| | W7 | MGTREFCLK1N_111 | SMA_MGT_REFCLK_N ⁽²⁾ | J31.1 | |

Notes:

1. AP SoC U1 GTX input clock nets are capacitively coupled to the FMC LPC J5 pins.
2. AP SoC U1 GTX input nets are capacitively coupled to the RX and MGT_REFCLK SMA pins.

For additional information on Zynq-7000 GTX transceivers, see *7 Series FPGAs GTX/GTH Transceivers User Guide* ([UG476](#)).

PCI Express Endpoint Connectivity

[Figure 1-2, callout 13]

The 4-lane PCI Express edge connector performs data transfers at the rate of 2.5 GT/s for a Gen1 application and 5.0 GT/s for a Gen2 application. The PCIe transmit and receive signal data paths have a characteristic impedance of $85\Omega \pm 10\%$. The PCIe clock is routed as a 100Ω differential pair.

The XC7Z045-2FFG900C AP SoC (-2 speed grade) included with the ZC706 board supports up to Gen2 x4.

The PCIe clock is input from the edge connector. It is AC coupled to the AP SoC through the MGTREFCLK0 pins of Quad 112. PCIE_CLK_Q0_P is connected to AP SoC U1 pin N8, and the _N net is connected to pin N7. The PCI Express clock circuit is shown in [Figure 1-17](#).

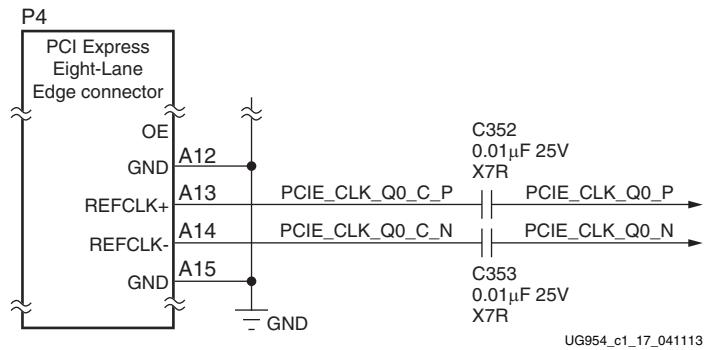


Figure 1-17: PCI Express Clock

PCIe lane width/size is selected by jumper J19 ([Figure 1-17](#)). The default lane size selection is 4-lane (J19 pins 3 and 4 jumpered).

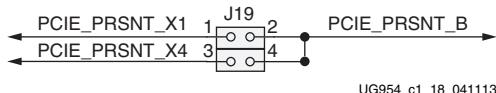


Figure 1-18: PCI Express Lane Size Select Jumper J19

[Table 1-17](#) lists the GTX Bank 112 interface connections between the AP SoC U1 and PCIe 4-lane connector P4.

Table 1-16: AP SoC GTX Bank 112 Interface Connections to PCIe 4-Lane Connector P4

| Transceiver Bank | AP SoC U1 Pin Number | AP SoC U1 Pin Name | Schematic Net Name | PCIe 4-Lane Conn. P4 Pin Number |
|------------------|----------------------|--------------------|--------------------|---------------------------------|
| GTX_BANK_112 | T2 | MGTPTXP0_112 | PCIE_TX3_P | A29 (1) |
| | T1 | MGTPTXN0_112 | PCIE_TX3_N | A30 (1) |
| | V6 | MGTPTXP0_112 | PCIE_RX3_P | B27 |
| | V5 | MGTPTXN0_112 | PCIE_RX3_N | B28 |
| | R4 | MGTPTXP1_112 | PCIE_TX2_P | A25 (1) |
| | R3 | MGTPTXN1_112 | PCIE_TX2_N | A26 (1) |
| | U4 | MGTPTXP1_112 | PCIE_RX2_P | B23 |
| | U3 | MGTPTXN1_112 | PCIE_RX2_N | B24 |
| | P2 | MGTPTXP2_112 | PCIE_TX1_P | A21 (1) |
| | P1 | MGTPTXN2_112 | PCIE_TX1_N | A22 (1) |

Table 1-16: AP SoC GTX Bank 112 Interface Connections to PCIe 4-Lane Connector P4 (Cont'd)

| Transceiver Bank | AP SoC U1 Pin Number | AP SoC U1 Pin Name | Schematic Net Name | PCIe 4-Lane Conn. P4 Pin Number |
|------------------|----------------------|--------------------|--------------------|---------------------------------|
| | T6 | MGTPRXP2_112 | PCIE_RX1_P | B19 |
| | T5 | MGTPRXN2_112 | PCIE_RX1_N | B20 |
| | N4 | MGTPTXP3_112 | PCIE_TX0_P | A16 (1) |
| | N3 | MGTPTXN3_112 | PCIE_TX0_N | A17 (1) |
| | P6 | MGTPRXP3_112 | PCIE_RX0_P | B14 |
| | P5 | MGTPRXN3_112 | PCIE_RX0_N | B15 |
| | N8 | MGTREFCLK0P_112 | PCIE_CLK_Q0_P | A13 (1) |
| | N7 | MGTREFCLK0N_112 | PCIE_CLK_Q0_N | A14 (1) |
| | R8 | MGTREFCLK1P_112 | NC | NA |
| | R7 | MGTREFCLK1N_112 | NC | NA |

Notes:

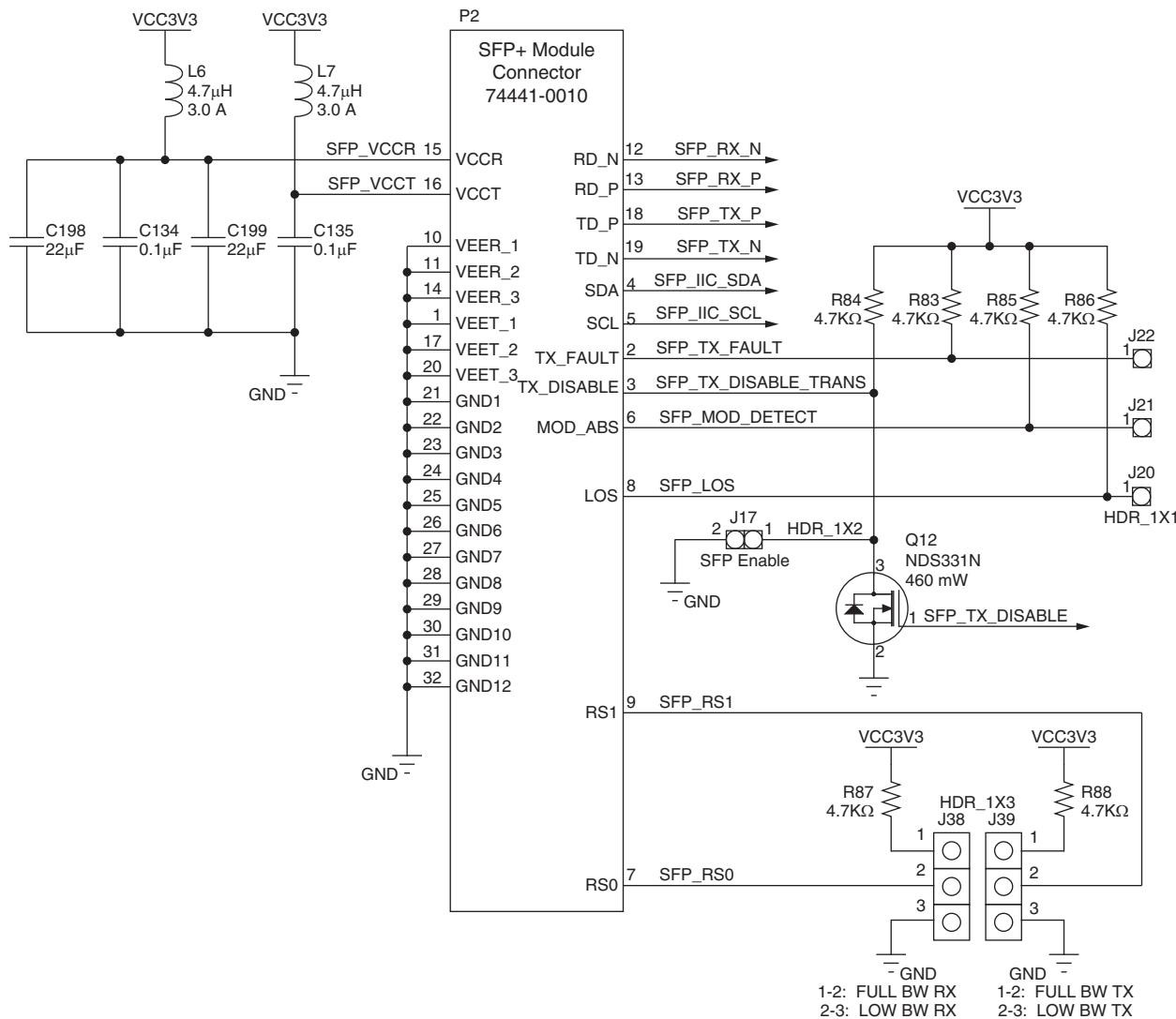
1. PCIE_TXn_P/N and PCIE_CLK_Q0_P/N are capacitively coupled to the PCIe edge connector P4.

For additional information about Zynq-7000 PCIe functionality, see *7 Series FPGAs Integrated Block for PCI Express User Guide* ([UG477](#)). For additional information about the PCIe standard, visit www.pcisig.com/specifications [Ref 14].

SFP/SFP+ Module Connector

[Figure 1-2, callout 14]

The ZC706 board contains a small form-factor pluggable (SFP/SFP+) connector and cage assembly P2 that accepts SFP or SFP+ modules. Figure 1-19 shows the SFP/SFP+ module connector circuitry.



UG954_c1_19_041113

Figure 1-19: SFP+ Module Connector

Table 1-17 lists the SFP+ module RX and TX connections to the AP SoC.

Table 1-17: AP SoC U1 to SFP+ Module Connections

| AP SoC (U1) Pin | Schematic Net name | SFP+ Module (P2) | |
|-----------------|----------------------|------------------|------------|
| | | Pin | Name |
| Y5 | SFP_RX_N | 12 | RD_N |
| Y6 | SFP_RX_P | 13 | RD_P |
| W4 | SFP_TX_P | 18 | TD_P |
| W3 | SFP_TX_N | 19 | TD_N |
| AA18 | SFP_TX_DISABLE_TRANS | 3 | TX_DISABLE |

Table 1-18 lists the SFP+ module control and status connections to the AP SoC.

Table 1-18: SFP+ Module Control and Status Connections

| SFP Control/ Status Signal | Board Connection | |
|----------------------------|------------------|--|
| SFP_TX_FAULT | Test Point J23 | High = Fault |
| | | Low = Normal operation |
| SFP_TX_DISABLE | Jumper 17 | Off = SFP Disabled |
| | | On = SFP enabled |
| SFP_MOD_DETECT | Test Point J24 | High = Module not present |
| | | Low = Module present |
| SFP_RS0 | Jumper 56 | Jumper pins 1-2 = Full RX bandwidth |
| | | Jumper pins 2-3 = Reduced RX bandwidth |
| SFP_RS1 | Jumper 55 | Jumper pins 1-2 = Full TX bandwidth |
| | | Jumper pins 2-3 = Reduced TX bandwidth |
| SFP_LOS | Test Point J25 | High = Loss of receiver signal |
| | | Low = Normal operation |

For additional information about the enhanced Small Form Factor Pluggable (SFP+) module, see the SFF-8431 specification at <ftp://ftp.seagate.com/sff>.

10/100/1,000 Mb/s Tri-Speed Ethernet PHY (PL)

[Figure 1-2, callout 15]

The ZC706 evaluation board uses the Marvell Alaska PHY device (88E1116R) at U51 for Ethernet communications at 10 Mb/s, 100 Mb/s, or 1,000 Mb/s. The board supports RGMII mode only. The PHY connection to a user-provided Ethernet cable is through a Halo HFJ11-1G01E RJ-45 connector (P3) with built-in magnetics.

On power-up, or on reset, the PHY is configured to operate in RGMII mode with PHY address 0b00111 using the settings shown in Table 1-19. These settings can be overwritten via software commands passed over the MDIO interface.

Table 1-19: Board Connections for PHY Configuration Pins

| U51 Pin | Setting | Configuration | |
|-------------|----------|---------------|------------|
| CONFIG (64) | VCCP1V8 | PHYAD[1]=1 | PHYAD[0]=1 |
| CONFIG1 (1) | PHY_LED0 | PHYAD[3]=0 | PHYAD[2]=1 |
| CONFIG2 (2) | GND | ENA_XC=0 | PHYAD[4]=0 |
| | PHY_LED0 | ENA_XC=0 | PHYAD[4]=1 |
| | VCCP1V8 | ENA_XC=1 | PHYAD[4]=1 |

Table 1-19: Board Connections for PHY Configuration Pins (Cont'd)

| U51 Pin | Setting | Configuration | |
|-------------|----------|---------------|------------|
| CONFIG3 (3) | GND | RGMII_TX=0 | RGMII_RX=0 |
| | PHY_LED0 | RGMII_TX=0 | RGMII_RX=1 |
| | PHY_LED1 | RGMII_TX=1 | RGMII_RX=0 |
| | VCCP1V8 | RGMII_TX=1 | RGMII_RX=1 |

The Ethernet connections from the XC7Z045 AP SoC at U1 to the 88E1116R PHY device at U51 are listed in [Table 1-20](#).

Table 1-20: Ethernet Connections, XC7Z045 AP SoC to the PHY Device

| XC7Z045 (U1) Pin | | | Schematic Net Name | M88E1116R PHY U51 | |
|------------------|------|------------|--------------------|-------------------|---------|
| Pin Name | Bank | Pin Number | | Pin | Name |
| PS_MIO53 | 501 | C18 | PHY_MDIO | 45 | MDIO |
| PS_MIO52 | 501 | D19 | PHY_MDC | 48 | MDC |
| PS_MIO16 | 501 | L19 | PHY_TX_CLK | 60 | TX_CLK |
| PS_MIO21 | 501 | J19 | PHY_TX_CTRL | 63 | TX_CTRL |
| PS_MIO20 | 501 | M20 | PHY_TXD3 | 62 | TXD3 |
| PS_MIO19 | 501 | J20 | PHY_TXD2 | 61 | TXD2 |
| PS_MIO18 | 501 | K20 | PHY_TXD1 | 59 | TXD1 |
| PS_MIO17 | 501 | K21 | PHY_TXD0 | 58 | TXD0 |
| PS_MIO22 | 501 | L20 | PHY_RX_CLK | 53 | RX_CLK |
| PS_MIO27 | 501 | G20 | PHY_RX_CTRL | 49 | RX_CTRL |
| PS_MIO26 | 501 | M17 | PHY_RXD3 | 55 | RXD3 |
| PS_MIO25 | 501 | G19 | PHY_RXD2 | 54 | RXD2 |
| PS_MIO24 | 501 | M19 | PHY_RXD1 | 51 | RXD1 |
| PS_MIO23 | 501 | J21 | PHY_RXD0 | 50 | RXD0 |

Ethernet PHY Clock Source

A 25.00 MHz 50 ppm crystal at X1 is the clock source for the 881116R PHY at U51. [Figure 1-20](#) shows the clock source.

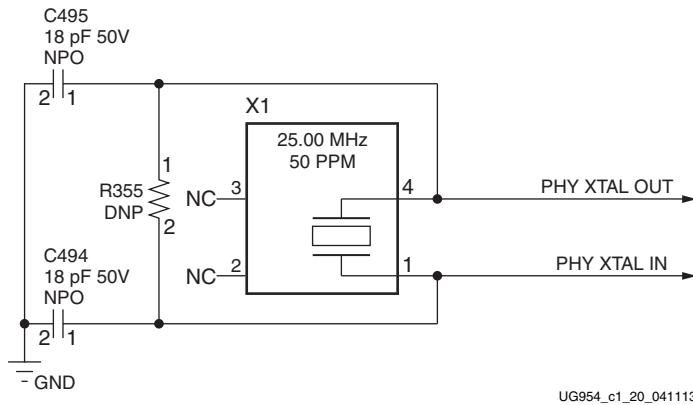


Figure 1-20: Ethernet PHY Clock Source

The data sheet can be obtained under NDA with Marvell, whose contact information may be found at www.marvell.com.

For additional information on the Zynq-7000 AP SoC device gigabit Ethernet controller, see *Zynq-7000 All Programmable SoC Overview* ([DS190](#)) and *Zynq-7000 All Programmable SoC Technical Reference Manual* ([UG585](#)).

USB-to-UART Bridge

[Figure 1-2, callout 17]

The ZC706 evaluation board contains a Silicon Labs CP2103GM USB-to-UART bridge device (U52) which allows a connection to a host computer with a USB port. The USB cable is supplied in the ZC706 evaluation kit (Standard-A end to host computer, Type Mini-B end to ZC706 evaluation board connector J21). The CP2103GM is powered by the USB 5V provided by the host PC when the USB cable is plugged into the USB port on the ZC706 evaluation board.

The CP2013GM TX and RX pins are wired to the UART_1 IP block within the XC7Z045 AP SoC PS IO Peripherals set. The XC7Z045 AP SoC supports the USB-to-UART bridge using two signal pins: Transmit (TX) and Receive (RX).

Silicon Labs provides royalty-free Virtual COM Port (VCP) drivers for the host computer. These drivers permit the CP2103GM USB-to-UART bridge to appear as a COM port to communications application software (for example, TeraTerm or HyperTerm) that runs on the host computer. The VCP device drivers must be installed on the host PC prior to establishing communications with the ZC706 evaluation board.

The USB Connector pin assignments and signal definitions between J21 and U52 are listed in [Table 1-21](#).

Table 1-21: USB Connector J21 Pin Assignments and Signal Definitions

| USB Connector (J21) | | Net Name | Description | CP2103GM (U52) | |
|---------------------|------|---------------|---|----------------|---------|
| Pin | Name | | | Pin | Name |
| 1 | VBUS | USB_UART_VBUS | +5V VBUS Powered | 7 | REGIN |
| | | | | 8 | VBUS |
| 2 | D_N | USB_UART_D_N | Bidirectional differential serial data (N-side) | 4 | D - |
| 3 | D_P | USB_UART_D_P | Bidirectional differential serial data (P-side) | 3 | D + |
| 5 | GND | USB_UART_GND | Signal ground | 2 | GND1 |
| | | | | 29 | CNR_GND |

Table 1-22 lists the USB connections between the XC7Z045 AP SoC PS Bank 501 and the CP2103 UART bridge.

Table 1-22: XC7Z045 AP SoC to CP2103 Connections

| XC7Z045 AP SoC (U1) | | | UART Function | Net Name | CP2103GM (U52) | |
|---------------------|------|------------|---------------|-------------|----------------|---------------|
| Pin Name | Bank | Pin Number | | | Pin | UART Function |
| PS_MIO48 | 501 | C19 | TX, data out | USB_UART_RX | 24 | RXD, data in |
| PS_MIO49 | 501 | D18 | RX, data in | USB_UART_TX | 25 | TXD, data out |

Refer to the Silicon Labs website for technical information on the CP2103GM and the VCP drivers (Silicon Labs: www.silabs.com).

For additional information on the Zynq-7000 AP SoC device UART controller, see *Zynq-7000 All Programmable SoC Overview* ([DS190](#)) and *Zynq-7000 All Programmable SoC Technical Reference Manual* ([UG585](#)).

HDMI Video Output

[Figure 1-2, callout 18]

The ZC706 evaluation board provides a high-definition multimedia interface (HDMI®) video output using an Analog Devices ADV7511KSTZ-P HDMI transmitter at U53. The HDMI transmitter U53 is connected to the XC7Z045 AP SoC PL-side banks 12 and 13 and its output is provided on a Molex 500254-1927 HDMI type-A receptacle at P1. The ADV7511 supports 1080P 60Hz, YCbCr 4:4:4 encoding via 24-bit input data mapping.

The ZC706 evaluation board supports the following HDMI device interfaces:

- 24 data lines
- Independent VSYNC, HSYNC
- Single-ended input CLK

- Interrupt Out pin to XC7Z045 AP SoC
- I²C
- SPDIF

Figure 1-21 shows the HDMI codec circuit.

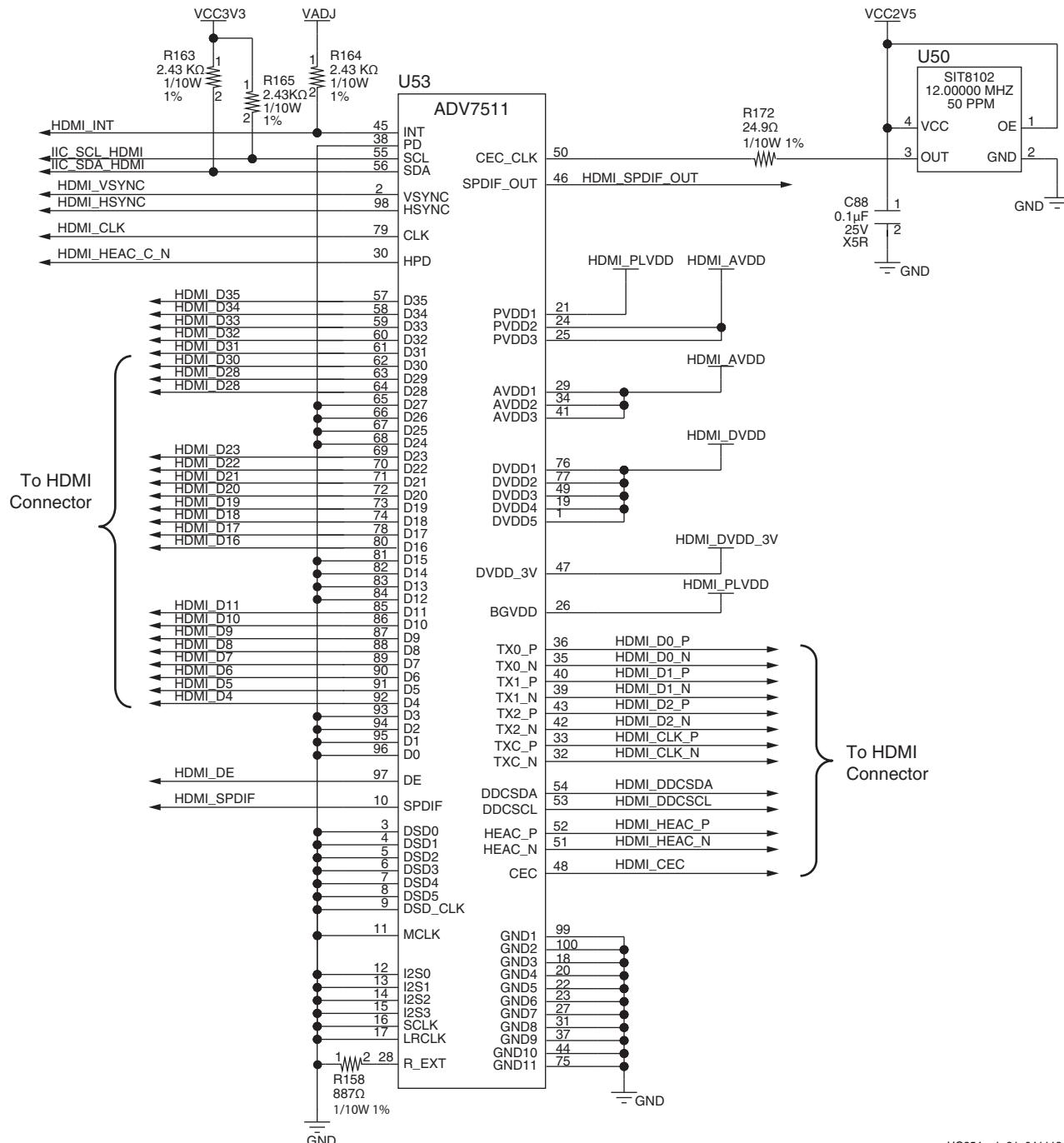


Figure 1-21: HDMI Codec Circuit

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Table 1-23 lists the connections between the codec and the XC7Z045 AP SoC.

Table 1-23: XC7Z045 AP SoC U1 to HDMI Codec Connections (ADV7511)

| XC7Z045 (U1) Pin | Net Name | ADV7511 (U53) | |
|------------------|-------------------|---------------|-----------|
| | | Pin | Name |
| U24 | HDMI_R_D4 | 92 | D4 |
| T22 | HDMI_R_D5 | 91 | D5 |
| R23 | HDMI_R_D6 | 90 | D6 |
| AA25 | HDMI_R_D7 | 89 | D7 |
| AE28 | HDMI_R_D8 | 88 | D8 |
| T23 | HDMI_R_D9 | 87 | D9 |
| AB25 | HDMI_R_D10 | 86 | D10 |
| T27 | HDMI_R_D11 | 85 | D11 |
| AD26 | HDMI_R_D16 | 80 | D16 |
| AB26 | HDMI_R_D17 | 78 | D17 |
| AA28 | HDMI_R_D18 | 74 | D18 |
| AC26 | HDMI_R_D19 | 73 | D19 |
| AE30 | HDMI_R_D20 | 72 | D20 |
| Y25 | HDMI_R_D21 | 71 | D21 |
| AA29 | HDMI_R_D22 | 70 | D22 |
| AD30 | HDMI_R_D23 | 69 | D23 |
| Y28 | HDMI_R_D28 | 64 | D28 |
| AF28 | HDMI_R_D29 | 63 | D29 |
| V22 | HDMI_R_D30 | 62 | D30 |
| AA27 | HDMI_R_D31 | 61 | D31 |
| U22 | HDMI_R_D32 | 60 | D32 |
| N28 | HDMI_R_D33 | 59 | D33 |
| V21 | HDMI_R_D34 | 58 | D34 |
| AC22 | HDMI_R_D35 | 57 | D35 |
| V24 | HDMI_R_DE | 97 | DE |
| R22 | HDMI_R_HSYNC | 98 | HSYNC |
| U21 | HDMI_R_VSYNC | 2 | VSYNC |
| P28 | HDMI_R_CLK | 79 | CLK |
| AC23 | HDMI_INT | 45 | INT |
| AC21 | HDMI_R_SPDIF | 10 | SPDIF |
| AB22 | HDMI_SPDIF_OUT_LS | 46 | SPDIF_OUT |

Table 1-24 lists the connections between the codec and the HDMI receptacle P1.

Table 1-24: ADV7511 to HDMI Receptacle Connections

| ADV7511 (U53) | Net Name | HDMI Receptacle P1 Pin |
|---------------|-------------|------------------------|
| 36 | HDMI_D0_P | 7 |
| 35 | HDMI_D0_N | 9 |
| 40 | HDMI_D1_P | 4 |
| 39 | HDMI_D1_N | 6 |
| 43 | HDMI_D2_P | 1 |
| 42 | HDMI_D2_N | 3 |
| 33 | HDMI_CLK_P | 10 |
| 32 | HDMI_CLK_N | 12 |
| 54 | HDMI_DDCSDA | 16 |
| 53 | HDMI_DDCSCL | 15 |
| 52 | HDMI_HEAC_P | 14 |
| 51 | HDMI_HEAC_N | 19 |
| 48 | HDMI_CEC | 13 |

Information about the ADV7511KSTZ-P is available on the Analog Devices website at www.analog.com/en/index.html.

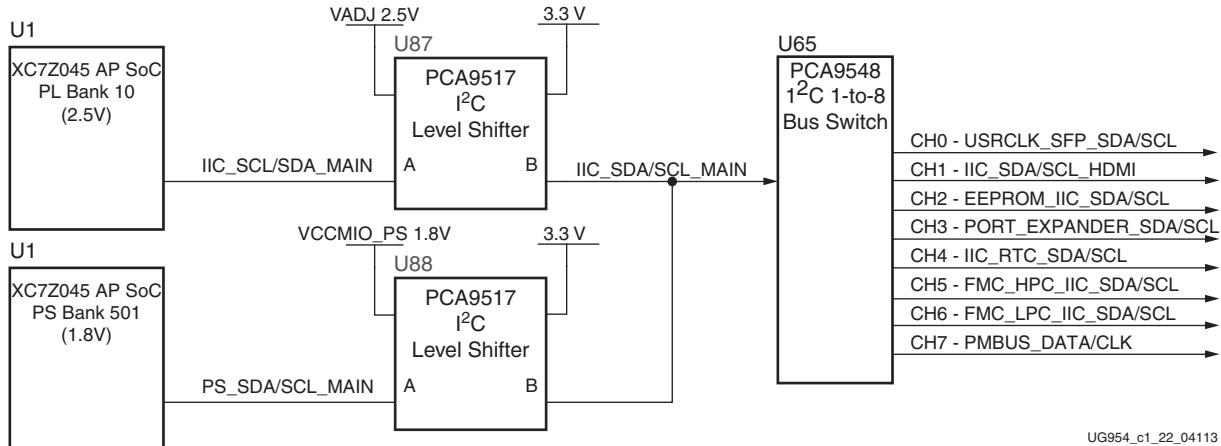
For additional information about HDMI IP options, see the *LogiCORE IP DisplayPort Product Guide (PG064)*.

I²C Bus

[Figure 1-2, callout 20]

The ZC706 evaluation board implements two I²C ports on the XC7Z045 AP SoC. The PL-side I²C port (IIC_SDA and _SCL_MAIN) is routed to level shifter U87. The PS-side I²C port (PS_SDA and _SCL_MAIN) is routed to level shifter U88. The "output" side of the two level shifters are wired to the common I²C bus IIC_SDA and _SCL_MAIN which is connected to TI Semiconductor PCA9548 1-to-8 channel I²C bus switch (U65). The bus switch can operate at speeds up to 400 kHz.

The ZC706 evaluation board I²C bus topology is shown in [Figure 1-22](#).

Figure 1-22: I²C Bus Topology

User applications that communicate with devices on one of the downstream I²C buses must first set up a path to the desired bus through the U65 bus switch at I²C address 0x74 (0b01110100). [Table 1-25](#) lists the address for each bus.

Table 1-25: I²C Bus Addresses

| I ² C Bus | I ² C Switch Position | I ² C Address | Device |
|------------------------------|----------------------------------|--------------------------|-------------------|
| PCA9548 8-Channel bus switch | NA | 0b1110100 | PCA9548 U65 |
| USRCLK_SDA/SCL | 0 | 0b1011101 | Si570 U37 |
| | | 0b1010000 | SFP+ Conn. P2 |
| IIC_SDA_HDMI | 1 | 0b0111001 | ADV7511 U53 |
| IIC_EEPROM_SDA/SCL | 2 | 0b1010100 | M24C08 U9 |
| IIC_PORT_EXPANDER_SDA/SCL | 3 | 0b0100001 | Port Expander U16 |
| | | 0b1010000 | DDR3 SODIMM J1 |
| | | 0b0011000 | |
| IIC_RTC_SDA/SCL | 4 | 0b1010001 | RTC8564JE U26 |
| | | 0b1101000 | SI5324 U60 |
| FMC_HPC_IIC_SDA/SCL | 5 | 0bxxxxxx00 | FMC HPC J37 |
| FMC_LPC_IIC_SDA/SCL | 6 | 0bxxxxxx00 | FMC LPC J5 |
| PMBUS_DATA/CLOCK | 7 | 0b1100101 | UCD90120A U48 |

Information about the PCA9548 is available on the TI Semiconductor website at www.ti.com.

For additional information on the Zynq-7000 AP SoC device I²C controller, see *Zynq-7000 All Programmable SoC Overview* ([DS190](#)) and *Zynq-7000 All Programmable SoC Technical Reference Manual* ([UG585](#)).

Real Time Clock (RTC)

The Epson RTC-8564JE (U26) is an I²C bus interface real-time clock that has a built-in 32.768 KHz oscillator with these features:

- Frequency output options: 32.768 KHz, 1,024 Hz, 32 Hz or 1 Hz
- Calendar output functions: Year, month, day, weekday, hour, minute and second
- Clock counter, alarm and fixed-cycle timer interrupt functions
- Back-up battery B3 Panasonic ML621S/DN, 3.0V rechargeable cell

Programming information for the RTC-8564JE is available in the *RTC-8564JE/NB Application Manual* [Ref 3].

Figure 1-23 shows the real time clock circuit.

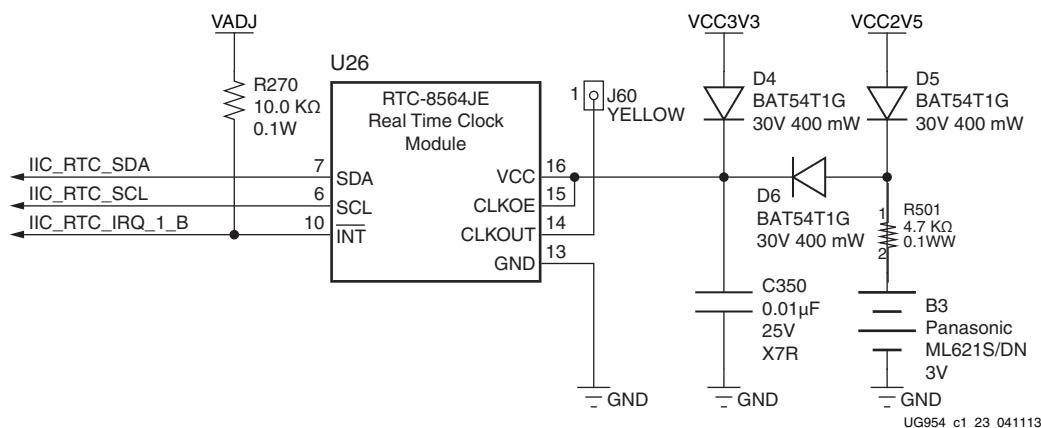


Figure 1-23: Real Time Clock Circuit

Real time clock connections to the XC7Z045 AP SoC and the PCA9548 8-Channel bus switch are listed in Table 1-26. Refer to Table 1-25 for the RTC I²C address.

Table 1-26: Real Time Clock Connections

| RTC-8564JE (U16) Pin | Net Name | Connects To |
|----------------------|-----------------|-------------------------------------|
| 6 | IIC_RTC_SCL | U65.11 (PCA9548 SC4) |
| 7 | IIC_RTC_SDA | U65.10 (PCA9548 SD4) |
| 10 | IIC_RTC_IRQ_1_B | U1.AA17 (XC7Z045 AP SoC PL BANK 10) |

Information about the RTC-8564JE is available at the Epson Electronics America website [Ref 4].

Status and User LEDs

Table 1-27 defines the status and user LEDs.

Table 1-27: Status LEDs

| Reference Designator | Net Name | LED Color | Description |
|----------------------|----------------------|-----------|---|
| DS1 | POR | RED | Processor System Power-ON reset is active |
| DS2 | FPGA_INIT_B | GRN/RED | Green: FPGA initialization was successful Red: FPGA initialization is in progress |
| DS3 | DONE | GRN | FPGA bit file download is complete |
| DS8 | GPIO_LED_LEFT | GRN | Geographically LEFT located user LED |
| DS9 | GPIO_LED_CENTER | GRN | Geographically CENTER located user LED |
| DS10 | GPIO_LED_RIGHT | GRN | Geographically RIGHT located user LED |
| DS11 | VCCINT | GRN | VCCINT voltage on indicator |
| DS13 | VCC1V5_PL | GRN | VCC1V5_PL voltage on indicator |
| DS15 | VADJ_FPGA | GRN | VADJ_FPGA voltage on indicator |
| DS16 | VCC3V3_FPGA | GRN | VCC3V3 voltage on indicator |
| DS20 | PS_DDR_LINEAR_PG | GRN | VTTDDR_PS voltage on indicator |
| DS21 | SODIMM_DDR_LINEAR_PG | GRN | VTTDDR_SODIMM voltage on indicator |
| DS22 | VCC12_P | GRN | VCC12_P voltage on indicator |
| DS23 | PWRCTL1_FMC_PG_C2M | GRN | FMC power good INDICATOR |
| DS24 | CTRL1_PWRGOOD | GRN | Power Controller controlled voltage regulator outputs are all \geq their minimum "good" threshold |
| DS25 | U22_FLG | RED | USB 2.0 MOSFET power switch fault |
| DS26 | LINEAR_POWER_GOOD | GRN | MGTAVCC, MGTAVTT, MGTVCCAUX voltage regulator outputs are all \geq their minimum "good" threshold |
| DS27 | VCCAUX | GRN | VCCAUX voltage on indicator |
| DS28 | PHY_LED0 | GRN | Ethernet PHY LED0 |
| DS29 | PHY_LED1 | GRN | Ethernet PHY LED1 |
| DS30 | PHY_LED2 | GRN | Ethernet PHY LED2 |
| DS35 | GPIO_LED_0 | GRN | General Purpose user LED |

Ethernet PHY User LEDs

[Figure 1-2, callout 21]

The three Ethernet PHY user LEDs shown in [Figure 1-24](#) are located near the RJ45 Ethernet jack P3. The on/off state for each LED is software dependent and has no specific meaning at Ethernet PHY power on.

Refer to the Marvell 881116R Alaska Gigabit Ethernet transceiver data sheet for details concerning the use of the Ethernet PHY user LEDs. They are referred in the data sheet as LED0, LED1, and LED2. The data sheet and other product information for the Marvell 881116R Alaska Gigabit Ethernet Transceiver is available at www.marvell.com/transceivers/alaska-qbe/.

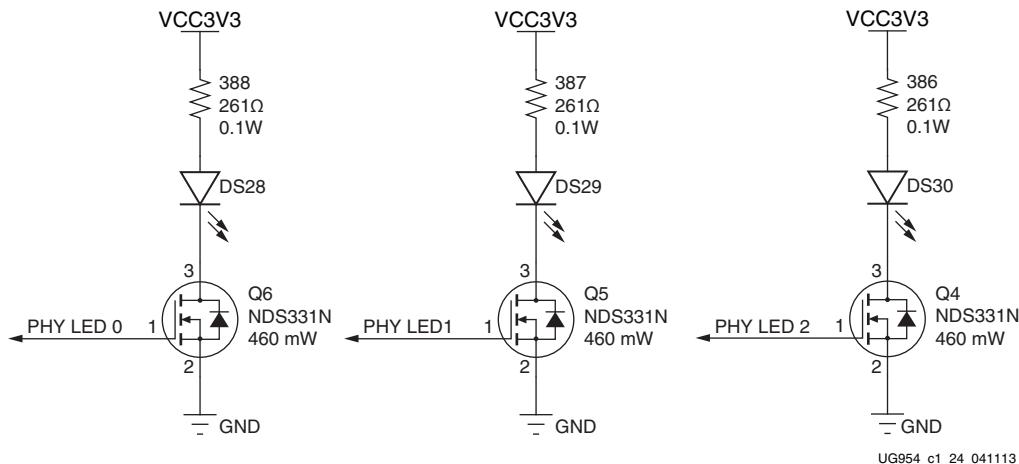


Figure 1-24: Ethernet PHY User LEDs

User I/O

[Figure 1-2, callout 22-24]

The ZC706 evaluation board provides the following user and general purpose I/O capabilities:

- Four user LEDs (callout 22)
 - GPIO_LED_LEFT DS8, GPIO_LED_CENTER DS9, GPIO_LED_RIGHT DS10, GPIO_LED_0 DS35
 - Three user pushbuttons (callout 23)
 - GPIO_SW_LEFT SW7, GPIO_SW_CENTER SW9, GPIO_SW_RIGHT SW8
 - PL CPU reset pushbutton
 - PL_CPU_RESET SW13

- 4-position user DIP Switch (callout 24)
 - GPIO_DIP_SW[3:0] SW12
- Two user GPIO male pin headers (callout 26)
- 2 x 6 0.1 in. pitch PMOD1 J57
- 2 x 6 0.1 in. pitch PMOD2 J58

User LEDs

[Figure 1-2, callout 22]

The ZC706 evaluation board supports four user LEDs connected to XC7Z045 AP SoC Banks 11, 33, and 35. Figure 1-25 shows the user LED circuits.

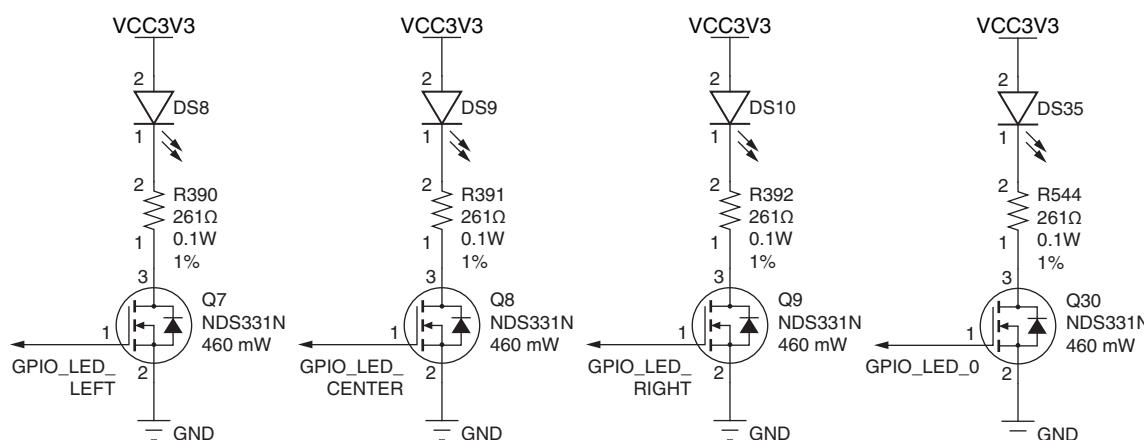


Figure 1-25: User LEDs

Table 1-28 lists the user LED connections to XC7Z045 AP SoC U1.

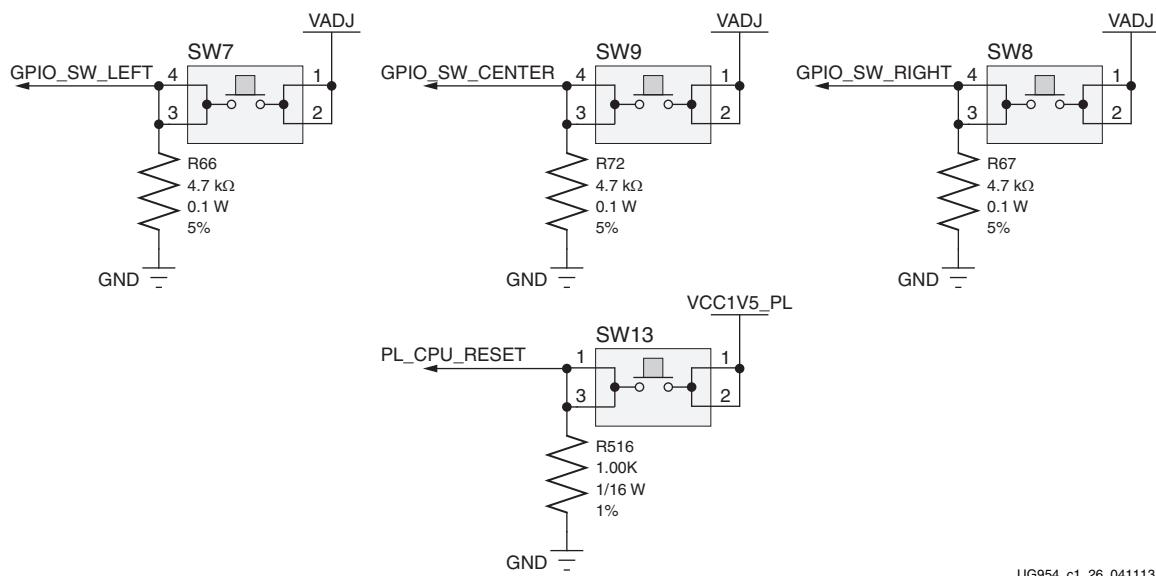
Table 1-28: User LED Connections to XC7Z045 AP SoC U1

| XC7Z045 AP SoC (U1) Pin | Net Name | LED Reference |
|-------------------------|-----------------|---------------|
| Y21 | GPIO_LED_LEFT | DS8 |
| G2 | GPIO_LED_CENTER | DS9 |
| W21 | GPIO_LED_RIGHT | DS10 |
| A17 | GPIO_LED_0 | DS35 |

User Pushbuttons

[Figure 1-2, callout 23]

Figure 1-26 shows the user pushbutton circuits.



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Figure 1-26: User Pushbuttons

Table 1-29 lists the user pushbutton connections to XC7Z045 AP SoC U1.

Table 1-29: User Pushbutton Connections to XC7Z045 AP SoC U1

| XC7Z045 AP SoC (U1) Pin | Net Name | Pushbutton Reference |
|-------------------------|----------------|----------------------|
| AK25 | GPIO_SW_LEFT | SW7 |
| K15 | GPIO_SW_CENTER | SW9 |
| R27 | GPIO_SW_RIGHT | SW8 |
| A8 | PL_CPU_RESET | SW13 |

GPIO DIP Switch

Figure 1-27 shows the GPIO DIP switch circuit.

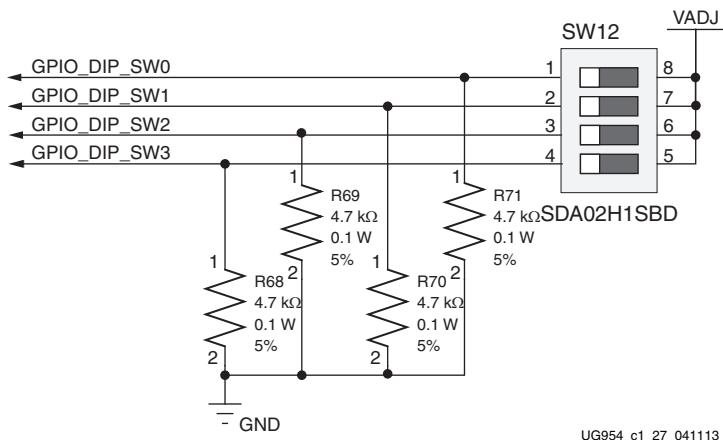


Figure 1-27: GPIO DIP Switch

Table 1-30 lists the GPIO DIP switch connections to XC7Z045 AP SoC U1.

Table 1-30: GPIO DIP Switch Connections to XC7Z045 AP SoC at U1

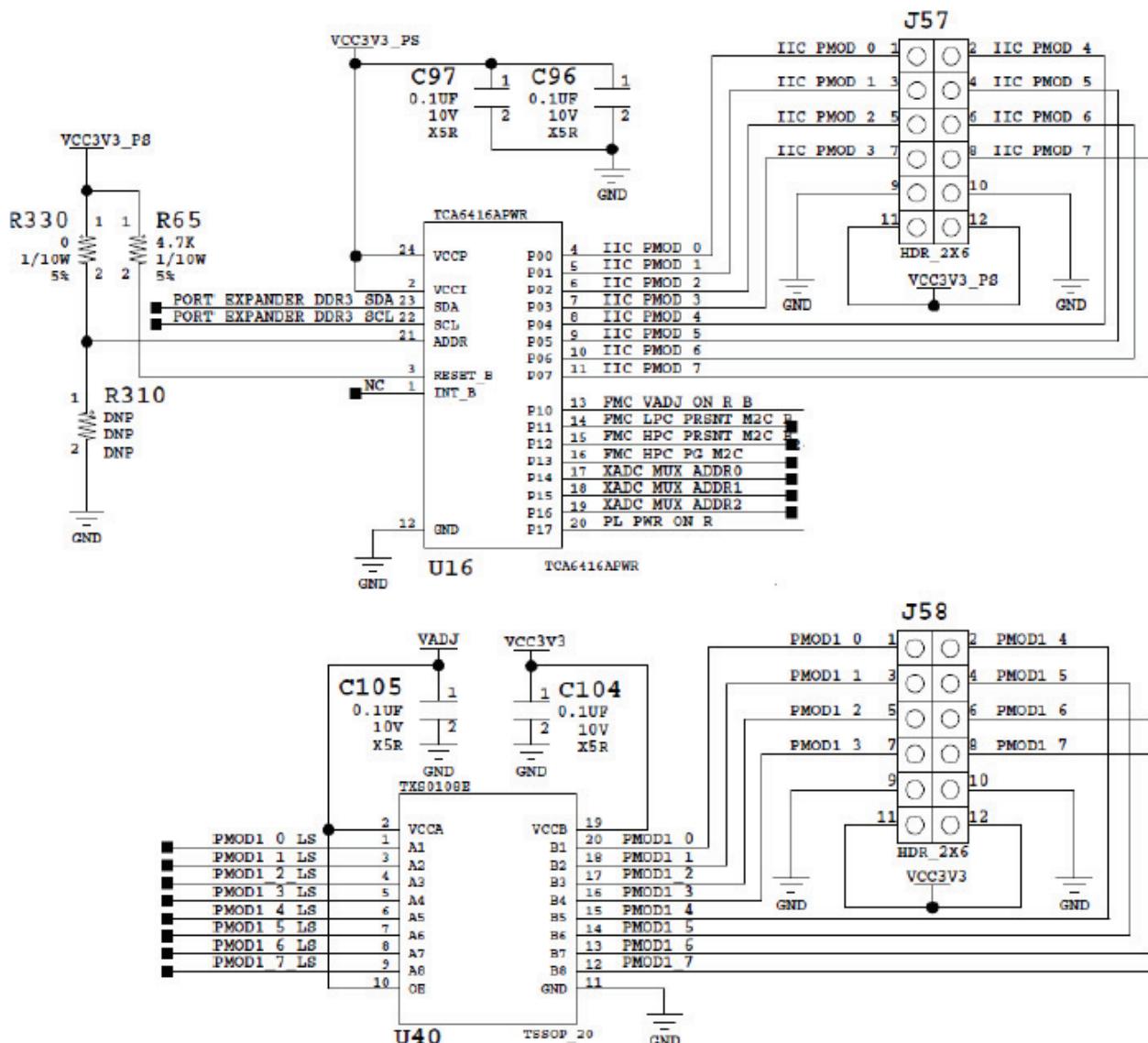
| XC7Z045 AP SOC (U1) Pin | Net Name | DIP Switch SW12 Pin |
|-------------------------|--------------|---------------------|
| AB17 | GPIO_DIP_SW0 | 1 |
| AC16 | GPIO_DIP_SW1 | 2 |
| AC17 | GPIO_DIP_SW2 | 3 |
| AJ13 | GPIO_DIP_SW3 | 4 |

User PMOD GPIO Headers

[Figure 1-2, callout 26]

The ZC706 evaluation board supports two GPIO headers J57 and J58. The PMOD nets connected to these headers are accessed via I²C bus expander U16 (PMOD0 J57) and level-shifter U40 (PMOD1 J58).

Figure 1-28 shows the user GPIO male pin header circuits.



UG954_c1_28_041113

Figure 1-28: User GPIO Headers

Table 1-31 lists the GPIO Header connections to XC7Z045 AP SoC U1.

Table 1-31: GPIO Header Connections to XC7Z045 AP SoC at U1

| TCA6416APWR (U16) PORT: Pin | Net Name | GPIO Header J57 Pin |
|-----------------------------|------------|---------------------|
| P00:4 | IIC_PMOD_0 | J57.1 |
| P01:5 | IIC_PMOD_1 | J57.3 |
| P02:6 | IIC_PMOD_2 | J57.5 |
| P03:7 | IIC_PMOD_3 | J57.7 |

Table 1-31: GPIO Header Connections to XC7Z045 AP SoC at U1 (Cont'd)

| TCA6416APWR (U16) PORT: Pin | Net Name | GPIO Header J57 Pin |
|-----------------------------|------------|---------------------|
| P04:8 | IIC_PMOD_4 | J57.2 |
| P05:9 | IIC_PMOD_5 | J57.4 |
| P06:10 | IIC_PMOD_6 | J57.6 |
| P07:11 | IIC_PMOD_7 | J57.8 |
| XC7Z045 AP SoC (U1) Pin | Net Name | GPIO Header J58 Pin |
| AJ21 | PMOD1_0 | J58.1 |
| AK21 | PMOD1_1 | J58.3 |
| AB21 | PMOD1_2 | J58.5 |
| AB16 | PMOD1_3 | J58.7 |
| Y20 | PMOD1_4 | J58.2 |
| AA20 | PMOD1_5 | J58.4 |
| AC18 | PMOD1_6 | J58.6 |
| AC19 | PMOD1_7 | J58.8 |

Refer to [UG585, Zynq-7000 All Programmable SoC Technical Reference Manual](#) for information about the PS PjTAG functionality.

Switches

The ZC706 evaluation board includes a power and a configuration (PL PROG_B) switch:

- Power On/Off slide switch SW1 (callout [27](#))
- SW10 (FPGA_PROG_B), active-Low pushbutton (callout [28](#))
- PS System Reset Pushbuttons

Power On/Off Slide Switch

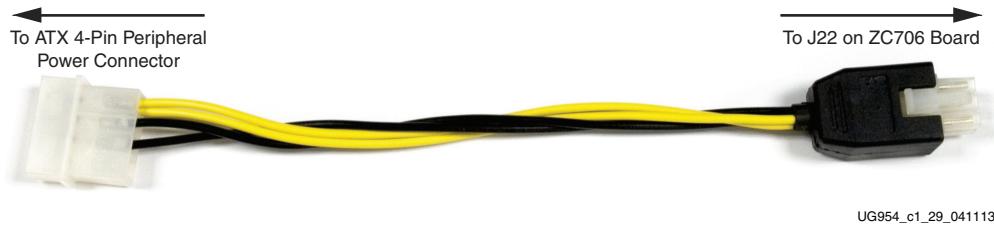
[[Figure 1-2](#), callout 27]

The ZC706 evaluation board power switch is SW1. Sliding the switch actuator from the Off to On position applies 12V power from J22 a 6-pin mini-fit connector. Green LED DS22 illuminates when the ZC706 evaluation board power is on. See [Power Management](#) for details on the onboard power system.



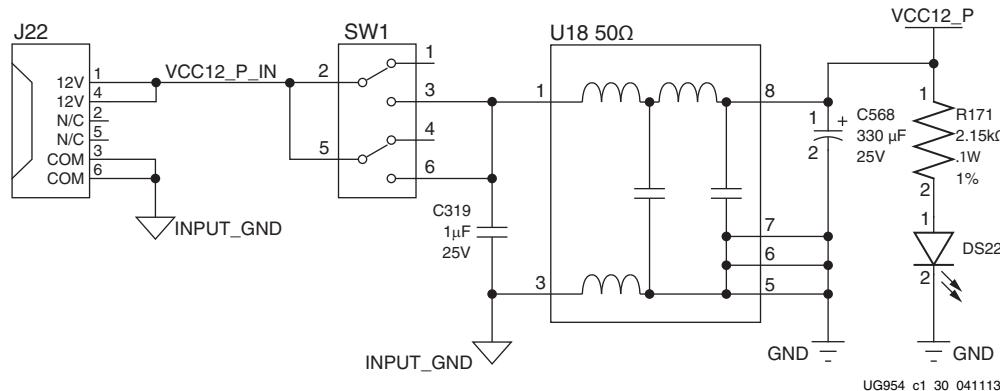
CAUTION! Do NOT plug a PC ATX power supply 6-pin connector into J22 on the ZC706 Evaluation Board. The ATX 6-pin connector has a different pinout than J22. Connecting an ATX 6-pin connector into J22 will damage the ZC706 Evaluation Board and void the board warranty.

The ZC706 evaluation kit provides the adapter cable shown in [Figure 1-29](#) for powering the ZC706 board from the ATX power supply 4-pin peripheral connector. The Xilinx part number for this cable is 2600304, and is equivalent to Sourcegate Technologies part number AZCBL-WH-1109-RA4.



[Figure 1-29: ATX Power Supply Adapter Cable](#)

[Figure 1-30](#) shows the power connector J22, power switch SW1 and indicator LED DS22.



[Figure 1-30: Power On/Off Switch SW1](#)

Program_B Pushbutton

[[Figure 1-2](#), callout 28]

Switch SW10 grounds the XC7Z045 AP SoC PROG_B pin when pressed. This action clears the programmable logic configuration. The FPGA_PROG_B signal is connected to XC7Z045 AP SoC U1 pin Y9.

See [UG470, 7 Series FPGAs Configuration User Guide](#) for further details on configuring the 7 series FPGAs.

[Figure 1-31](#) shows SW10.

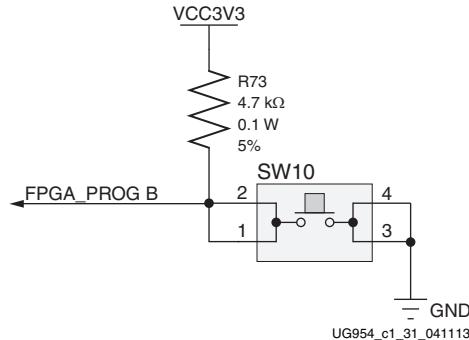
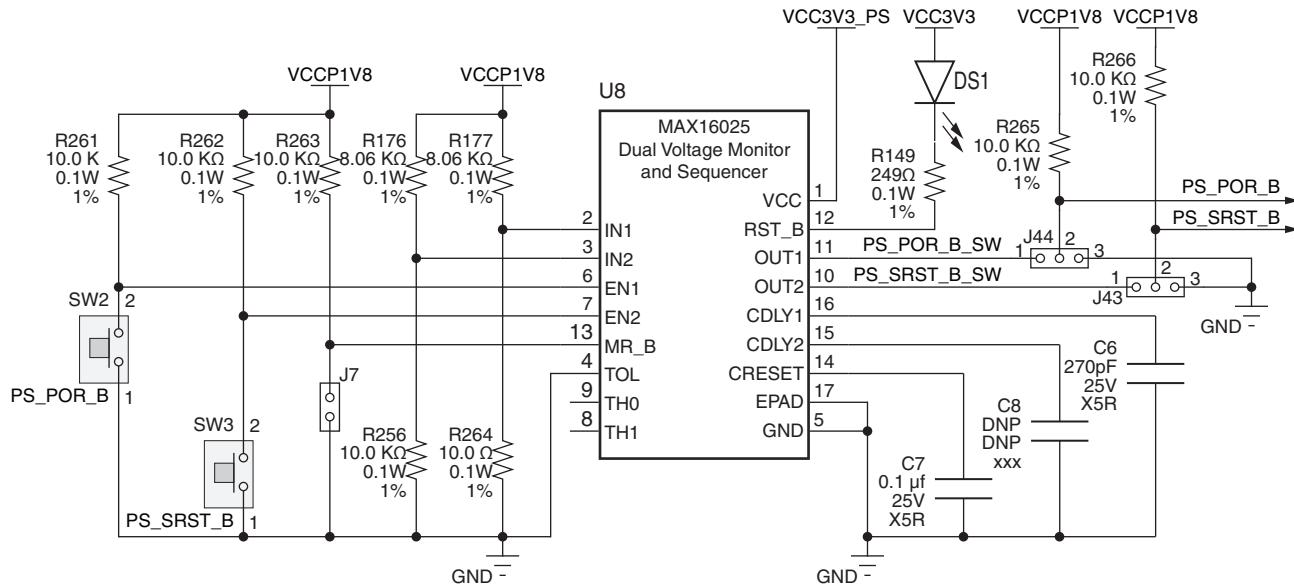


Figure 1-31: PROG_B Pushbutton SW10

PS Power-On and System Reset Pushbuttons

Figure 1-32 shows the reset circuitry for the processing system.



C8 = DNP, SRST delay = 35 µS
 C6 = 270 pF, POR delay = 1.08 ms

UG954_c1_32_041113

Figure 1-32: PS Power On and System Reset Circuitry

Depressing and then releasing pushbutton SW1 causes PS_POR_B_SW to strobe low.

PS_POR_B: This reset is used to hold the PS in reset until all PS power supplies are at the required voltage levels. It must be held Low through PS power-up. PS_POR_B should be generated by the power supply *power-good* signal.

Depressing and then releasing pushbutton SW3 causes PS_SRST_B_SW (connected to the XC7Z045 AP SoC U1 dedicated PS Bank 500 pin D21) to strobe low.

PS_SRST_B: This reset is used to force a system reset. It can be tied or pulled High, and can be High during the PS supply power ramps.

Refer to [UG585](#), *Zynq-7000 All Programmable SoC Technical Reference Manual* for information concerning the resets.

FPGA Mezzanine (FMC) Card Interface

[[Figure 1-2](#), callout 30 and 31]

The ZC706 evaluation board supports the VITA 57.1 FPGA Mezzanine Card (FMC) specification by providing subset implementations of the high pin count (HPC) connector at J37 and low pin count (LPC) version at J5. Both connectors use a 10 x 40 form factor. The HPC connector is populated with 400 pins, while the LPC connector is partially populated with 160 pins. The connectors are keyed so that a mezzanine card, when installed in either of these FMC connectors on the ZC706 evaluation board, faces away from the ZC706 board.

Signaling Speed Ratings:

- Single-ended: 9 GHz (18 Gb/s)
- Differential Optimal Vertical: 9 GHz (18 Gb/s)
- Differential Optimal Horizontal: 16 GHz (32 Gb/s)
- High Density Vertical: 7 GHz (15 Gb/s)

The Samtec connector system is rated for signaling speeds up to 9 GHz (18 Gb/s) based on a –3 dB insertion loss point within a two-level signaling environment.

Connector Type:

- Samtec SEAF Series, 1.27 mm (0.050 in) pitch. Mates with SEAM series connector

For more information about SEAF series connectors, go to the Samtec website at www.samtec.com.

HPC Connector J37

[[Figure 1-2](#), callout 30]

The 400-pin HPC connector defined by the FMC specification ([Figure B-1, page 89](#)) provides connectivity for up to:

- 160 single-ended or 80 differential user-defined signals
- 10 GTX transceivers
- 2 GTX clocks
- 4 differential clocks

- 159 ground and 15 power connections

The connections between the HPC connector at J37 and AP SoC U1 ([Table 1-32](#)) implements a subset of this connectivity:

- 34 differential user-defined pairs (34 LA pairs, LA00–LA33)
- 8 GTX transceivers
- 2 GTX clocks
- 2 differential clocks
- 159 ground and 15 power connections

The ZC706 board V_{ADJ} voltage for the J37 and J5 connectors is determined by the FMC V_{ADJ} power sequencing logic described in the [Power Management, page 77](#).

[Table 1-32](#) shows the J37 HPC FMC to AP SoC U1 connections.

Table 1-32: J37 HPC FMC Connections to XC7Z045 AP SoC U1

| J37 Pin | Net Name | XC7Z045 (U1) Pin | J37 Pin | Net Name | XC7Z045 (U1) Pin |
|---------|-------------------|------------------|---------|-----------------------|------------------|
| A2 | FMC_HPC_DP1_M2C_P | AJ8 | B1 | NC | |
| A3 | FMC_HPC_DP1_M2C_N | AJ7 | B4 | NC | |
| A6 | FMC_HPC_DP2_M2C_P | AG8 | B5 | NC | |
| A7 | FMC_HPC_DP2_M2C_N | AG7 | B8 | NC | |
| A10 | FMC_HPC_DP3_M2C_P | AE8 | B9 | NC | |
| A11 | FMC_HPC_DP3_M2C_N | AE7 | B12 | FMC_HPC_DP7_M2C_P | AD6 |
| A14 | FMC_HPC_DP4_M2C_P | AH6 | B13 | FMC_HPC_DP7_M2C_N | AD5 |
| A15 | FMC_HPC_DP4_M2C_N | AH5 | B16 | FMC_HPC_DP6_M2C_P | AF6 |
| A18 | FMC_HPC_DP5_M2C_P | AG4 | B17 | FMC_HPC_DP6_M2C_N | AF5 |
| A19 | FMC_HPC_DP5_M2C_N | AG3 | B20 | FMC_HPC_GBTCLK1_M2C_P | AA8 |
| A22 | FMC_HPC_DP1_C2M_P | AK6 | B21 | FMC_HPC_GBTCLK1_M2C_N | AA7 |
| A23 | FMC_HPC_DP1_C2M_N | AK5 | B24 | NC | |
| A26 | FMC_HPC_DP2_C2M_P | AJ4 | B25 | NC | |
| A27 | FMC_HPC_DP2_C2M_N | AJ3 | B28 | NC | |
| A30 | FMC_HPC_DP3_C2M_P | AK2 | B29 | NC | |
| A31 | FMC_HPC_DP3_C2M_N | AK1 | B32 | FMC_HPC_DP7_C2M_P | AD2 |
| A34 | FMC_HPC_DP4_C2M_P | AH2 | B33 | FMC_HPC_DP7_C2M_N | AD1 |
| A35 | FMC_HPC_DP4_C2M_N | AH1 | B36 | FMC_HPC_DP6_C2M_P | AE4 |
| A38 | FMC_HPC_DP5_C2M_P | AF2 | B37 | FMC_HPC_DP6_C2M_N | AE3 |
| A39 | FMC_HPC_DP5_C2M_N | AF1 | B40 | NC | |

Table 1-32: J37 HPC FMC Connections to XC7Z045 AP SoC U1 (Cont'd)

| J37 Pin | Net Name | XC7Z045 (U1) Pin | J37 Pin | Net Name | XC7Z045 (U1) Pin |
|---------|-------------------|------------------|---------|-------------------------|------------------|
| | | | | | |
| C2 | FMC_HPC_DP0_C2M_P | AK10 | D1 | PWRCTL1_FMC_PG_C2M | AB20 |
| C3 | FMC_HPC_DP0_C2M_N | AK9 | D4 | FMC_HPC_GBTCLK0_M2C_P | AD10 |
| C6 | FMC_HPC_DP0_M2C_P | AH10 | D5 | FMC_HPC_GBTCLK0_M2C_N | AD9 |
| C7 | FMC_HPC_DP0_M2C_N | AH9 | D8 | FMC_HPC_LA01_CC_P | AG21 |
| C10 | FMC_HPC_LA06_P | AG22 | D9 | FMC_HPC_LA01_CC_N | AH21 |
| C11 | FMC_HPC_LA06_N | AH22 | D11 | FMC_HPC_LA05_P | AH23 |
| C14 | FMC_HPC_LA10_P | AG24 | D12 | FMC_HPC_LA05_N | AH24 |
| C15 | FMC_HPC_LA10_N | AG25 | D14 | FMC_HPC_LA09_P | AD21 |
| C18 | FMC_HPC_LA14_P | AC24 | D15 | FMC_HPC_LA09_N | AE21 |
| C19 | FMC_HPC_LA14_N | AD24 | D17 | FMC_HPC_LA13_P | AA22 |
| C22 | FMC_HPC_LA18_CC_P | W25 | D18 | FMC_HPC_LA13_N | AA23 |
| C23 | FMC_HPC_LA18_CC_N | W26 | D20 | FMC_HPC_LA17_CC_P | V23 |
| C26 | FMC_HPC_LA27_P | V28 | D21 | FMC_HPC_LA17_CC_N | W24 |
| C27 | FMC_HPC_LA27_N | V29 | D23 | FMC_HPC_LA23_P | P25 |
| C30 | FMC_HPC_IIC_SCL | U65.13 | D24 | FMC_HPC_LA23_N | P26 |
| C31 | FMC_HPC_IIC_SDA | U65.12 | D26 | FMC_HPC_LA26_P | R28 |
| C34 | GND | | D27 | FMC_HPC_LA26_N | T28 |
| C35 | VCC12_P | | D29 | FMC_HPC_TCK_BUF | U23.15 |
| C37 | VCC12_P | | D30 | FMC_TDI_BUF | U23.18 |
| C39 | VCC3V3 | | D31 | FMC_HPC_TDO_FMC_LPC_TDI | U32.2 |
| | | | D32 | VCC3V3 | |
| | | | D33 | FMC_HPC_TMS_BUF | U23.17 |
| | | | D34 | NC | |
| | | | D35 | GND | |
| | | | D36 | VCC3V3 | |
| | | | D38 | VCC3V3 | |
| | | | D40 | VCC3V3 | |
| | | | | | |
| E2 | NC | | F1 | FMC_HPC_PG_M2C | U16.16 |
| E3 | NC | | F4 | NC | |
| E6 | NC | | F5 | NC | |
| E7 | NC | | F7 | NC | |
| E9 | NC | | F8 | NC | |

Table 1-32: J37 HPC FMC Connections to XC7Z045 AP SoC U1 (Cont'd)

| J37 Pin | Net Name | XC7Z045 (U1) Pin | J37 Pin | Net Name | XC7Z045 (U1) Pin |
|---------|--------------------|------------------|---------|---------------------|------------------|
| E10 | NC | | F10 | NC | |
| E12 | NC | | F11 | NC | |
| E13 | NC | | F13 | NC | |
| E15 | NC | | F14 | NC | |
| E16 | NC | | F16 | NC | |
| E18 | NC | | F17 | NC | |
| E19 | NC | | F19 | NC | |
| E21 | NC | | F20 | NC | |
| E22 | NC | | F22 | NC | |
| E24 | NC | | F23 | NC | |
| E25 | NC | | F25 | NC | |
| E27 | NC | | F26 | NC | |
| E28 | NC | | F28 | NC | |
| E30 | NC | | F29 | NC | |
| E31 | NC | | F31 | NC | |
| E33 | NC | | F32 | NC | |
| E34 | NC | | F34 | NC | |
| E36 | NC | | F35 | NC | |
| E37 | NC | | F37 | NC | |
| E39 | VADJ | | F38 | NC | |
| | | | F40 | VADJ | |
| | | | | | |
| G2 | FMC_HPC_CLK1_M2C_P | U26 | H1 | NC | |
| G3 | FMC_HPC_CLK1_M2C_N | U27 | H2 | FMC_HPC_PRSNT_M2C_B | U16.15 |
| G6 | FMC_HPC_LA00_CC_P | AF20 | H4 | FMC_HPC_CLK0_M2C_P | AE22 |
| G7 | FMC_HPC_LA00_CC_N | AG20 | H5 | FMC_HPC_CLK0_M2C_N | AF22 |
| G9 | FMC_HPC_LA03_P | AH19 | H7 | FMC_HPC_LA02_P | AK17 |
| G10 | FMC_HPC_LA03_N | AJ19 | H8 | FMC_HPC_LA02_N | AK18 |
| G12 | FMC_HPC_LA08_P | AF19 | H10 | FMC_HPC_LA04_P | AJ20 |
| G13 | FMC_HPC_LA08_N | AG19 | H11 | FMC_HPC_LA04_N | AK20 |
| G15 | FMC_HPC_LA12_P | AF23 | H13 | FMC_HPC_LA07_P | AJ23 |
| G16 | FMC_HPC_LA12_N | AF24 | H14 | FMC_HPC_LA07_N | AJ24 |
| G18 | FMC_HPC_LA16_P | AA24 | H16 | FMC_HPC_LA11_P | AD23 |
| G19 | FMC_HPC_LA16_N | AB24 | H17 | FMC_HPC_LA11_N | AE23 |

Table 1-32: J37 HPC FMC Connections to XC7Z045 AP SoC U1 (Cont'd)

| J37 Pin | Net Name | XC7Z045 (U1) Pin | J37 Pin | Net Name | XC7Z045 (U1) Pin |
|---------|----------------|------------------|---------|----------------|------------------|
| G21 | FMC_HPC_LA20_P | U25 | H19 | FMC_HPC_LA15_P | Y22 |
| G22 | FMC_HPC_LA20_N | V26 | H20 | FMC_HPC_LA15_N | Y23 |
| G24 | FMC_HPC_LA22_P | V27 | H22 | FMC_HPC_LA19_P | T24 |
| G25 | FMC_HPC_LA22_N | W28 | H23 | FMC_HPC_LA19_N | T25 |
| G27 | FMC_HPC_LA25_P | T29 | H25 | FMC_HPC_LA21_P | W29 |
| G28 | FMC_HPC_LA25_N | U29 | H26 | FMC_HPC_LA21_N | W30 |
| G30 | FMC_HPC_LA29_P | R25 | H28 | FMC_HPC_LA24_P | T30 |
| G31 | FMC_HPC_LA29_N | R26 | H29 | FMC_HPC_LA24_N | U30 |
| G33 | FMC_HPC_LA31_P | N29 | H31 | FMC_HPC_LA28_P | P30 |
| G34 | FMC_HPC_LA31_N | P29 | H32 | FMC_HPC_LA28_N | R30 |
| G36 | FMC_HPC_LA33_P | N26 | H34 | FMC_HPC_LA30_P | P23 |
| G37 | FMC_HPC_LA33_N | N27 | H35 | FMC_HPC_LA30_N | P24 |
| G39 | VADJ | | H37 | FMC_HPC_LA32_P | P21 |
| | | | H38 | FMC_HPC_LA32_N | R21 |
| | | | H40 | VADJ | |
| | | | | | |
| J2 | NC | | K1 | NC | |
| J3 | NC | | K4 | NC | |
| J6 | NC | | K5 | NC | |
| J7 | NC | | K7 | NC | |
| J9 | NC | | K8 | NC | |
| J10 | NC | | K10 | NC | |
| J12 | NC | | K11 | NC | |
| J13 | NC | | K13 | NC | |
| J15 | NC | | K14 | NC | |
| J16 | NC | | K16 | NC | |
| J18 | NC | | K17 | NC | |
| J19 | NC | | K19 | NC | |
| J21 | NC | | K20 | NC | |
| J22 | NC | | K22 | NC | |
| J24 | NC | | K23 | NC | |
| J25 | NC | | K25 | NC | |
| J27 | NC | | K26 | NC | |
| J28 | NC | | K28 | NC | |

Table 1-32: J37 HPC FMC Connections to XC7Z045 AP SoC U1 (Cont'd)

| J37 Pin | Net Name | XC7Z045 (U1) Pin | J37 Pin | Net Name | XC7Z045 (U1) Pin |
|---------|----------|------------------|---------|----------|------------------|
| J30 | NC | | K29 | NC | |
| J31 | NC | | K31 | NC | |
| J33 | NC | | K32 | NC | |
| J34 | NC | | K34 | NC | |
| J36 | NC | | K35 | NC | |
| J37 | NC | | K37 | NC | |
| J39 | NC | | K38 | NC | |
| | | K40 | NC | | |

LPC Connector J5

[Figure 1-2, callout 31]

The 160-pin LPC connector defined by the FMC specification (Figure B-1, page 89) provides connectivity for up to:

- 68 single-ended or 34 differential user-defined signals
- 1 GTX transceiver
- 1 GTX clock
- 2 differential clocks
- 61 ground and 10 power connections

The connections between the HPC connector at J5 and AP SoC U1 implements a subset of this connectivity:

- 34 differential user-defined pairs (34 LA pairs, LA00–LA33)
- 1 GTX transceiver
- 1 GTX clock
- 2 differential clocks
- 61 ground and 9 power connections

Table 1-33 shows the FMC LPC connections between J5 and XC7Z045 AP SoC U1.

Table 1-33: J5 LPC FMC Connections to AP SoC U1

| J5 Pin | Net Name | XC7Z045 (U1) Pin | J5 Pin | Net Name | XC7Z045 (U1) Pin |
|--------|--------------------|------------------|--------|-------------------------|------------------|
| C2 | FMC_LPC_DP0_C2M_P | AB2 | D1 | PWRCTL1_FMC_PG_C2M | AB20 |
| C3 | FMC_LPC_DP0_C2M_N | AB1 | D4 | FMC_LPC_GBTCLK0_M2C_P | U8 |
| C6 | FMC_LPC_DP0_M2C_P | AC4 | D5 | FMC_LPC_GBTCLK0_M2C_N | U7 |
| C7 | FMC_LPC_DP0_M2C_N | AC3 | D8 | FMC_LPC_LA01_CC_P | AF15 |
| C10 | FMC_LPC_LA06_P | AB12 | D9 | FMC_LPC_LA01_CC_N | AG15 |
| C11 | FMC_LPC_LA06_N | AC12 | D11 | FMC_LPC_LA05_P | AE16 |
| C14 | FMC_LPC_LA10_P | AC14 | D12 | FMC_LPC_LA05_N | AE15 |
| C15 | FMC_LPC_LA10_N | AC13 | D14 | FMC_LPC_LA09_P | AH14 |
| C18 | FMC_LPC_LA14_P | AF18 | D15 | FMC_LPC_LA09_N | AH13 |
| C19 | FMC_LPC_LA14_N | AF17 | D17 | FMC_LPC_LA13_P | AH17 |
| C22 | FMC_LPC_LA18_CC_P | AE27 | D18 | FMC_LPC_LA13_N | AH16 |
| C23 | FMC_LPC_LA18_CC_N | AF27 | D20 | FMC_LPC_LA17_CC_P | AB27 |
| C26 | FMC_LPC_LA27_P | AJ28 | D21 | FMC_LPC_LA17_CC_N | AC27 |
| C27 | FMC_LPC_LA27_N | AJ29 | D23 | FMC_LPC_LA23_P | AJ26 |
| C30 | FMC_LPC_IIC_SCL | U65.15 | D24 | FMC_LPC_LA23_N | AK26 |
| C31 | FMC_LPC_IIC_SDA | U65.14 | D26 | FMC_LPC_LA26_P | AJ30 |
| C34 | GND | | D27 | FMC_LPC_LA26_N | AK30 |
| C35 | VCC12_P | | D29 | FMC_LPC_TCK_BUF | U23.14 |
| C37 | VCC12_P | | D30 | FMC_HPC_TDO_FMC_LPC_TDI | U31.1 |
| C39 | VCC3V3 | | D31 | FMC_LPC_TDO_FPGA_TDI | U31.2 |
| | | | D32 | VCC3V3 | |
| | | | D33 | FMC_LPC_TMS_BUF | U23.16 |
| | | | D34 | NC | |
| | | | D35 | GND | |
| | | | D36 | VCC3V3 | |
| | | | D38 | VCC3V3 | |
| | | | D40 | VCC3V3 | |
| | | | | | |
| G2 | FMC_LPC_CLK1_M2C_P | AC28 | H1 | NC | |
| G3 | FMC_LPC_CLK1_M2C_N | AD28 | H2 | FMC_LPC_PRSNT_M2C_B | U16.14 |
| G6 | FMC_LPC_LA00_CC_P | AE13 | H4 | FMC_LPC_CLK0_M2C_P | AG17 |
| G7 | FMC_LPC_LA00_CC_N | AF13 | H5 | FMC_LPC_CLK0_M2C_N | AG16 |
| G9 | FMC_LPC_LA03_P | AG12 | H7 | FMC_LPC_LA02_P | AE12 |
| G10 | FMC_LPC_LA03_N | AH12 | H8 | FMC_LPC_LA02_N | AF12 |

Table 1-33: J5 LPC FMC Connections to AP SoC U1 (Cont'd)

| J5 Pin | Net Name | XC7Z045 (U1) Pin | J5 Pin | Net Name | XC7Z045 (U1) Pin |
|--------|----------------|------------------|--------|----------------|------------------|
| G12 | FMC_LPC_LA08_P | AD14 | H10 | FMC_LPC_LA04_P | AJ15 |
| G13 | FMC_LPC_LA08_N | AD13 | H11 | FMC_LPC_LA04_N | AK15 |
| G15 | FMC_LPC_LA12_P | AD16 | H13 | FMC_LPC_LA07_P | AA15 |
| G16 | FMC_LPC_LA12_N | AD15 | H14 | FMC_LPC_LA07_N | AA14 |
| G18 | FMC_LPC_LA16_P | AE18 | H16 | FMC_LPC_LA11_P | AJ16 |
| G19 | FMC_LPC_LA16_N | AE17 | H17 | FMC_LPC_LA11_N | AK16 |
| G21 | FMC_LPC_LA20_P | AG26 | H19 | FMC_LPC_LA15_P | AB15 |
| G22 | FMC_LPC_LA20_N | AG27 | H20 | FMC_LPC_LA15_N | AB14 |
| G24 | FMC_LPC_LA22_P | AK27 | H22 | FMC_LPC_LA19_P | AH26 |
| G25 | FMC_LPC_LA22_N | AK28 | H23 | FMC_LPC_LA19_N | AH27 |
| G27 | FMC_LPC_LA25_P | AF29 | H25 | FMC_LPC_LA21_P | AH28 |
| G28 | FMC_LPC_LA25_N | AG29 | H26 | FMC_LPC_LA21_N | AH29 |
| G30 | FMC_LPC_LA29_P | AE25 | H28 | FMC_LPC_LA24_P | AF30 |
| G31 | FMC_LPC_LA29_N | AF25 | H29 | FMC_LPC_LA24_N | AG30 |
| G33 | FMC_LPC_LA31_P | AC29 | H31 | FMC_LPC_LA28_P | AD25 |
| G34 | FMC_LPC_LA31_N | AD29 | H32 | FMC_LPC_LA28_N | AE26 |
| G36 | FMC_LPC_LA33_P | Y30 | H34 | FMC_LPC_LA30_P | AB29 |
| G37 | FMC_LPC_LA33_N | AA30 | H35 | FMC_LPC_LA30_N | AB30 |
| G39 | VADJ | | H37 | FMC_LPC_LA32_P | Y26 |
| | | | H38 | FMC_LPC_LA32_N | Y27 |
| | | | H40 | VADJ | |

ZC706 Board Power System

The ZC706 board hosts a power system based on the Texas Instruments (TI) UCD90120A power supply sequencer and monitor, and the TI TPS84K and LMZ22000 family voltage regulators.

UCD90120A Description

The UCD90120A is a 12-rail PMBus/I²C addressable power-supply sequencer and monitor. The device integrates a 12-bit ADC for monitoring up to 12 power-supply voltage inputs. Twenty-six GPIO pins can be used for power supply enables, power-on reset signals, external interrupts, cascading, or other system functions. Twelve of these pins offer pulse width modulation (PWM) functionality. Using these pins, the UCD90120A offers support for margining and general purpose PWM functions.

The TI Fusion Digital Power™ designer software is provided for device configuration. This PC-based graphical user interface (GUI) offers an intuitive interface for configuring, storing, and monitoring all system operating parameters.

TPS84K Family Regulator Description

The TPS84621RUQ (6A) and TPS84320RUQ (3A) regulators are integrated synchronous buck power solutions that combine a DC-DC converter with power MOSFETs, an inductor, and passives into low profile BQFN packages. The TPS84K devices accept an input voltage rail between 4.5V and 14.5V and deliver an adjustable output voltage in the 0.6V to 5.5V range. This type of power solution allows as few as three external components and eliminates the loop compensation and magnetic parts selection process.

LMZ22000 Family Regulator Description

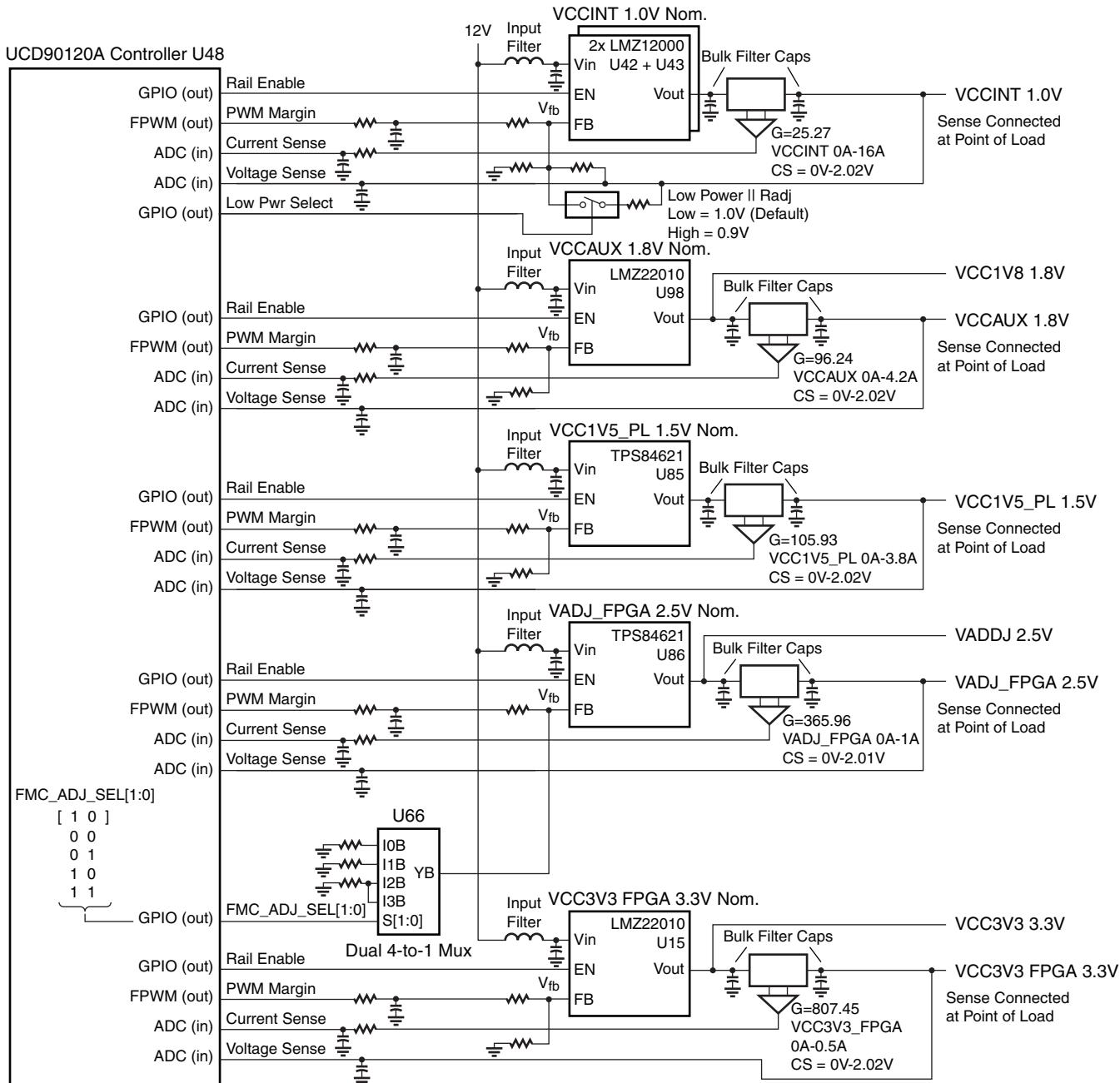
The LMZ22010 SIMPLE SWITCHER® power module is a step-down DC-DC solution capable of driving up to 10A load. The LMZ22010 module can accept an input voltage rail between 6V and 20V and deliver an adjustable and highly accurate output voltage as low as 0.8V. The LMZ22010 module only requires two external resistors and external capacitors to complete the power solution. The LMZ22010 module is a reliable and robust design with the following protection features: thermal shutdown, programmable input under-voltage lockout, output over-voltage protection, short-circuits protection, output current limit, and allows startup into a pre-biased output. The sync input allows synchronization over the 314 kHz to 600 kHz switching frequency range and up to six modules can be connected in parallel for higher load currents.

[Table 1-34](#) shows the ZC706 board TI power system configuration for controller U48.

Table 1-34: ZC706 TI Controller U48 Power System Configuration

| Sequencer | Schematic Page | | | Regulator Type, U# | Voltage | Current |
|----------------------------------|----------------|------------------|--------------------|--------------------|---------|---------|
| | Page | Contents | Net Name | | | |
| U48 PMBus Addr 101 5 Rails | 49 | UCD90120A | | | | |
| | 50 | Addr 101, Rail 1 | VCCINT | 2xLMZ22008 U42,U43 | 1.0V | 16A |
| | 51 | Addr 101, Rail 2 | VCCAUX | LMZ22010 | 1.8V | 10A |
| | 52 | Addr 101, Rail 3 | VCC1V5_PL | TPS84621 U85 | 1.5V | 6A |
| | 53 | Addr 101, Rail 4 | VADJ_FPGA,VADJ | TPS84621 U86 | 2.5V | 6A |
| | 54 | Addr 101, Rail 5 | VCC3V3_FPGA,VCC3V3 | LMZ22010 | 3.3V | 10A |

[Figure 1-33](#) shows the power system for UCD90120A U48 controller.

**Notes:**

1. Capacitors labeled Cf are bulk filter capacitors.
2. Voltage Sense is connected a point of load.

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Figure 1-33: ZC706 TI UCD90120A Controller U48 Power System

Both the TPS84K and LMZ22000 family adjustable voltage regulators have their output voltage set through an external resistor. The regulator topology on the ZC706 board permits the TI UCD90120A module to monitor rail voltage and current. Voltage margining at +5% and -5% is also implemented.

Each voltage regulator's external V_{OUT} setting resistor is calculated and implemented as if the regulator is stand-alone. The TI UCD90120A module has two ADC inputs allocated per voltage rail, one input for the remote voltage sense connection, the other for the current sense resistor op amp output voltage connection. The TI UCD90120A ADC full scale input is 2.5V. The remote voltage feedback is scaled to approximately 2V if it exceeds 2V, that is, the V_{CCO_VADJ} rail for the 2.5V and 3.3V modes, and the $FPGA_3V3$ rail also at 3.3V are resistor-attenuated to scale the remotely sensed voltage at a ratio of 0.606 to give approximately 2V at the ADC input pin for a 3.3V remote sense value. Rails below 2V are not scaled.

Each rail's current sense op amp has its gain set to provide approximately 2V maximum at the TI UCD90120A ADC input pin when the rail current is at its expected maximum current level, as can be seen in the U48 controller power system figure ([Figure 1-33](#)).

The TI UCD90120A module has an assignable group of GPIO pins with PWM capability. Each controller "channel" has a PWM GPIO pin wired to the associated voltage regulator V_{ADJ} pin. The external V_{OUT} setting resistor is also wired to this pin. The PWM GPIO pin is configured in 3-state mode. This pin is not driven unless a Margin command is executed. The Margin command is available within the TI Fusion Digital Power™ designer software.

During the margin-High or Low operation, the PWM GPIO pin drives a voltage into the voltage regulator V_{ADJ} pin, which causes a slight voltage change resulting in the regulator V_{OUT} moving to the margin +5% or -5% voltage commanded.

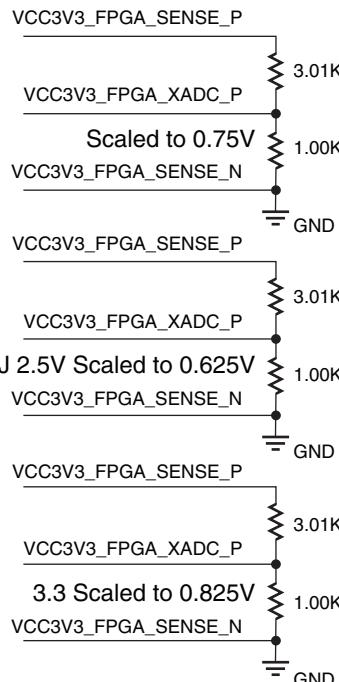
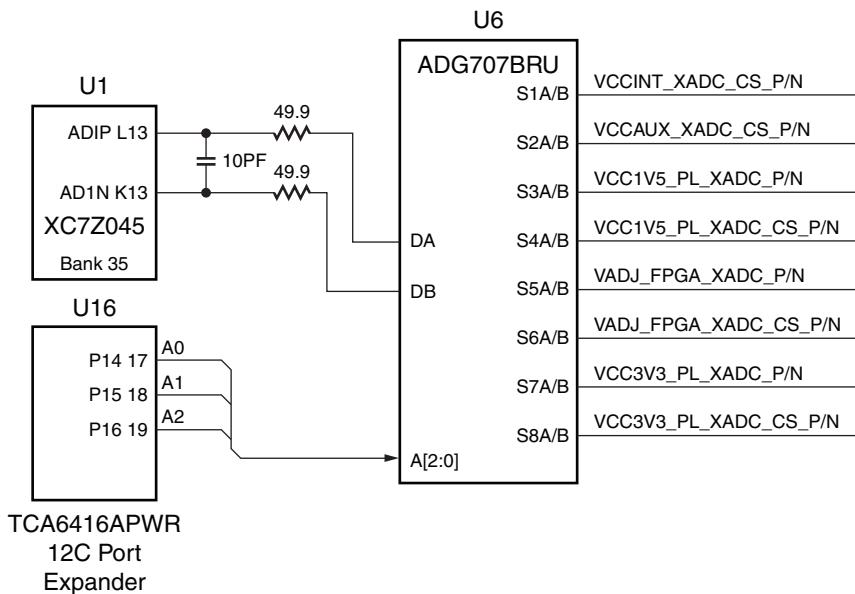
XADC Power System Measurement

The ZC706 board XADC interface includes power system voltage and current measuring capability. The V_{CCINT} and V_{CCAUX} rail voltages are measured using the XADC internal voltage measurement capability. Other rails are measured through an external Analog Devices ADG707BRU multiplexer U6. Each rail has a separate TI INA333 op amp strapped across its series current sense resistor Kelvin terminals. This op amp has its gain adjusted to give approximately 1V at the expected full scale current value for the rail.

[Figure 1-34](#) shows the XADC external MUX block diagram.

Notes:

- 1. _XADC_P/N = Remote Voltage Sense
 - 2. _XADC_CS_P/N = Current Sense From OP Amp



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Figure 1-34: XADC External MUX Block Diagram

See [Table 1-35](#) which lists the ZC706 XADC power system voltage and current measurement details for the external MUX U6.

Table 1-35: XADC Measurements through MUX U6

| Meas. Type | Rail Name | Current Range | Isense Op Amp | | | Schematic Net Name | 8-to-1 MUX U6 | | MUX A[2:0] | | |
|------------|--------------|---------------|---|------|----------|---------------------|---------------|----------|------------|--|--|
| | | | Reference Designator | Gain | Vo Range | | Pin Num | Pin Name | | | |
| V | VCCINT | NA | NA | NA | NA | XADC INTERNAL | NA | NA | NA | | |
| I | VCCINT CS | 0A-8A | U69 | 20 | 0V-0.8V | VCCINT_XADC_CS_P | 19 | S1A | 000 | | |
| | | | | | | VCCINT_XADC_CS_N | 11 | S1B | | | |
| V | VCCAUX | NA | NA | NA | NA | XADC INTERNAL | NA | NA | NA | | |
| I | VCCAUX CS | 0A-4A | U68 | 50 | 0V-1V | VCCAUX_XADC_CS_P | 20 | S2A | 001 | | |
| | | | | | | VCCAUX_XADC_CS_N | 10 | S2B | | | |
| V | VCC1V5_PL | NA | VCC1V5_PL REMOTE SENSE DIVIDED TO DELIVER 0.75V ON VCC1V5_PL_XADC_P | | | VCC1V5_PL_XADC_P | 21 | S3A | 010 | | |
| | | | | | | VCC1V5_PL_SENSE_N | 9 | S3B | | | |
| I | VCC1V5_PL CS | 0A-2A | U67 | 100 | 0V-1V | VCC1V5_PL_XADC_CS_P | 22 | S4A | 011 | | |
| | | | | | | VCC1V5_PL_XADC_CS_N | 8 | S4B | | | |
| V | VADJ_FPGA | NA | VADJ_FPGA 2.5V REMOTE SENSE DIVIDED TO DELIVER 0.625V ON VADJ_FPGA_XADC_P | | | VADJ_FPGA_XADC_P | 23 | S5A | 100 | | |
| | | | | | | VADJ_FPGA_SENSE_N | 7 | S5B | | | |

Table 1-35: XADC Measurements through MUX U6 (Cont'd)

| Meas. Type | Rail Name | Current Range | Isense Op Amp | | | Schematic Net Name | 8-to-1 MUX U6 | | MUX A[2:0] | | |
|------------|----------------|---------------|--|------|----------|-----------------------|---------------|----------|------------|--|--|
| | | | Reference Designator | Gain | Vo Range | | Pin Num | Pin Name | | | |
| I | VADJ_FPGA CS | 0A-2A | U70 | 100 | 0V-1V | VADJ_FPGA_XADC_CS_P | 24 | S6A | 101 | | |
| | | | | | | VADJ_FPGA_XADC_CS_N | 6 | S6B | | | |
| V | VCC3V3_FPGA | NA | VCC3V3_FPGA REMOTE SENSE DIVIDED TO DELIVER 0.825V ON VCC3V3_FPGA_XADC_P | | | VCC3V3_FPGA_XADC_P | 25 | S7A | 110 | | |
| | | | | | | VCC3V3_FPGA_SENSE_N | 5 | S7B | | | |
| I | VCC3V3_FPGA CS | 0A-2A | U97 | 100 | 0V-1V | VCC3V3_FPGA_XADC_CS_P | 26 | S8A | 111 | | |
| | | | | | | VCC3V3_FPGA_XADC_CS_N | 4 | S8B | | | |

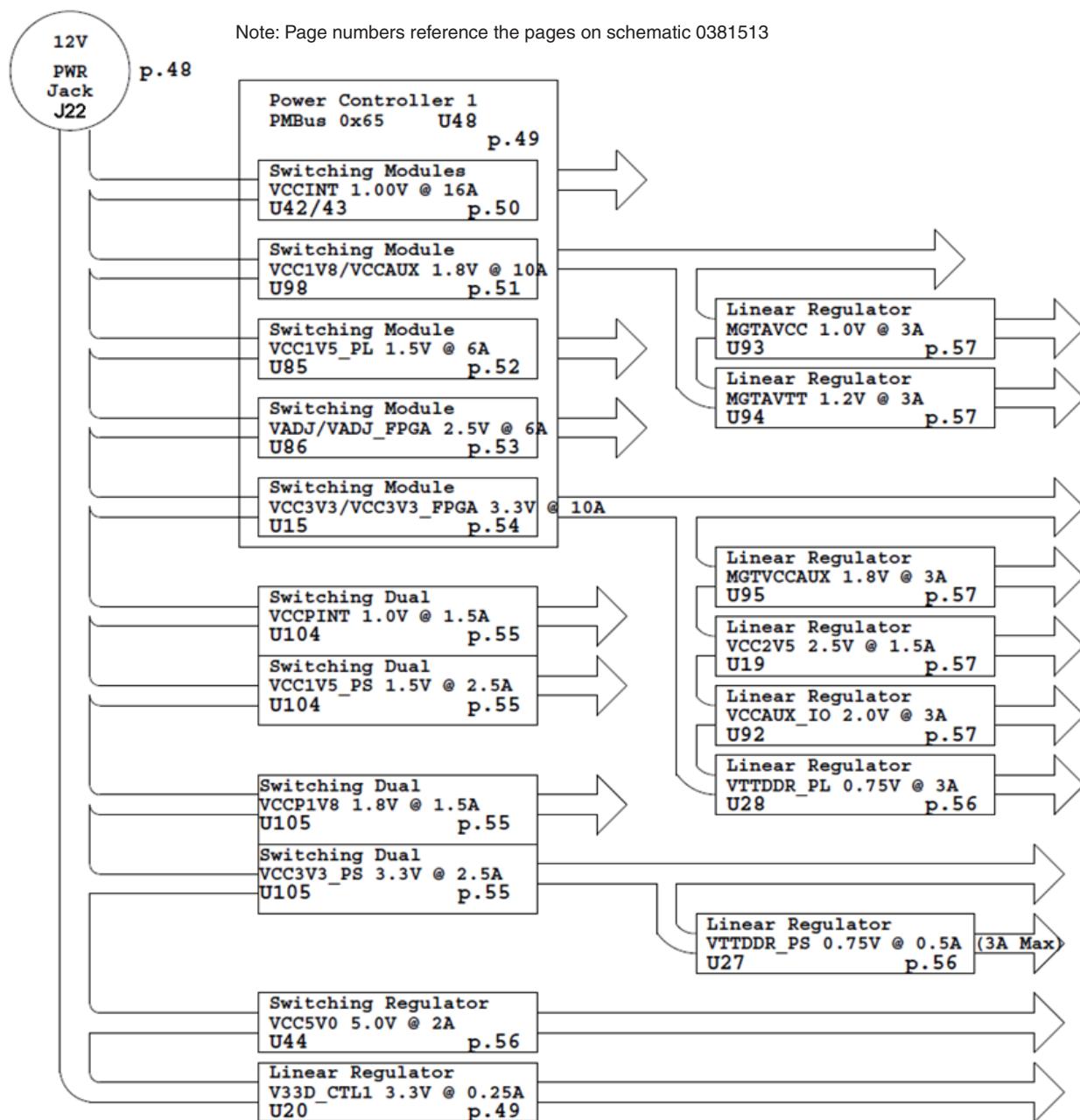
Power Management

[Figure 1-2, callout 32]

The ZC706 board uses power regulators and a PMBus-compliant system controller from Texas Instruments to supply core and auxiliary voltages. The Texas Instruments Fusion Digital Power graphical user interface is used to monitor the voltage and current levels of the board power modules.

The PCB layout and power system design meet the recommended criteria described in *Zynq-7000 All Programmable SoC PCB Design and Pin Planning Guide* ([UG933](#)).

The ZC706 evaluation board power distribution diagram is shown in [Figure 1-35](#).



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Figure 1-35: Onboard Power Regulators

The ZC706 evaluation board uses power regulators and PMBus compliant PWM system controllers from Texas Instruments to supply the core and auxiliary voltages listed in Table 1-36.

Table 1-36: Onboard Power System Devices

| Device Type | Reference Designator | Description | Power Rail Net Name | Power Rail Voltage | Schematic Page |
|---------------------------|----------------------|---|----------------------------|--------------------|----------------|
| UCD90120A | U48 | PMBus Controller, PMBus Addr = 101 | | | 49 |
| LMZ22008TZ ⁽¹⁾ | U42 | 1 of 2 8A 0.8V - 6V shared Adj. Switching Regulator | VCCINT ⁽²⁾ | 1.00V | 50 |
| LMZ22008TZ ⁽¹⁾ | U43 | 2 of 2 8A 0.8V - 6V shared Adj. Switching Regulator | VCCINT | 1.00V | 50 |
| LMZ22010TZ | U98 | 10A 0.8V - 6V Adj. Switching Regulator | VCCAUX ⁽³⁾ | 1.80V | 51 |
| TPS84621RUQ | U85 | 6A 0.6V - 5.5V Adj. Switching Regulator | VCC1V5_PL | 1.50V | 52 |
| TPS84621RUQ | U86 | 6A 0.6V - 5.5V Adj. Switching Regulator | VADJ_FPGA ⁽⁴⁾ | 2.50V | 53 |
| LMZ22010TZ | U15 | 10A 0.8V - 6V Adj. Switching Regulator | VCC3V3_FPGA ⁽⁵⁾ | 3.30V | 54 |
| | | | | | |
| TPS54291PWP (Dual Output) | U104 | 2.5A 0.8V - 10V Adj. Switching Regulator | VCCPINT | 1.00V | 55 |
| | | 2.5A 0.8V - 10V Adj. Switching Regulator | VCC1V5_PS | 1.50V | 55 |
| TPS54291PWP (Dual Output) | U105 | 2.5A 0.8V - 10V Adj. Switching Regulator | VCCP1V8 | 1.80V | 55 |
| | | 2.5A 0.8V - 10V Adj. Switching Regulator | VCC3V3_PS | 3.30V | 55 |
| TPS51200DR | U27 | 3A Push/Pull Tracking Regulator | VTTDDR_PS | 0.75V | 56 |
| TPS51200DR | U28 | 3A Push/Pull Tracking Regulator | VTTDDR_SODIMM | 0.75V | 56 |
| TPS74901RGW | U92 | 3A 0.8V - 3.6V Adj. Linear Regulator | VCCAUX_IO | 2.00V | 57 |
| TPS74901RGW | U93 | 3A 0.8V - 3.6V Adj. Linear Regulator | MGTAVCC | 1.00V | 57 |
| TPS74901RGW | U94 | 3A 0.8V - 3.6V Adj. Linear Regulator | MGTAVTT | 1.20V | 57 |
| TPS74901RGW | U95 | 3A 0.8V - 3.6V Adj. Linear Regulator | MGTVCAXAUX | 1.80V | 57 |
| TL1963A | U19 | 1.5A 1.21V - 3.3V Adj. Linear Regulator | VCC2V5 | 2.50V | 57 |
| TPS79433 | U20 | 0.25A 3.3V Fixed Linear Regulator | V33D_CTL1 | 3.30V | 49 |

Notes:

1. VCCINT max. current is 16A
2. VCCBRAM 1.0V is also sourced from the Vccint rail
3. VCC1V8 1.80V is also sourced from the Vccaux rail
4. VADJ (1.80V/2.50V/3.30V) for the FMC connectors is also sourced from the Vadj_fpga rail
5. VCC3V3 3.30V is also sourced from the Vcc3v3_fpga rail

VADJ Voltage Control

The V_{ADJ} rail is set to 2.5V. When the ZC706 evaluation board is powered on, the state of the FMC_VADJ_ON_B signal wired to header J18 is sampled by the TI UCD90120A controller U48. If a jumper is installed on J18 signal FMC_VADJ_ON_B is held Low, and the TI controller U48 energizes the V_{ADJ} rail at power on.

Because the rail turn on decision is made at power on time based on the presence of the J18 jumper, removing the jumper at J18 after the board is powered up does not affect the 2.5V power delivered to the V_{ADJ} rail and it remains on.

A jumper installed at J18 is the default setting.

In this mode the user can control when to turn on V_{ADJ} and to which voltage level (1.8V, 2.5V, 3.3V). With V_{ADJ} off the XC7Z045 AP SoC still configures and has access to the TI controller PMBUS along with the FMC_VADJ_ON_B signal. The combination of these allows the user to develop code to command the V_{ADJ} rail to be set to something other than the default setting of 2.5V. Once the new V_{ADJ} voltage level has been programmed into TI controller U48, the FMC_VADJ_ON_B signal can be driven low by the user logic and the V_{ADJ} rail comes up at the new V_{ADJ} voltage level. Installing a jumper at J18 after a ZC706 board powers up in the V_{ADJ} off (no jumper on J18 at ZC706 power up) mode turns on the V_{ADJ} rail.

The FMC_VADJ_ON_B signal is connected to the TCA6416APWR I²C port expander U16 pin 13 (see [Figure 1-28](#)). The XC7Z045 AP SoC is thus able to drive the FMC_VADJ_ON_B signal by writing to the I²C port expander U16.

The I²C port expander IIC_PORT_EXPANDER SDA/SCL bus is wired to the PCA9548ARGER I²C U65 bus switch (see [I²C Bus, page 53](#)).

Documentation describing PMBUS programming for the UCD90120A power controller is available at www.ti.com/fusiondocs

AP SoC Programmable Logic (PL) Voltage Control

All PL and PS power rails are enabled by default. When the ZC706 board is powered on, the state of the PL_PWR_ON signal wired to 2-pin header J66 is sampled by the TI UCD90120A controller U48. If a jumper is not installed on J66, signal PL_PWR_ON is held high, and the TI controller U48 energizes all the PL and PS power rails.

Because the rail turn on decision is made at power on time based on the presence of the J66 jumper, installing the jumper at J66 after the board is powered up does not affect power delivered to the any PS or PL rails, all rails remain on.

A jumper not installed at J66 is the default setting.

If a jumper is installed on J66 when the ZC706 board is powered on, signal PL_PWR_ON is held low, and the ZC706 board does not energize the PL side power rails at power on.

Monitoring Voltage and Current

Voltage and current monitoring and control are available for selected power rails through Texas Instruments' Fusion Digital Power Designer graphical user interface. The onboard TI power controller (U48 at address 101) is accessed through the PMBus connector J4, which is provided for use with the TI USB Interface Adapter PMBus pod (TI part number EVM USB-TO-GPIO), which can be ordered from the Texas Instruments website

www.ti.com/xilinx_usb and associated TI Fusion Digital Power Designer GUI (downloadable from www.ti.com/fusion-gui). This is the simplest and most convenient way to monitor the voltage and current values for the power rails listed in [Table 1-37](#).

In the table, the Power Good (PG) On Threshold is the setpoint at or above which the particular rail is deemed "good". The PG Off Threshold is the setpoint at or below which the particular rail is no longer deemed "good". The controller internally OR's these per rail PG conditions together and drives an output PG pin high only if all active rail PG states are "good". The On and Off Delay and parameters are relative to when the board power on-off slide switch SW12 is turned on and off.

[Table 1-37](#) Power Rail Specifications for UCD90120A PMBus controller at Address 101 defines the voltage and current values for each power rail controlled by the UCD90120A U48.



IMPORTANT: In [Table 1-37](#), the values defined in the Shutdown columns are the voltage and current thresholds that cause the regulator to shut down if the value is exceeded.

Table 1-37: Power Rail Specifications for UCD90120A PMBus Controller at Address 101

| Device | Address | Rail | Nominal Voltage | Power Good On | Power Good Off | Turn On Delay (ms) ⁽²⁾ | Turn Off Delay (ms) | Shutdown ⁽¹⁾ | | |
|---------------|---------|------|-----------------|---------------|----------------|-----------------------------------|---------------------|-------------------------|--------------|-------|
| | | | | | | | | Over Voltage | Over Current | |
| UCD90120A U48 | 101d | 1 | VCCINT | 1.000 | 0.900 | 0.850 | 0.0 | 25.0 | 1.150 | 11.50 |
| | | 2 | VCCAUX | 1.800 | 1.620 | 1.530 | 5.0 | 20.0 | 2.070 | 6.91 |
| | | 3 | VCC1V5_PL | 1.500 | 1.350 | 1.275 | 5.0 | 10.0 | 1.725 | 3.50 |
| | | 4 | VADJ_FPGA | 2.500 | 2.250 | 2.125 | 5.0 | 5.0 | 2.875 | 3.50 |
| | | 5 | VCC3V3_FPGA | 3.300 | 2.970 | 2.805 | 5.0 | 15.0 | 3.795 | 6.91 |

Notes:

1. The values defined in these columns are the voltage and current thresholds that cause the regulator to shut down if the value is exceeded.
2. See [Table 1-39](#) for rail turn on dependency details.

The ZC706 power system rail turn on timing is not strictly controlled through the Turn On Delay shown in [Table 1-37](#). The [Table 1-37](#) Turn On Delay values are applied after the preceding rail has reached 90% of its nominal voltage. See [Table 1-38](#) for rail turn on dependency details.

Table 1-38: Power Rail Sequence On Dependencies for UCD90120A PMBus Controller at Address 101

| Device | Address | Rail | Nominal Voltage | Turn On Order | Turn On Timing | |
|-----------|---------|------|-----------------|---------------|----------------|------------------------------|
| UCD90120A | 101d | 1 | VCCINT | 1.000 | 1 | Turn on at board power-on |
| | | 2 | VCCAUX | 1.800 | 2 | 5ms after VCCINT hits 90% |
| | | 5 | VCC3V3_FPGA | 3.300 | 3 | 5ms after VCCAUX hits 90% |
| | | 3 | VCC1V5_PL | 1.500 | 4 | 5ms after VCC3V3 hits 90% |
| | | 4 | VADJ_FPGA | 2.500 | 5 | 5ms after VCC1V5_PL hits 90% |

Cooling Fan

The XC7Z045 AP SoC cooling fan connector is shown in [Figure 1-36](#).

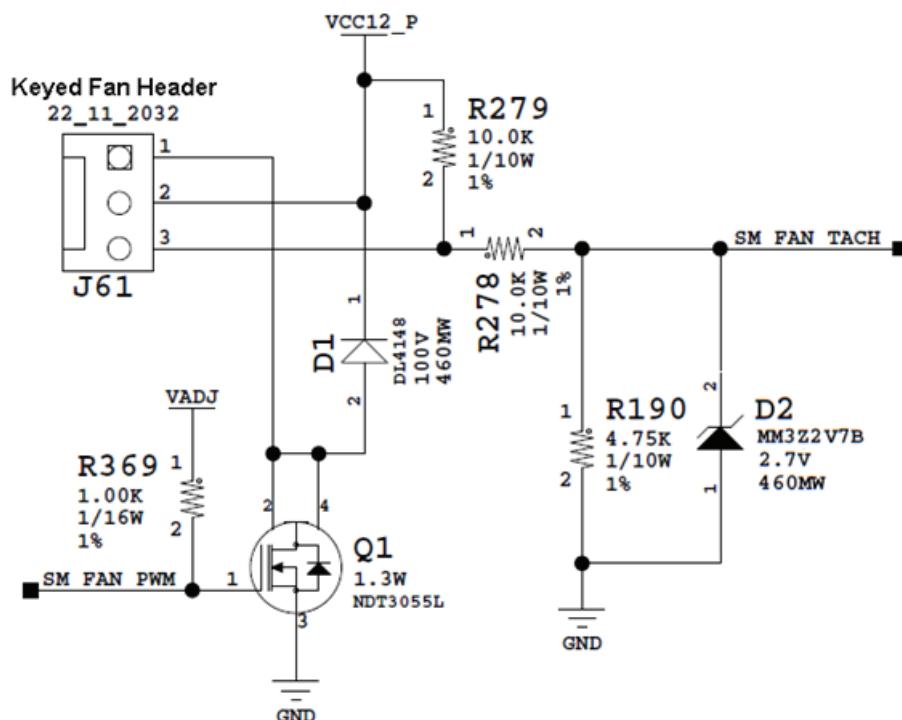


Figure 1-36: Cooling Fan Circuit

The fan turns on when the ZC706 is power up due to pull-up resistor R369. The SM_FAN_PWM and SM_FAN_TACH signals are wired to XC7Z045 AP SoC U1 pins AB19 and AA19 respectively, enabling the user to implement their own fan speed control IP in the AP SoC PL logic.

More information about the power system components used by the ZC706 evaluation board are available from the Texas Instruments digital power website at www.ti.com/ww/en/analog/digital-power/index.html

XADC Analog-to-Digital Converter

[Figure 1-2, callout 33]

The XC7Z045 AP SoC provides an Analog Front End XADC block. The XADC block includes a dual 12-bit, 1 MSPS Analog-to-Digital Convertor (ADC) and on-chip sensors. See [UG480, 7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide](#) for details on the capabilities of the analog front end. [Figure 1-37](#) shows the XADC block diagram.

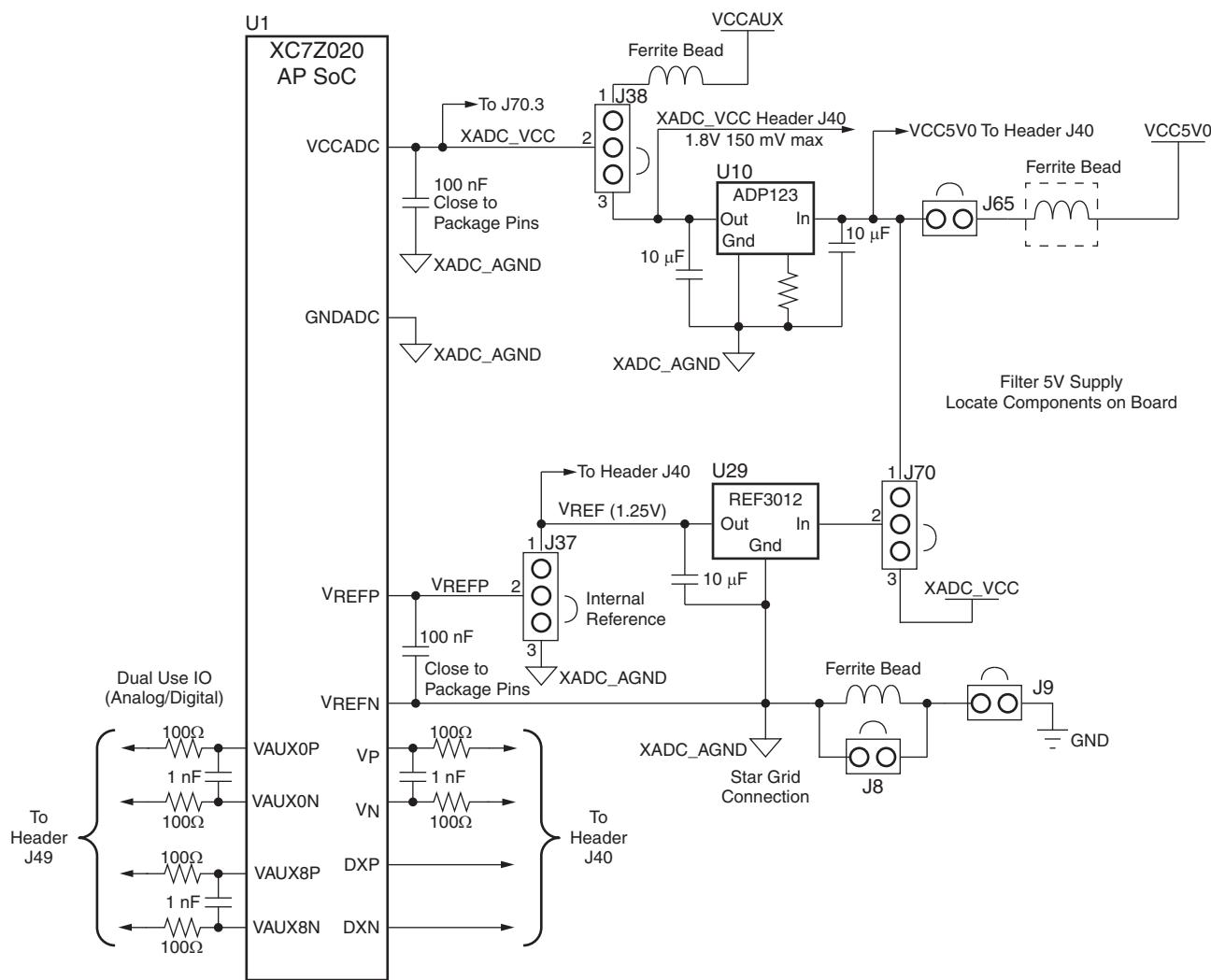


Figure 1-37: XADC Block Diagram

The ZC706 evaluation board supports both the internal XC7Z045 AP SoC sensor measurements and the external measurement capabilities of the XADC. Internal measurements of the die temperature, VCCINT, VCCAUX, and VCCBRAM are available.

Jumper J52 can be used to select either an external voltage reference (VREF) or on-chip voltage reference for the analog-to-digital converter.

For external measurements an XADC header (J63) is provided. This header can be used to provide analog inputs to the XC7Z045 AP SoC's dedicated VP/VN channel, and to the VAUXP[0]/VAUXN[0], VAUXP[8]/VAUXN[8] auxiliary analog input channels. Simultaneous sampling of Channel 0 and Channel 8 is supported.

A user-provided analog signal multiplexer card can be used to sample additional external analog inputs using the 4 GPIO pins available on the XADC header as multiplexer address lines. [Figure 1-38](#) shows the XADC header connections.

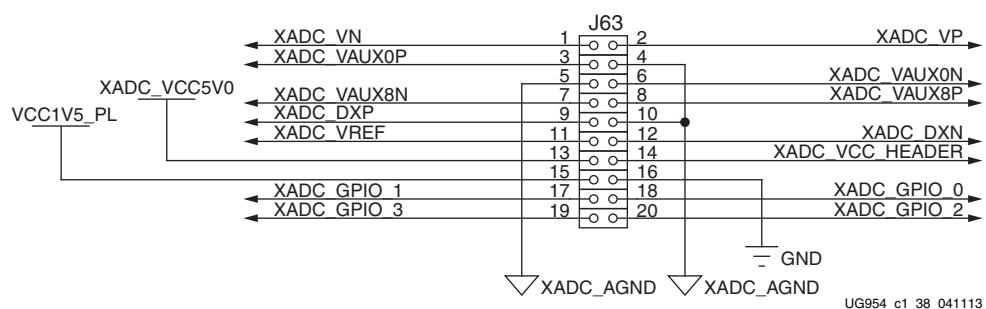


Figure 1-38: XADC Header (J63)

Table 1-39 describes the XADC header J40 pin functions.

Table 1-39: XADC Header J63 Pinout

| Net Name | J63 Pin Number | Description |
|-----------------|----------------|--|
| VN, VP | 1, 2 | Dedicated analog input channel for the XADC. |
| XADC_VAUX0P, N | 3, 6 | Auxiliary analog input channel 0. Also supports use as IO inputs when anti alias capacitor is not present. |
| XADC_VAUX8N, P | 7, 8 | Auxiliary analog input channel 8. Also supports use as IO inputs when anti alias capacitor is not present. |
| DXP, DXN | 9, 12 | Access to thermal diode. |
| XADC_AGND | 4, 5, 10 | Analog ground reference. |
| XADC_VREF | 11 | 1.25V reference from the board. |
| XADC_VCC5V0 | 13 | Filtered 5V supply from board. |
| XADC_VCC_HEADER | 14 | Analog 1.8V supply for XADC. |
| VCC1V5_PL | 15 | VCCO supply for bank which is the source of DIO pins. |

Table 1-39: XADC Header J63 Pinout (Cont'd)

| Net Name | J63 Pin Number | Description |
|----------------------|----------------|--|
| GND | 16 | Digital Ground (board) Reference |
| XADC_GPIO_3, 2, 1, 0 | 19, 20, 17, 18 | Digital IO. These pins should come from the same bank. These IOs should not be shared with other functions because they are required to support three-state operation. |

Default Switch and Jumper Settings

The default switch and jumper settings for the ZC706 evaluation board are provided in this appendix.

Switches

[[Figure 1-2](#), callout 24]

Default switch settings are listed in [Table A-1](#).

Table A-1: Default Switch Settings

| Switch | Function | Default | Selects | Figure 1-2 Callout |
|--------|---|----------|---------------------------|------------------------------------|
| SW1 | Board main power On-Off Slide Switch | OFF | Delivered in OFF position | 27 |
| SW4 | 2-pole SPST DIP Switch, JTAG mode select signals JTAG_SEL[1:2] | 10 | JTAG = cable connector J3 | 34 |
| SW11 | 5-pole DPDT DIP Switch, PS Boot Mode select signals MIO[6:2]_SELECT | All Down | JTAG flat cable header J3 | 29 |
| SW12 | 4-pole SPST DIP Switch, user signals GPIO_DIP_SW[0:3], poles [1:4] | All OFF | All = 0 (4.7K p/d to GND) | 24 |

Jumpers

[[Figure 1-2](#), callout 24]

Default jumper positions are listed in [Table A-2](#).

Table A-2: Default Jumper Settings

| Jumper | Function | Default Position | Selects |
|-----------|---|------------------|------------------------|
| HDR_1 X 2 | | | |
| J6 | AP SoC U1 Bank 0 CFGBVS pin V9 pull-down to GND | OPEN | Not pulled down to GND |

Table A-2: Default Jumper Settings (Cont'd)

| Jumper | Function | Default Position | Selects |
|-----------|--|------------------|-------------------------------|
| J7 | U8 Power-On Reset Device MR_B pin to GND | OPEN | MR_B pin not GND |
| J8 | JTAG Header J62 pin 2 can be connected to 3.3V | OPEN | J62.2 not conn. to 3.3V |
| J9 | U51 Ethernet PHY CONFIG2 pin 2 1K pulldown to GND Select Header | 1-2 | CONFIG2 = 0 (p/d to GND) |
| J10 | U12 USB3320 2.0 Host/OTG or Device Select Header | 1-2 | HOST sources VBUS power |
| J11 | U12 USB3320 2.0 RESET Header | OPEN | U12 not held in RESET |
| J12 | U38 REF3012 VREF XADC_AGND-to-GND L3 inductor bypass | OPEN | L3 not bypassed |
| J13 | U38 REF3012 VREF XADC_AGND-to-GND Select Header | 1-2 | XADC_GND conn. to GND |
| J14 | XADC circuit VCC5V0 sources XADC_VCC5V0 Select Header | 1-2 | XADC_VCC5V0 = filtered VCC5V0 |
| J15 | ARM PJTAG Header J64 pin 2 can be connected to VADJ | OPEN | J64.2 not conn. to VADJ |
| J17 | SPF+ P2 SFP_TX_DISABLE_TRANS Header | OPEN | SFP+ P2 TX enabled |
| J18 | FMC_VADJ_ON_B Header | 1-2 | VADJ rail enabled |
| J19 | PCIe Lane Width Select Header | 3-4 | PCIe = 4-Lanes |
| J66 | PL_PWR_ON Header | OPEN | PL power enabled |
| J69 | XADC Power System Vccint Current Sense OpAmp Gain Select Header | OPEN | Gain = 10 |
| J70 | MIO Select Header MIO2 (Note: DIP SW11 pole 1 affects this signal) | 1-2 | QSPI0_IO0 = MIO2_SELECT |
| J71 | MIO Select Header MIO3 (Note: DIP SW11 pole 2 affects this signal) | 1-2 | QSPI0_IO1 = MIO3_SELECT |
| J72 | MIO Select Header MIO4 (Note: DIP SW11 pole 3 affects this signal) | 1-2 | QSPI0_IO4 = MIO2_SELECT |
| J73 | MIO Select Header MIO5 (Note: DIP SW11 pole 4 affects this signal) | 1-2 | QSPI0_IO5 = MIO2_SELECT |
| J74 | MIO Select Header MIO6 (Note: DIP SW11 pole 5 affects this signal) | 1-2 | QSPI0_CLK = MIO6_SELECT |
| | | | |
| HDR_1 X 3 | | | |
| J43 | PS_SRST_B Select Header | 1-2 | Sourced by U8 POR MAX16025 |
| J44 | PS_POR_B Select Header | 1-2 | Sourced by U8 POR MAX16025 |

Table A-2: Default Jumper Settings (Cont'd)

| Jumper | Function | Default Position | Selects |
|--------|--|------------------|----------------------------|
| J45 | U51 Ethernet PHY CONFIG3 pin 3 1K pullup to 1.8V or 1K pulldown to GND Select Header | 1-2 | CONFIG3 = 1 (p/u to 1.8V) |
| J46 | U51 Ethernet PHY CONFIG2 pin 2 tie to 1.8V or LED0 Select Header | OPEN | J9 sets CONFIG2 condition |
| J47 | U51 Ethernet PHY CONFIG3 pin 3 LED1 or LED0 Select Header | OPEN | J44 sets CONFIG3 condition |
| J48 | U12 USB3320 2.0 MODE Select Header | 2-3 | HOST/OTG mode |
| J49 | USB 2.0 Micro-B connector J2 ID pin 4 function Select Header | 1-2 | Function = USB ID |
| J50 | USB_VBUS_SEL capacitor to GND Select Header | 2-3 | 120uF to GND |
| J51 | USB 2.0 Micro-B connector J2 ID shield pins connection Select Header | 1-2 | J2 shield pins to GND |
| J52 | XADC_VREFP source Select Header | 1-2 | XADC_VREFP = XADC_VREF |
| J53 | XADC_VCC source Select Header | 2-3 | XADC_VCC = U14 ADP123 |
| J54 | U38 REF3012 VREF Vin Select Header | 2-3 | U38 powered by XADC_VCC |
| J55 | SPF+ P2 SFP_RS1 BW Select Header | 2-3 | Low BW TX |
| J56 | SPF+ P2 SFP_RS0 BW Select Header | 2-3 | Low BW RX |

VITA 57.1 FMC Connector Pinouts

Figure B-1 shows the pinout of the FPGA mezzanine card (FMC) low pin count (LPC) connector defined by the VITA 57.1 FMC specification. For a description of how the ZC706 evaluation board implements the FMC specification, see [FPGA Mezzanine \(FMC\) Card Interface, page 65](#) and [LPC Connector J5, page 70](#).

| | <i>K</i> | <i>J</i> | <i>H</i> | <i>G</i> | <i>F</i> | <i>E</i> | <i>D</i> | <i>C</i> | <i>B</i> | <i>A</i> |
|----|----------|----------|--------------|------------|----------|----------|---------------|-----------|----------|----------|
| 1 | NC | NC | VREF_A_M2C | GND | NC | NC | PG_C2M | GND | NC | NC |
| 2 | NC | NC | PRSNTR_M2C_L | CLK1_M2C_P | NC | NC | GND | DP0_C2M_P | NC | NC |
| 3 | NC | NC | GND | CLK1_M2C_N | NC | NC | GND | DP0_C2M_N | NC | NC |
| 4 | NC | NC | CLK0_M2C_P | GND | NC | NC | GBTCLK0_M2C_P | GND | NC | NC |
| 5 | NC | NC | CLK0_M2C_N | GND | NC | NC | GBTCLK0_M2C_N | GND | NC | NC |
| 6 | NC | NC | GND | LA00_P_CC | NC | NC | GND | DP0_M2C_P | NC | NC |
| 7 | NC | NC | LA02_P | LA00_N_CC | NC | NC | GND | DP0_M2C_N | NC | NC |
| 8 | NC | NC | LA02_N | GND | NC | NC | LA01_P_CC | GND | NC | NC |
| 9 | NC | NC | GND | LA03_P | NC | NC | LA01_N_CC | GND | NC | NC |
| 10 | NC | NC | LA04_P | LA03_N | NC | NC | GND | LA06_P | NC | NC |
| 11 | NC | NC | LA04_N | GND | NC | NC | LA05_P | LA06_N | NC | NC |
| 12 | NC | NC | GND | LA08_P | NC | NC | LA05_N | GND | NC | NC |
| 13 | NC | NC | LA07_P | LA08_N | NC | NC | GND | GND | NC | NC |
| 14 | NC | NC | LA07_N | GND | NC | NC | LA09_P | LA10_P | NC | NC |
| 15 | NC | NC | GND | LA12_P | NC | NC | LA09_N | LA10_N | NC | NC |
| 16 | NC | NC | LA11_P | LA12_N | NC | NC | GND | GND | NC | NC |
| 17 | NC | NC | LA11_N | GND | NC | NC | LA13_P | GND | NC | NC |
| 18 | NC | NC | GND | LA16_P | NC | NC | LA13_N | LA14_P | NC | NC |
| 19 | NC | NC | LA15_P | LA16_N | NC | NC | GND | LA14_N | NC | NC |
| 20 | NC | NC | LA15_N | GND | NC | NC | LA17_P_CC | GND | NC | NC |
| 21 | NC | NC | GND | LA20_P | NC | NC | LA17_N_CC | GND | NC | NC |
| 22 | NC | NC | LA19_P | LA20_N | NC | NC | GND | LA18_P_CC | NC | NC |
| 23 | NC | NC | LA19_N | GND | NC | NC | LA23_P | LA18_N_CC | NC | NC |
| 24 | NC | NC | GND | LA22_P | NC | NC | LA23_N | GND | NC | NC |
| 25 | NC | NC | LA21_P | LA22_N | NC | NC | GND | GND | NC | NC |
| 26 | NC | NC | LA21_N | GND | NC | NC | LA26_P | LA27_P | NC | NC |
| 27 | NC | NC | GND | LA25_P | NC | NC | LA26_N | LA27_N | NC | NC |
| 28 | NC | NC | LA24_P | LA25_N | NC | NC | GND | GND | NC | NC |
| 29 | NC | NC | LA24_N | GND | NC | NC | TCK | GND | NC | NC |
| 30 | NC | NC | GND | LA29_P | NC | NC | TDI | SCL | NC | NC |
| 31 | NC | NC | LA28_P | LA29_N | NC | NC | TDO | SDA | NC | NC |
| 32 | NC | NC | LA28_N | GND | NC | NC | 3P3VAUX | GND | NC | NC |
| 33 | NC | NC | GND | LA31_P | NC | NC | TMS | GND | NC | NC |
| 34 | NC | NC | LA30_P | LA31_N | NC | NC | TRST_L | GA0 | NC | NC |
| 35 | NC | NC | LA30_N | GND | NC | NC | GA1 | 12P0V | NC | NC |
| 36 | NC | NC | GND | LA33_P | NC | NC | 3P3V | GND | NC | NC |
| 37 | NC | NC | LA32_P | LA33_N | NC | NC | GND | 12P0V | NC | NC |
| 38 | NC | NC | LA32_N | GND | NC | NC | 3P3V | GND | NC | NC |
| 39 | NC | NC | GND | VADJ | NC | NC | GND | 3P3V | NC | NC |
| 40 | NC | NC | VADJ | GND | NC | NC | 3P3V | GND | NC | NC |

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Figure B-1: FMC LPC Connector Pinout

Figure B-2 shows the pinout of the FPGA mezzanine card (FMC) high pin count (HPC) connector defined by the VITA 57.1 FMC specification. For a description of how the ZC706 evaluation board implements the FMC specification, see [FPGA Mezzanine \(FMC\) Card Interface, page 65](#) and [HPC Connector J37, page 65](#).

| | K | J | H | G | F | E | D | C | B | A |
|----|------------|------------|-------------|------------|-----------|-----------|---------------|-----------|---------------|-----------|
| 1 | VREF_B_M2C | GND | VREF_A_M2C | GND | PG_M2C | GND | PG_C2M | GND | RES1 | GND |
| 2 | GND | CLK3_M2C_P | PRSNT_M2C_L | CLK1_M2C_P | GND | HA01_P_CC | GND | DP0_C2M_P | GND | DP1_M2C_P |
| 3 | GND | CLK3_M2C_N | GND | CLK1_M2C_N | GND | HA01_N_CC | GND | DP0_C2M_N | GND | DP1_M2C_N |
| 4 | CLK2_M2C_P | GND | CLK0_M2C_P | GND | HA00_P_CC | GND | GBTCLK0_M2C_P | GND | DP9_M2C_P | GND |
| 5 | CLK2_M2C_N | GND | CLK0_M2C_N | GND | HA00_N_CC | GND | GBTCLK0_M2C_N | GND | DP9_M2C_N | GND |
| 6 | GND | HA03_P | GND | LA00_P_CC | GND | HA05_P | GND | DP0_M2C_P | GND | DP2_M2C_P |
| 7 | HA02_P | HA03_N | LA02_P | LA00_N_CC | HA04_P | HA05_N | GND | DP0_M2C_N | GND | DP2_M2C_N |
| 8 | HA02_N | GND | LA02_N | GND | HA04_N | GND | LA01_P_CC | GND | DP8_M2C_P | GND |
| 9 | GND | HA07_P | GND | LA03_P | GND | HA09_P | LA01_N_CC | GND | DP8_M2C_N | GND |
| 10 | HA06_P | HA07_N | LA04_P | LA03_N | HA08_P | HA09_N | GND | LA06_P | GND | DP3_M2C_P |
| 11 | HA06_N | GND | LA04_N | GND | HA08_N | GND | LA05_P | LA06_N | GND | DP3_M2C_N |
| 12 | GND | HA11_P | GND | LA08_P | GND | HA13_P | LA05_N | GND | DP7_M2C_P | GND |
| 13 | HA10_P | HA11_N | LA07_P | LA08_N | HA12_P | HA13_N | GND | GND | DP7_M2C_N | GND |
| 14 | HA10_N | GND | LA07_N | GND | HA12_N | GND | LA09_P | LA10_P | GND | DP4_M2C_P |
| 15 | GND | HA14_P | GND | LA12_P | GND | HA16_P | LA09_N | LA10_N | GND | DP4_M2C_N |
| 16 | HA17_P_CC | HA14_N | LA11_P | LA12_N | HA15_P | HA16_N | GND | GND | DP6_M2C_P | GND |
| 17 | HA17_N_CC | GND | LA11_N | GND | HA15_N | GND | LA13_P | GND | DP6_M2C_N | GND |
| 18 | GND | HA18_P | GND | LA16_P | GND | HA20_P | LA13_N | LA14_P | GND | DP5_M2C_P |
| 19 | HA21_P | HA18_N | LA15_P | LA16_N | HA19_P | HA20_N | GND | LA14_N | GND | DP5_M2C_N |
| 20 | HA21_N | GND | LA15_N | GND | HA19_N | GND | LA17_P_CC | GND | GBTCLK1_M2C_P | GND |
| 21 | GND | HA22_P | GND | LA20_P | GND | HB03_P | LA17_N_CC | GND | GBTCLK1_M2C_N | GND |
| 22 | HA23_P | HA22_N | LA19_P | LA20_N | HB02_P | HB03_N | GND | LA18_P_CC | GND | DP1_C2M_P |
| 23 | HA23_N | GND | LA19_N | GND | HB02_N | GND | LA23_P | LA18_N_CC | GND | DP1_C2M_N |
| 24 | GND | HB01_P | GND | LA22_P | GND | HB05_P | LA23_N | GND | DP9_C2M_P | GND |
| 25 | HB00_P_CC | HB01_N | LA21_P | LA22_N | HB04_P | HB05_N | GND | GND | DP9_C2M_N | GND |
| 26 | HB00_N_CC | GND | LA21_N | GND | HB04_N | GND | LA26_P | LA27_P | GND | DP2_C2M_P |
| 27 | GND | HB07_P | GND | LA25_P | GND | HB09_P | LA26_N | LA27_N | GND | DP2_C2M_N |
| 28 | HB06_P_CC | HB07_N | LA24_P | LA25_N | HB08_P | HB09_N | GND | GND | DP8_C2M_P | GND |
| 29 | HB06_N_CC | GND | LA24_N | GND | HB08_N | GND | TCK | GND | DP8_C2M_N | GND |
| 30 | GND | HB11_P | GND | LA29_P | GND | HB13_P | TDI | SCL | GND | DP3_C2M_P |
| 31 | HB10_P | HB11_N | LA28_P | LA29_N | HB12_P | HB13_N | TDO | SDA | GND | DP3_C2M_N |
| 32 | HB10_N | GND | LA28_N | GND | HB12_N | GND | 3P3VAUX | GND | DP7_C2M_P | GND |
| 33 | GND | HB15_P | GND | LA31_P | GND | HB19_P | TMS | GND | DP7_C2M_N | GND |
| 34 | HB14_P | HB15_N | LA30_P | LA31_N | HB16_P | HB19_N | TRST_L | GA0 | GND | DP4_C2M_P |
| 35 | HB14_N | GND | LA30_N | GND | HB16_N | GND | GA1 | 12P0V | GND | DP4_C2M_N |
| 36 | GND | HB18_P | GND | LA33_P | GND | HB21_P | 3P3V | GND | DP6_C2M_P | GND |
| 37 | HB17_P_CC | HB18_N | LA32_P | LA33_N | HB20_P | HB21_N | GND | 12P0V | DP6_C2M_N | GND |
| 38 | HB17_N_CC | GND | LA32_N | GND | HB20_N | GND | 3P3V | GND | GND | DP5_C2M_P |
| 39 | GND | VIO_B_M2C | GND | VADJ | GND | VADJ | GND | 3P3V | GND | DP5_C2M_N |
| 40 | VIO_B_M2C | GND | VADJ | GND | VADJ | GND | 3P3V | GND | RES0 | GND |

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Figure B-2: FMC HPC Connector Pinout

Master UCF Listing

The master user constraints file (UCF) template provides for designs targeting the ZC706 evaluation board. Net names in the constraints listed below correlate with net names on the latest ZC706 evaluation board schematic. Users must identify the appropriate pins and replace the net names with net names in the user RTL. See UG625, *Constraints Guide* for more information.

For detailed I/O standards information required for a particular interface, users can refer to the UCF files generated by tools like the Memory Interface Generator (MIG) and Base System Builder (BSB).

The FMC connectors J37 and J5 are connected to 2.5V V_{ADJ} banks. Because different FMC cards implement different circuitry, the FMC bank I/O standards must be uniquely defined by each customer.

Note: The constraints file listed in this appendix might not be the latest version. Always refer to the Virtex-7 ZC706 Evaluation Kit Product Page (www.xilinx.com/zc706) listed in [Appendix F, Additional Resources](#) for the latest FPGA pins constraints file.

ZC706 Evaluation Board UCF Listing

| | | | | | |
|-----|-----------------------|------------|----------------------------|----|--------------------------------------|
| NET | PMOD1_4_LS | LOC = Y20 | IOSTANDARD=LVCMS25; # Bank | 9 | VCCO - VADJ_FPGA - IO_L6P_T0_9 |
| NET | PMOD1_5_LS | LOC = AA20 | IOSTANDARD=LVCMS25; # Bank | 9 | VCCO - VADJ_FPGA - IO_L6N_T0_VREF_9 |
| NET | PMOD1_6_LS | LOC = AC18 | IOSTANDARD=LVCMS25; # Bank | 9 | VCCO - VADJ_FPGA - IO_L11P_T1_SRCC_9 |
| NET | PMOD1_7_LS | LOC = AC19 | IOSTANDARD=LVCMS25; # Bank | 9 | VCCO - VADJ_FPGA - IO_L11N_T1_SRCC_9 |
| NET | USER_SMA_CLOCK_P | LOC = AD18 | IOSTANDARD=LVDS_25; # Bank | 9 | VCCO - VADJ_FPGA - IO_L12P_T1_MRCC_9 |
| NET | USER_SMA_CLOCK_N | LOC = AD19 | IOSTANDARD=LVDS_25; # Bank | 9 | VCCO - VADJ_FPGA - IO_L12N_T1_MRCC_9 |
| NET | SFP_TX_DISABLE | LOC = AA18 | IOSTANDARD=LVCMS25; # Bank | 9 | VCCO - VADJ_FPGA - IO_L13P_T2_MRCC_9 |
| NET | SM_FAN_TACH | LOC = AA19 | IOSTANDARD=LVCMS25; # Bank | 9 | VCCO - VADJ_FPGA - IO_L13N_T2_MRCC_9 |
| NET | SM_FAN_PWM | LOC = AB19 | IOSTANDARD=LVCMS25; # Bank | 9 | VCCO - VADJ_FPGA - IO_L14P_T2_SRCC_9 |
| NET | PWRCTL1_FMC_PG_C2M_LS | LOC = AB20 | IOSTANDARD=LVCMS25; # Bank | 9 | VCCO - VADJ_FPGA - IO_L14N_T2_SRCC_9 |
| NET | REC_CLOCK_C_P | LOC = AD20 | IOSTANDARD=LVDS_25; # Bank | 9 | VCCO - VADJ_FPGA - IO_L19P_T3_9 |
| NET | REC_CLOCK_C_N | LOC = AE20 | IOSTANDARD=LVDS_25; # Bank | 9 | VCCO - VADJ_FPGA - IO_L19N_T3_VREF_9 |
| NET | PL_PJTAG_TDO_R | LOC = AA13 | IOSTANDARD=LVCMS25; # Bank | 10 | VCCO - VADJ_FPGA - IO_0_10 |
| NET | PL_PJTAG_TCK | LOC = AK13 | IOSTANDARD=LVCMS25; # Bank | 10 | VCCO - VADJ_FPGA - IO_L1P_T0_10 |
| NET | PL_PJTAG_TMS | LOC = AK12 | IOSTANDARD=LVCMS25; # Bank | 10 | VCCO - VADJ_FPGA - IO_L1N_T0_10 |
| NET | PL_PJTAG_TDI | LOC = AH18 | IOSTANDARD=LVCMS25; # Bank | 10 | VCCO - VADJ_FPGA - IO_L2P_T0_10 |
| NET | IIC_SDA_MAIN_LS | LOC = AJ18 | IOSTANDARD=LVCMS25; # Bank | 10 | VCCO - VADJ_FPGA - IO_L2N_T0_10 |
| NET | IIC_SCL_MAIN_LS | LOC = AJ14 | IOSTANDARD=LVCMS25; # Bank | 10 | VCCO - VADJ_FPGA - IO_L3P_T0_DQS_10 |
| NET | GPIO_DIP_SW3 | LOC = AJ13 | IOSTANDARD=LVCMS25; # Bank | 10 | VCCO - VADJ_FPGA - IO_L3N_T0_DQS_10 |
| NET | FMC_LPC_LA11_P | LOC = AJ16 | IOSTANDARD=LVCMS25; # Bank | 10 | VCCO - VADJ_FPGA - IO_L4P_T0_10 |
| NET | FMC_LPC_LA11_N | LOC = AK16 | IOSTANDARD=LVCMS25; # Bank | 10 | VCCO - VADJ_FPGA - IO_L4N_T0_10 |
| NET | FMC_LPC_LA04_P | LOC = AJ15 | IOSTANDARD=LVCMS25; # Bank | 10 | VCCO - VADJ_FPGA - IO_L5P_T0_10 |
| NET | FMC_LPC_LA04_N | LOC = AK15 | IOSTANDARD=LVCMS25; # Bank | 10 | VCCO - VADJ_FPGA - IO_L5N_T0_10 |
| NET | FMC_LPC_LA13_P | LOC = AH17 | IOSTANDARD=LVCMS25; # Bank | 10 | VCCO - VADJ_FPGA - IO_L6P_T0_10 |

| | | |
|------------------------|---|--|
| NET FMC_LPC_LA13_N | LOC = AH16 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L6N_T0_VREF_10 |
| NET FMC_LPC_LA02_P | LOC = AE12 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L7P_T1_10 |
| NET FMC_LPC_LA02_N | LOC = AF12 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L7N_T1_10 |
| NET FMC_LPC_LA09_P | LOC = AH14 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L8P_T1_10 |
| NET FMC_LPC_LA09_N | LOC = AH13 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L8N_T1_10 |
| NET FMC_LPC_LA08_P | LOC = AD14 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L9P_T1_DQS_10 |
| NET FMC_LPC_LA08_N | LOC = AD13 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L9N_T1_DQS_10 |
| NET FMC_LPC_LA03_P | LOC = AG12 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L10P_T1_10 |
| NET FMC_LPC_LA03_N | LOC = AH12 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L10N_T1_10 |
| NET FMC_LPC_LA00_CC_P | LOC = AE13 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L11P_T1_SRCC_10 |
| NET FMC_LPC_LA00_CC_N | LOC = AF13 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L11N_T1_SRCC_10 |
| NET USRCLK_P | LOC = AF14 IOSTANDARD=LVDS_25; # Bank | 10 VCCO - VADJ_FPGA - IO_L12P_T1_MRCC_10 |
| NET USRCLK_N | LOC = AG14 IOSTANDARD=LVDS_25; # Bank | 10 VCCO - VADJ_FPGA - IO_L12N_T1_MRCC_10 |
| NET FMC_LPC_CLK0_M2C_P | LOC = AG17 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L13P_T2_MRCC_10 |
| NET FMC_LPC_CLK0_M2C_N | LOC = AG16 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L13N_T2_MRCC_10 |
| NET FMC_LPC_LA01_CC_P | LOC = AF15 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L14P_T2_SRCC_10 |
| NET FMC_LPC_LA01_CC_N | LOC = AG15 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L14N_T2_SRCC_10 |
| NET FMC_LPC_LA14_P | LOC = AF18 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L15P_T2_DQS_10 |
| NET FMC_LPC_LA14_N | LOC = AF17 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L15N_T2_DQS_10 |
| NET FMC_LPC_LA05_P | LOC = AE16 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L16P_T2_10 |
| NET FMC_LPC_LA05_N | LOC = AE15 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L16N_T2_10 |
| NET FMC_LPC_LA16_P | LOC = AE18 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L17P_T2_10 |
| NET FMC_LPC_LA16_N | LOC = AE17 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L17N_T2_10 |
| NET FMC_LPC_LA12_P | LOC = AD16 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L18P_T2_10 |
| NET FMC_LPC_LA12_N | LOC = AD15 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L18N_T2_10 |
| NET FMC_LPC_LA10_P | LOC = AC14 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L19P_T3_10 |
| NET FMC_LPC_LA10_N | LOC = AC13 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L19N_T3_VREF_10 |
| NET FMC_LPC_LA07_P | LOC = AA15 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L20P_T3_10 |
| NET FMC_LPC_LA07_N | LOC = AA14 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L20N_T3_10 |
| NET FMC_LPC_LA06_P | LOC = AB12 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L21P_T3_DQS_10 |
| NET FMC_LPC_LA06_N | LOC = AC12 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L21N_T3_DQS_10 |
| NET FMC_LPC_LA15_P | LOC = AB15 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L22P_T3_10 |
| NET FMC_LPC_LA15_N | LOC = AB14 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L22N_T3_10 |
| NET GPIO_DIP_SW2 | LOC = AC17 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L23P_T3_10 |
| NET GPIO_DIP_SW1 | LOC = AC16 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L23N_T3_10 |
| NET GPIO_DIP_SW0 | LOC = AB17 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L24P_T3_10 |
| NET PMOD1_3_LS | LOC = AB16 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_L24N_T3_10 |
| NET IIC_RTC_IRQ_1_B | LOC = AA17 IOSTANDARD=LVCMS25; # Bank | 10 VCCO - VADJ_FPGA - IO_25_10 |
| NET SI5324_RST_LS | LOC = W23 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_0_11 |
| NET SI5324_INT_ALM_LS | LOC = AJ25 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L1P_T0_11 |
| NET GPIO_SW_LEFT | LOC = AK25 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L1N_T0_11 |
| NET PCIE_WAKE_B_LS | LOC = AK22 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L2P_T0_11 |
| NET PCIE_PERST_LS | LOC = AK23 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L2N_T0_11 |
| NET PMOD1_0_LS | LOC = AJ21 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L3P_T0_DQS_11 |
| NET PMOD1_1_LS | LOC = AK21 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L3N_T0_DQS_11 |
| NET FMC_HPC_LA07_P | LOC = AJ23 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L4P_T0_11 |
| NET FMC_HPC_LA07_N | LOC = AJ24 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L4N_T0_11 |
| NET FMC_HPC_LA05_P | LOC = AH23 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L5P_T0_11 |
| NET FMC_HPC_LA05_N | LOC = AH24 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L5N_T0_11 |
| NET FMC_HPC_LA06_P | LOC = AG22 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L6P_T0_11 |
| NET FMC_HPC_LA06_N | LOC = AH22 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L6N_T0_VREF_11 |
| NET FMC_HPC_LA14_P | LOC = AC24 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L7P_T1_11 |
| NET FMC_HPC_LA14_N | LOC = AD24 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L7N_T1_11 |
| NET FMC_HPC_LA10_P | LOC = AG24 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L8P_T1_11 |
| NET FMC_HPC_LA10_N | LOC = AG25 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L8N_T1_11 |
| NET FMC_HPC_LA12_P | LOC = AF23 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L9P_T1_DQS_11 |
| NET FMC_HPC_LA12_N | LOC = AF24 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L9N_T1_DQS_11 |
| NET FMC_HPC_LA09_P | LOC = AD21 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L10P_T1_11 |
| NET FMC_HPC_LA09_N | LOC = AE21 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L10N_T1_11 |
| NET FMC_HPC_LA11_P | LOC = AD23 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L11P_T1_SRCC_11 |
| NET FMC_HPC_LA11_N | LOC = AE23 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L11N_T1_SRCC_11 |
| NET FMC_HPC_CLK0_M2C_P | LOC = AE22 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L12P_T1_MRCC_11 |
| NET FMC_HPC_CLK0_M2C_N | LOC = AF22 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L12N_T1_MRCC_11 |
| NET FMC_HPC_LA01_CC_P | LOC = AG21 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L13P_T2_MRCC_11 |
| NET FMC_HPC_LA01_CC_N | LOC = AH21 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L13N_T2_MRCC_11 |
| NET FMC_HPC_LA00_CC_P | LOC = AF20 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L14P_T2_SRCC_11 |
| NET FMC_HPC_LA00_CC_N | LOC = AG20 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L14N_T2_SRCC_11 |
| NET FMC_HPC_LA04_P | LOC = AJ20 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L15P_T2_DQS_11 |

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| NET FMC_HPC_LA04_N | LOC = AK20 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L15N_T2_DQS_11 |
| NET FMC_HPC_LA02_P | LOC = AK17 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L16P_T2_11 |
| NET FMC_HPC_LA02_N | LOC = AK18 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L16N_T2_11 |
| NET FMC_HPC_LA03_P | LOC = AH19 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L17P_T2_11 |
| NET FMC_HPC_LA03_N | LOC = AJ19 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L17N_T2_11 |
| NET FMC_HPC_LA08_P | LOC = AF19 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L18P_T2_11 |
| NET FMC_HPC_LA08_N | LOC = AG19 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L18N_T2_11 |
| NET PMOD1_2_LS | LOC = AB21 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L19P_T3_11 |
| NET HDMI_SPDIF_OUT_LS | LOC = AB22 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L19N_T3_VREF_11 |
| NET GPIO_LED_RIGHT | LOC = W21 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L20P_T3_11 |
| NET GPIO_LED_LEFT | LOC = Y21 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L20N_T3_11 |
| NET FMC_HPC_LA15_P | LOC = Y22 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L21P_T3_DQS_11 |
| NET FMC_HPC_LA15_N | LOC = Y23 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L21N_T3_DQS_11 |
| NET FMC_HPC_LA16_P | LOC = AA24 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L22P_T3_11 |
| NET FMC_HPC_LA16_N | LOC = AB24 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L22N_T3_11 |
| NET FMC_HPC_LA13_P | LOC = AA22 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L23P_T3_11 |
| NET FMC_HPC_LA13_N | LOC = AA23 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L23N_T3_11 |
| NET HDMI_R_D35 | LOC = AC22 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L24P_T3_11 |
| NET HDMI_INT | LOC = AC23 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_L24N_T3_11 |
| NET HDMI_R_SPDIF | LOC = AC21 IOSTANDARD=LVCMS25; # Bank | 11 VCCO - VADJ_FPGA - IO_25_11 |
| NET HDMI_R_D21 | LOC = Y25 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_0_12 |
| NET FMC_LPC_LA33_P | LOC = Y30 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L1P_T0_12 |
| NET FMC_LPC_LA33_N | LOC = AA30 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L1N_T0_12 |
| NET FMC_LPC_LA30_P | LOC = AB29 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L2P_T0_12 |
| NET FMC_LPC_LA30_N | LOC = AB30 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L2N_T0_12 |
| NET FMC_LPC_LA32_P | LOC = Y26 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L3P_T0_DQS_12 |
| NET FMC_LPC_LA32_N | LOC = Y27 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L3N_T0_DQS_12 |
| NET HDMI_R_D28 | LOC = Y28 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L4P_T0_12 |
| NET HDMI_R_D22 | LOC = AA29 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L4N_T0_12 |
| NET HDMI_R_D31 | LOC = AA27 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L5P_T0_12 |
| NET HDMI_R_D18 | LOC = AA28 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L5N_T0_12 |
| NET HDMI_R_D10 | LOC = AB25 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L6P_T0_12 |
| NET HDMI_R_D17 | LOC = AB26 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L6N_T0_VREF_12 |
| NET HDMI_R_D19 | LOC = AC26 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L7P_T1_12 |
| NET HDMI_R_D16 | LOC = AD26 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L7N_T1_12 |
| NET HDMI_R_D23 | LOC = AD30 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L8P_T1_12 |
| NET HDMI_R_D20 | LOC = AE30 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L8N_T1_12 |
| NET FMC_LPC_LA31_P | LOC = AC29 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L9P_T1_DQS_12 |
| NET FMC_LPC_LA31_N | LOC = AD29 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L9N_T1_DQS_12 |
| NET FMC_LPC_LA28_P | LOC = AD25 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L10P_T1_12 |
| NET FMC_LPC_LA28_N | LOC = AE26 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L10N_T1_12 |
| NET FMC_LPC_LA17_CC_P | LOC = AB27 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L11P_T1_SRCC_12 |
| NET FMC_LPC_LA17_CC_N | LOC = AC27 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L11N_T1_SRCC_12 |
| NET FMC_LPC_CLK1_M2C_P | LOC = AC28 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L12P_T1_MRCC_12 |
| NET FMC_LPC_CLK1_M2C_N | LOC = AD28 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L12N_T1_MRCC_12 |
| NET HDMI_R_D8 | LOC = AE28 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L13P_T2_MRCC_12 |
| NET HDMI_R_D29 | LOC = AF28 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L13N_T2_MRCC_12 |
| NET FMC_LPC_LA18_CC_P | LOC = AE27 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L14P_T2_SRCC_12 |
| NET FMC_LPC_LA18_CC_N | LOC = AF27 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L14N_T2_SRCC_12 |
| NET FMC_LPC_LA25_P | LOC = AF29 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L15P_T2_DQS_12 |
| NET FMC_LPC_LA25_N | LOC = AG29 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L15N_T2_DQS_12 |
| NET FMC_LPC_LA24_P | LOC = AF30 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L16P_T2_12 |
| NET FMC_LPC_LA24_N | LOC = AG30 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L16N_T2_12 |
| NET FMC_LPC_LA20_P | LOC = AG26 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L17P_T2_12 |
| NET FMC_LPC_LA20_N | LOC = AG27 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L17N_T2_12 |
| NET FMC_LPC_LA29_P | LOC = AE25 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L18P_T2_12 |
| NET FMC_LPC_LA29_N | LOC = AF25 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L18N_T2_12 |
| NET FMC_LPC_LA21_P | LOC = AH28 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L19P_T3_12 |
| NET FMC_LPC_LA21_N | LOC = AH29 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L19N_T3_VREF_12 |
| NET FMC_LPC_LA26_P | LOC = AJ30 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L20P_T3_12 |
| NET FMC_LPC_LA26_N | LOC = AK30 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L20N_T3_12 |
| NET FMC_LPC_LA27_P | LOC = AJ28 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L21P_T3_DQS_12 |
| NET FMC_LPC_LA27_N | LOC = AJ29 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L21N_T3_DQS_12 |
| NET FMC_LPC_LA22_P | LOC = AK27 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L22P_T3_12 |
| NET FMC_LPC_LA22_N | LOC = AK28 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L22N_T3_12 |
| NET FMC_LPC_LA19_P | LOC = AH26 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L23P_T3_12 |
| NET FMC_LPC_LA19_N | LOC = AH27 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L23N_T3_12 |
| NET FMC_LPC_LA23_P | LOC = AJ26 IOSTANDARD=LVCMS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L24P_T3_12 |

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| NET FMC_LPC_LA23_N | LOC = AK26 | IOSTANDARD=LVCMOS25; # Bank | 12 VCCO - VADJ_FPGA - IO_L24N_T3_12 |
| NET HDMI_R_D7 | LOC = AA25 | IOSTANDARD=LVCMOS25; # Bank | 12 VCCO - VADJ_FPGA - IO_25_12 |
| NET HDMI_R_VSYNC | LOC = U21 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_0_13 |
| NET FMC_HPC_LA28_P | LOC = P30 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L1P_T0_13 |
| NET FMC_HPC_LA28_N | LOC = R30 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L1N_T0_13 |
| NET FMC_HPC_LA24_P | LOC = T30 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L2P_T0_13 |
| NET FMC_HPC_LA24_N | LOC = U30 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L2N_T0_13 |
| NET HDMI_R_D33 | LOC = N28 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L3P_T0_DQS_13 |
| NET HDMI_R_CLK | LOC = P28 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L3N_T0_DQS_13 |
| NET FMC_HPC_LA31_P | LOC = N29 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L4P_T0_13 |
| NET FMC_HPC_LA31_N | LOC = P29 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L4N_T0_13 |
| NET FMC_HPC_LA25_P | LOC = T29 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L5P_T0_13 |
| NET FMC_HPC_LA25_N | LOC = U29 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L5N_T0_13 |
| NET FMC_HPC_LA26_P | LOC = R28 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L6P_T0_13 |
| NET FMC_HPC_LA26_N | LOC = T28 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L6N_T0_VREF_13 |
| NET FMC_HPC_LA27_P | LOC = V28 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L7P_T1_13 |
| NET FMC_HPC_LA27_N | LOC = V29 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L7N_T1_13 |
| NET FMC_HPC_LA21_P | LOC = W29 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L8P_T1_13 |
| NET FMC_HPC_LA21_N | LOC = W30 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L8N_T1_13 |
| NET FMC_HPC_LA22_P | LOC = V27 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L9P_T1_DQS_13 |
| NET FMC_HPC_LA22_N | LOC = W28 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L9N_T1_DQS_13 |
| NET FMC_HPC_LA18_CC_P | LOC = W25 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L10P_T1_13 |
| NET FMC_HPC_LA18_CC_N | LOC = W26 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L10N_T1_13 |
| NET FMC_HPC_LA20_P | LOC = U25 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L11P_T1_SRCC_13 |
| NET FMC_HPC_LA20_N | LOC = V26 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L11N_T1_SRCC_13 |
| NET FMC_HPC_CLK1_M2C_P | LOC = U26 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L12P_T1_MRCC_13 |
| NET FMC_HPC_CLK1_M2C_N | LOC = U27 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L12N_T1_MRCC_13 |
| NET FMC_HPC_LA29_P | LOC = R25 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L13P_T2_MRCC_13 |
| NET FMC_HPC_LA29_N | LOC = R26 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L13N_T2_MRCC_13 |
| NET GPIO_SW_RIGHT | LOC = R27 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L14P_T2_SRCC_13 |
| NET HDMI_R_D11 | LOC = T27 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L14N_T2_SRCC_13 |
| NET FMC_HPC_LA33_P | LOC = N26 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L15P_T2_DQS_13 |
| NET FMC_HPC_LA33_N | LOC = N27 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L15N_T2_DQS_13 |
| NET FMC_HPC_LA23_P | LOC = P25 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L16P_T2_13 |
| NET FMC_HPC_LA23_N | LOC = P26 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L16N_T2_13 |
| NET FMC_HPC_LA19_P | LOC = T24 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L17P_T2_13 |
| NET FMC_HPC_LA19_N | LOC = T25 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L17N_T2_13 |
| NET FMC_HPC_LA30_P | LOC = P23 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L18P_T2_13 |
| NET FMC_HPC_LA30_N | LOC = P24 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L18N_T2_13 |
| NET FMC_HPC_LA32_P | LOC = P21 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L19P_T3_13 |
| NET FMC_HPC_LA32_N | LOC = R21 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L19N_T3_VREF_13 |
| NET HDMI_R_D5 | LOC = T22 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L20P_T3_13 |
| NET HDMI_R_D9 | LOC = T23 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L20N_T3_13 |
| NET HDMI_R_HSYNC | LOC = R22 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L21P_T3_DQS_13 |
| NET HDMI_R_D6 | LOC = R23 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L21N_T3_DQS_13 |
| NET HDMI_R_D32 | LOC = U22 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L22P_T3_13 |
| NET HDMI_R_D30 | LOC = V22 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L22N_T3_13 |
| NET HDMI_R_D4 | LOC = U24 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L23P_T3_13 |
| NET HDMI_R_DE | LOC = V24 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L23N_T3_13 |
| NET FMC_HPC_LA17_CC_P | LOC = V23 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L24P_T3_13 |
| NET FMC_HPC_LA17_CC_N | LOC = W24 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_L24N_T3_13 |
| NET HDMI_R_D34 | LOC = V21 | IOSTANDARD=LVCMOS25; # Bank | 13 VCCO - VADJ_FPGA - IO_25_13 |
| #NET VRN_33 | LOC = L5 | IOSTANDARD=SSTL15; # Bank | 33 VCCO - VCC1V5_PL - IO_0_VRN_33 |
| NET PL_DDR3_D3 | LOC = J4 | IOSTANDARD=SSTL15; # Bank | 33 VCCO - VCC1V5_PL - IO_L1P_T0_33 |
| NET PL_DDR3_DMO | LOC = J3 | IOSTANDARD=SSTL15; # Bank | 33 VCCO - VCC1V5_PL - IO_L1N_T0_33 |
| NET PL_DDR3_D0 | LOC = L1 | IOSTANDARD=SSTL15; # Bank | 33 VCCO - VCC1V5_PL - IO_L2P_T0_33 |
| NET PL_DDR3_D4 | LOC = K1 | IOSTANDARD=SSTL15; # Bank | 33 VCCO - VCC1V5_PL - IO_L2N_T0_33 |
| NET PL_DDR3_DQSO_P | LOC = K3 | IOSTANDARD=DIFF_SSTL15; # Bank | 33 VCCO - VCC1V5_PL - IO_L3P_T0_DQS_33 |
| NET PL_DDR3_DQSO_N | LOC = K2 | IOSTANDARD=DIFF_SSTL15; # Bank | 33 VCCO - VCC1V5_PL - IO_L3N_T0_DQS_33 |
| NET PL_DDR3_D5 | LOC = L3 | IOSTANDARD=SSTL15; # Bank | 33 VCCO - VCC1V5_PL - IO_L4P_T0_33 |
| NET PL_DDR3_D1 | LOC = L2 | IOSTANDARD=SSTL15; # Bank | 33 VCCO - VCC1V5_PL - IO_L4N_T0_33 |
| NET PL_DDR3_D2 | LOC = K5 | IOSTANDARD=SSTL15; # Bank | 33 VCCO - VCC1V5_PL - IO_L5P_T0_33 |
| NET PL_DDR3_D6 | LOC = J5 | IOSTANDARD=SSTL15; # Bank | 33 VCCO - VCC1V5_PL - IO_L5N_T0_33 |
| NET PL_DDR3_D7 | LOC = K6 | IOSTANDARD=SSTL15; # Bank | 33 VCCO - VCC1V5_PL - IO_L6P_T0_33 |
| #NET VTTVREF_SODIMM | LOC = J6 | IOSTANDARD=SSTL15; # Bank | 33 VCCO - VCC1V5_PL - IO_L6N_T0_VREF_33 |
| NET GPIO_LED_CENTER | LOC = G2 | IOSTANDARD=LVCMOS15; # Bank | 33 VCCO - VCC1V5_PL - IO_L7P_T1_33 |
| NET PL_DDR3_DM1 | LOC = F2 | IOSTANDARD=SSTL15; # Bank | 33 VCCO - VCC1V5_PL - IO_L7N_T1_33 |
| NET PL_DDR3_D10 | LOC = H6 | IOSTANDARD=SSTL15; # Bank | 33 VCCO - VCC1V5_PL - IO_L8P_T1_33 |

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NET PL_DDR3_D8          LOC = G6 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L8N_T1_33
NET PL_DDR3_DQS1_P       LOC = J1 | IOSTANDARD=DIFF_SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L9P_T1_DQS_33
NET PL_DDR3_DQS1_N       LOC = H1 | IOSTANDARD=DIFF_SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L9N_T1_DQS_33
NET PL_DDR3_D13          LOC = H2 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L10P_T1_33
NET PL_DDR3_D12          LOC = G1 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L10N_T1_33
NET PL_DDR3_D9           LOC = H4 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L11P_T1_SRCC_33
NET PL_DDR3_D11          LOC = H3 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L11N_T1_SRCC_33
NET PL_DDR3_D14          LOC = G5 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L12P_T1_MRCC_33
NET PL_DDR3_D15          LOC = G4 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L12N_T1_MRCC_33
NET PL_DDR3_D19          LOC = E5 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L13N_T2_MRCC_33
NET PL_DDR3_D20          LOC = F4 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L14P_T2_SRCC_33
NET PL_DDR3_D21          LOC = F3 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L14N_T2_SRCC_33
NET PL_DDR3_DQS2_P       LOC = E6 | IOSTANDARD=DIFF_SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L15P_T2_DQS_33
NET PL_DDR3_DQS2_N       LOC = D5 | IOSTANDARD=DIFF_SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L15N_T2_DQS_33
NET PL_DDR3_D18          LOC = D4 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L16P_T2_33
NET PL_DDR3_D23          LOC = D3 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L16N_T2_33
NET PL_DDR3_D17          LOC = E3 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L17P_T2_33
NET PL_DDR3_D16          LOC = E2 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L17N_T2_33
NET PL_DDR3_DM2          LOC = E1 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L18P_T2_33
NET PL_DDR3_D22          LOC = D1 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L18N_T2_33
NET PL_DDR3_D31          LOC = C4 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L19P_T3_33
#NET VTTVREF_SODIMM      LOC = C3 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L19N_T3_VREF_33
NET PL_DDR3_D27          LOC = B5 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L20P_T3_33
NET PL_DDR3_D26          LOC = B4 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L20N_T3_33
NET PL_DDR3_DQS3_P       LOC = A5 | IOSTANDARD=DIFF_SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L21P_T3_DQS_33
NET PL_DDR3_DQS3_N       LOC = A4 | IOSTANDARD=DIFF_SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L21N_T3_DQS_33
NET PL_DDR3_DM3          LOC = C2 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L22P_T3_33
NET PL_DDR3_D30          LOC = C1 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L22N_T3_33
NET PL_DDR3_D25          LOC = B2 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L23P_T3_33
NET PL_DDR3_D29          LOC = B1 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L23N_T3_33
NET PL_DDR3_D28          LOC = A3 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L24P_T3_33
NET PL_DDR3_D24          LOC = A2 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_L24N_T3_33
#NET VRP_33              LOC = L4 | IOSTANDARD=SSTL15; # Bank 33 VCCO - VCC1V5_PL - IO_25_VRP_33
NET PL_DDR3_A8           LOC = B10 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L1P_T0_34
NET PL_DDR3_A13          LOC = A10 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L1N_T0_34
NET PL_DDR3_A1           LOC = B9 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L2P_T0_34
NET PL_DDR3_A3           LOC = A9 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L2N_T0_34
NET PL_CPU_RESET         LOC = A8 | IOSTANDARD=LVCMOS15; # Bank 34 VCCO - VCC1V5_PL - IO_L3P_T0_DQS_PUDC_B_34
NET PL_DDR3_BA2          LOC = A7 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L3N_T0_DQS_34
NET PL_DDR3_CKE1         LOC = C7 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L4P_T0_34
NET PL_DDR3_A11          LOC = B7 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L4N_T0_34
NET PL_DDR3_A15          LOC = C6 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L5P_T0_34
NET PL_DDR3_A5           LOC = B6 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L5N_T0_34
NET PL_DDR3_ODT1         LOC = C9 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L6P_T0_34
#NET VTTVREF_SODIMM      LOC = C8 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L6N_T0_VREF_34
NET PL_DDR3_S0_B          LOC = J11 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L7P_T1_34
NET PL_DDR3_RAS_B         LOC = H11 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L7N_T1_34
NET PL_DDR3_A2           LOC = E11 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L8P_T1_34
NET PL_DDR3_A4           LOC = D11 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L8N_T1_34
NET PL_DDR3_A12          LOC = H12 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L9P_T1_DQS_34
NET PL_DDR3_A14          LOC = G11 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L9N_T1_DQS_34
NET PL_DDR3_A0           LOC = E10 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L10P_T1_34
NET PL_DDR3_CKE0         LOC = D10 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L10N_T1_34
NET PL_DDR3_CLK0_P        LOC = G10 | IOSTANDARD=DIFF_SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L11P_T1_SRCC_34
NET PL_DDR3_CLK0_N        LOC = F10 | IOSTANDARD=DIFF_SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L11N_T1_SRCC_34
NET PL_DDR3_CLK1_P        LOC = D9 | IOSTANDARD=DIFF_SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L12P_T1_MRCC_34
NET PL_DDR3_CLK1_N        LOC = D8 | IOSTANDARD=DIFF_SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L12N_T1_MRCC_34
NET SYSCLK_P              LOC = H9 | IOSTANDARD=LVDS; # Bank 34 VCCO - VCC1V5_PL - IO_L13P_T2_MRCC_34
NET SYSCLK_N              LOC = G9 | IOSTANDARD=LVDS; # Bank 34 VCCO - VCC1V5_PL - IO_L13N_T2_MRCC_34
NET PL_DDR3_A6             LOC = F9 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L14P_T2_SRCC_34
NET PL_DDR3_A7             LOC = E8 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L14N_T2_SRCC_34
NET PL_DDR3_A9             LOC = J8 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L15P_T2_DQS_34
NET PL_DDR3_S1_B            LOC = H8 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L15N_T2_DQS_34
NET PL_DDR3_BA0            LOC = F8 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L16P_T2_34
NET PL_DDR3_WE_B           LOC = F7 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L16N_T2_34
NET PL_DDR3_CAS_B           LOC = E7 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L17P_T2_34
NET PL_DDR3_A10            LOC = D6 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L17N_T2_34
NET PL_DDR3_BA1            LOC = H7 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L18P_T2_34

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NET PL_DDR3_ODT0 | LOC = G7 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L18N_T2_34
NET PL_DDR3_D39 | LOC = L7 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L19P_T3_34
#NET VTTVREF_SODIMM | LOC = K7 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L19N_T3_VREF_34
NET PL_DDR3_D38 | LOC = J10 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L20P_T3_34
NET PL_DDR3_D35 | LOC = J9 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L20N_T3_34
NET PL_DDR3_DQS4_P | LOC = L8 | IOSTANDARD=DIFF_SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L21P_T3_DQS_34
NET PL_DDR3_DQS4_N | LOC = K8 | IOSTANDARD=DIFF_SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L21N_T3_DQS_34
NET PL_DDR3_D36 | LOC = K11 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L22P_T3_34
NET PL_DDR3_D32 | LOC = K10 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L22N_T3_34
NET PL_DDR3_D37 | LOC = L10 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L23P_T3_34
NET PL_DDR3_D33 | LOC = L9 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L23N_T3_34
NET PL_DDR3_DM4 | LOC = L12 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L24P_T3_34
NET PL_DDR3_D34 | LOC = K12 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_L24N_T3_34
NET PL_DDR3_TEMP_EVENT | LOC = M10 | IOSTANDARD=SSTL15; # Bank 34 VCCO - VCC1V5_PL - IO_25_VRP_34
#NET VRN_35 | LOC = K16 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_0_VRN_35
NET XADC_VAUX0P_R | LOC = L15 | IOSTANDARD=LVCMOS5; # Bank 35 VCCO - VCC1V5_PL - IO_L1P_T0_AD0P_35
NET XADC_VAUX0N_R | LOC = L14 | IOSTANDARD=LVCMOS15; # Bank 35 VCCO - VCC1V5_PL - IO_L1N_T0_AD0N_35
NET XADC_VAUX8P_R | LOC = J13 | IOSTANDARD=LVCMOS15; # Bank 35 VCCO - VCC1V5_PL - IO_L2P_T0_AD8P_35
NET XADC_VAUX8N_R | LOC = H13 | IOSTANDARD=LVCMOS15; # Bank 35 VCCO - VCC1V5_PL - IO_L2N_T0_AD8N_35
NET XADC_AD1_R_P | LOC = L13 | IOSTANDARD=LVCMOS15; # Bank 35 VCCO - VCC1V5_PL - IO_L3P_T0_DQS_AD1P_35
NET XADC_AD1_R_N | LOC = K13 | IOSTANDARD=LVCMOS15; # Bank 35 VCCO - VCC1V5_PL - IO_L3N_T0_DQS_AD1N_35
NET XADC_GPIO_3 | LOC = J14 | IOSTANDARD=LVCMOS15; # Bank 35 VCCO - VCC1V5_PL - IO_L4P_T0_35
NET XADC_GPIO_0 | LOC = H14 | IOSTANDARD=LVCMOS15; # Bank 35 VCCO - VCC1V5_PL - IO_L4N_T0_35
NET GPIO_SW_CENTER | LOC = K15 | IOSTANDARD=LVCMOS15; # Bank 35 VCCO - VCC1V5_PL - IO_L5P_T0_AD9P_35
NET XADC_GPIO_1 | LOC = J15 | IOSTANDARD=LVCMOS15; # Bank 35 VCCO - VCC1V5_PL - IO_L5N_T0_AD9N_35
NET XADC_GPIO_2 | LOC = J16 | IOSTANDARD=LVCMOS15; # Bank 35 VCCO - VCC1V5_PL - IO_L6P_T0_35
#NET VTTVREF_SODIMM | LOC = H16 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L6N_T0_VREF_35
NET PL_DDR3_RESET_B | LOC = G17 | IOSTANDARD=LVCMOS15; # Bank 35 VCCO - VCC1V5_PL - IO_L7P_T1_AD2P_35
NET PL_DDR3_D43 | LOC = G16 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L7N_T1_AD2N_35
NET PL_DDR3_D44 | LOC = G15 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L8P_T1_AD10P_35
NET PL_DDR3_D55 | LOC = G14 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L8N_T1_AD10N_35
NET PL_DDR3_DQS5_P | LOC = G12 | IOSTANDARD=DIFF_SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L9P_T1_DQS_AD3P_35
NET PL_DDR3_DQS5_N | LOC = F12 | IOSTANDARD=DIFF_SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L9N_T1_DQS_AD3N_35
NET PL_DDR3_D42 | LOC = F13 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L10P_T1_AD11P_35
NET PL_DDR3_D45 | LOC = E12 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L10N_T1_AD11N_35
NET PL_DDR3_D47 | LOC = E13 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L11P_T1_SRCC_35
NET PL_DDR3_D46 | LOC = D13 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L11N_T1_SRCC_35
NET PL_DDR3_D41 | LOC = F15 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L12P_T1_MRCC_35
NET PL_DDR3_D40 | LOC = F14 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L12N_T1_MRCC_35
NET PL_DDR3_D51 | LOC = E16 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L13P_T2_MRCC_35
NET PL_DDR3_D49 | LOC = E15 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L13N_T2_MRCC_35
NET PL_DDR3_D48 | LOC = D15 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L14P_T2_AD4P_SRCC_35
NET PL_DDR3_D54 | LOC = D14 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L14N_T2_AD4N_SRCC_35
NET PL_DDR3_DQS6_P | LOC = F17 | IOSTANDARD=DIFF_SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L15P_T2_DQS_AD12P_35
NET PL_DDR3_DQS6_N | LOC = E17 | IOSTANDARD=DIFF_SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L15N_T2_DQS_AD12N_35
NET PL_DDR3_D50 | LOC = D16 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L16P_T2_35
NET PL_DDR3_DM6 | LOC = C16 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L16N_T2_35
NET PL_DDR3_D52 | LOC = C17 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L17P_T2_AD5P_35
NET PL_DDR3_D53 | LOC = B16 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L17N_T2_AD5N_35
NET PL_DDR3_D55 | LOC = B17 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L18P_T2_AD13P_35
NET GPIO_LED_0 | LOC = A17 | IOSTANDARD=LVCMOS15; # Bank 35 VCCO - VCC1V5_PL - IO_L18N_T2_AD13N_35
NET PL_DDR3_D62 | LOC = C14 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L19P_T3_35
NET PL_DDR3_D57 | LOC = C13 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L19N_T3_VREF_35
NET PL_DDR3_D56 | LOC = C12 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L20P_T3_AD6P_35
NET PL_DDR3_D58 | LOC = B12 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L20N_T3_AD6N_35
NET PL_DDR3_DQS7_P | LOC = B15 | IOSTANDARD=DIFF_SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L21P_T3_DQS_AD14P_35
NET PL_DDR3_DQS7_N | LOC = A15 | IOSTANDARD=DIFF_SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L21N_T3_DQS_AD14N_35
NET PL_DDR3_DM7 | LOC = C11 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L22P_T3_AD7P_35
NET PL_DDR3_D61 | LOC = B11 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L22N_T3_AD7N_35
NET PL_DDR3_D63 | LOC = B14 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L23P_T3_35
NET PL_DDR3_D59 | LOC = A14 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L23N_T3_35
NET PL_DDR3_D60 | LOC = A13 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L24P_T3_AD15P_35
NET PL_DDR3_D58 | LOC = A12 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_L24N_T3_AD15N_35
#NET VRP_35 | LOC = M16 | IOSTANDARD=SSTL15; # Bank 35 VCCO - VCC1V5_PL - IO_25_VRP_35
NET FMC_HPC_DP3_C2M_P | LOC = AK2 | ; # Bank 109 - MGTXTP3_109
NET FMC_HPC_DP3_M2C_P | LOC = AE8 | ; # Bank 109 - MGTXRP3_109
NET FMC_HPC_DP3_C2M_N | LOC = AK1 | ; # Bank 109 - MGTXTN3_109
NET FMC_HPC_DP3_M2C_N | LOC = AE7 | ; # Bank 109 - MGTXRN3_109
NET FMC_HPC_DP2_C2M_P | LOC = AJ4 | ; # Bank 109 - MGTXTP2_109

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NET  FMC_HPC_DP2_M2C_P      LOC = AG8          ; # Bank 109      - MGTXRXP2_109
NET  FMC_HPC_DP2_C2M_N      LOC = AJ3          ; # Bank 109      - MGTXTXN2_109
NET  FMC_HPC_GBTCLK0_M2C_C_P LOC = AD10         ; # Bank 109      - MGTREFCLK0P_109
NET  FMC_HPC_DP2_M2C_N      LOC = AG7          ; # Bank 109      - MGTXRXN2_109
NET  FMC_HPC_GBTCLK0_M2C_C_N LOC = AD9          ; # Bank 109      - MGTREFCLK0N_109
NET  FMC_HPC_DP1_C2M_P      LOC = AK6          ; # Bank 109      - MGTXTXP1_109
NET  FMC_HPC_DP1_M2C_P      LOC = AJ8          ; # Bank 109      - MGTXRXP1_109
NET  FMC_HPC_DP1_C2M_N      LOC = AK5          ; # Bank 109      - MGTXTXN1_109
NET  FMC_HPC_DP1_M2C_N      LOC = AJ7          ; # Bank 109      - MGTXRXN1_109
NET  FMC_HPC_DP0_C2M_P      LOC = AK10         ; # Bank 109      - MGTXTXP0_109
NET  FMC_HPC_DP0_M2C_P      LOC = AH10         ; # Bank 109      - MGTXRXP0_109
NET  FMC_HPC_DP0_C2M_N      LOC = AK9          ; # Bank 109      - MGTXTXN0_109
NET  FMC_HPC_DP0_M2C_N      LOC = AH9          ; # Bank 109      - MGTXRXN0_109
NET  FMC_HPC_DP7_C2M_P      LOC = AD2          ; # Bank 110      - MGTXTXP3_110
NET  FMC_HPC_DP7_M2C_P      LOC = AD6          ; # Bank 110      - MGTXRXP3_110
NET  FMC_HPC_DP7_C2M_N      LOC = AD1          ; # Bank 110      - MGTXTXN3_110
NET  FMC_HPC_DP7_M2C_N      LOC = AD5          ; # Bank 110      - MGTXRXN3_110
NET  FMC_HPC_DP6_C2M_P      LOC = AE4          ; # Bank 110      - MGTXTXP2_110
NET  FMC_HPC_DP6_M2C_P      LOC = AF6          ; # Bank 110      - MGTXRXP2_110
NET  FMC_HPC_DP6_C2M_N      LOC = AE3          ; # Bank 110      - MGTXTXN2_110
NET  FMC_HPC_GBTCLK1_M2C_C_P LOC = AA8          ; # Bank 110      - MGTREFCLK0P_110
NET  FMC_HPC_DP6_M2C_N      LOC = AF5          ; # Bank 110      - MGTXRXN2_110
NET  FMC_HPC_GBTCLK1_M2C_C_N LOC = AA7          ; # Bank 110      - MGTREFCLK0N_110
NET  SI5324_OUT_C_N        LOC = AC7          ; # Bank 110      - MGTREFCLK1N_110
NET  SI5324_OUT_C_P        LOC = AC8          ; # Bank 110      - MGTREFCLK1P_110
NET  FMC_HPC_DP5_C2M_P      LOC = AF2          ; # Bank 110      - MGTXTXP1_110
NET  FMC_HPC_DP5_M2C_P      LOC = AG4          ; # Bank 110      - MGTXRXP1_110
NET  FMC_HPC_DP5_C2M_N      LOC = AF1          ; # Bank 110      - MGTXTXN1_110
NET  FMC_HPC_DP5_M2C_N      LOC = AG3          ; # Bank 110      - MGTXRXN1_110
NET  FMC_HPC_DP4_C2M_P      LOC = AH2          ; # Bank 110      - MGTXTXP0_110
NET  FMC_HPC_DP4_M2C_P      LOC = AH6          ; # Bank 110      - MGTXRXP0_110
NET  FMC_HPC_DP4_C2M_N      LOC = AH1          ; # Bank 110      - MGTXTXN0_110
NET  FMC_HPC_DP4_M2C_N      LOC = AH5          ; # Bank 110      - MGTXRXN0_110
NET  SFP_TX_P               LOC = W4           ; # Bank 111      - MGTXTXP2_111
NET  SFP_RX_P               LOC = Y6           ; # Bank 111      - MGTXRXP2_111
NET  SFP_TX_N               LOC = W3           ; # Bank 111      - MGTXTXN2_111
NET  FMC_LPC_GBTCLK0_M2C_C_P LOC = U8           ; # Bank 111      - MGTREFCLK0P_111
NET  SFP_RX_N               LOC = Y5           ; # Bank 111      - MGTXRXN2_111
NET  FMC_LPC_GBTCLK0_M2C_C_N LOC = U7           ; # Bank 111      - MGTREFCLK0N_111
NET  SMA_MGT_REFCLK_N       LOC = W7           ; # Bank 111      - MGTREFCLK1N_111
NET  SMA_MGT_REFCLK_P       LOC = W8           ; # Bank 111      - MGTREFCLK1P_111
NET  SMA_MGT_TX_P           LOC = Y2           ; # Bank 111      - MGTXTXP1_111
NET  SMA_MGT_RX_P           LOC = AB6          ; # Bank 111      - MGTXRXP1_111
NET  SMA_MGT_TX_N           LOC = Y1           ; # Bank 111      - MGTXTXN1_111
NET  SMA_MGT_RX_N           LOC = AB5          ; # Bank 111      - MGTXRXN1_111
NET  FMC_LPC_DP0_C2M_P      LOC = AB2          ; # Bank 111      - MGTXTXP0_111
NET  FMC_LPC_DP0_M2C_P      LOC = AC4          ; # Bank 111      - MGTXRXP0_111
NET  FMC_LPC_DP0_C2M_N      LOC = AB1          ; # Bank 111      - MGTXTXN0_111
NET  FMC_LPC_DP0_M2C_N      LOC = AC3          ; # Bank 111      - MGTXRXN0_111
NET  PCIE_RX0_P              LOC = N4           ; # Bank 112      - MGTXTXP3_112
NET  PCIE_RX0_P              LOC = P6           ; # Bank 112      - MGTXRXP3_112
NET  PCIE_RX0_N              LOC = N3           ; # Bank 112      - MGTXTXN3_112
NET  PCIE_RX0_N              LOC = P5           ; # Bank 112      - MGTXRXN3_112
NET  PCIE_TX1_P              LOC = P2           ; # Bank 112      - MGTXTXP2_112
NET  PCIE_RX1_P              LOC = T6           ; # Bank 112      - MGTXRXP2_112
NET  PCIE_TX1_N              LOC = P1           ; # Bank 112      - MGTXTXN2_112
NET  PCIE_CLK_QO_P           LOC = N8           ; # Bank 112      - MGTREFCLK0P_112
NET  PCIE_RX1_N              LOC = T5           ; # Bank 112      - MGTXRXN2_112
NET  PCIE_CLK_QO_N           LOC = N7           ; # Bank 112      - MGTREFCLK0N_112
NET  PCIE_TX2_P              LOC = R4           ; # Bank 112      - MGTXTXP1_112
NET  PCIE_RX2_P              LOC = U4           ; # Bank 112      - MGTXRXP1_112
NET  PCIE_TX2_N              LOC = R3           ; # Bank 112      - MGTXTXN1_112
NET  PCIE_RX2_N              LOC = U3           ; # Bank 112      - MGTXRXN1_112
NET  PCIE_TX3_P              LOC = T2           ; # Bank 112      - MGTXTXP0_112
NET  PCIE_RX3_P              LOC = V6           ; # Bank 112      - MGTXRXP0_112
NET  PCIE_TX3_N              LOC = T1           ; # Bank 112      - MGTXTXN0_112
NET  PCIE_RX3_N              LOC = V5           ; # Bank 112      - MGTXRXN0_112

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Board Setup

Installing the ZC706 Board in a PC Chassis

Installation of the ZC706 board inside a computer chassis is required when developing or testing PCI Express functionality.

When the ZC706 board is used inside a computer chassis (that is, plugged in to the PCIe® slot), power is provided from the ATX power supply 4-pin peripheral connector through the ATX adapter cable shown in [Figure D-1](#) to J22 on the ZC706 board. The Xilinx part number for this cable is 2600304.



Figure D-1: ATX Power Supply Adapter Cable

To install the ZC706 board in a PC chassis:

1. On the ZC706 board, remove all six rubber feet and standoffs and the PCIe bracket. The standoffs and feet are affixed to the board by screws on the top side of the board. Remove all six screws.
2. Re-attach the PCIe bracket to the ZC706 board using two of the previously removed screws.
3. Power down the host computer and remove the power cord from the PC.
4. Open the PC chassis following the instructions provided with the PC.
5. Select a vacant PCIe expansion slot and remove the expansion cover (at the back of the chassis) by removing the screws on the top and bottom of the cover.
6. Plug the ZC706 board into the PCIe connector at this slot and secure its PCIe bracket to the chassis with a screw at the top of the bracket.

7. The ZC706 board is taller than standard PCIe cards. Ensure that the height of the card is free of obstructions.
8. Connect the ATX power supply to the ZC706 board using the ATX power supply adapter cable as shown in [Figure D-1](#):
 - a. Plug the 6-pin 2 x 3 Molex connector on the adapter cable into J22 on the ZC706 board.
 - b. Plug the 4-pin 1 x 4 peripheral power connector from the ATX power supply into the 4-pin adapter cable connector.
9. Slide the ZC706 board power switch SW1 to the ON position. The PC can now be powered on.

Board Specifications

Dimensions

Height 5.5 inch (14.0 cm)

Length 10.5 inch (26.7 cm)

Note: The ZC706 board height exceeds the standard 4.376 inch (11.15 cm) height of a PCI Express card.

Environmental

Temperature

Operating: 0°C to +45°C

Storage: -25°C to +60°C

Humidity

10% to 90% non-condensing

Operating Voltage

+12 V_{DC}

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website at:

www.xilinx.com/support.

For continual updates, add the Answer Record to your myAlerts:

www.xilinx.com/support/myalerts.

For a glossary of technical terms used in Xilinx documentation, see:

www.xilinx.com/company/terms.htm.

Solution Centers

See the [Xilinx Solution Centers](#) for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Further Resources

The most up to date information related to the ZC706 board and its documentation is available on the following websites.

The Xilinx Zynq-7000 AP SoC ZC706 Evaluation Kit product page:

www.xilinx.com/zc706

The Zynq-7000 AP SoC ZC706 Evaluation Kit - Known Issues and Release Notes Master Answer Record:

www.xilinx.com/support/answers/51899.htm

These Xilinx documents provide supplemental material useful with this guide:

[DS190](#), *Zynq-7000 All Programmable SoC Overview*

[PG064](#), *LogiCORE IP DisplayPort Product Guide*

[UG138](#), *LogiCORE IP Tri-Mode Ethernet MAC v4.2 User Guide*

[UG473](#), *7 Series FPGAs Memory Resources User Guide*

[UG470](#), *7 Series FPGAs Configuration User Guide*

[UG476](#), *7 Series FPGAs GTX/GTH Transceivers User Guide*

[UG477](#), *7 Series FPGAs Integrated Block for PCI Express User Guide*

[UG480](#), *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide*

[UG585](#), *Zynq-7000 All Programmable SoC Technical Reference Manual*

[UG586](#), *7 Series FPGAs Memory Interface Solutions User Guide*

[UG865](#), *Zynq-7000 All Programmable SoC Packaging and Pinout Product Specification*

[UG886](#), *AMS101 Evaluation Card User Guide*

[UG933](#), *Zynq-7000 All Programmable SoC PCB Design and Pin Planning Guide*

The ZC706 evaluation board schematics are available for download from:

www.xilinx.com/zc706

Other documents associated with Xilinx devices, design tools, intellectual property, boards, and kits are available at the Xilinx documentation website at:

www.xilinx.com/support/documentation/index.htm

References

Documents associated with other devices used by the ZC706 evaluation board are available at these vendor websites:

1. Analog Devices: www.analog.com/en/index.html
(ADP 123, ADV7511KSTZ-P)
2. Digilent: www.digilentinc.com
(Pmod Peripheral Modules)
3. *RTC-8564JE/NB Application Manual:*
www.epsondevice.com/docs/qd/en/DownloadServlet?id=ID000498
4. Epson Electronics America: www.eea.epson.com.
(RTC-8564JE)
5. Marvell Semiconductor: www.marvell.com
(881116R)
6. Micron Semiconductor: www.micron.com
7. Spansion Inc.: www.spansion.com
(S25FL128SAGMFIR01)
8. Samtec: www.samtec.com.
(SEAF series connectors)
9. SiTime: www.sitime.com
(SiT9102)
10. Silicon Labs: www.silabs.com
(Si570, Si5324C)
11. Standard Microsystems Corporation: www.smsc.com/
(USB3320)
12. Texas Instruments: www.ti.com
(UCD90120A, TPS84621RUQ, LMZ22010TZ, LMZ12008TZ, LMZ12002, TPS54291PWP,
TPS51200DR, PCA9548)
13. Maxim Integrated: www.maximintegrated.com
(Maxim MAX13035E)
14. PCI Express standard: www.pcisig.com/specifications
15. SFF-8431 specification: ftp.seagate.com/sff

Regulatory and Compliance Information

This product is designed and tested to conform to the European Union directives and standards described in this section.

Refer to the Zynq-7000 AP SoC ZC706 Evaluation Kit - Known Issues and Release Notes Master Answer Record concerning the CE requirements for the PC Test Environment:

www.xilinx.com/support/answers/51899.htm

Declaration of Conformity

To view the Declaration of Conformity online, please visit:

www.xilinx.com/support/documentation/boards_and_kits/ce-declarations-of-conformity-xtp251.zip

Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Markings



This product complies with Directive 2002/96/EC on waste electrical and electronic equipment (WEEE). The affixed product label indicates that the user must not discard this electrical or electronic product in domestic household waste.



This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.



This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.