# Study of High-$k$/Metal-Gate Work Function Variation in FinFET: The Modified RGG Concept

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***Abstract*— Because the existing ratio of average grain size to gate area (RGG) method is not applicable for calculating the work function variation (WFV) in nonplanar device structures, a modified RGG method is used to quantitatively estimate the WFV in a high-$k$/metal-gate (HK/MG) FinFET. A plot of the calculated WFV against the RGG for the FinFET with a TiN gate-stack is validated by previous simulation results. The standard deviation of the WFV, $\sigma$(WFV), of the nonplanar multigate device structure (e.g., the FinFET) is lower than that of a planar device structure by ∼30%.**

***Index Terms*— Characterization, CMOS, FinFET, MOSFET, ratio of average grain size to gate area (RGG), variability, work function variation (WFV).**

## I. Introduction

THE increase in the intrinsic/random threshold voltage ($V_{TH}$) variation in sub-30-nm semiconductor process technology caused by factors such as line edge roughness (LER), random dopant fluctuation (RDF), and work function variation (WFV) is one of the major technical challenges in CMOS technology development [1]. To overcome this problem, advanced device structures such as fully depleted silicon-on-insulator MOSFETs and multigate MOSFETs (e.g., FinFETs) are being adopted in industry. To meet the aggressive demand of device scaling beyond the physical limitation of $SiO_2$-based gate oxide, these devices use a high-$k$/metal-gate (HK/MG) gate-stack to improve gate-to-channel capacitive coupling. However, the atomic layer deposition (ALD) technique used in the gate-stack processes of HK/MG CMOS technology generates a lot of small grains, so that they tend to combine with the other grains, which have the same orientation (e.g., <100> and <111> orientations for TiN [2]). As a result, they become a larger grain in the annealing step of the ALD process, so that the real grains can have various sizes. Hence, randomly shaped grains cause variances in the work function values among the devices in an integrated circuit (IC). Such WFV can seriously worsen the $V_{TH}$ mismatch in the analog/digital circuit block of the IC, and the magnitude of the WFV-induced $V_{TH}$ variation is larger than that induced by either LER or RDF in sub-30-nm process technology [2], [3]. To quantitatively estimate WFV, previous studies have proposed analytical modeling [3], [4] or conducted experimental verification [5], [6]. Following these studies, more realistic 3-D simulations have been conducted [7], [8]. We simply characterized the WFV using two major variables: 1) the average grain size of the gate material and 2) the gate area. As the modeled WFV is closely associated with the manner in which the grain shapes are generated and distributed in the gate material, the use of the Rayleigh distribution [9], [10] and a more physically realistic method of generating grain shapes enable the construction of a plot of the ratio of average grain size to gate area (RGG) [9] that can be fitted to experimental data. Such work, however, has thus far been limited to conventional planar device structures, even though the industry is increasingly choosing nonplanar device structures that use HK/MG technology.

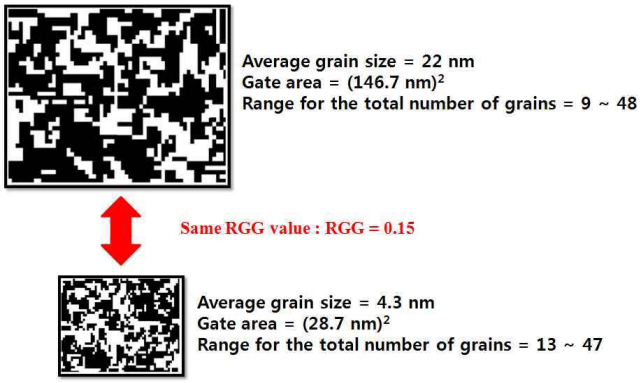


Fig. 1. Two animated figures with different average grain sizes and gate areas but identical RGG values. Note that the range for the total number of grains is comparable for the two different devices' gate material.

In this letter, we propose a modified RGG concept for estimating the WFV-induced $V_{TH}$ variation in HK/MG FinFETs. By matching previous simulation results [7] with an RGG plot for the HK/MG FinFET, the magnitude of $\sigma$(WFV) in the FinFET can be easily estimated.

## II. WFV Modeling in FinFET

Fig. 1 shows the RGG concept in detail. As the RGG of a device is defined as the ratio of the average grain size to the gate area [i.e., RGG = average grain size (nm) × gate area$^{-1/2}$ (nm$^{-1}$)], a scaled-down transistor should also scale down the average grain size of its gate material to retain its RGG value and prevent its WFV from increasing. In other

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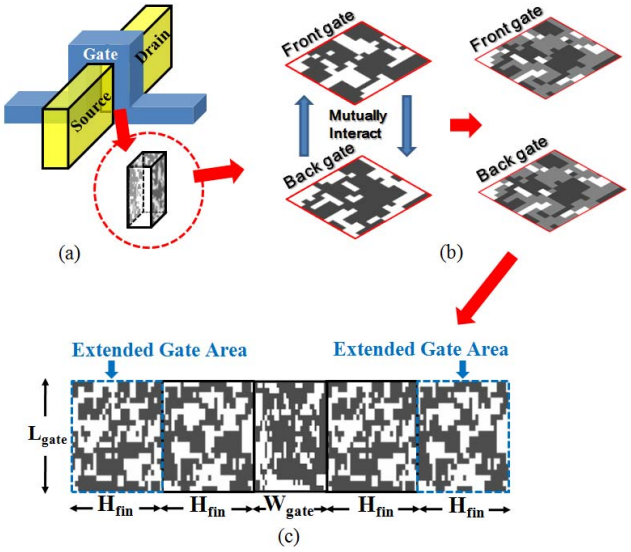


Fig. 2. (a) 3-D bird's eye view of a FinFET. (b) Front and back gates are mutually interacting, so that the new grain is generated as the EGA. The gate area in left and right sides is doubled by the EGA effect. (c) Unfolded planar figure showing the channel region of the FinFET with the EGAs. Note that $L_{gate}$ is the channel length, $H_{fin}$ is the fin height, and $W_{gate}$ is the gate width.

words, it is noted that, regardless of their average grain sizes and the gate areas, two devices with the identical RGG values should have a comparable amount of the WFV. This is because these devices have a comparable range for the total number of grains. Using Monte Carlo simulation, it is verified that the two different devices can have the identical magnitude of $\sigma$(WFV) for the same RGG value [9]. Since the usefulness of the RGG concept has been verified for conventional planar bulk MOSFET structure [9], the RGG calculation should be modified in the case of FinFET-type device structures because they control the channel potential using double, as opposed to single, gates.

Fig. 2 shows a modified method for estimating the WFV in a FinFET. The two face-to-face [i.e., front and back in Fig. 2(b)] gates in the FinFET mutually interact when building up an inversion layer or channel, so that the new grains in these gates will be generated with a new probability and work function. Hence, a modified method for the FinFET RGG calculation should consider the extended gate area (EGA) generated by these gates. Correspondingly, the total gate area over which to calculate the FinFET RGG should be defined as: $[\{W_{gate} + (4 \times H_{fin})\} \times L_{gate}]$ [as opposed to $W_{gate} \times L_{gate}$ for a planar MOSFET, and also opposed to $\{W_{gate} + (2 \times H_{fin})\} \times L_{gate}$ for a FinFET without EGA].

## III. Results and Discussion

A plot of the estimated WFV versus the RGG for a FinFET using a TiN gate is shown in Fig. 3. The use of the conventional RGG method to estimate the WFV versus RGG based on a conventional gate area (red triangles) results in a large deviation from the RGG data (blue circles) for a FinFET. However, using the modified RGG method with the EGA values (green rectangles) produces the results that are closely matched to the original RGG plot (blue circles). Because the total effective gate area physically controlled by the double

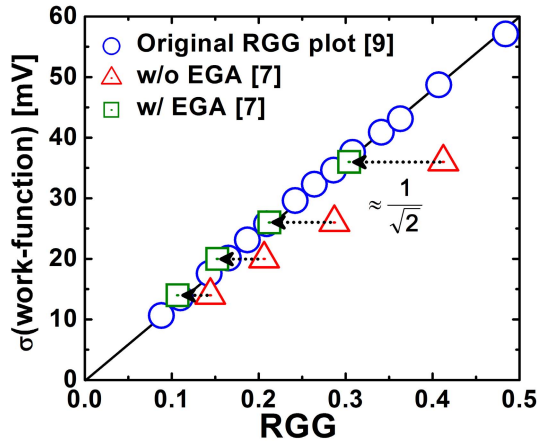


Fig. 3. $\sigma$(WFV) versus RGG for a FinFET. Note that the RGG plot for TiN is included.

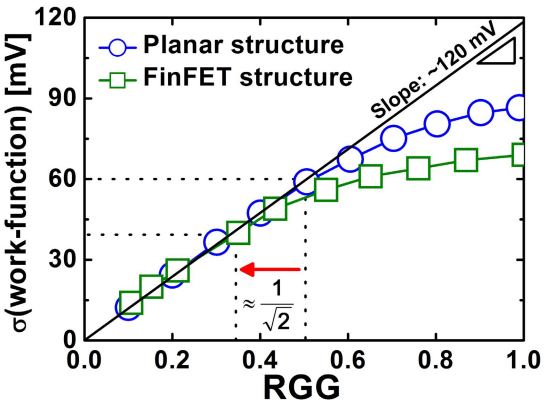


Fig. 4. $\sigma$(WFV) versus RGG for the planar (circle) and FinFET (square) structures. Note that the critical point is shifted by the factor of $\sim (1/2)^{0.5}$ due to the consideration of the EGA, in calculating the RGG values for the FinFET.

gates in the FinFET is nearly doubled in comparison with a planar bulk MOSFET, the EGA should be included in computing the RGG, which then shifts the RGG value for a given WFV by $\sim(1/2)^{0.5}$ (Fig. 3), causing the FinFET data values to match to the original RGG plot. Note that the original purpose of plotting the RGG values was to determine a unique estimate of the WFV for a given material. As long as the appropriate RGG calculation method is used, the RGG plot of a material will remain unique regardless of device structure.

As shown in [9] and [10] (i.e., the blue line in Fig. 4), the RGG plot can be divided into two regions: a region where $\sigma$(WFV) is linearly increasing and the other region where it is increasing nonlinearly. The critical point for the planar structure in the plot occurs at RGG = 0.5, primarily because the total number of the grains starts to saturate at RGG = 0.5 (blue line in Fig. 5). Interestingly, the critical point for the FinFET structure is shifted from 0.5 to 0.35 (i.e., green line in Fig. 5) by a factor of $\sim(1/2)^{0.5}$. This is because the range for the total number of grains is also shifted by the EGA effect, as shown in Fig. 5. If the range was not shifted, the RGG plot for the FinFET structure would be the same as that of the planar device structure.

Finally, it was reported in [6] that the amount of $\sigma V_{TH}$ for the FinFET diminishes by ~30%, as compared with the

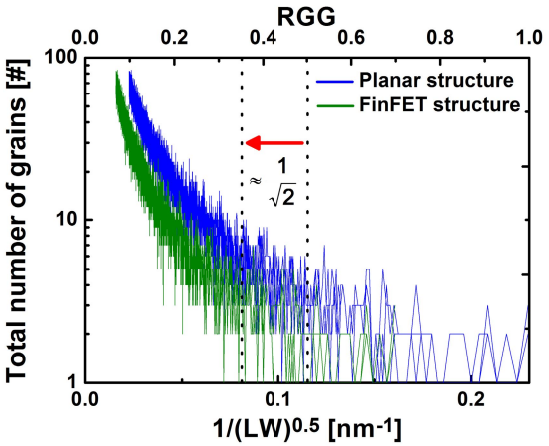


Fig. 5. Total number of the grains versus (gate area)$^{-0.5}$. Note that the total number of the grains saturates from the RGG of 0.5 in the planar structure, and from the RGG of 0.35 in the FinFET structure.

planar bulk MOSFET. This may well be caused by the ∼30% decreased RGG for the double-gate device structures with the EGA effect in the given layout area; this is achieved without the use of a new material (e.g., a material with a slope of <120 mV in the RGG plot, and/or with a smaller average grain size). Thus, the double-gate device architecture represents a promising way for significantly suppressing the WFV in HK/MG CMOS technology by ∼30%.

## IV. Conclusion

As the existing method for calculating the RGG is not valid for advanced device structures, the RGG method has been modified for the FinFET devices, by considering the EGA as the physical gate area. The WFV of a TiN gate-stack FinFET was quantitatively estimated using the modified RGG values, and the results, validated by previous simulation results, showed that the $\sigma$(WFV) in the FinFET is lower than that in a planar device structure by ∼30%.

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