Digital Automotive Two-Wire Pixel Link

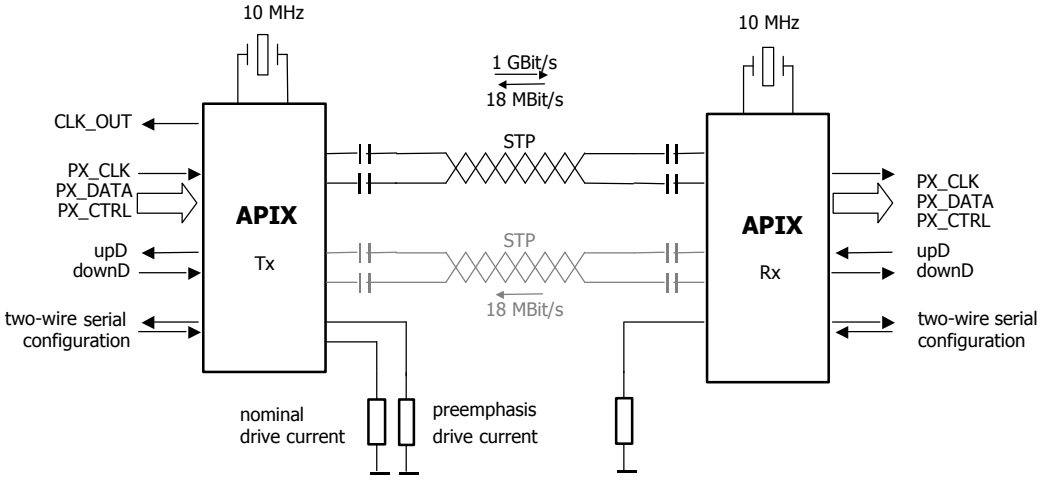
INAP125T10
INAP125T18
INAP125T24
INAP125R10
INAP125R24

The APIX long-distance link is a bit serial high speed DC-balanced, low latency and low EMI interconnect for dispatched displays or cameras linked to central video/ imaging processors. Basically the APIX requires only one twisted cable pair for full duplex video and sideband operation but for EMI sensitive applications a separate feedback path occupying one additional twisted pair maybe used alternatively.
A bi-directional sideband data channel, which e.g. allows for control of CMOS camera sensors or display settings, is provided.
The combination of adjustable driver characteristics, selectable operating modes of 0.5 or 1 Gbit/s and Spread Spectrum-Clocking enables the minimal EMI at maximum transmissions distances and lowest power consumption.
The whole feature set reduces system cost while providing enhanced functionality when compared to standard Serializer/Deserializer chip sets.

Features:
- Low EMI, Two- or Four-Wire Full Duplex Link
- Up to 1 Gbit/s Downstream Link Bandwidth
- Up to 18 Mbit/s Upstream Link Bandwidth
- 15 m+ Distance with small profile STP/UTP cables
- Tx: 10/12/18/24 bit RGB Interface
- Rx: 10/12/18/24 bit RGB Interface
- DC-balanced decoding supports AC-coupling
- Adjustable Output Driver Characteristics
- Link Setup/Control through Microwire-Compatible Interface
- Dual +1.8 V / 3.3 V Power Supply
- Extended Temperature Range: -40…+105°C

Package:
- Package: 44/48/52/64 pin QFN

Applications:
- In-Car Information Displays
- Automotive Dashboard Displays
- Head-Up Displays
- Rear-Seat Infotainment
- Automotive Vision Systems
  - Lane Departure Warning
  - Obstacle Detection
  - Sign Recognition
  - Rear & Side Mirror Replacement
  - Blind Spot Detection
- Passenger Infotainment Systems
- Security Systems
- Machine Vision
- Military Head-Up and Helmet Displays



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1 Introduction

The APIX Transmitter and Receiver chip incorporates the APIX SerDes for the physical layer and provides a digital pixel data interface plus a bi-directional sideband data interface.

The link transmits uncompressed pixel data utilizing one single pair of a STP cable. Further a bi-directional sideband channel for the transfer of control data is provided, using the same physical layer technology as the downstream channel. The link supports distances of up to 15m+.

To serve a wide range of pixel data transmission applications, such as camera link from CCD chip to a display or image processing unit, or display data from a graphics processor to an in-seat display, the APIX chip set provides a configurable parallel pixel data interface.

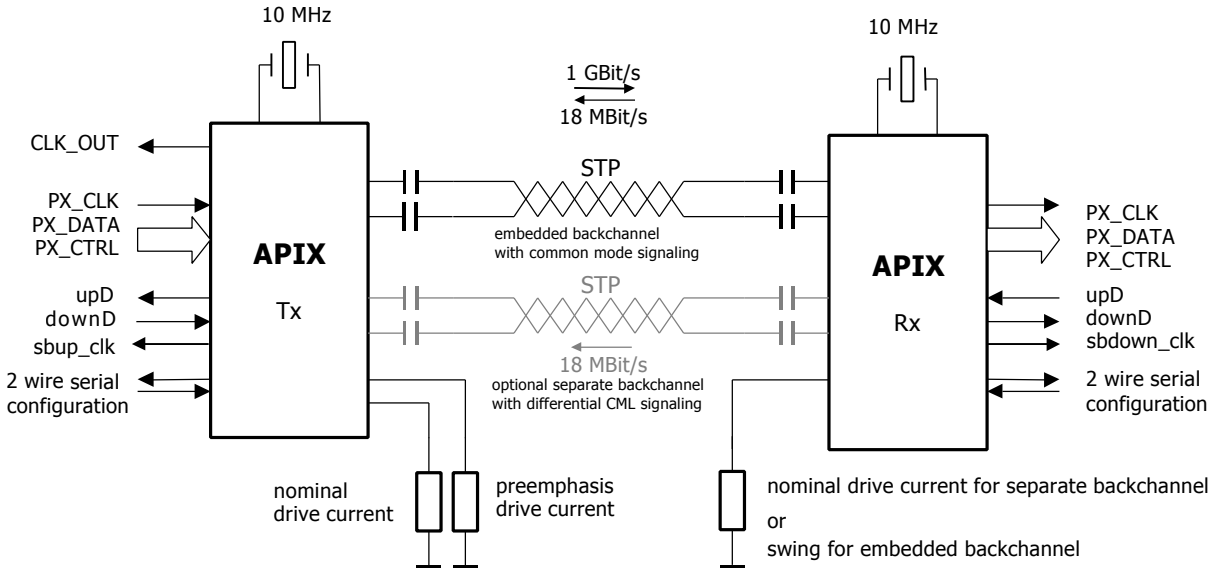


Figure 1: Automotive Pixel Link Chip Set

1.1 Link Bandwidth Capabilities

Downstream		
Operation Mode	**@ 1000 Mbit/s**	**@ 500 Mbit/s**
10 bit	max. 60 MHz PxClk	max. 36 MHz PxClk
18 bit	max. 42 MHz PxClk	max. 21 MHz PxClk
24 bit	max. 32 MHz PxClk	max. 16 MHz PxClk
Sideband Channel	2 x 1 bit at 12 Mbit/s max.	2 x 1 bit at 6 Mbit/s max.
Upstream		
Sideband Channel	2 x 1 bit at 9 Mbit/s max.	

Table 1: Bandwidths of Up-/Downstream Links

2 APIX Transmitter

Features:

- Configurable 10, 12, 18 and 24-bit pixel interface
- Three general purpose framing control lines for vsync, hsync, de or frameStart, lineStart, valid
- Pixel clock range: 6 – 60 MHz
- Serial interface: Line coding (DC-balanced) for ground-free AC-coupling
- Link Bandwidth: 1000 Mbit/s down and 18 Mbit/s up
- Configuration via Microwire-Compatible Interface
- Temperature range: -40 – +105°C
- ESD: ≥ 4 kV (EN 61000-4-2)
- Integrated oscillator circuit with external low-cost crystal
- Programmable clock multiplier for clock supply of image sensor
- Core supply voltage: 1.8 V
- I/O tolerance: 3.3 V
- QFN 44/52/64-Pin

2.1 Interfaces

2.1.1 Physical Layer Interface

The downstream channel provides a maximum sustained bandwidth of 1000 Mbit/s for video data, sideband data (downstream) and overhead for synchronization. 18 Mbit/s is the maximum sustained net bandwidth at the upstream channel for sideband data. The link bandwidth can be selected to be half of the max. bandwidth (500 Mbit/s instead 1000 Mbit/s). The need to lower the provided bandwidth is basically driven by the requirement to reduce power (line driver strength) and EMI. Therefore the transmission rate at the serial data line needs to be reduced.

2.1.2 Downstream

The downstream serial link interface provides a differential, serial output in current mode logic (CML).

Minimizing EMI is supported by a resistor programmable IO drive strength for nominal and pre-emphasis current. Pre-emphasis is provided on a per bit basis for the entire bit time.

2.1.3 Upstream

The upstream serial link interface provides two different options, which occupies either a separate second STP cable pair for upstream data transmission or also utilizes the downstream STP cable for upstream data transfer in parallel to the downstream data transmission. Both options can be selected alternatively. The upstream link can be disabled totally.

Option 1 comprises a differential, serial output, which is implemented with current mode logic (CML). Tx and Rx are connected with a separate STP cable.
Option 2 utilizes a common mode signaling technique, which makes use of the downstream STP cable pair and consequently does not require a separate STP cable and IO pair.

Minimizing EMI is supported by a resistor programmable IO drive strength for nominal current for the first option and a resistor programmable common mode swing for the second option.

2.1.4 Pixel Data Interface

Up to 24 bit of parallel pixel data, representing the pixel's RGB values, is received via the pixel interface. The parallel pixel interface supports pixel formats of 10bit, 12bit, 18bit, and 24bit.

The pixel data and the control signals are registered with the pixel interface clock. The active edge can be configured to be rising or falling. The logic level of this interface is 3.3V.

2.1.5 Sideband Data Interface

The sideband data interface provides two 2 bit wide data interfaces, one for downstream data and one for upstream data. At the input (downstream interface) 2 bits of data are sampled. At the output of the upstream interface the data, which were sampled at the Rx upstream input, are provided together with corresponding clock.

2.1.6 Signal Description

Signal Name	Direction	Description
px_data[23…0]	IN	24 bit of RGB pixel data
px_clk	IN	Pixel data and pixel control signals are sampled with respect to the rising or falling edge of pxClk.
px_ctrl[2…0]	IN	Pixel control signals, such as hsync, vsync, de or lineSync, frameSync, valid.
sbdown_data[1…0]	IN	Generic 2 bit of data which are sampled with a sampling rate of 12 Mbit/s.
sbup_data[1…0]	OUT	Generic 2 bit of data which are provided based on a sampling rate of 9 Mbit/s.
sbup_clk	OUT	Clock output for sbup_data.
reset_n	IN	Hardware reset asynchronus.
tx_error	OUT	Error indicator for upstream link
eeprom_data	IN/OUT	Serial data input output for configuration
eeprom_clk	OUT	Serial shift clock for configuration
xtal_in	IN	Oscillator input or reference clock input, 10MHz
xtal_out	OUT	Oscillator output
bas_cur	PASSIV	External resistor to vdda to set base drive current for downstream serial data output. Min.value 250 Ohm (20mA) and max.value 18kOhm (0.8mA)
pre_cur	PASSIV	External resistor to vdda to set preemphasis drive current for downstream serial data output. Min.value 250 Ohm (4mA) and max.value 18kOhm (0.15mA)
sdout_p	OUT	CML serial data interface downstream. Interface to differential transmission line or STP cable with Zdiff=100Ohm.
sdout_n	OUT	
sdin_p	IN	CML serial data interface upstream. Interface to differential transmission line or STP cable with Zdiff=100Ohm.
sdin_n	IN	
vdd_vco	IN	Regulated power supply for VCO 1.8V, 7mA
vco_tune_in	IN	VCO loop filter tuning voltage
pfd_out	OUT	Current output for VCO loop filter
VDD	PWR	1.8V core supply
DVDD	PWR	3.3V io supply
VSS	PWR	Digital core ground
DVSS	PWR	Digital io ground
vdda	PWR	1.8V analog supply
gnda	PWR	Analog ground
VDD_OSC	PWR	1.8V oscillator supply
DVDD_OSC	PWR	3.3V oscillator supply
VSS_OSC	PWR	Oscillator ground
DVSS_OSC	PWR	Oscillator io ground

Table 2: Transmitter Signal Description

3 APIX Receiver

Features:

- Configurable 10, 12, 18 and 24-bit pixel interface
- Three general purpose framing control lines for vsync, hsync, de or frameStart, lineStart, valid
- Pixel clock range: 6 – 60 MHz
- Serial interface: Line coding (DC-balanced) for ground-free AC-coupling
- Link Bandwidth: 1000 Mbit/s (gross rate) down and 18 Mbit/s (net rate) up
- Configuration via Microwire-Compatible Interface
- Temperature range: -40 – +105°C
- ESD: ≥ 4 kV (EN 61000-4-2)
- Integrated oscillator circuit with external low-cost crystal
- PxCLk Jitter better than 1 ns
- Core supply voltage: 1.8 V
- I/O tolerance: 3.3 V
- QFN 48/64-Pin

3.1 Interfaces

3.1.1 Downstream

The downstream serial link interface comprises a differential, serial input, which is implemented with current mode logic (CML). An analog equalizer is provided to preprocess the incoming serial signal.

Further the link bandwidth can be selected to be half of the max. bandwidth (500 Mbit/s instead of 1000 Mbit/s).

3.1.2 Upstream

The upstream serial link interface provides two different options, which support either a second separate STP cable pair for upstream data transmission or utilize the downstream STP cable for upstream data transfer in parallel to the downstream data transmission. Option one and two can be selected alternatively. The upstream can be disabled totally.

Minimizing EMI is supported by a resistor programmable IO drive strength for nominal current for the first option and a resistor programmable common mode swing for the second option.

3.1.3 Pixel Data Interface

Up to 24 bit of parallel pixel data, representing the pixel's RGB value, are provided at the pixel interface. The parallel pixel interface supports pixel formats of 10 bit, 12bit, 18bit, and 24bit.

Pixel data and the control signals are provided with reference to the pixel interface clock. The active edge can be configured to be rising or falling. The pixel clock jitter is better than 1 ns.

The logic level of the interface is 3.3V CMOS logic level.

3.1.4 Sideband Data Interface

The sideband data interface provides two 2 bit wide data interfaces, one for downstream data and one for upstream data. At the input (upstream interface) 2 bits of data are sampled with a sampling rate of 9 MHz. At the output of the downstream interface the data, which were sampled at the Tx downstream input, are provided.

3.2 Signal Description

Signal Name	Direction	Description
px_data[23…0]	OUT	24 bit of RGB pixel data if parallel mode
px_clk	OUT	Pixel data and pixel control signals are sampled with respect to the rising or falling edge of pxClk (parallel mode)
px_ctrl[2…0]	OUT	Pixel control signals, such as hsync, vsync, de or lineSync, frameSync, valid
sbup_data[1…0]	IN	Generic 2 bit of data which are sampled with a sampling rate of 9 Mbit/s.
sbdown_data[1…0]	OUT	Generic 2 bit of data which are provided based on a sampling rate of 12 Mbit/s.
sbdown_clk	OUT	Clock output for sbdown_data
reset_n	IN	Hardware reset asynchronous
rx_error	OUT	Error Indicator
eeprom_data	IN/OUT	Serial data input output for configuration
eeprom_clk	OUT	Serial shift clock for configuration
xtal_in	IN	Oscillator input or reference clock input, 10MHz
xtal_out	OUT	Oscillator output
px_vco_in	IN	VCO for pixel clock generation – Input
px_vco_out	OUT	VCO for pixel clock generation – Output
bas_cur	PASSIV	External resistor to vdda to set base drive current for upstream serial data output. Min.value 250 Ohm (20mA) and max.value 18kOhm (0.8mA)
sdout_n sdout_p	OUT OUT	CML serial data interface upstream. Interface to differential transmission line or STP cable with Zdiff=100Ohm.
sdin_p sdin_n	IN IN	CML serial data interface downstream. Interface to differential transmission line or STP cable with Zdiff=100Ohm.
vdd_vco	IN	Regulated power supply for VCO 1.8V, 7mA
vco_tune_in	IN	VCO loop filter tuning voltage
pfd_out	OUT	Current output for VCO loop filter
VDD	PWR	1.8V core supply
DVDD	PWR	3.3V io supply
VSS	PWR	Digital core ground
DVSS	PWR	Digital io ground
vdda	PWR	1.8V analog supply
gnda	PWR	Analog ground
VDD_OSC	PWR	1.8V oscillator supply
DVDD_OSC	PWR	3.3V oscillator supply
VSS_OSC	PWR	Oscillator ground
DVSS_OSC	PWR	Oscillator io ground

Table 3: Receiver Signal Description

4 Configuration and Reset

The asynchronous reset can be entered at any time and sets the devices into a defined state.

The following parameters and settings are configurable through the two-wire serial interface:

Setting / Parameter	Description
Active Pixelclock Edge	Sets Active Edge of Pixelclock
Pixel Interface Mode	Sets Pixel Interface Mode to 10/12/18/24bit
Equalizer	Enables/Disables Equalizer in Downstream Path
Bandwidth Downstream	Sets Downstream Link Bandwidth to 500 Mbit/s or 1000 Mbit/s
Staggered Outputs	Enables Staggered Outputs' Switching
Bandwidth Upstream	Sets Upstream Link Bandwidth

Table 4: Configuration Settings

The serial configuration interface is compatible to the Microwire Interface from Michrochip.

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

The absolute maximum ratings define values beyond which damage to the device may occur. Inova Semiconductors may not be held liable for any product degradation or damage caused by a violation of the absolute maximum ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above those indicated in the recommended operating conditions is not guaranteed.

Parameter	Symbol	Min.	Max.	Units	Note
DC Supply Voltage	V_{CC}	t.b.d.	t.b.d.	V	
Input Voltage	V_{IN}	t.b.d.	t.b.d.		
I/O Current (DC or transient any pin)	I_D	-20	+20	mA	See handling precautions (6)
Junction Temperature (under bias)	T_j	-45	+140	° C	
Storage Temperature	T_{stg}	-55	+150	° C	
Soldering Temp./Time	T_{SLD} / t_{SLD}				
Static Discharge Voltage (CMOS dig. I/O versus respective GND & Supply rails)	V_{SDCMOS}		± 4000	V	Human Body Model
Static Discharge Voltage (all other pin combinations including CML I/O pins)	V_{SDCML}		± 2000	V	Human Body Model

Table 5: Absolute Maximum Ratings

5.2 Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
DC Supply Voltage Core	V_{CC_CORE}	1.71	1.89	V	
DC Supply Voltage IO	V_{CC_IO}	3.15	3.45	V	
CML Output Current	I_{OUTCML}	0.8	24	mA	
Junction Temperature (under bias)	T_j	-40	+125	° C	
Ambient Temperature	T_a	-40	+105	° C	

Table 6: Recommended Operating Conditions

5.3 AC–Characteristics

Parameter	Min.	Typ.	Max.	Units
Input Capacitance, any pin		3	5	pF
Serial Transmission Gross Data Rate (Downstream)	500		1000	Mbit/s
Serial Transmission Net Data Rate (Upstream)		18		Mbit/s
CMOS Output Rise / Fall Time (C_L = 10 pF)		5	10	ns

Table 7: AC–Characteristics

5.4 DC–Characteristics (under recommended operating conditions)

Parameter	Symbol	Test Condition	Min.	Max.	Unit
CMOS Input High Voltage	V_{IH}	Vcc = 1.71 V to 1.89 V	0.65 x Vcc_io		V
		Vcc = 2.3 V to 2.7 V	1.7		V
CMOS Input Low Voltage	V_{IL}	Vcc = 1.71 V to 1.89 V		0.35 x Vcc_io	V
		Vcc = 2.3 V to 2.7 V		0.7	V
CMOS Input High Current	I_{IH}	V_{IN} = Vcc		40	µA
CMOS Input Low Current	I_{IL}	V_{IN} = 0 V		40	µA
CMOS Output High Voltage	V_{OH}	I_{OH} = -0.5 mA, Vcc = 1.71			V
		I_{OH} = -1.5 mA, Vcc = 2.5			V
CMOS Output Low Voltage	V_{OL}	I_{OL} = 0.5 mA, Vcc = 1.71			V
		I_{OL} = 1.5 mA, Vcc = 2.5			V
CMOS Output High Current	I_{OH}	V_{OH} = 0.9xVcc, Vcc = 1.71			mA
		V_{OH} = 0.9xVcc, Vcc = 2.5			mA
CMOS Output Low Current	I_{OL}	V_{OL} = 0.1xVcc, Vcc = 1.71			mA
		V_{OL} = 0.1xVcc, Vcc = 2.5			mA
Power Dissipation	P_{RX}	Max. data transmission rate		400	mW

Table 8: DC–Characteristics

Note: Floating CMOS inputs can result in excessive supply current therefore unused inputs should be tied to Vcc or GND.

5.5 Reference Clock Specification (Ta = -40 to +105° C; Vcc=1.71 - 1.89V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Nominal Frequency	f_{OSC}	t.b.d.	10	t.b.d.	MHz	
Frequency Tolerance	F_{TOL}	-100		+100	Ppm	

Table 9: Reference Clock Specification

6 Package Options / Pinouts / Package Dimensions

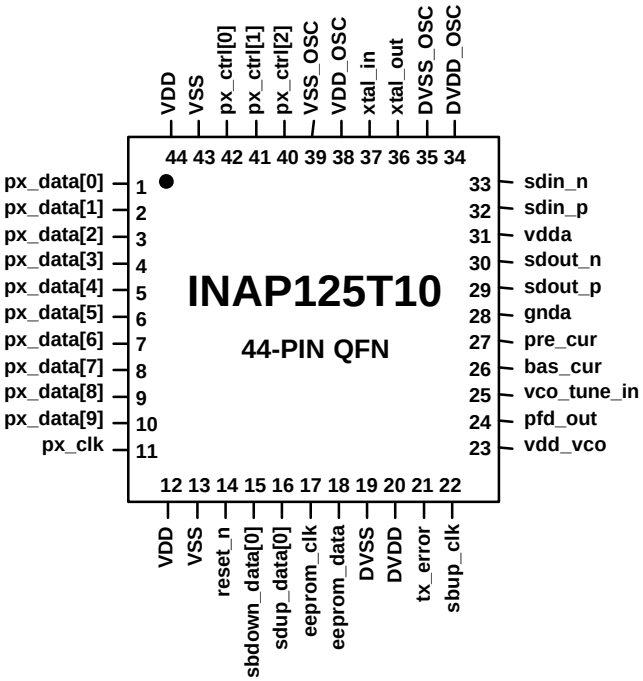
6.1 Package Options

To reducing pin count and saving board space at dedicated applications, the APIX chips are available in packages with different pin counts.

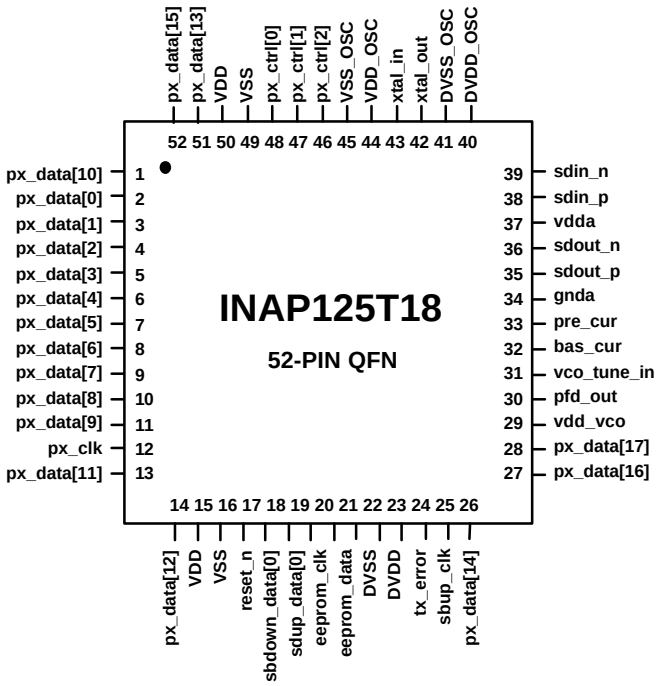
Device	Description	Package
Transmitter		
INAT125P10	Tx with 10bits Interface + 1 bit Sideband	QFN44
INAT125P18	Tx with 18bits Interface + 2 bits Sideband	QFN52
INAT125P24	Tx with 18…24bits Interface + 2 bits Sideband	QFN64
Receiver		
INAR125P10	Rx with 10bits Interface + 1bit Sideband	QFN48
INAR125P24	Rx with 18…24bits Interface + 2bits Sideband	QFN64

6.2 Pinouts

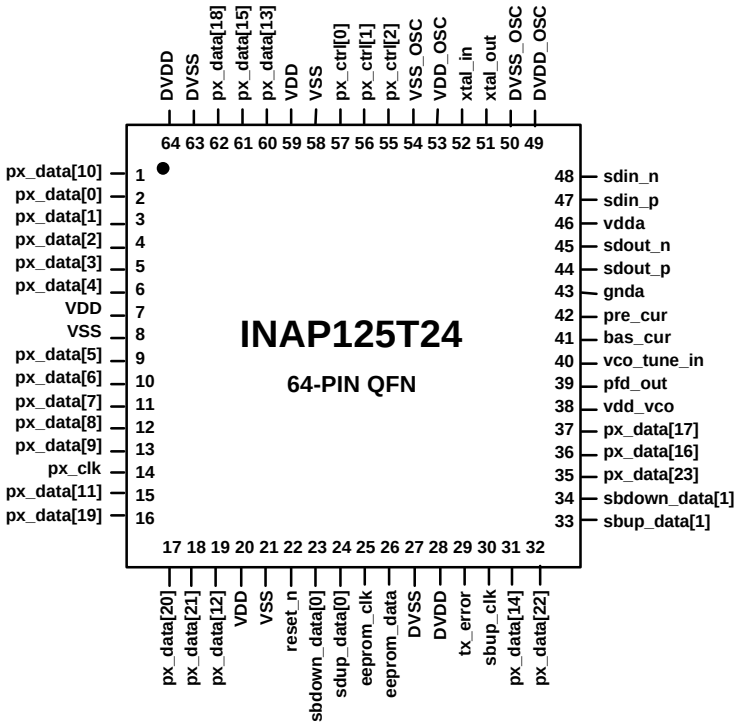
6.2.1 APIX Transmitter INAP125T10



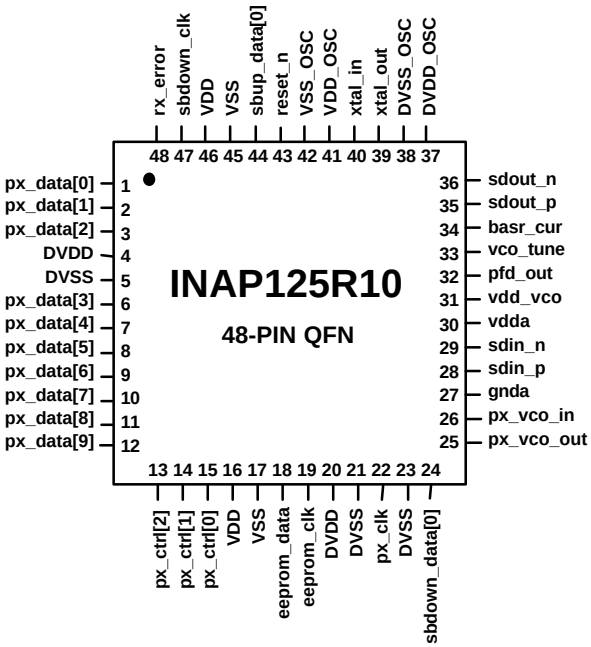
6.2.2 APIX Transmitter INAP125T18



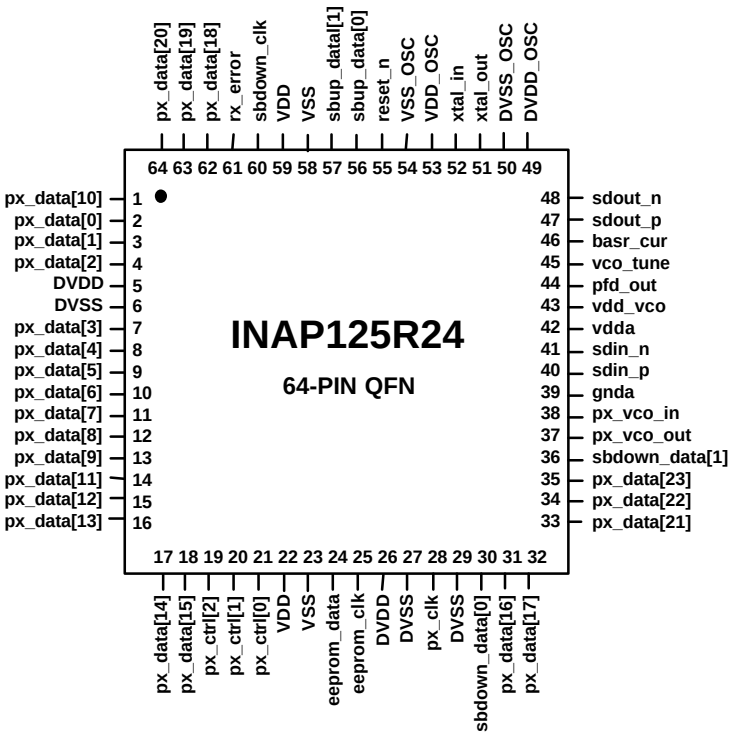
6.2.3 APIX Transmitter INAP125T24



6.2.4 APIX Receiver INAP125R10

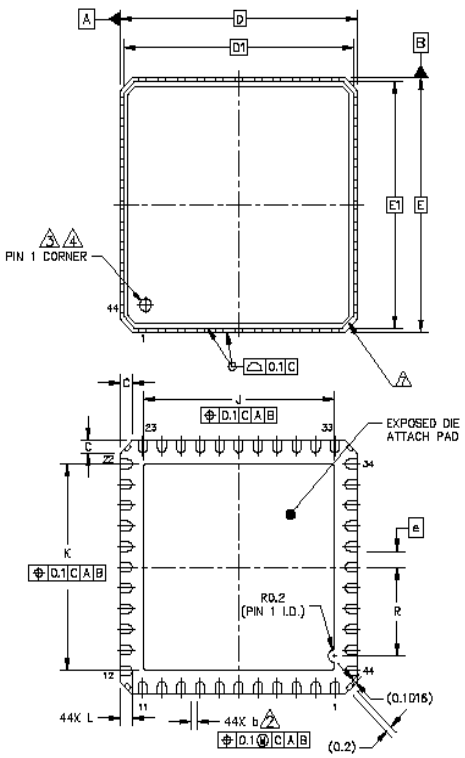


6.2.5 APIX Receiver INAP125R24



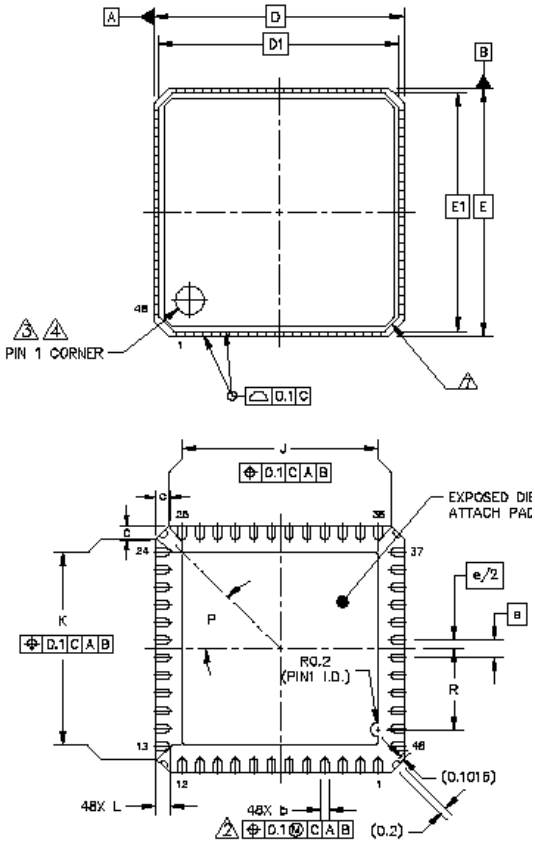
6.3 Package Dimensions (all values in mm)

44-PIN QFN



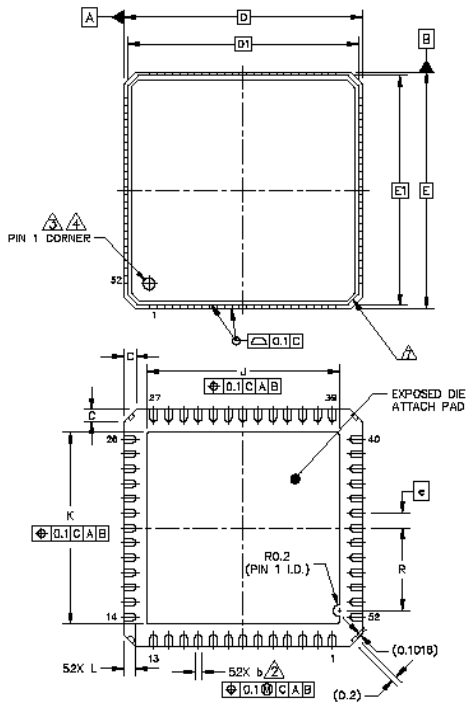
DIM	MIN	NOM	MAX
A	0.8		0.9
A1	0	0.02	0.05
A2	0.65		0.69
A3		0.203 REF	
b	0.25	0.3	0.35
C	0.24	0.42	0.6
D		8 BSC	
D1		7.75 BSC	
E		8 BSC	
E1		7.75 BSC	
e		0.65 BSC	
J	6.37	6.47	6.57
K	6.37	6.47	6.57
L	0.35	0.4	0.45
R	2.685	2.785	2.885

48-PIN QFN



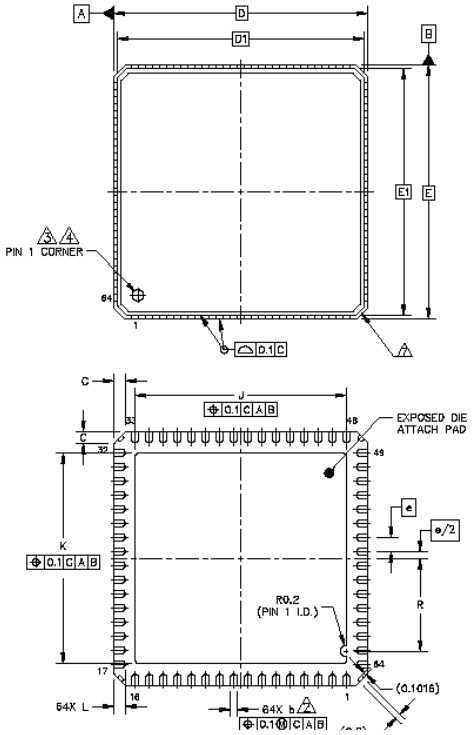
DIM	MIN	NOM	MAX
A	0.8		0.9
A1	0	0.02	0.05
A2	0.65		0.69
A3		0.203 REF.	
b	0.18	0.25	0.3
C	0.24	0.42	0.6
D		7 BSC	
D1		6.75 BSC	
E		7 BSC	
E1		6.75 BSC	
e		0.5 BSC	
J	5.37	5.47	5.57
K	5.37	5.47	5.57
L	0.3	0.4	0.5
P		45° REF	
R	2.185	2.285	2.385

52-PIN QFN



DIM	MIN	NOM	MAX
A	0.8		0.9
A1	0	0.02	0.05
A2	0.65		0.69
A3		0.203 REF	
b	0.18	0.25	0.3
C	0.24	0.42	0.6
D		8 BSC	
D1		7.75 BSC	
E		8 BSC	
E1		7.75 BSC	
e		0.5 BSC	
J	6.37	6.47	6.57
K	6.37	6.47	6.57
L	0.3	0.4	0.5
R	2.685	2.785	2.885

64-PIN QFN



DIM	MIN	NOM	MAX
A	0.8		0.9
A1	0	0.02	0.05
A2	0.65		0.69
A3		0.203 REF	
b	0.18	0.25	0.3
C	0.24	0.42	0.6
D		9 BSC	
D1		8.75 BSC	
E		9 BSC	
E1		8.75 BSC	
e		0.5 BSC	
J	7.37	7.47	7.57
K	7.37	7.47	7.57
L	0.3	0.4	0.5
R	3.185	3.285	3.385

7 Revision History

- v 0.1 Initial *Preliminary Product Preview*
- v 0.2 Upstream Bandwidth changed to 18 Mbit/s*;*
- v 0.*3* *- Updated Rx Pin Table & Description*
  - Core Supply Voltage set to 1.8V±5%.
- ***v 0.31 Changed/replaced Rx Bypass-Pin to/with DVSS***

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