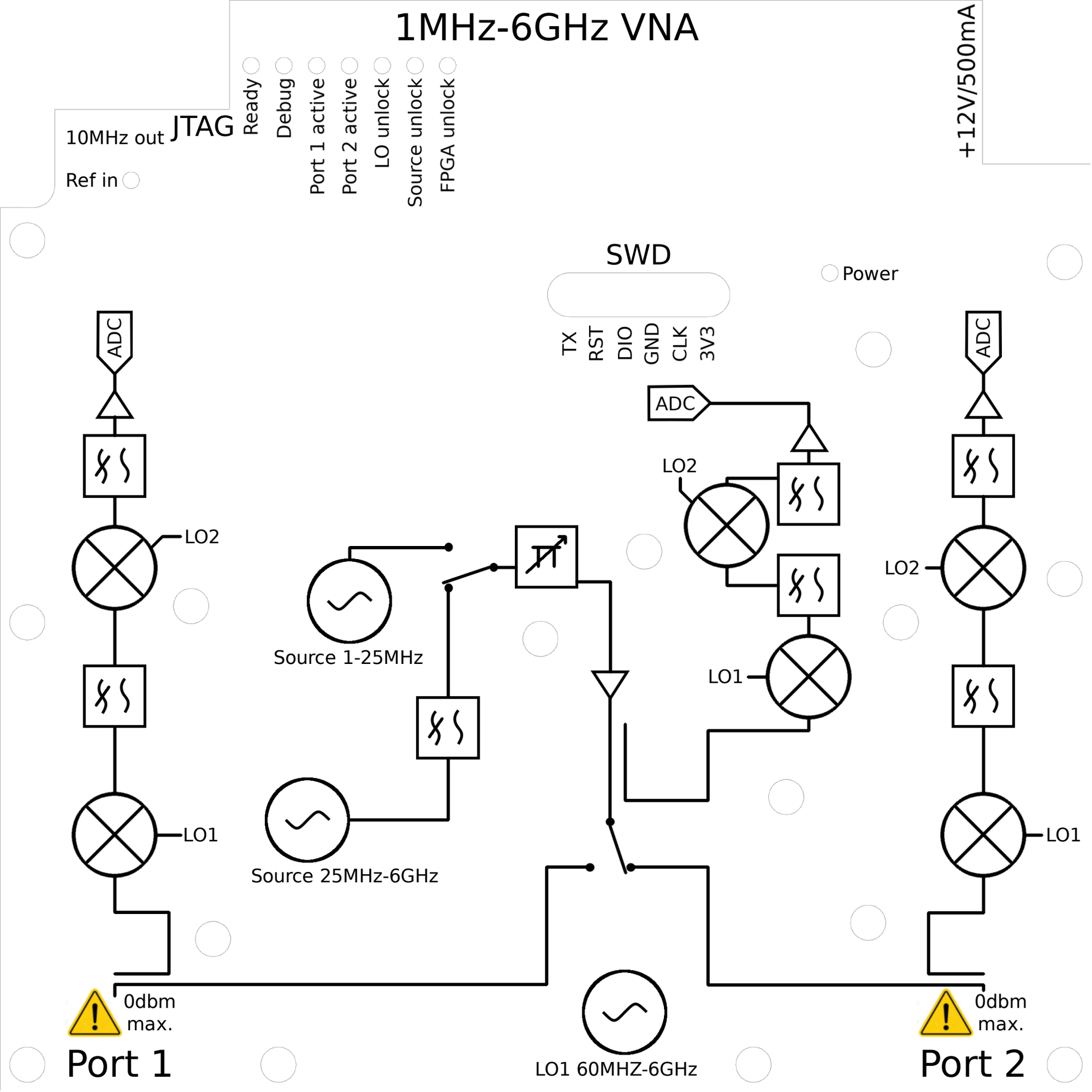
1MHz-6GHz VNA
10MHz out
JTAG
Ref in
Ready
Debug
Port 1 active
Port 2 active
LO unlock
Source unlock
FPGA unlock
+12V/500mA
SWD
TX
RST
DIO
GND
CLK
3V3
Power
ADC
LO2
LO1
Source 1-25MHz
Source 25MHz-6GHz
0dbm
max.
Port 1
LO1 60MHZ-6GHz
Port 2