1 Digital Interface

Pin	Direction	Function
SCK	in	SCK for SPI communication/SCK for PLL communication
MOSI	in	MOSI for SPI communication/MOSI for PLL communication
MISO	out	MISO for SPI communication/MUX for PLL communication
NSS	in	Chip Select for SPI communication/LE for PLL communication
INTR	out	Active high interrupt indicator
RESET	in	FPGA reset
AUX1	in	Selector for direct communication with Source PLL
AUX2	in	Selector for direct communication with LO PLL
AUX3	in	Active low sweep enable. Has to be high when changing settings

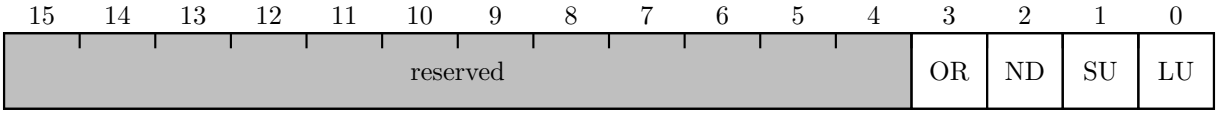
Depending on the voltage on AUX1/AUX2 the SPI port controls either the FPGA or one of the MAX2871 PLLs:

AUX1	AUX2	Function
low	low	SPI communication with FPGA
high	low	Direct feedthrough of SCK, MOSI, MISO and NSS to Source PLL
low	high	Direct feedthrough of SCK, MOSI, MISO and NSS to LO PLL
high	high	Invalid

When communicating with a PLL, the MUX output of the MAX2871 is forwarded to MISO and the NSS signal is forwarded to the LE pin. As the LE pin should stay low until after a valid register has been shifted in (see MAX2871 datasheet), set NSS low before switching to PLL communication mode.

2 SPI Protocol

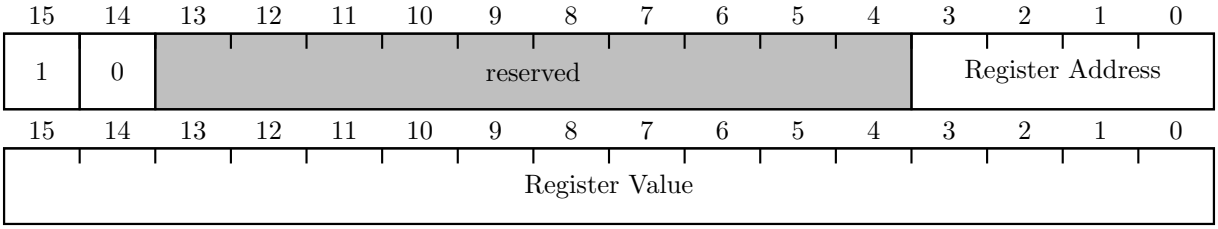
Each SPI transfer starts with pulling NSS low and ends with NSS returning to high level. SPI communication is done in words of 16 bits. The first word after NSS is pulled low is the command word and determines the amount and meaning of the following words. The word received while transmitting the command word is the interrupt status register:



- **OR:** Data overrun occured (only cleared by resetting the FPGA)
- **ND:** New data available
- **SU:** Source unlocked
- **LU:** LO unlocked

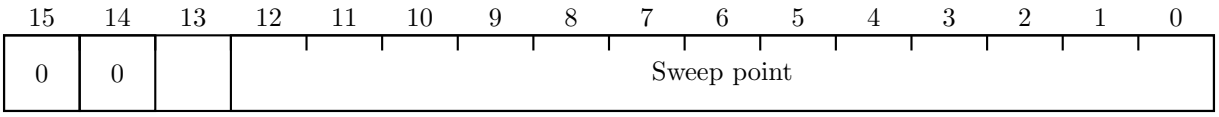
2.1 Writing a register

Writing a register requires the transfer of two words: First the control word selecting the destination address and a second word containing the new register value:



2.2 Writing SweepConfig

Initiate the sweep config transfer by sending the command word:

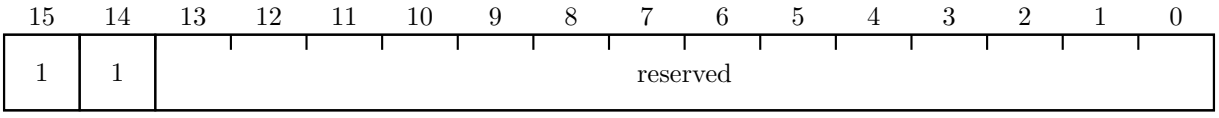


The maximum number of points per sweep is 4501, thus the highest valid value for "Sweep point" is 4500. After the control word, send the seven words of the sweep config (see section 4) while keeping NSS low. The sweep config is transmitted MSB first.

2.3 Reading a sampling result

Whenever the ND bit in the interrupt status register is set, new sampling data is available and can be read via SPI. It has to be read before the next sampling data arrives otherwise the old data will be overwritten.

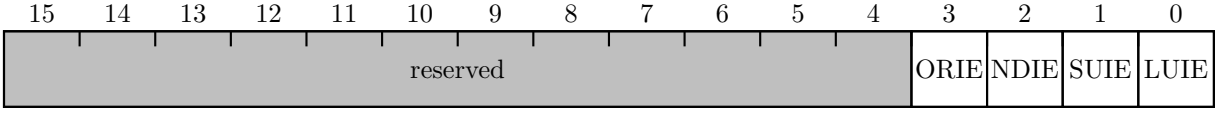
Initiate the reading of sampling data by sending the command word:



Afterwards, read 18 words before setting NSS high. These 18 words will contain the sampling result (see section 5), transmitted with the least significant word first.

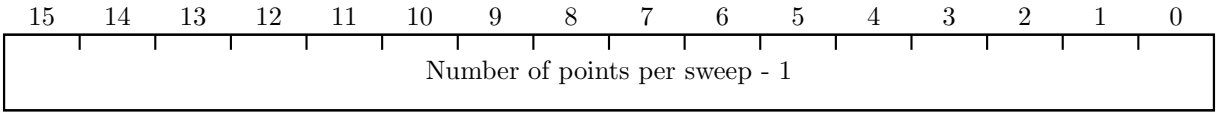
3 Registers

3.1 Interrupt Mask Register: 0x00



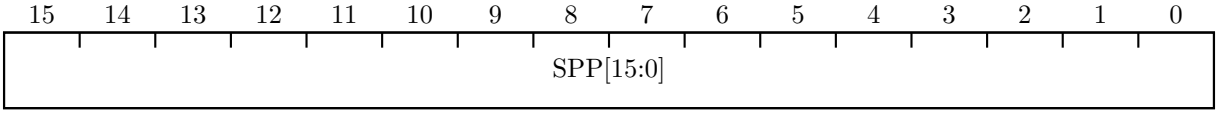
- **ORIE:** Data overrun interrupt enable
- **NDIE:** New data interrupt enable
- **SUIE:** Source unlocked interrupt enable
- **LUIE:** LO unlocked interrupt enable

3.2 Sweep Points Register: 0x01



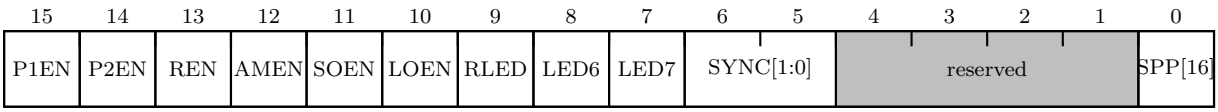
The register contains the number of points per sweep negative one, e.g. set to 11b if the sweep contains four points.

3.3 Samples Per Point Register: 0x02



- **SPP[16:0]:** The register contains the number of samples per point negative one, e.g. set to 11b if each point contains four samples. Also see register 0x03 for MSB.

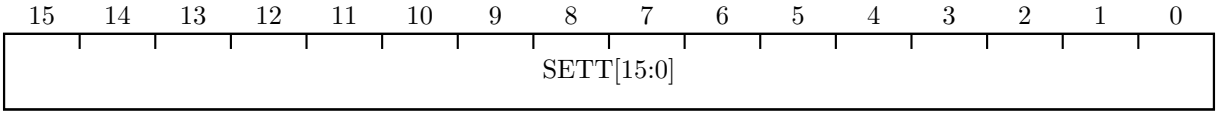
3.4 System Control Register: 0x03



- **P1EN:** Port 1 Mixers/Amplifier enable
- **P2EN:** Port 2 Mixers/Amplifier enable
- **REN:** Reference Mixers/Amplifier enable
- **AMEN:** Source amplifier enable
- **SOEN:** Source enable
- **LOEN:** LO enable
- **RLED:** External frequency LED control
- **LED6:**User LED 6 control
- **LED7:**User LED 7 control
- **SYNC[1:0]:**Synchronization control for switching regulator

Setting	Functionality
00	disabled
01	1 MHz signal
10	locked to ADC sampling (slightly less than 1 MHz)
11	disabled

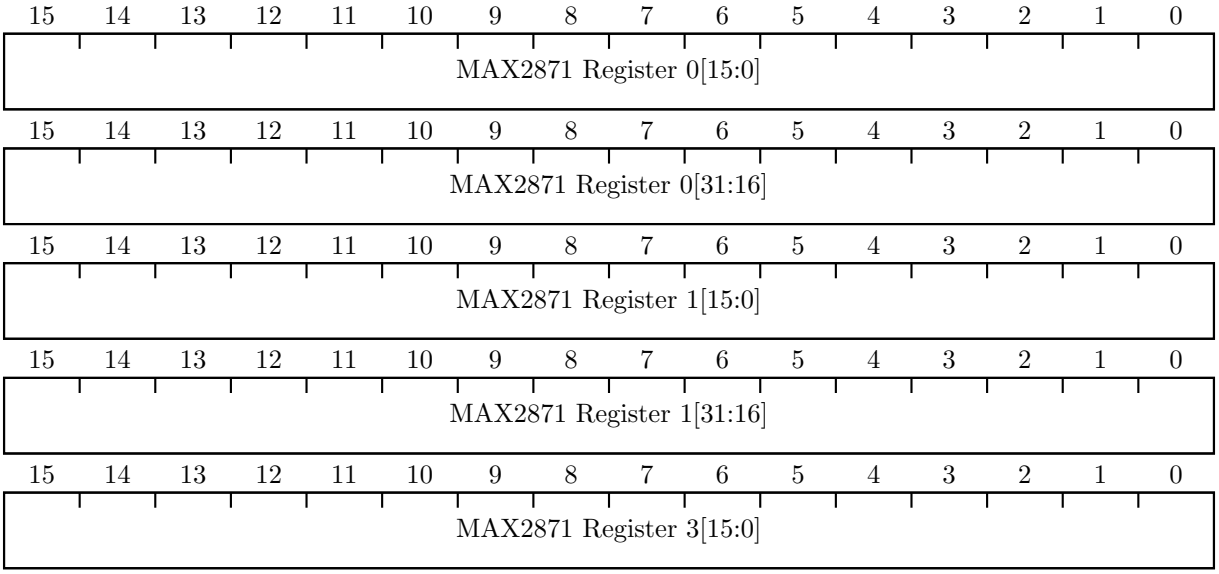
3.5 Settling Time Register: 0x04

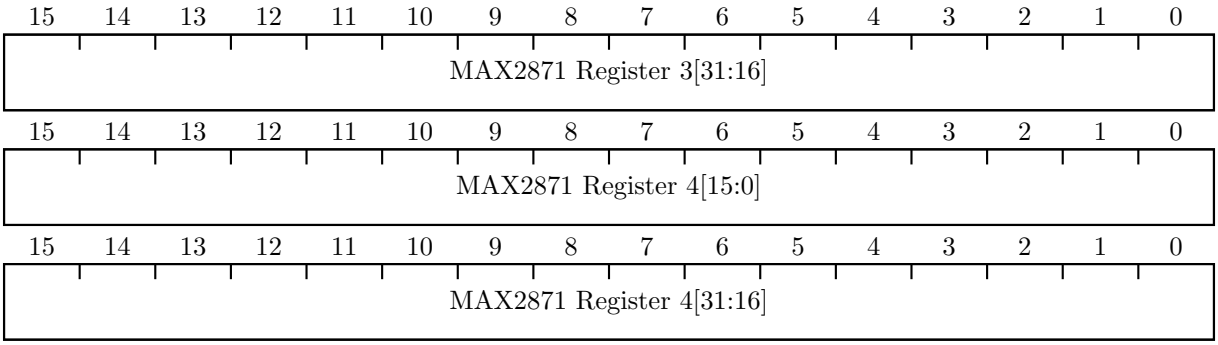


- **SETT[15:0]:** Number of CLK cycles between locking of PLLs and sampling of the ADCs. One CLK cycle is equivalent to 6.25 ns

3.6 MAX2871 Default Values Registers: 0x08-0x0F

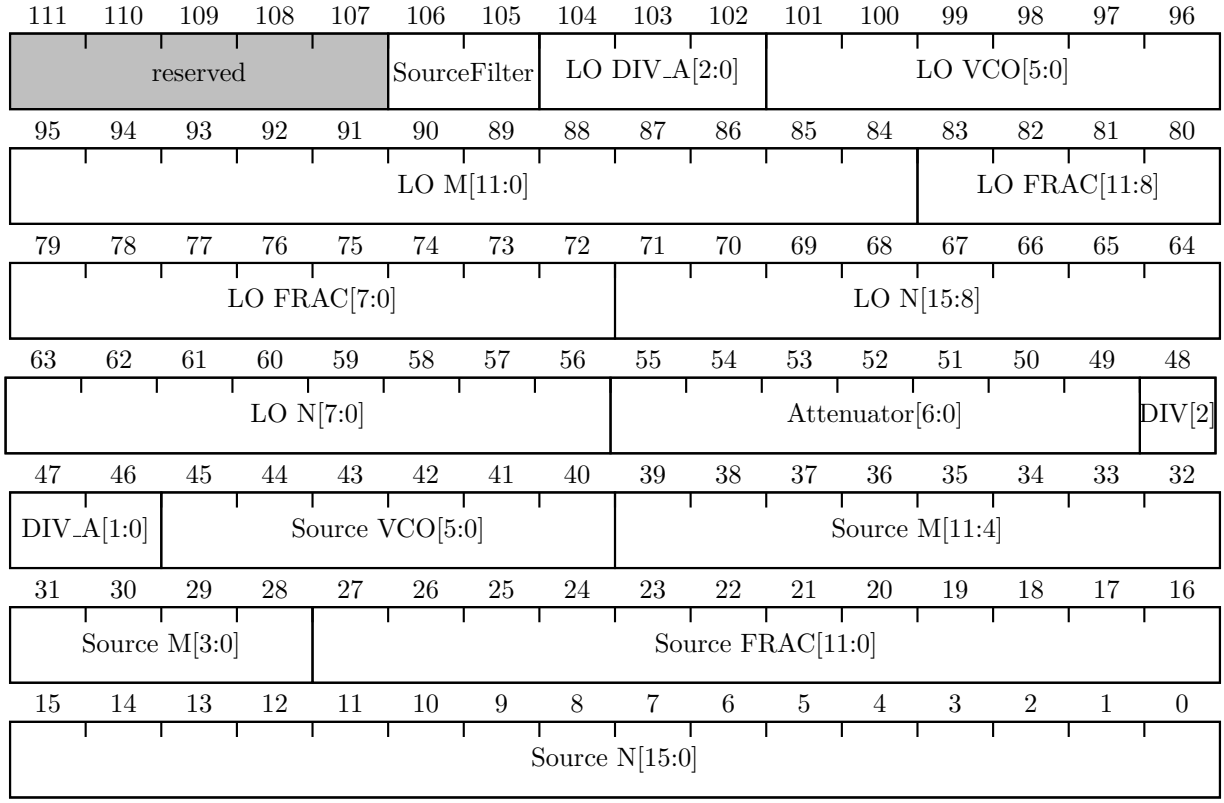
See datasheet of MAX2871 for bit descriptions. Bits for the fields N, FRAC, M, VCO and DIV_A are "don't care" as they will be overwritten by the SweepConfig setting.





4 SweepConfig

The SweepConfig contains data for the source and LO1 PLL as well as the attenuator and source filter. Each point in the sweep, needs a valid SweepConfig before the sweep is started.



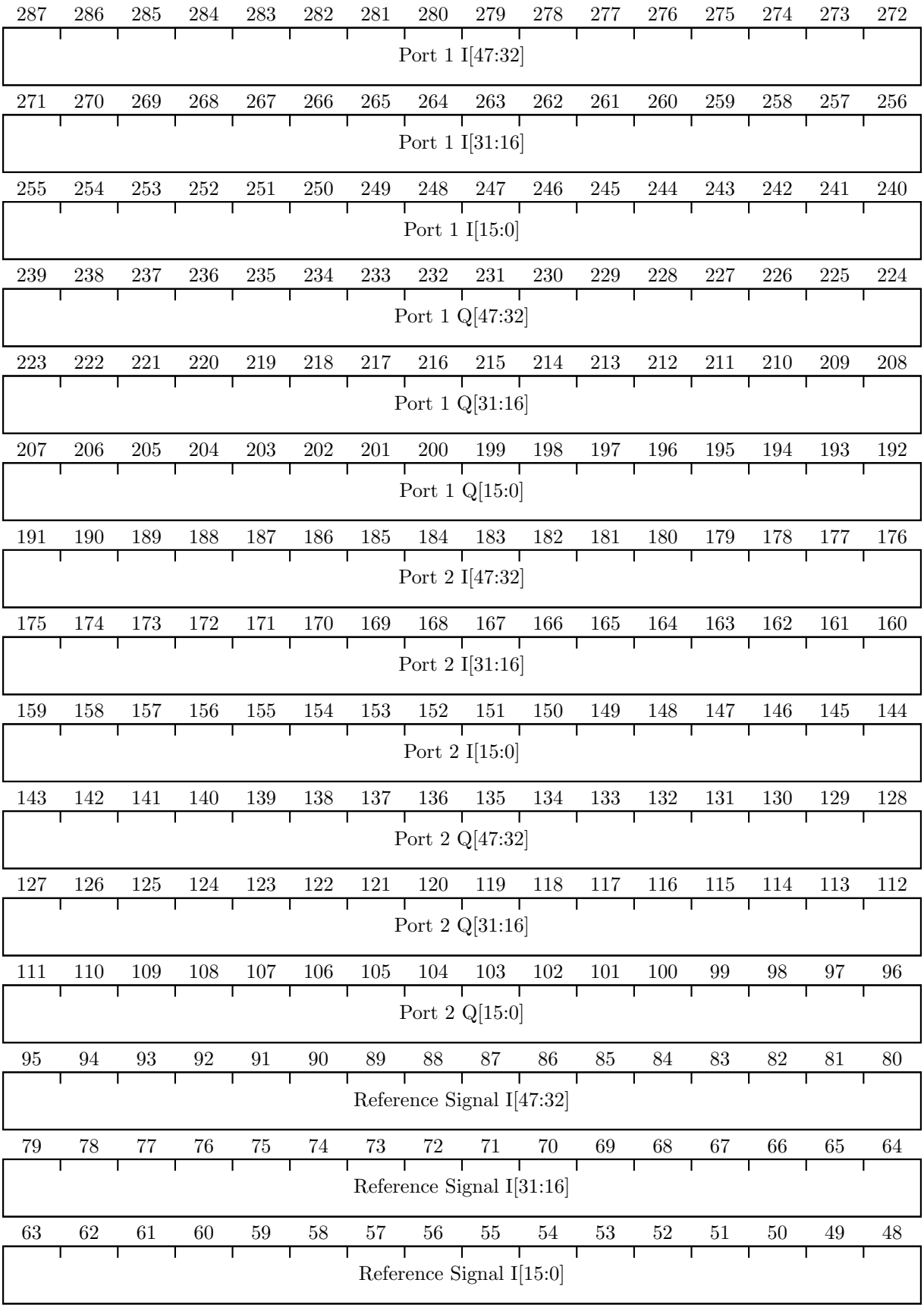
- **SourceFilter:** Low pass filter selection for source signal

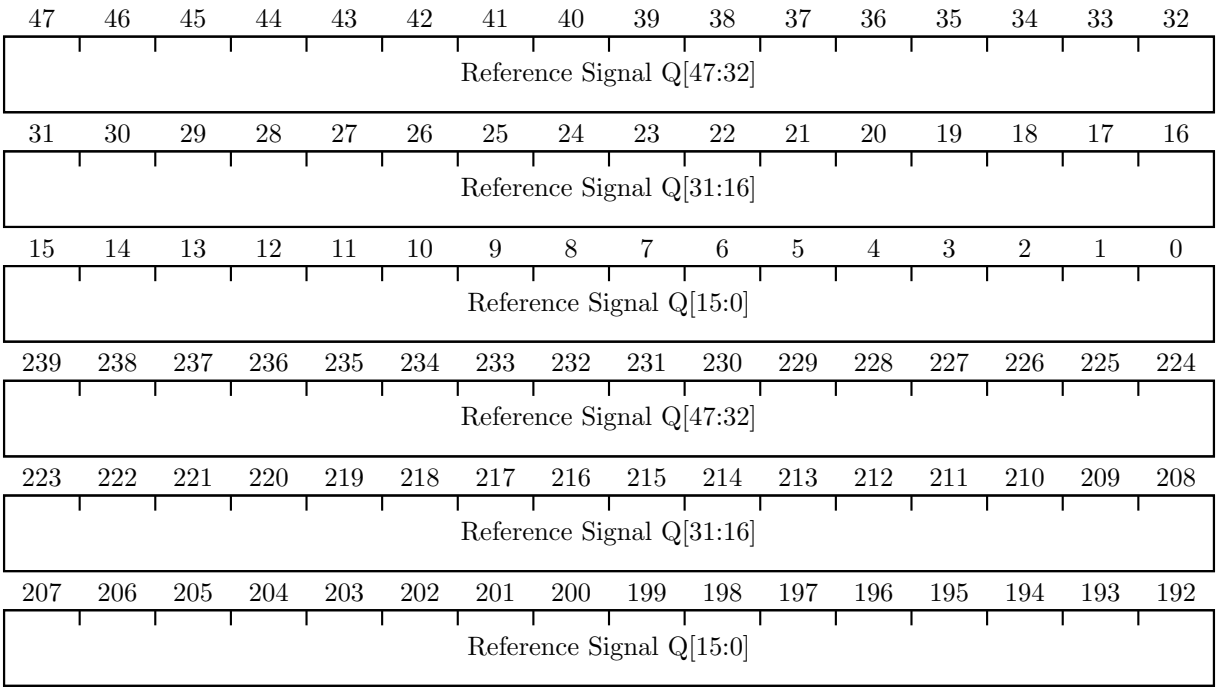
Setting	Selected Band
00	0 MHz to 900 MHz
01	900 MHz to 1800 MHz
10	1800 MHz to 3500 MHz
11	3500 MHz to 6000 MHz

- **Attenuator:** Attenuation of source signal in 0.25 dB.

5 Sampling Result

Each point in the sweep generates two sampling results. The first one contains the measurement when the source was routed to Port 1, the second sampling result was taken when the source was routed to Port 2. The sampling result does not indicate which point in the sweep it belongs to, that information is implicitly given by the order of transmitted sampling results.


287 286 285 284 283 282 281 280 279 278 277 276 275 274 273 272
Port 1 I[47:32]
271 270 269 268 267 266 265 264 263 262 261 260 259 258 257 256
Port 1 I[31:16]
255 254 253 252 251 250 249 248 247 246 245 244 243 242 241 240
Port 1 I[15:0]
239 238 237 236 235 234 233 232 231 230 229 228 227 226 225 224
Port 1 Q[47:32]
223 222 221 220 219 218 217 216 215 214 213 212 211 210 209 208
Port 1 Q[31:16]
207 206 205 204 203 202 201 200 199 198 197 196 195 194 193 192
Port 1 Q[15:0]
191 190 189 188 187 186 185 184 183 182 181 180 179 178 177 176
Port 2 I[47:32]
175 174 173 172 171 170 169 168 167 166 165 164 163 162 161 160
Port 2 I[31:16]
159 158 157 156 155 154 153 152 151 150 149 148 147 146 145 144
Port 2 I[15:0]
143 142 141 140 139 138 137 136 135 134 133 132 131 130 129 128
Port 2 Q[47:32]
127 126 125 124 123 122 121 120 119 118 117 116 115 114 113 112
Port 2 Q[31:16]
111 110 109 108 107 106 105 104 103 102 101 100 99 98 97 96
Port 2 Q[15:0]
95 94 93 92 91 90 89 88 87 86 85 84 83 82 81 80
Reference Signal I[47:32]
79 78 77 76 75 74 73 72 71 70 69 68 67 66 65 64
Reference Signal I[31:16]
63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48
Reference Signal I[15:0]


47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32
Reference Signal Q[47:32]
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16
Reference Signal Q[31:16]
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Reference Signal Q[15:0]
239 238 237 236 235 234 233 232 231 230 229 228 227 226 225 224
Reference Signal Q[47:32]
223 222 221 220 219 218 217 216 215 214 213 212 211 210 209 208
Reference Signal Q[31:16]
207 206 205 204 203 202 201 200 199 198 197 196 195 194 193 192
Reference Signal Q[15:0]