Modelsim/Questa Starter Guide

Before beginning this tutorial, ensure you have completed assignment 2 and are ready to write your assignment 3 testbench or already have it. You will use the code you have written in those exercises for this tutorial.

Why Modelsim/Questa?

- Questa is on the NTNU programfarm, which should allow any OS to simulate VHDL. This is possible if on campus or with a VPN to campus. See here https://farm.ntnu.no/.

- As an Alternative, you can install it on a system with less memory if Vivado is too large. Modelsim/Questa is 4GB and supports the same operating systems.

- Using Modelsim/Questa is an alternative to Vivado for simulation, and pairs better with using your own IDE, e;g Vscode with a VHDL plugin (e;g TerosHDL). Vivado is neither a great IDE nor simulator, but it is a very good tool for analysing your implemented designs.

- Modelsim/Questa can allow you to use more productive simulation tools such as UVVM. https://github.com/UVVM/UVVM

Setting Up Modelsim/Questa

To install Modelsim go to https://www.intel.com/content/www/us/en/software-kit/750368/modelsim-intel-fpgas-standard-edition-software-version-18-1.html. This is the latest free version.

The same applies to Questasim under “Individual downloads” tab.

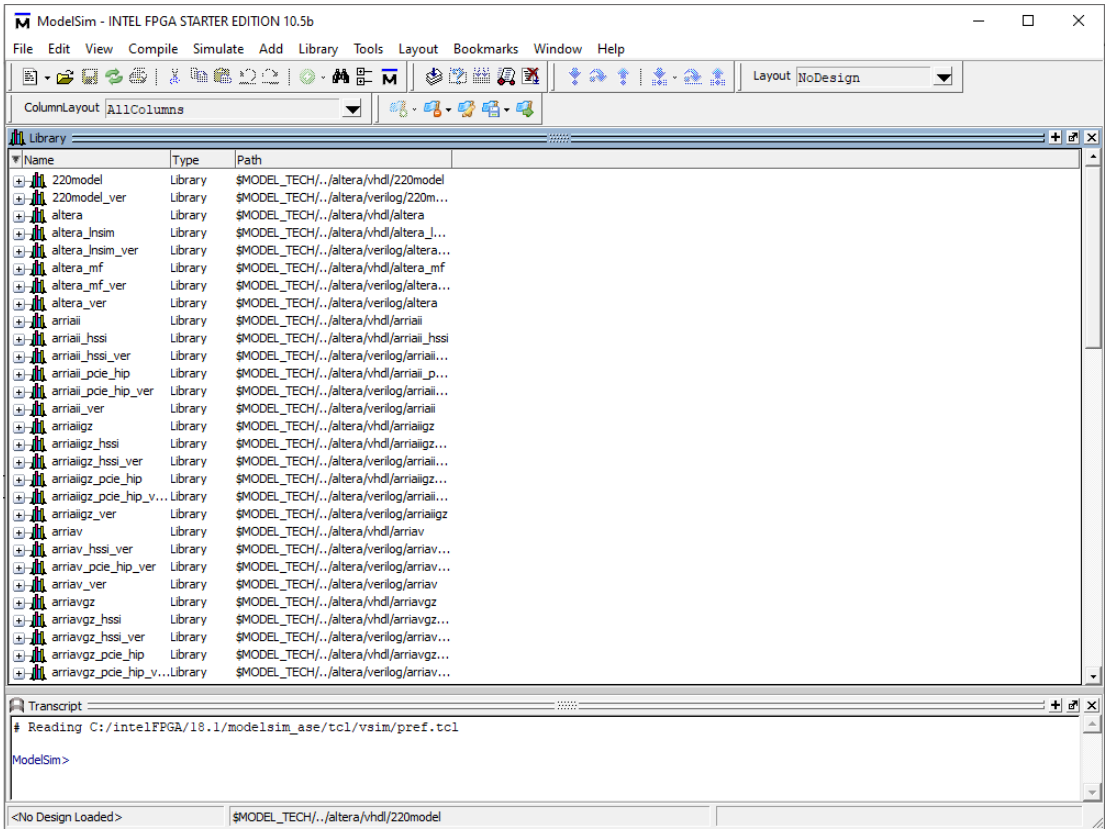
https://www.intel.com/content/www/us/en/software-kit/785085/intel-quartus-prime-lite-edition-design-software-version-22-1-2-for-linux.html?

To use Questa on the program farm, you first need a VPN to NTNU, or to be on the university network. https://i.ntnu.no/wiki/-/wiki/English/Install+vpn. Cisco anyconnect works on Linux, Windows and Mac. Questa is located in this folder https://farm.ntnu.no/RDWeb/Pages/en-US/Default.aspx/Scientific . Try to login using your username@ntnu.no (without stud), when launching Questa.

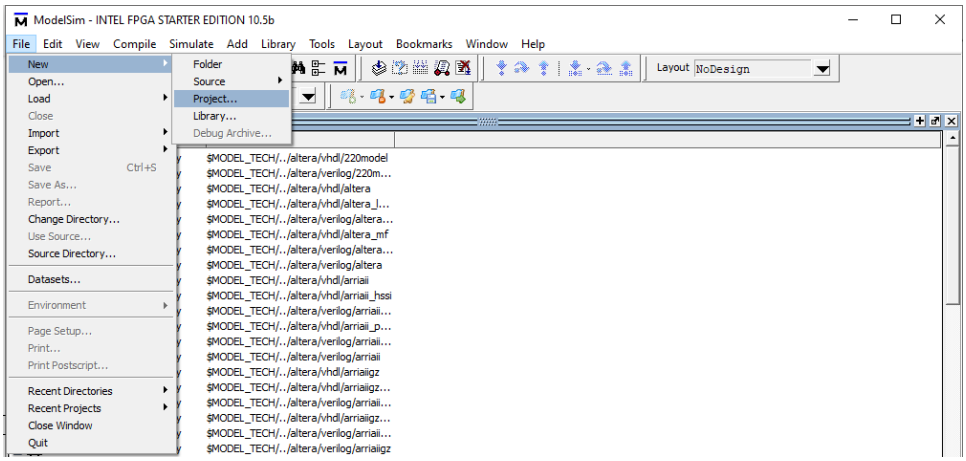
Type vsim if you have installed it on Linux to open it. Or launch it from the installation directory

Using the tools

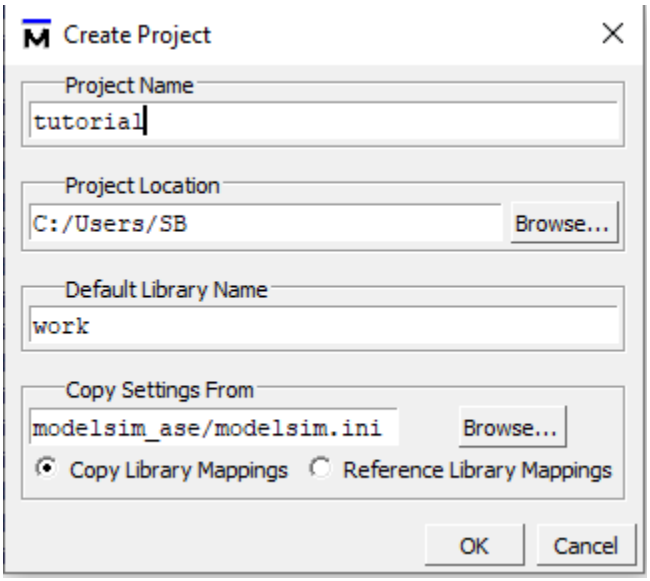
Open Modelsim/Questa, and you will be greeted by the default screen. If at any point you remove a window and feel stuck go into the layout setting in the top panel and click reset.



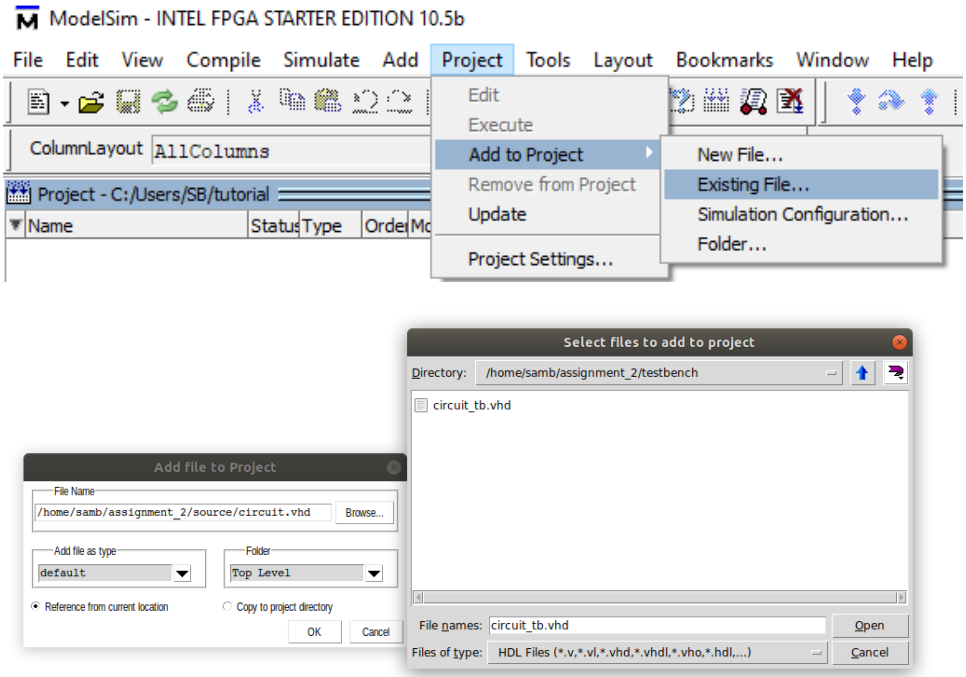
Firstly, create a project.



Put the project wherever you like, just avoid complicated path names.

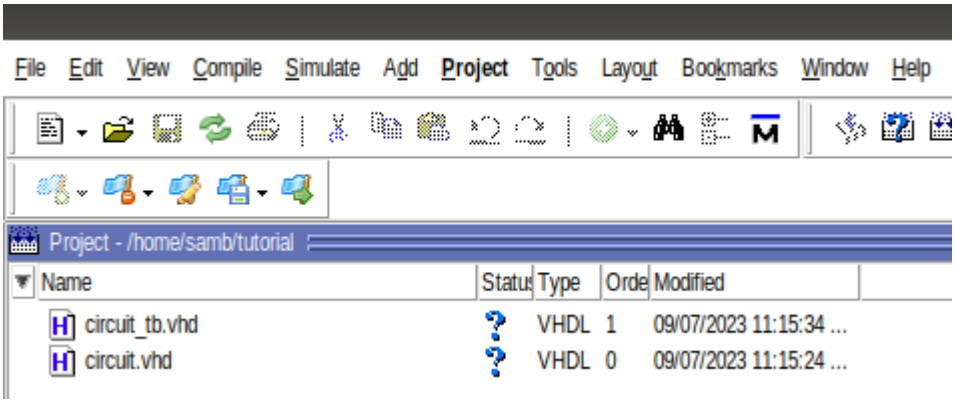


Click OK and you have a project. Close the option to add files, because you will want to learn how to do that while you are working on your project. It is accessed through project -> existing file or new files. You can add many files at once. It is not necessary to click ok more than once, but open can be clicked for multiple files.

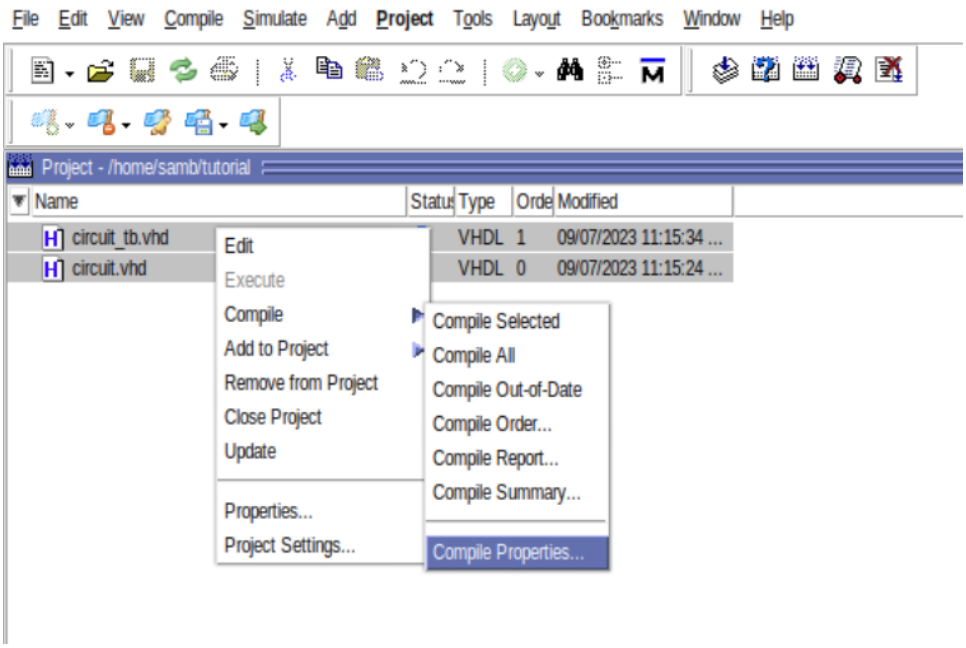


Use the existing files option and select “reference from current location”. This links Modelsim/Questa to your file and when you edit it, Modelsim/Questa will automatically update. Avoid editing in Modelsim/Questa, if you do accidentally make sure to reload the file and do not save it in Modelsim/Questa.

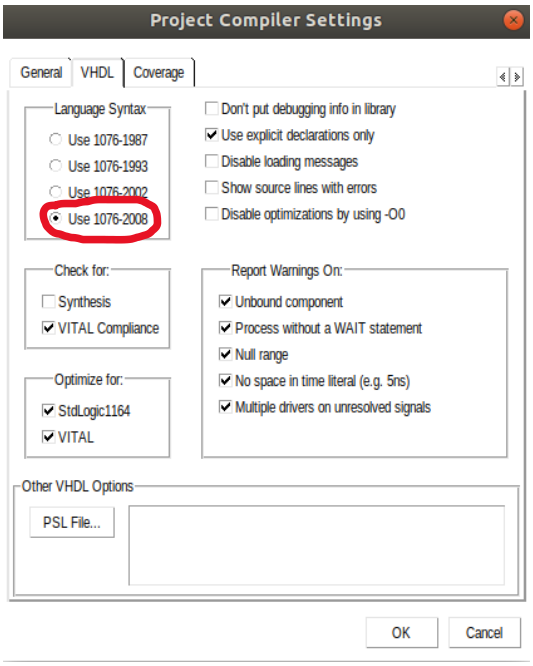
Add your files from the end of assignment 2, the circuit and circuit testbench.



All files are shown equally with ?, this means they have not yet been compiled. First let’s highlight them both with ctrl click or shift click and right click them to change both to use VHDL 2008 standard, the same as Vivado.

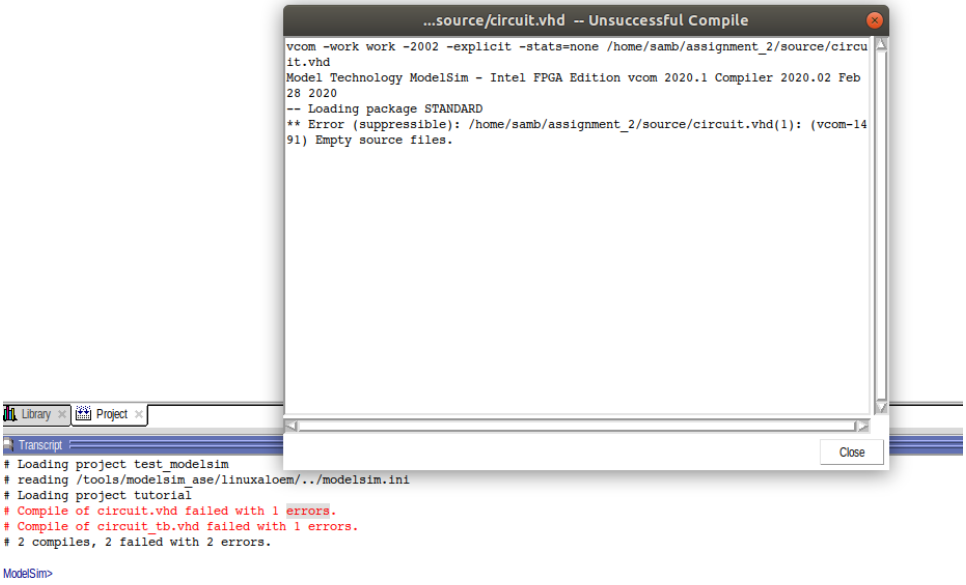


Change the project compiler settings to use the 2008 standard.

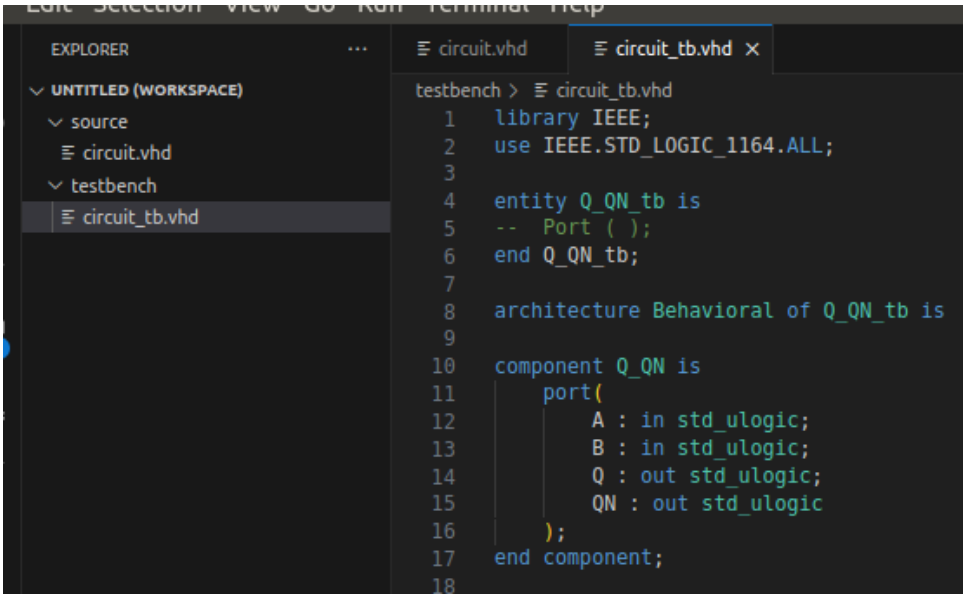


Click ok, Now right click a vhd file and select compile all.

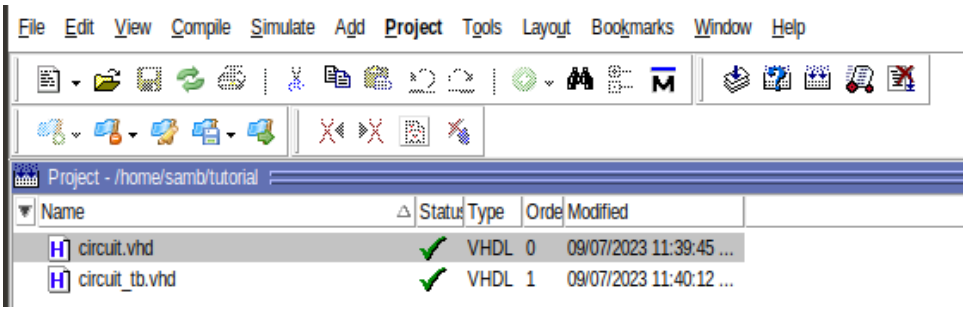
You might see some errors. They will be indicated by a red cross and in the log at the bottom the number of errors will be listed. Double click the red text and the errors will be listed alongside the cause. In my case the files are both empty.



If you have set up your Modelsim/Questa as described, you should be able to edit files, save them and immediately recompile them and hence re-simulate. This is the main advantage over Vivado which almost forces you to use their IDE. Let's try it now. Use vscode, vim or your favourite IDE with a plugin (e;g TerosHDL) that supports VHDL and use them to remove any errors in your code. Edit, compile, edit compile until the errors are gone. Here's a brief snippet of Vscode.

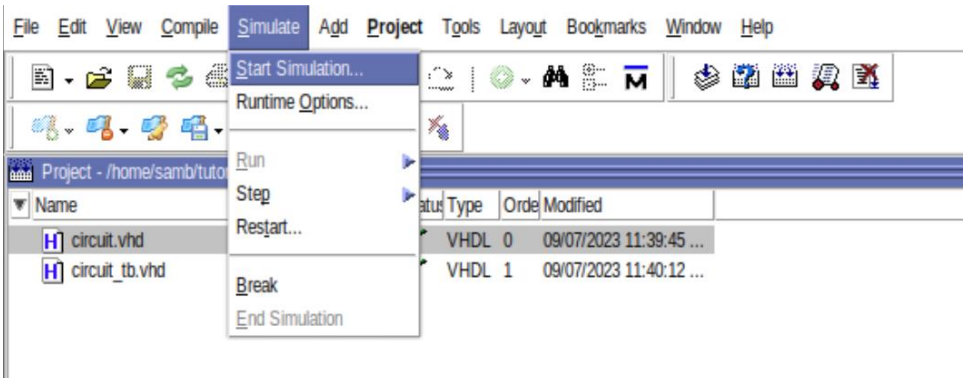


Once you are done editing, recompile the code in Modelsim/Questa. It will automatically reload the newest version of the edited file.

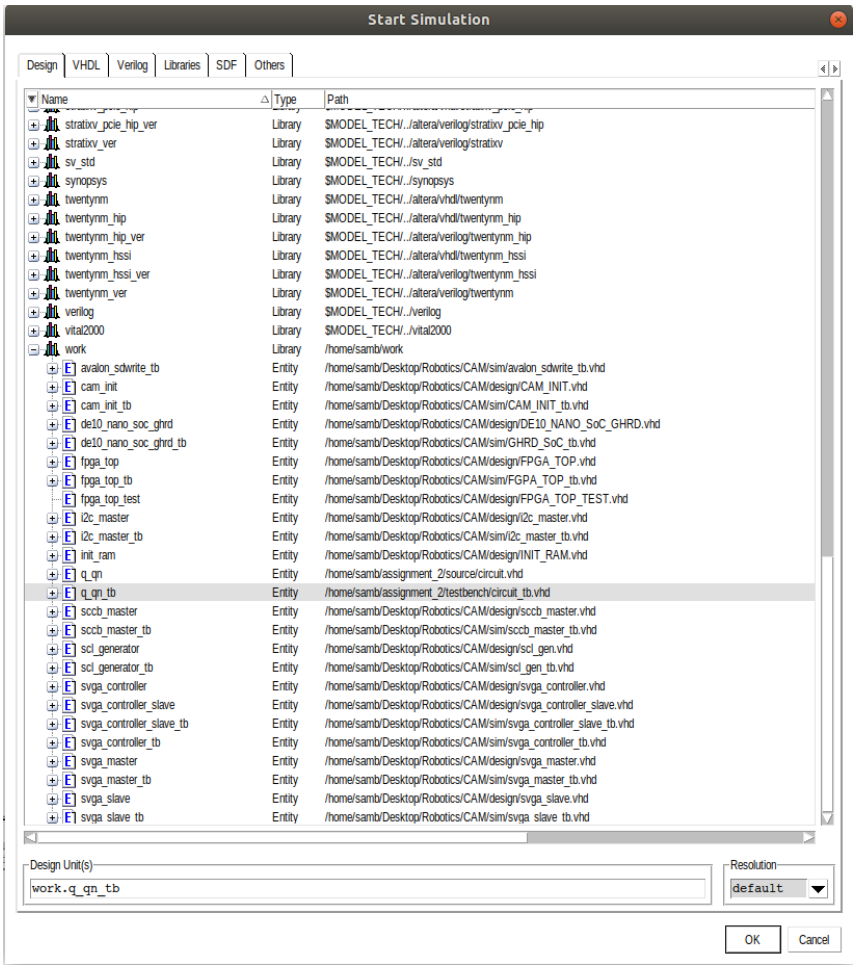


The green tick indicates it no longer has any errors. Time to simulate.

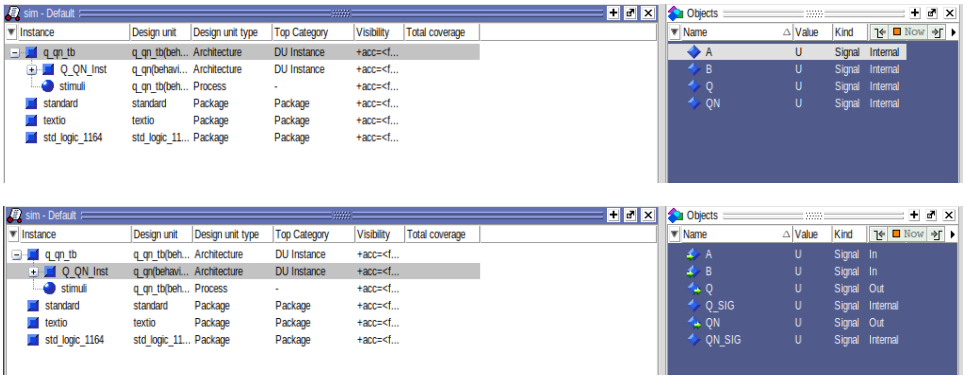
Go into the simulate tab and click start simulation.



In your library, work is the default user library, you will have your testbench listed as the name of your testbench entity. You will need to click this one and click ok to start the simulation.

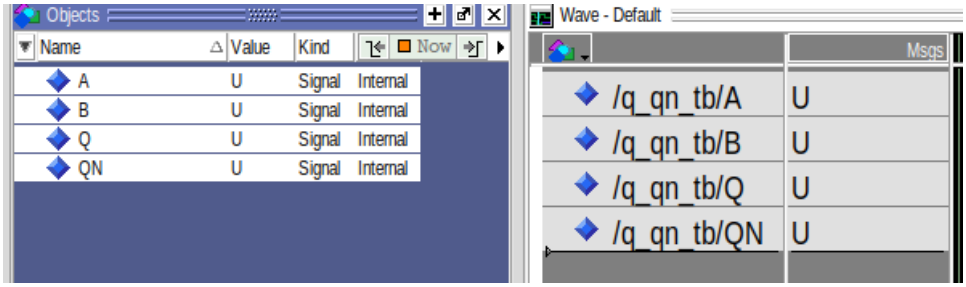


The simulation window will open up, the left window pane is a hierarchy that allows you to see signals within, entering and being output from a module, these are displayed in the middle window.

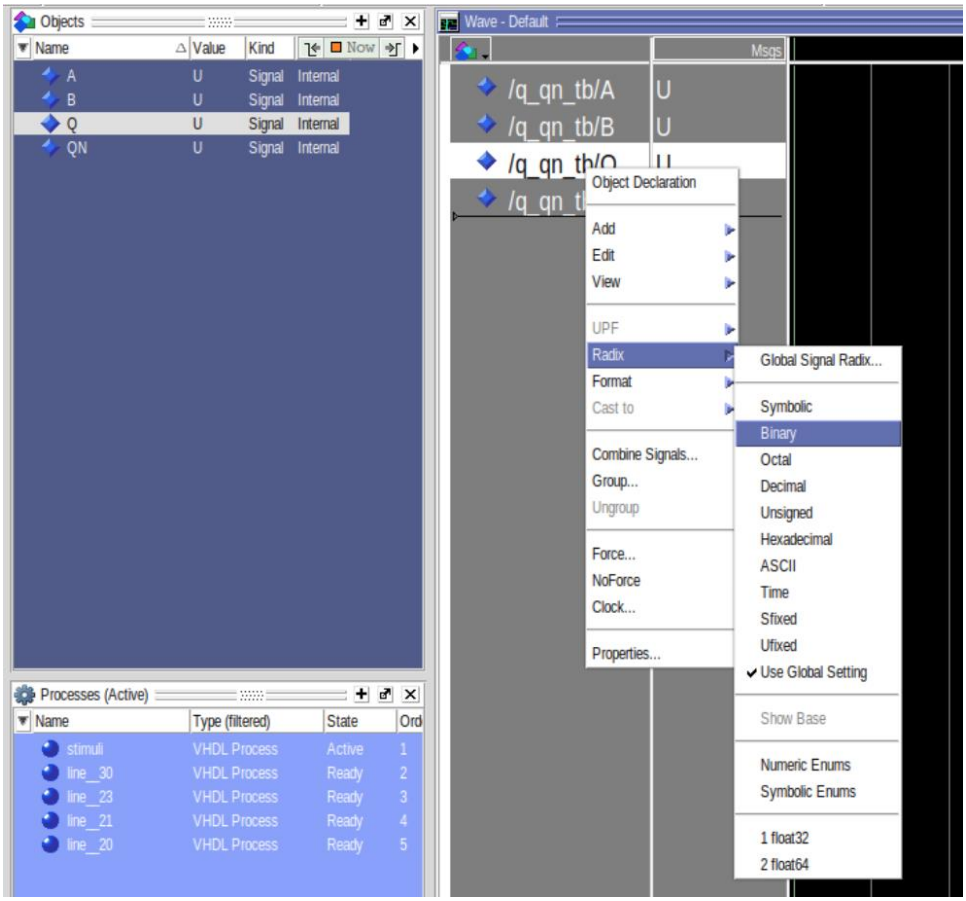


If you instantiate a component within another entity, it will be displayed hierarchically within that, you can access those signals by clicking it. The top is always the testbench. Select and drag the signals you would like to see into the wave window. Right click a signal in the wave window to change its radix. Do not change it.

*Note If you do not see the simulation window by default, right clicking a signal instead of dragging and selecting a wave related option should add the wave window back.



You can access any signal, change the representation in the waveform as a byte, hexadecimal, decimal.

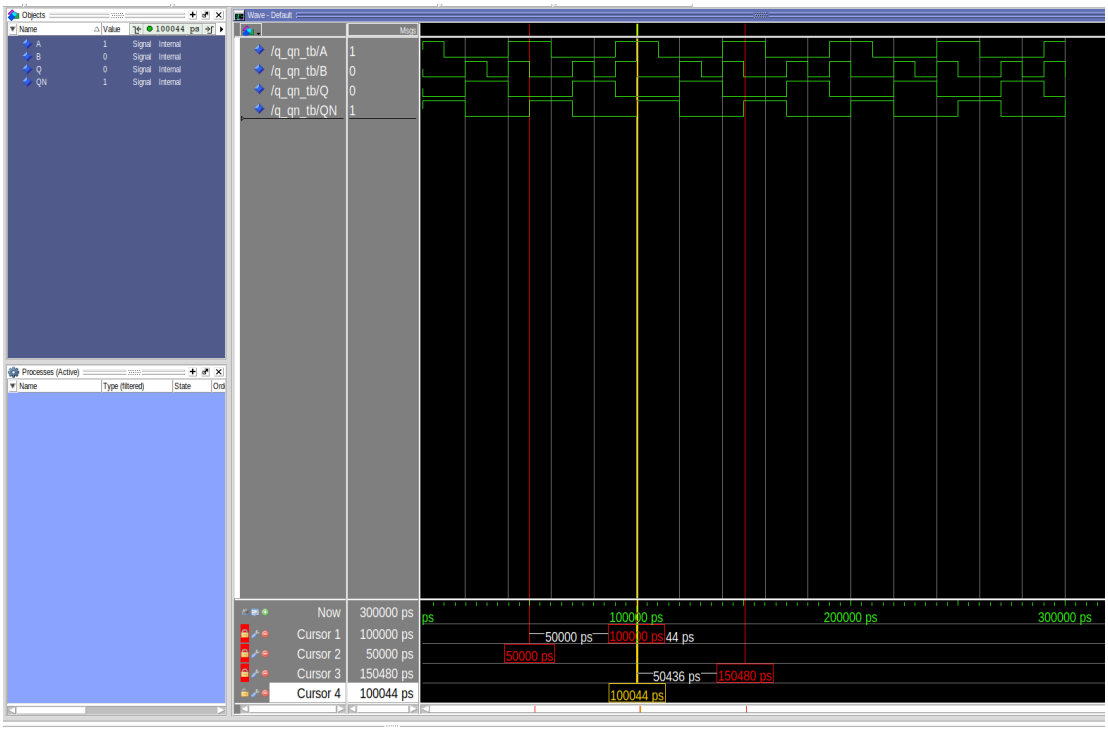


Now let's move to the simulation bar.

Hover your mouse pointer over them and read what they do, most important is run, stop, and run length.

Set run length to 50ns, then click run (the paper with an arrow).

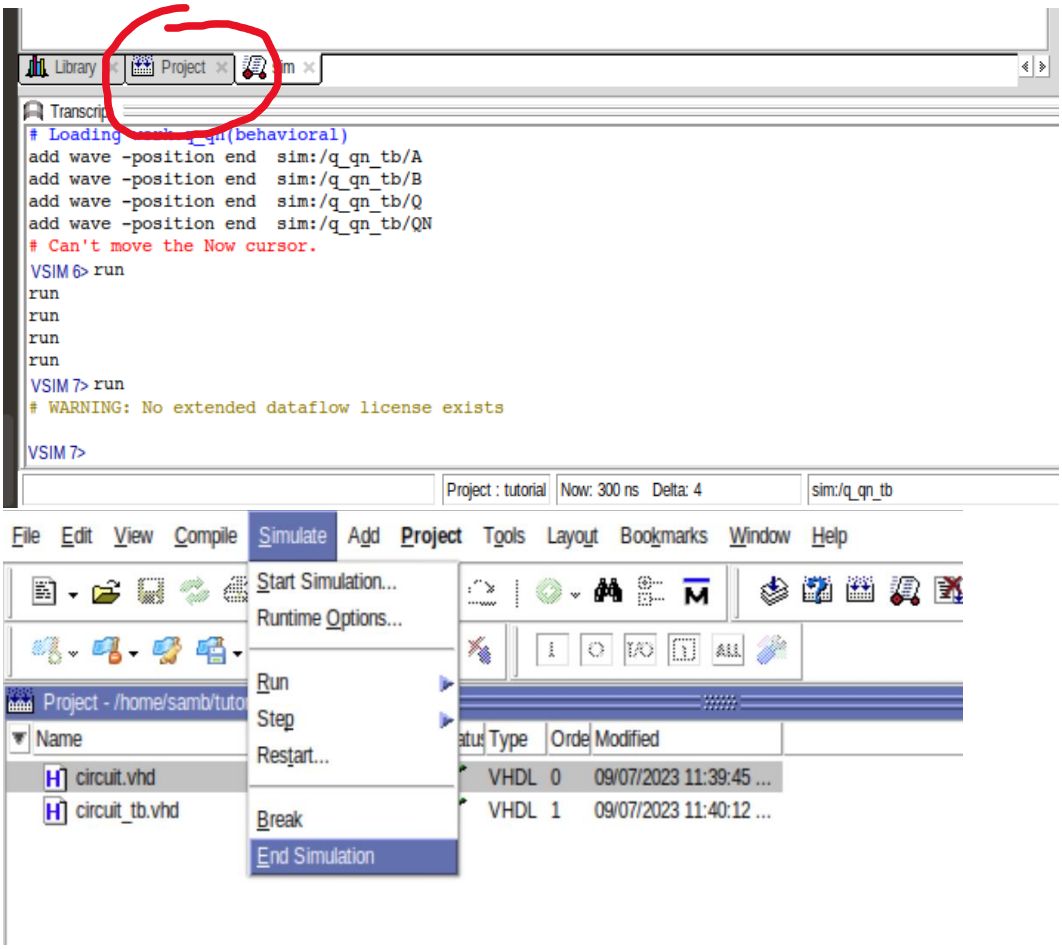
This should be completed quickly, then you can look at the waveform. If you click run multiple times the testbench you have made should automatically repeat itself.



You can click anywhere to get the value of signals at that time, and to measure the time between signals you can lock the cursor by clicking the lock and the plus to add another, at the bottom of the screen.

To escape this screen, there is a tab in the bottom left corner. In the top left of this picture where it says sim, click project. Alternatively, you can end the simulation by clicking simulation in the top toolbar and end simulation. Then in the same left corner click project. Now you are back where you started and can continue developing.

Remember, if you mess up the layout, click layout, then reset.



This concludes the basics of Modelsim/Questa.