NTNU
Department of Electronic Systems
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TFE4141 Design of digital systems 1

Assignment 2: VHDL Simulation and Synthesis

Task 1: Understanding the Delta Delay

1. Read the paper: *Time and delta-delay in VHDL* (found under *Learning materials* on *Blacboard*).
2. Explain in your own words what happens in a simulation cycle. You may illustrate your explanation with a flow diagram. Keep your answer short.
3. Explain what happens to signals that are assigned values with and without **explicit delays**.

Task 2: Go through the Tutorial

This tutorial is meant to guide you through the design flows of the Vivado Design Suite and get you familiarized with the workspace.

1. Go through Lab 2 of the tutorial attached to this assignement. Start by reading Page 4 through 7 and then jump to Page 21.
2. Answer the questions in Task 3 when you have completed the tutorial.

Task 3: Questions from the Tutorial

1. How many flip-flops are used in the design?
2. How many LUTs are used in the design?
3. What is a LUT?
4. What is the total on-chip power?
5. Mention things you can explore in the flowing steps of the design flow:
   - Simulation
   - Synthesis
   - Implementation
6. Hand in answers to the questions.

Task 4: Simulation in Vivado with delay

Given the following two concurrent processes in an architecture:

```
Q <= A nor QN;
QN <= B nor Q;
```

and the following stimuli:

```
A <= '1' ; B <= '0' ;
wait for 10 ns ;
A <= '0' ;
wait for 10 ns ;
B <= '1' ;
wait for 10 ns ;
B <= '0' ;
wait for 10 ns ;
B <= '1' ; A <= '1' ;
```

1. Make a new project in Vivado as you did in the tutorail and write VHDL-code with entity and architecture that implements the processes Q and QN. Write a testbench which applies the given stimuli to this entity. Use the type **std_ulogic** (described below).
2. Simulate your code in Vivado using Behavioral Simulation. Are the results as expected? Does the simulation stop after all stimuli have been applied and the two processes Q and QN are suspended, or do you experience oscillations like in the paper on *Time and delta-delay* discussed in Task 1?
3. What would the simulation look like if Vivado did not use VHDL's model of time, but instead executed the two processes sequentially (first Q and then QN) each time the stimuli changed?
4. The waveform viewer in Vivado does not show individual delta cycles, only the final values after each change of stimuli (try using Questa instead if you want to see individual delta cycles). To see individual realistic delays, simulate your code in Vivado using Post-Synthesis Timing Simulation and Post-Implementation Timing Simulation. Zoom in at 20 ns in the simulation waveforms. Explain what you see in each case.

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Use the type std_ulogic which is defined as follows:

```
TYPE std_ulogic IS ( 'U',  -- Uninitialized
                     'X',  -- Forcing Unknown
                     '0',  -- Forcing 0
                     '1',  -- Forcing 1
                     'Z',  -- High Impedance
                     'W', -- Weak Unknown
                     'L',  -- Weak 0
                     'H',  -- Weak 1
                     '-',  -- Don't care );
```

Note: To make this type available you must include the following in your code:

```
library ieee ;
use ieee.std_logic_1164.all ;
```

These code lines must be written above the entity and architecture declaration.
When a simulation starts, a signal not given a specific initialization value, will be assigned the first value in the list, in this case '**U**' – (**U**ninitialized). Later on the signal value will typically change into '**X**', '**1**' or '**0**'.