NTNU
Kunnskap for en bedre verden

Faculty of Information Technology and Electrical Engineering

TFE4152 - Term Project MIDTERM REPORT

Memory Unit: 8x8 bit RAM

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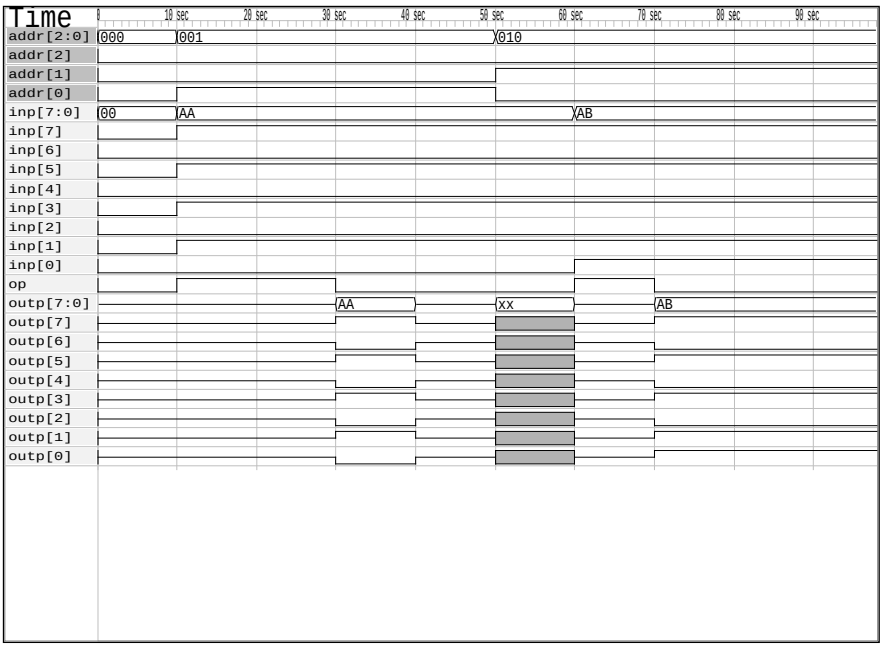
1 Brief reflection

"A brief reflection on your progress so far, and an overview of the remaining work. Which circuits do you have to design/implement? Which simulations are you planning to run? Are there any parts of the work that you have already done that you plan to improve/change?"

We have focused extensively on Verilog, and thus implemented the 8x8 memory completely and done testing on its functionality. We started out with a different design and have iterated on it several times. The architecture is close, but somewhat different, to the specifications requested, since the task says "should" and not "shall". Here is a testbench for the entire 8x8 memory:



We have however yet to implement the FSM. And after that is implemented we will set up a testbench that completes all of the digital circuitry testing, such as writing our own initials in ASCII into the memory.

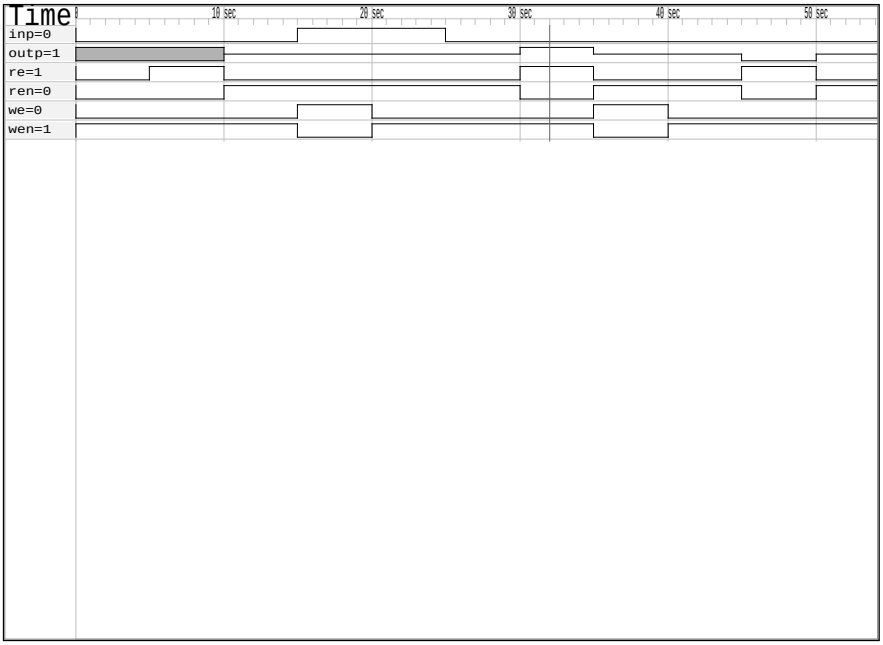
When it comes to AimSPICE we are somewhat stuck, as both of us have done the bare minimum of AimSPICE-ing to pass the exercises thus far, and will do more AimSPICE after consulting the TAs. What an ancient language and editor that language has. Our frustration with PainSPICE is immesureable, and my week is ruined. Had there just been somewhat of a linter available. Ignore our rants for now, and make sure to send as many TAs to øvingstime as possible, and we will tame the beast known as AimSPICE before the project deadline.

We have however taken analog design principles into account in our digital design, so the analog simulations should perform well. We are a bit worried about how fast the bitcell flips values, but that is all.

2 Testbench bitcell

Testbench for your chosen bitcell, where you have simulated it's functionality on structural level using only Boolean gates and interconnect using Verilog and ActiveHDL.

Here is the testbench we used for the bitcell:



We designed our bitcell like the latch with two NOT gates feeding each others output to the others input that was introduced in the lecture Wednesday 16/10. We made sure to include transmission gates on the input, on the backpropagation and on the output. Thus the output is high resistance when not reading, and we don't need any MUX to choose which byte to read or anything like that, but just read from a shared databus.

That means we strayed somewhat from the design specifications, which say they would like only 4 inputs, but we desided that taking these inputs would reduce the total amount of transistors needed, since inverting control signals could be shared between all bitcells.

We have implemented it all in Verilog (not System Verilog) in VSCode, and compiled with Icarus Verilog.

3 Aimspice

Demonstration of the functionality of your bitcell using AIMSpice. Demonstrate the functionality of the bitcell for the TT, FF, SS, SF and FS corners, for -20, 27, 50 degrees Celsius.

We are not very close to getting this to work yet, but are working on it.

4 Contributions

A short description of each group member's contribution to the work.

Both members have been working together at campus 6 hours per week since the project started. Sebastian learned Verilog somewhat on his own and kickstarted the Verilog programming on our second work session. Lorang has drawn all circuits on his tablet and implemented updates to the Verilog code between work sessions. Right now, Sebastian is writing this midterm report whilst Lorang has gone to the TA session in order to learn more about AimSPICE for us to implement it sooner rather than later. Both members have been focused on project work when we have our work sessions.