Aditya Kommi ECE 448
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Lab 1

## Tasks:

1. Write a testbench capable of verifying Lab1 core, using all combinations of inputs A and B.

In testbench file.

2. Write a short report describing all discrepancies between the above specification and the faulty model.

All discrepancies happened in Lab1_psm_1. In MODE = 0, Errors 1-10 were missing outputs with B = 1 calculating div16 instead of div8 and B=2 calculating div26 instead of div13. In Mode=1, the model incorrectly rounded the B value to up to the nearest odd number. This caused 197 errors in the sequential operation. In total, there were 209 errors.

## Deliverables:

1. VHDL code of the testbench.

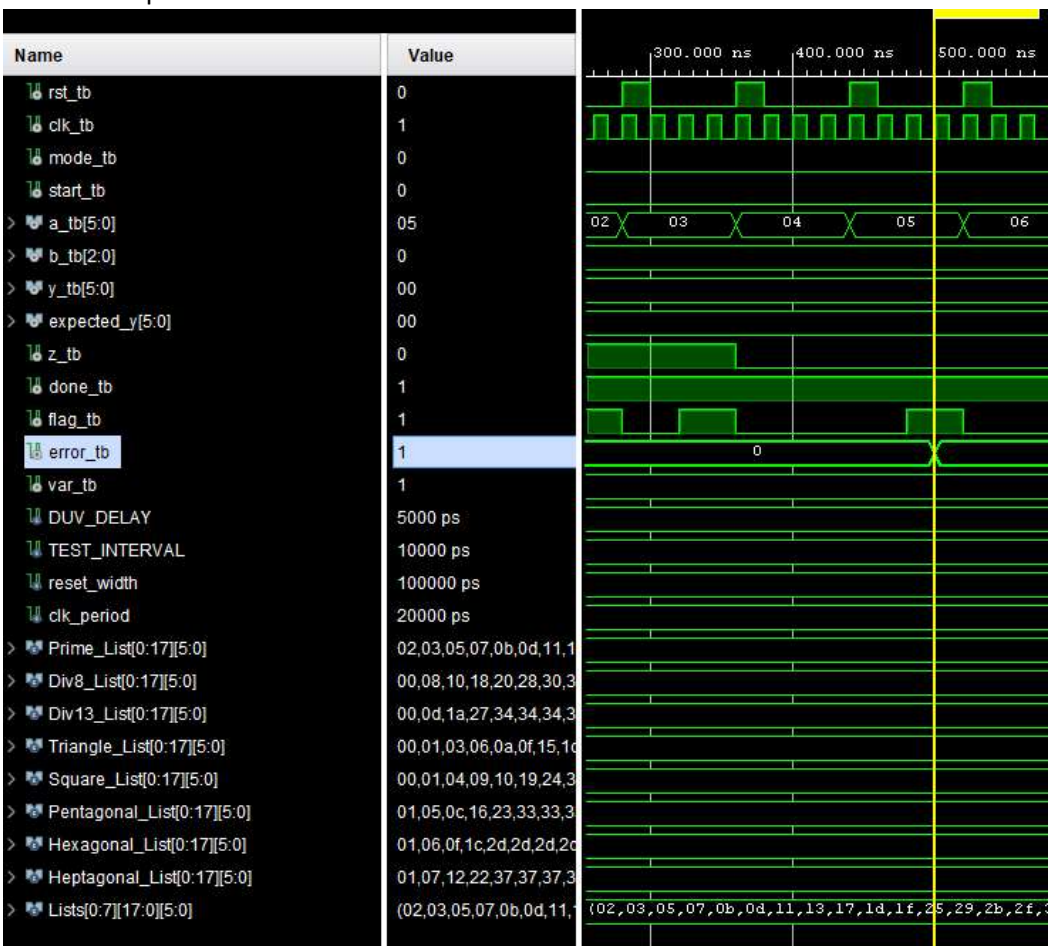
In the testbench file.

2. Parts of the waveforms obtained by running your testbench in the Vivado Simulator (in the PDF format) demonstrating 10 discrepancies between actual outputs and expected outputs.

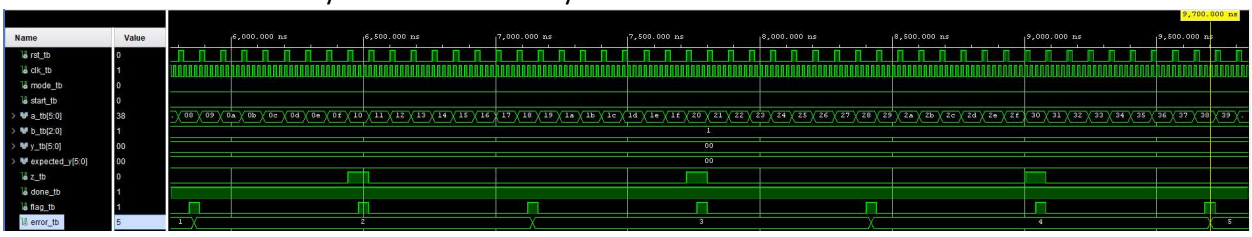
Both Waveforms are in the files as wcfg files.

DUT: Lab1_psm_1

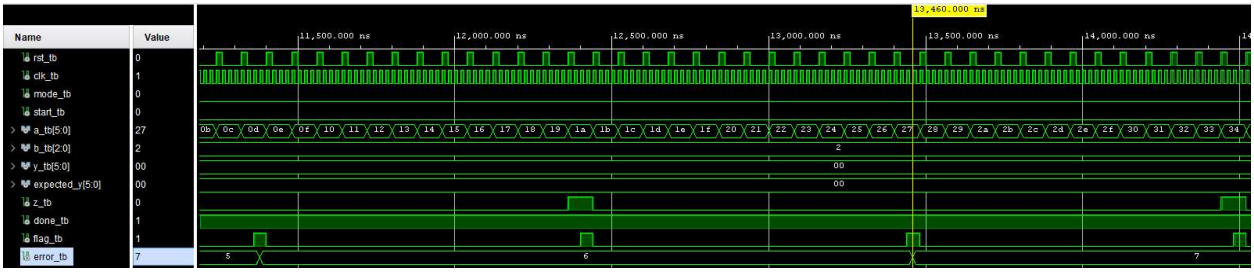
Error 1: 5 is prime



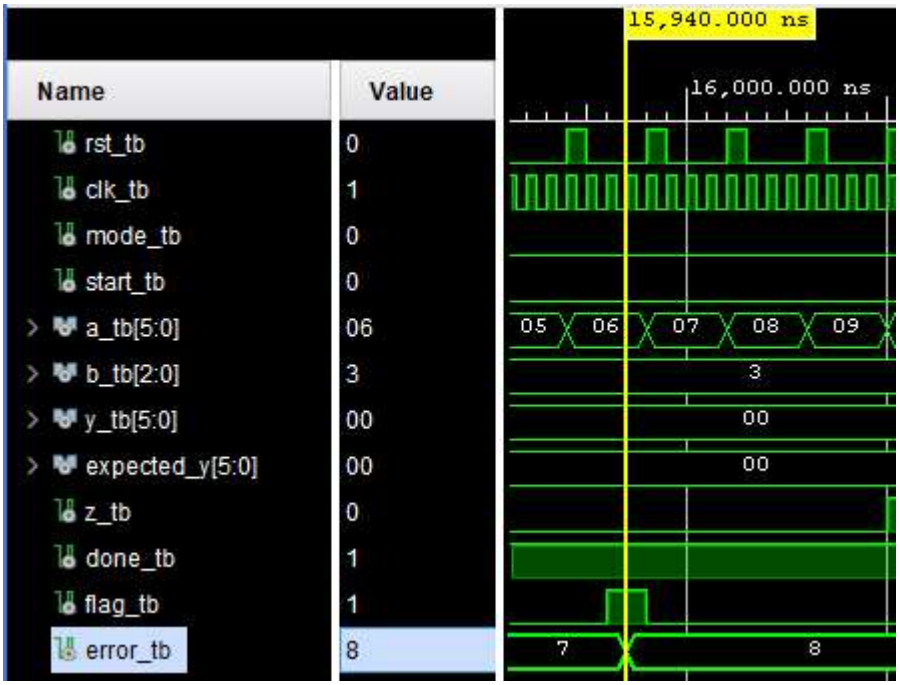

Errors 2-5: Calculated div by 16 instead of div by 8



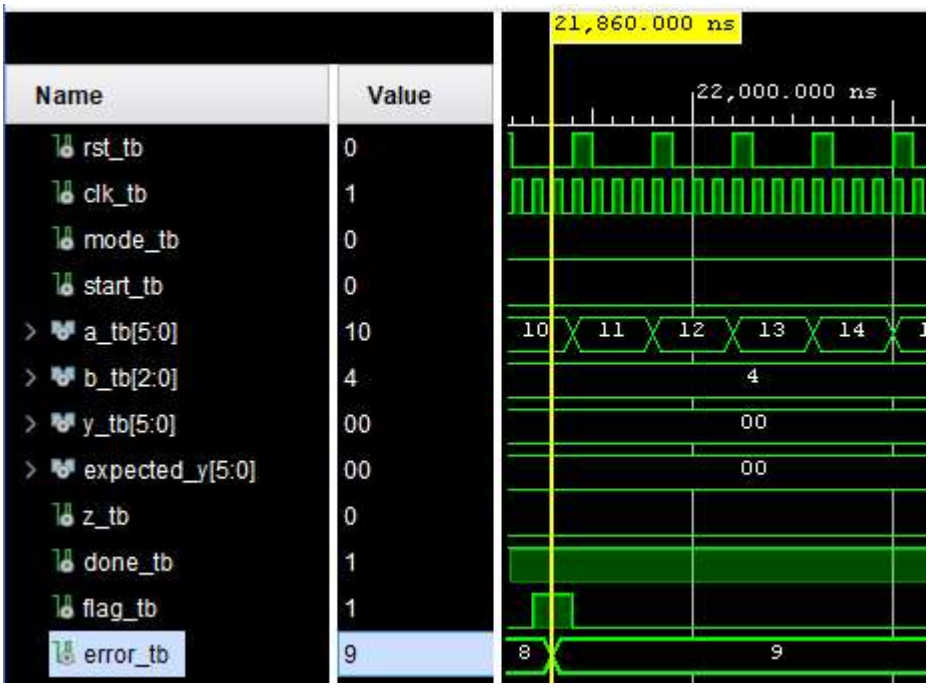
Errors 6-7: Calculated div by 26 instead of div by 13



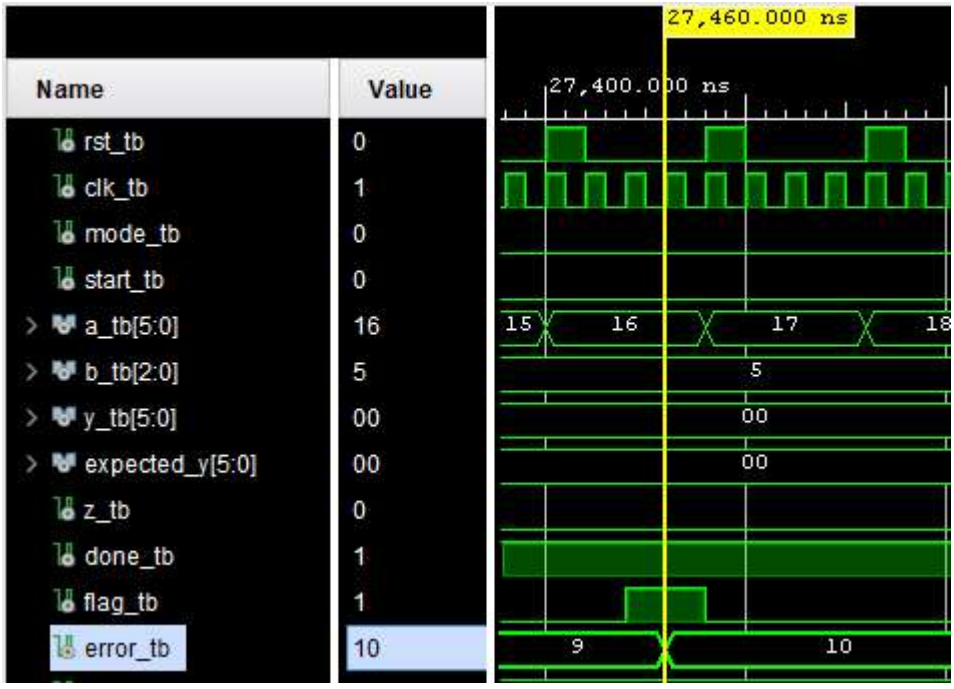
Error 8: 6 is a Triangular Number



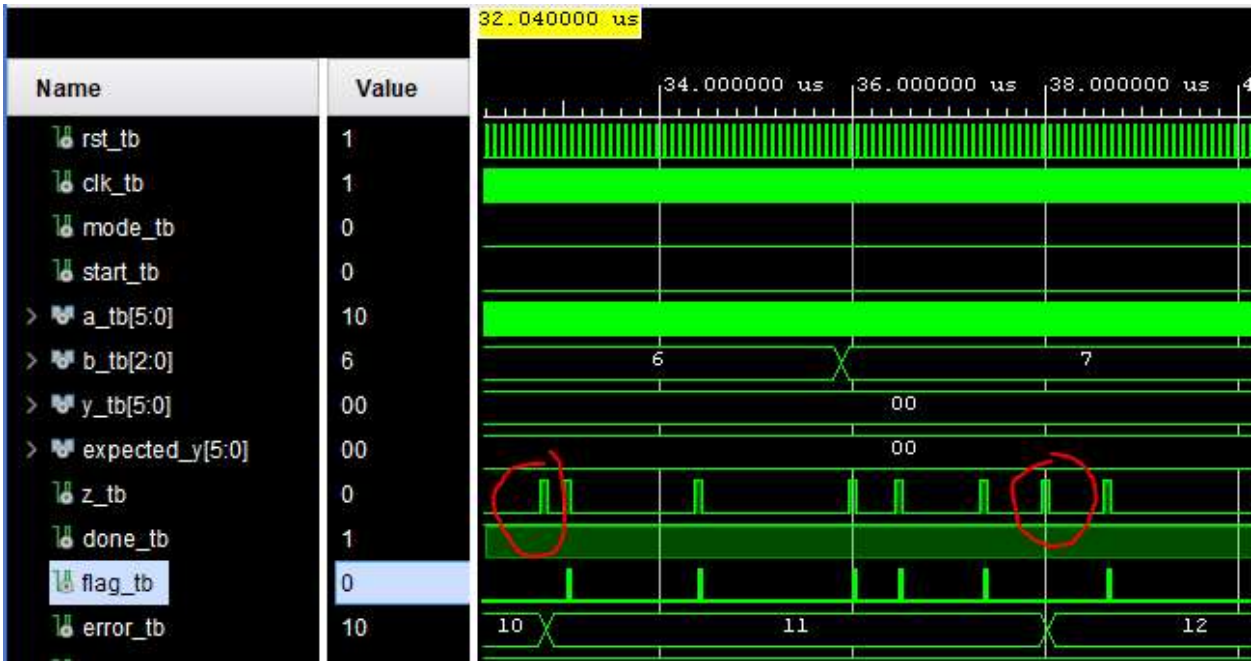

Error 9: 16 is a Square Number



Error 10: 22 is a Pentagonal Number




Errors 11 & 12 : Extra output

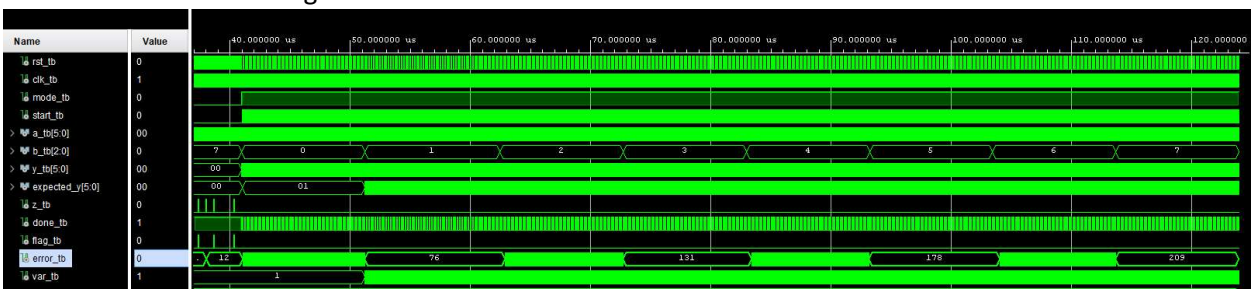


Errors 13-76: Evaluating as B = 1 instead of B = 0

Errors 77-131: Evaluating as B = 3 instead of B = 2

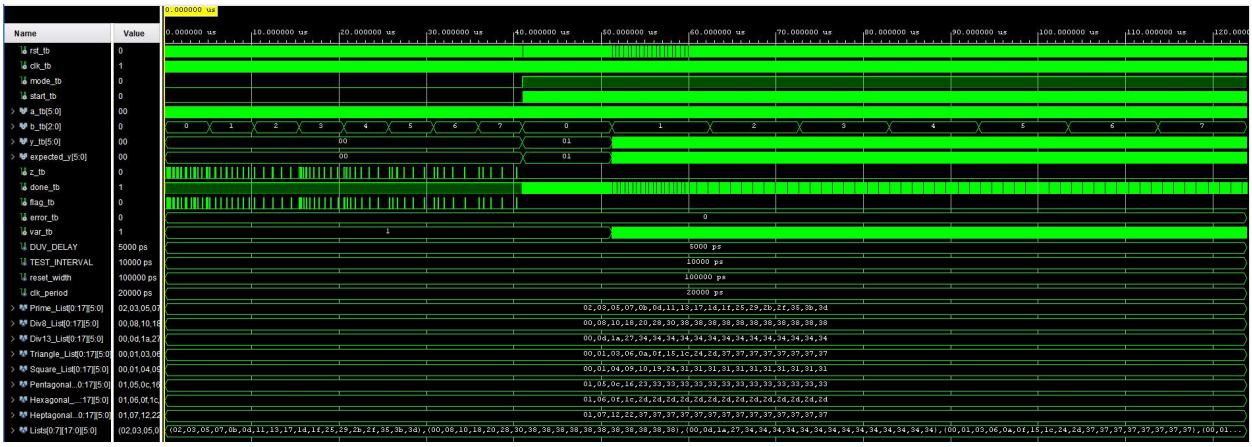
Errors 132-178: Evaluating as B = 5 instead of B = 4

Errors 179-209: Evaluating as B = 7 instead of B = 6




DUT: Lab1_psm_2

No Errors




3. All messages written by the testbench to the standard output.

In Lab1_psm_1_output_log.txt and Lab1_psm_2_output_log.txt files

4. Report describing all discrepancies you have managed to detect. For MODE=1, try to determine what is a common feature of all inputs giving incorrect outputs.

Above in Tasks #2.