Lab 1
Developing and Using Testbenches

Develop a testbench, written in VHDL, to be used to verify the operation of the Lab1 core, specified below:

Interface:

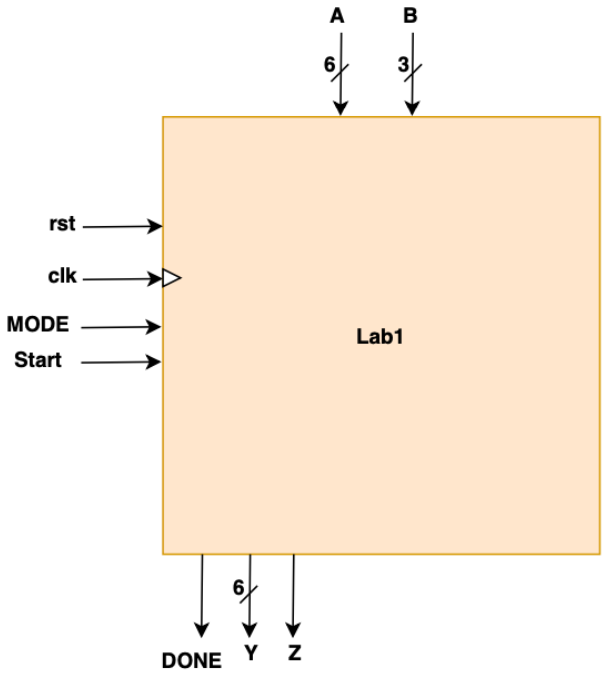

Table of input/output ports:

Name	Mode	Width	Meaning
rst	INPUT	1	Asynchronous reset
clk	INPUT	1	Clock
MODE	INPUT	1	Circuit mode: 0 – Combinational 1 – Sequential
Start	INPUT	1	Start of the sequential operation in MODE 1
A	INPUT	6	For Mode 0: Input to the combinational operation defined by B For Mode 1: Input A to the sequential operation $Y=A^B$ mod 64
B	INPUT	3	For Mode 0: Operation to be performed on A, as defined in the table below For Mode 1: Input B to the sequential operation $Y=A^B$ mod 64

Y	OUTPUT	6	Output of the sequential operation $Y=A^B \bmod 64$
Z	OUTPUT	1	Output of the combinational operation
DONE	OUTPUT	1	Indicator that the output Z is valid in MODE 0 and the output Y is valid in MODE 1.

If **MODE=0** (Combinational mode), then A is the main input and B describes an operation (OP), to be performed on A, as defined below:

A	**B (OP)**	**Operation described using words**
Prime	000	Z = 1 if A is Prime
Divisible by 8	001	Z = 1 if A is divisible by 8
Divisible by 13	010	Z = 1 if A is divisible by 13
Triangular Number	011	Z = 1 if A is a Triangular Number
Square Number	100	Z = 1 if A is a Square Number
Pentagonal Number	101	Z = 1 if A is a Pentagonal Number
Hexagonal Number	110	Z = 1 if A is a Hexagonal Number
Heptagonal Number	111	Z = 1 if A is a Heptagonal Number

In this mode, Y should be always set to 0 and DONE to 1.

For the definitions of Triangular, Square, Pentagonal, Hexagonal, and Heptagonal numbers, please see:
https://en.wikipedia.org/wiki/List_of_types_of_numbers#Types_of_integer

If **MODE=1** (Sequential mode), the core should wait for an active value of the **Start** signal. When this signal is asserted, the core should calculate $Y=A^B \bmod 64$. When the result is ready, the DONE signal should be asserted for one clock cycle.
In this mode, Z should be always set to 0.

Examples:
A = 2 (000010_2), B = 5 (101_2), then Y should be $2^5 \bmod 64 = 32$ (100000_2).
A = 4 (000100_2), B = 4 (100_2), then Y should be $4^4 \bmod 64 = 0$ (000000_2).
Z should be set to 0 in both cases.

Your task is to write a testbench that can be used to verify the provided two post-synthesis models, Lab1_psm_1.vhd and Lab1_psm_2.vhd for agreement with the above

specification. **One** of the provided models is **correct**. The other model contains multiple **discrepancies** compared to the specification.

These discrepancies may have, for example, the following forms:

1. Incorrect output Z for a subset of allowed values of A and B in the combinational mode.
2. Incorrect output Y for a subset of allowed values of A and B in the sequential mode.

Your task is to find which model is correct and then document all discrepancies detected in the other model.

Your testbench should automatically compare actual outputs with expected outputs for

1. MODE=0 and MODE=1
2. All values of the inputs A and B.

Your testbench should also report when a discrepancy is found and **count** a total number of errors.

Tasks:

1. Write a testbench capable of verifying Lab1 core, using all combinations of inputs A and B
2. Write a short report describing all discrepancies between the above specification and the faulty model.

Deliverables:

1. VHDL code of the testbench.
2. Parts of the waveforms obtained by running your testbench in the Vivado Simulator (in the PDF format) demonstrating **10** discrepancies between actual outputs and expected outputs.
3. All messages written by the testbench to the standard output.
4. Report describing all discrepancies you have managed to detect. For MODE=1, try to determine what is a common feature of all inputs giving incorrect outputs.

Important Dates

	Tuesday Section	Wednesday Section	Friday Section
Hands-on Session and Introduction to the Experiment	02/02/2021	02/03/2021	02/05/2021
Deliverables Due	**02/12/2021 8:10 AM**	**02/12/2021 8:10 AM**	**02/12/2021 8:10 AM**
Q&A	**TBD**	**TBD**	**02/12/2021 8:40-11:20am**