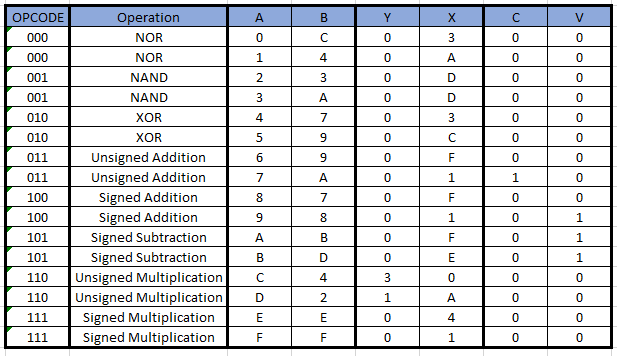
Tasks:

1. Supplement missing values of expected outputs in Table 4.

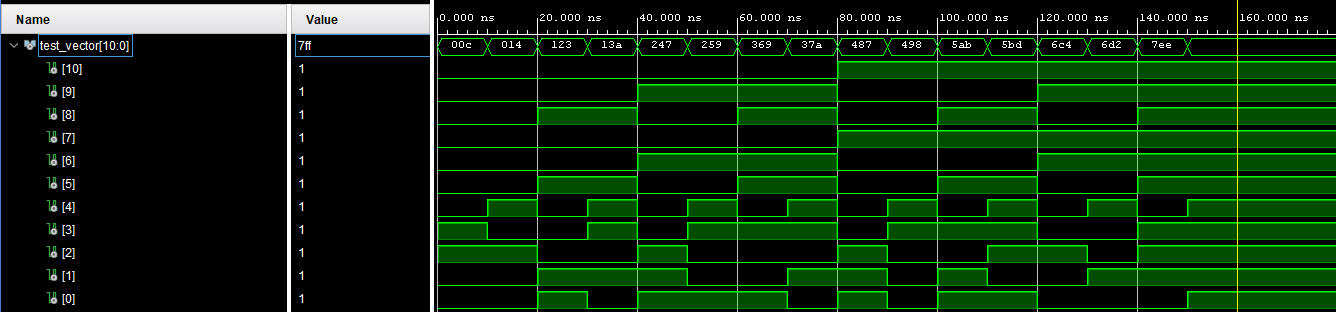


2. Develop VHDL code of the testbench.

In testbench file.

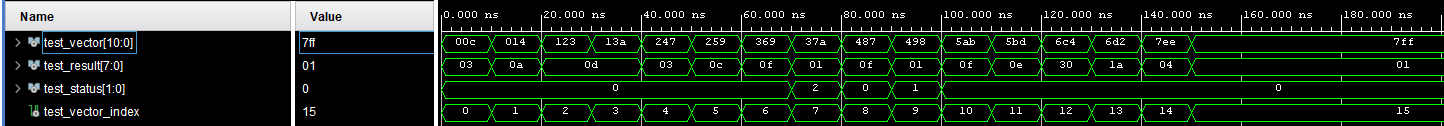
3. Verify the correctness of input waveforms for the inputs OPCODE, A, and B generated by your testbench.

The input waveforms are correct.

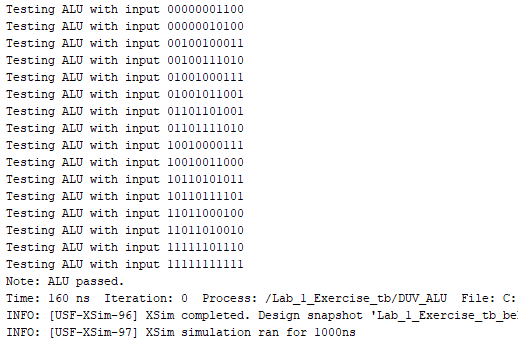


4. Add an instantiation of ALU, compile your testbench together with a. ALU\_psm\_1.vhd b. ALU\_psm\_2.vhd and verify the operation of each model separately.

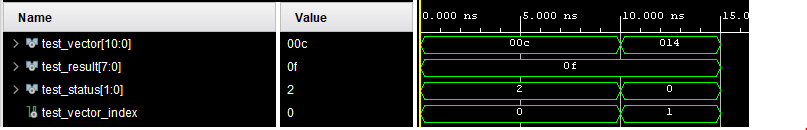
a. ALU\_psm\_1



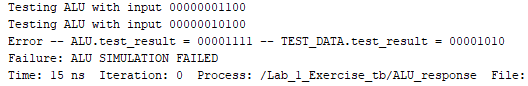
Tcl Console Log:



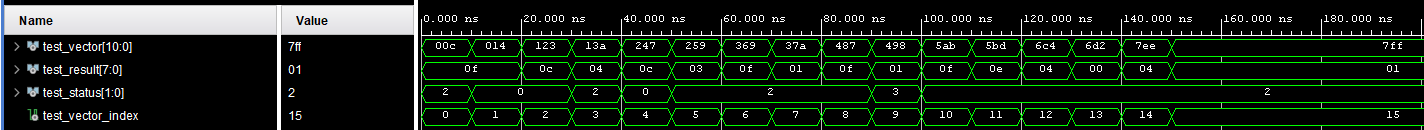
b. ALU\_psm\_2



Tcl Console Log:



With Test Result of (1 NOR 4) changed:



5. Determine a list of at least 3 errors in the faulty model.

The faulty ALU is ALU\_psm\_2.

1. Opcode 0 NAND is switched with Opcode 1 NOR.
2. Opcode 2 XOR is replaced with NOT(A XOR B).
3. Opcode 6 Unsigned Multiplication is replaced with AND.
4. The ALU is using the C indicator outside of unsigned operations and signed operations respectively.