LAB 3 Report

Name: Donald Maze-England

UT EID: dsm2588

Section: 15465

Checklist:

Part 2 -

i. Constraint File (Just the uncommented portion)

Part 3 -

ii. Truth Table of the function
iii. K-maps showing minimization of the logic functions (outputs)
iv. Algebraic expression of the minimized logic functions (outputs)
v. Verilog codes of module and testbench for structural modelling
vi. Simulation waveform for structural modelling
vii. Constraint File (Just the uncommented portion)

Note → *The Verilog codes and the uncommented portions of the constraint files should be copied in your lab report and the actual Verilog (.v) and Constraint (.xdc) files need to be zipped and submitted as well on Canvas. You are not allowed to change your Verilog codes after final submission as the TAs may download the submitted codes from Canvas during checkouts. For the truth Table, K-maps minimizations and algebraic expressions, you are free to draw them on paper and then put the pictures in your lab report, but please make sure it is legible for the TAs to grade it properly.*

Part 2:

Constraints File:

```
set_property PACKAGE_PIN V17 [get_ports {cd}]
        set_property IOSTANDARD LVCMOS33 [get_ports {cd}]
set_property PACKAGE_PIN V16 [get_ports {bd}]
```

```
        set_property IOSTANDARD LVCMOS33 [get_ports {bd}]
set_property PACKAGE_PIN W16 [get_ports {ad}]
        set_property IOSTANDARD LVCMOS33 [get_ports {ad}]


set_property PACKAGE_PIN W13 [get_ports {ed}]
        set_property IOSTANDARD LVCMOS33 [get_ports {ed}]


set_property PACKAGE_PIN E19 [get_ports {d0}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d0}]
set_property PACKAGE_PIN U19 [get_ports {d1}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d1}]
set_property PACKAGE_PIN V19 [get_ports {d2}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d2}]
set_property PACKAGE_PIN W18 [get_ports {d3}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d3}]
set_property PACKAGE_PIN U15 [get_ports {d4}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d4}]
set_property PACKAGE_PIN U14 [get_ports {d5}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d5}]
set_property PACKAGE_PIN V14 [get_ports {d6}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d6}]
set_property PACKAGE_PIN V13 [get_ports {d7}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d7}]
```

Part 3:

Truth Table:

Decimal	A	B	C	D	a	b	c	d	e	f	g	dp
0	0	0	0	0	0	0	0	0	0	0	1	1
1	0	0	0	1	1	0	0	1	1	1	1	1
2	0	0	1	0	0	0	1	0	0	1	0	1
3	0	0	1	1	0	0	0	0	1	1	0	1
4	0	1	0	0	1	0	0	1	1	0	0	1
5	0	1	0	1	0	1	0	0	1	0	0	1
6	0	1	1	0	1	1	0	0	0	0	0	1
7	0	1	1	1	0	0	0	1	1	1	1	1
8	1	0	0	0	0	0	0	0	0	0	0	1
9	1	0	0	1	0	0	0	1	1	0	0	1
greater than 9					1	1	1	1	1	1	1	1
…				…	…	…	…	…	…	…	…	…

K Maps:

a:

CD \ AB	00	01	11	10
00	0	1	1	0
01	1	0	1	0
11	0	0	1	1
10	0	1	1	1

a = A'B'C'D+A'BD'+AB+AC

b:

CD \ AB	00	01	11	10
00	0	0	1	0
01	0	1	1	0
11	0	0	1	1
10	0	1	1	1

b = AC+AB+BC'D+BCD'

c:

CD \ AB	00	01	11	10
00	0	0	1	0
01	0	0	1	0
11	0	0	1	1
10	1	0	1	**1**

c = AB+ AC+B'CD'

d:

CD \ AB	00	01	11	10
00	0	1	1	0
01	1	0	1	1
11	0	1	1	1
10	0	0	1	1

d = AB + AC+AD+BCD+BC'D'+B'C'D

e:

CD \ AB	00	01	11	10
00	0	1	1	0
01	1	1	1	1
11	1	1	1	1
10	0	0	1	1

e = D+BC'+AC

f:

CD \ AB	00	01	11	10
00	0	0	1	0
01	1	0	1	0
11	1	1	1	1
10	1	0	1	1

f = CD+AB+AC+A'B'D+B'CD'

g:

CD \ AB	00	01	11	10
00	1	0	1	0
01	1	0	1	0
11	0	1	1	1
10	0	0	1	1

g = AB+AC+BCD+A'B'C'

Minimized Equations:

a = A'B'C'D+A'BD'+AB+AC
b = AC+AB+BC'D+BCD'
c = AB+ AC+B'CD'
d = AB + AC+AD+BCD+BC'D'+B'C'D
e = D+BC'+AC
f = CD+AB+AC+A'B'D+B'CD'
g = AB+AC+BCD+A'B'C'

Verilog Code For 7 Segment Display:

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 02/21/2018 09:19:49 PM
// Design Name:
// Module Name: 7SegmentDisplay
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module SegmentDisplay(
    input A,
    input B,
    input C,
    input D,
    output a,
    output b,
    output c,
    output d,
    output e,
    output f,
    output g,
    output dp,
    output AN0,
    output AN1,
    output AN2,
    output AN3
    );
```

```
    //wires for not gates
    wire A_not, B_not, C_not, D_not;
    //wire for and gates
    wire AnBnCnD, AnBDn, AB, AC, BCnD, BCDn, BnCDn, AD, BDn, BC, BnCnD, BCn, CD, AnBnD, BCD,
AnBnCn, BCnDn;
    //register to transmit a 1 constantly
    reg sendOne = 1'b1;
    //register to transmit a 0 constantly
    reg sendZero = 1'b0;

    //not gates
    not notA (A_not, A);
    not notB (B_not, B);
    not notC (C_not, C);
    not notD (D_not, D);

    //instantiating and gates as needed by the truth table
    and and_AnBnCnD (AnBnCnD, A_not, B_not, C_not, D);
    and and_AnBDn (AnBDn, A_not, B, D_not);
    and and_AB (AB, A, B);
    and and_AC (AC, A, C);
    and and_BCnD (BCnD, B, C_not, D);
    and and_BCDn (BCDn, B, C, D_not);
    and and_BnCDn (BnCDn, B_not, C, D_not);
    and and_AD (AD, A, D);
    and and_BDn (BDn, B, D_not);
    and and_BC (BC, B, C);
    and and_BnCnD (BnCnD, B_not, C_not, D);
    and and_BCn (BCn, B, C_not);
    and and_CD (CD, C, D);
    and and_AnBnD (AnBnD, A_not, B_not, D);
    and and_BCD (BCD, B, C, D);
    and and_AnBnCn (AnBnCn, A_not, B_not, C_not);
    and and_BCnDn (BCnDn, B, C_not, D_not);

    and andSendZero (AN0, sendZero, sendOne);

    //instantiating or gates as needed by the truth table
    or or_a (a, AnBnCnD, AnBDn, AB, AC);
    or or_b (b, AC, AB, BCnD, BCDn);
    or or_c (c, AB, AC, BnCDn);
    or or_d (d, AB, AC, AD, BCD, BCnDn, BnCnD);
    or or_e (e, D, BCn, AC);
    or or_f (f, CD, AB, AC, AnBnD, BnCDn);
    or or_g (g, AB, AC, BCD, AnBnCn);

    or orSendOne1(dp, sendOne, sendZero);
    or orSendOne2(AN3, sendOne, sendZero);
    or orSendOne3(AN2, sendOne, sendZero);
    or orSendOne4(AN1, sendOne, sendZero);

endmodule
```

Test Bench Code for 7 Segment Display:

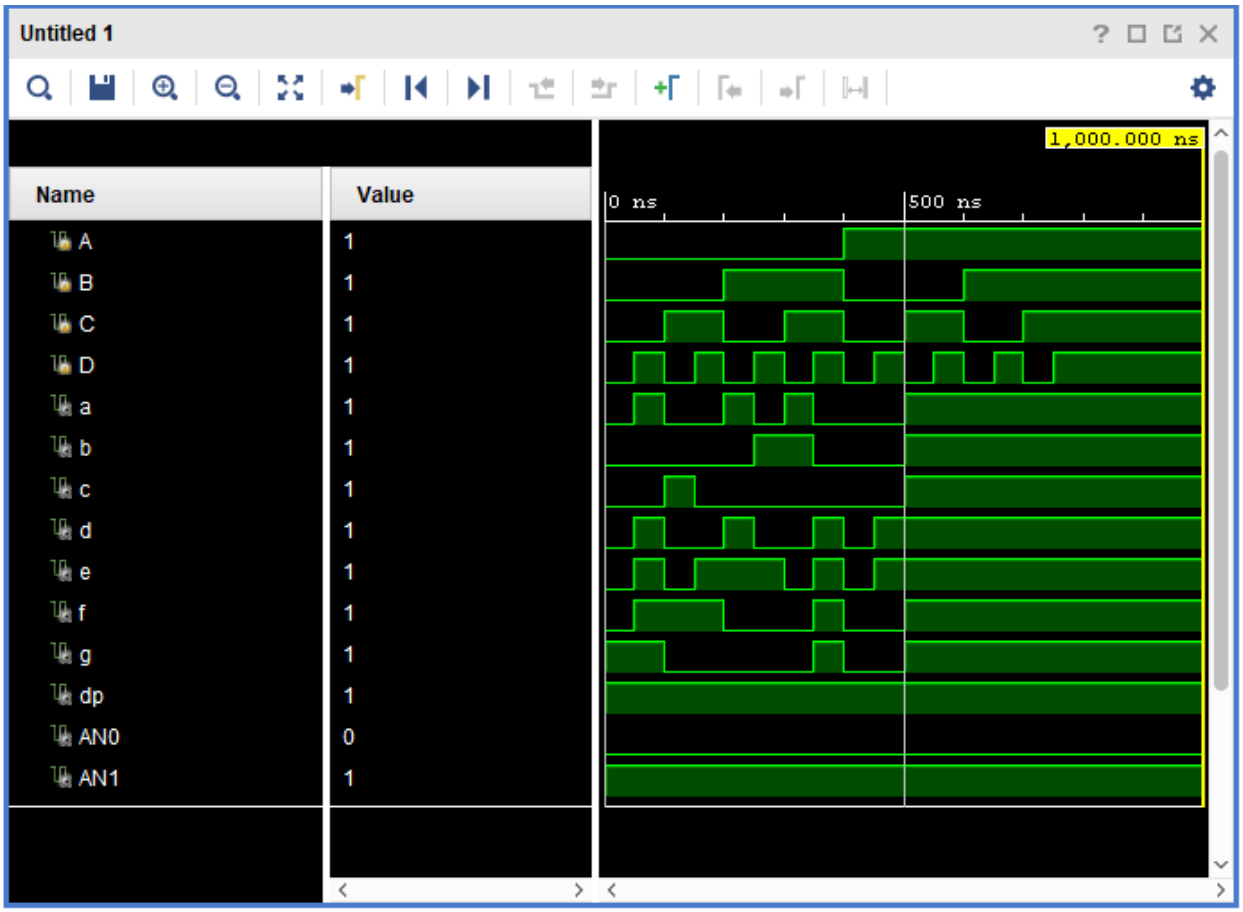
```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 02/22/2018 08:52:36 AM
// Design Name:
// Module Name: tb_SegmentDisplay
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////

`timescale 1ns / 1ps

module tb_Decoder_Structural;

    //inputs to be defined as registers
    reg A;
    reg B;
    reg C;
    reg D;

    //outputs to be defined as wires
    wire a;
    wire b;
    wire c;
    wire d;
    wire e;
    wire f;
    wire g;
```

```
wire dp;
wire AN0;
wire AN1;
wire AN2;
wire AN3;

//Initiat the unit under test (UUT)
SegmentDisplay uut (
    .A(A),
    .B(B),
    .C(C),
    .D(D),
    .a(a),
    .b(b),
    .c(c),
    .d(d),
    .e(e),
    .f(f),
    .g(g),
    .dp(dp),
    .AN0(AN0),
    .AN1(AN1),
    .AN2(AN2),
    .AN3(AN3)
);

initial begin
//initialze inputs
A = 0;
B = 0;
C = 0;
D = 0;

#50; //wait 50 seconds for global reset to finish

//stimulus - all input combinations followed by some wait time to observe the o/p

$display ("TC01");
if ({a,b,c,d,e,f,g} != 7'b0000001) $display ("Result is wrong");
A = 0;
B = 0;
C = 0;
D = 1;
#50
$display ("TC02");
if ({a,b,c,d,e,f,g} != 7'b1001111) $display ("Result is wrong");

A = 0;
B = 0;
C = 1;
D = 0;
#50
$display ("TC03");
if ({a,b,c,d,e,f,g} != 7'b0010010) $display ("Result is wrong");

A = 0;
```

```
B = 0;
C = 1;
D = 1;
#50
$display ("TC04");
if ({a,b,c,d,e,f,g} != 7'b0000110) $display ("Result is wrong");

A = 0;
B = 1;
C = 0;
D = 0;
#50
$display ("TC05");
if ({a,b,c,d,e,f,g} != 7'b1001100) $display ("Result is wrong");

A = 0;
B = 1;
C = 0;
D = 1;
#50
$display ("TC06");
if ({a,b,c,d,e,f,g} != 7'b0100100) $display ("Result is wrong");

A = 0;
B = 1;
C = 1;
D = 0;
#50
$display ("TC07");
if ({a,b,c,d,e,f,g} != 7'b1100000) $display ("Result is wrong");

A = 0;
B = 1;
C = 1;
D = 1;
#50
$display ("TC08");
if ({a,b,c,d,e,f,g} != 7'b0001111) $display ("Result is wrong");

A = 1;
B = 0;
C = 0;
D = 0;
#50
$display ("TC11");
if ({a,b,c,d,e,f,g} != 7'b0000000) $display ("Result is wrong");

A = 1;
B = 0;
C = 0;
D = 1;
#50
$display ("TC12");
if ({a,b,c,d,e,f,g} != 7'b0001100) $display ("Result is wrong");

A = 1;
```

```
    B = 0;
    C = 1;
    D = 0;
    #50
    $display ("TC13");
    if ({a,b,c,d,e,f,g} != 7'b1111111) $display ("Result is wrong");

    A = 1;
    B = 0;
    C = 1;
    D = 1;
    #50
    $display ("TC14");
    if ({a,b,c,d,e,f,g} != 7'b1111111) $display ("Result is wrong");

    A = 1;
    B = 1;
    C = 0;
    D = 0;
    #50
    $display ("TC15");
    if ({a,b,c,d,e,f,g} != 7'b1111111) $display ("Result is wrong");

    A = 1;
    B = 1;
    C = 0;
    D = 1;
    #50
    $display ("TC16");
    if ({a,b,c,d,e,f,g} != 7'b1111111) $display ("Result is wrong");

    A = 1;
    B = 1;
    C = 1;
    D = 0;
    #50
    $display ("TC17");
    if ({a,b,c,d,e,f,g} != 7'b1111111) $display ("Result is wrong");

    A = 1;
    B = 1;
    C = 1;
    D = 1;
    #50
    $display ("TC18");
    if ({a,b,c,d,e,f,g} != 7'b1111111) $display ("Result is wrong");

    end

endmodule
```

Simulation Wave Form:



7 Segment Display Constraint File:

```
set_property PACKAGE_PIN V17 [get_ports {D}]
        set_property IOSTANDARD LVCMOS33 [get_ports {D}]
set_property PACKAGE_PIN V16 [get_ports {C}]
        set_property IOSTANDARD LVCMOS33 [get_ports {C}]
set_property PACKAGE_PIN W16 [get_ports {B}]
        set_property IOSTANDARD LVCMOS33 [get_ports {B}]
set_property PACKAGE_PIN W17 [get_ports {A}]
        set_property IOSTANDARD LVCMOS33 [get_ports {A}]


set_property PACKAGE_PIN W7 [get_ports {a}]
        set_property IOSTANDARD LVCMOS33 [get_ports {a}]
set_property PACKAGE_PIN W6 [get_ports {b}]
        set_property IOSTANDARD LVCMOS33 [get_ports {b}]
set_property PACKAGE_PIN U8 [get_ports {c}]
        set_property IOSTANDARD LVCMOS33 [get_ports {c}]
set_property PACKAGE_PIN V8 [get_ports {d}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d}]
set_property PACKAGE_PIN U5 [get_ports {e}]
        set_property IOSTANDARD LVCMOS33 [get_ports {e}]
set_property PACKAGE_PIN V5 [get_ports {f}]
        set_property IOSTANDARD LVCMOS33 [get_ports {f}]
set_property PACKAGE_PIN U7 [get_ports {g}]
        set_property IOSTANDARD LVCMOS33 [get_ports {g}]

set_property PACKAGE_PIN V7 [get_ports {dp}]
        set_property IOSTANDARD LVCMOS33 [get_ports {dp}]

set_property PACKAGE_PIN U2 [get_ports {AN0}]
        set_property IOSTANDARD LVCMOS33 [get_ports {AN0}]
set_property PACKAGE_PIN U4 [get_ports {AN1}]
        set_property IOSTANDARD LVCMOS33 [get_ports {AN1}]
set_property PACKAGE_PIN V4 [get_ports {AN2}]
        set_property IOSTANDARD LVCMOS33 [get_ports {AN2}]
set_property PACKAGE_PIN W4 [get_ports {AN3}]
        set_property IOSTANDARD LVCMOS33 [get_ports {AN3}]
```