EE 316 Spring 2018, Nur Touba, 15320

1/26/2018

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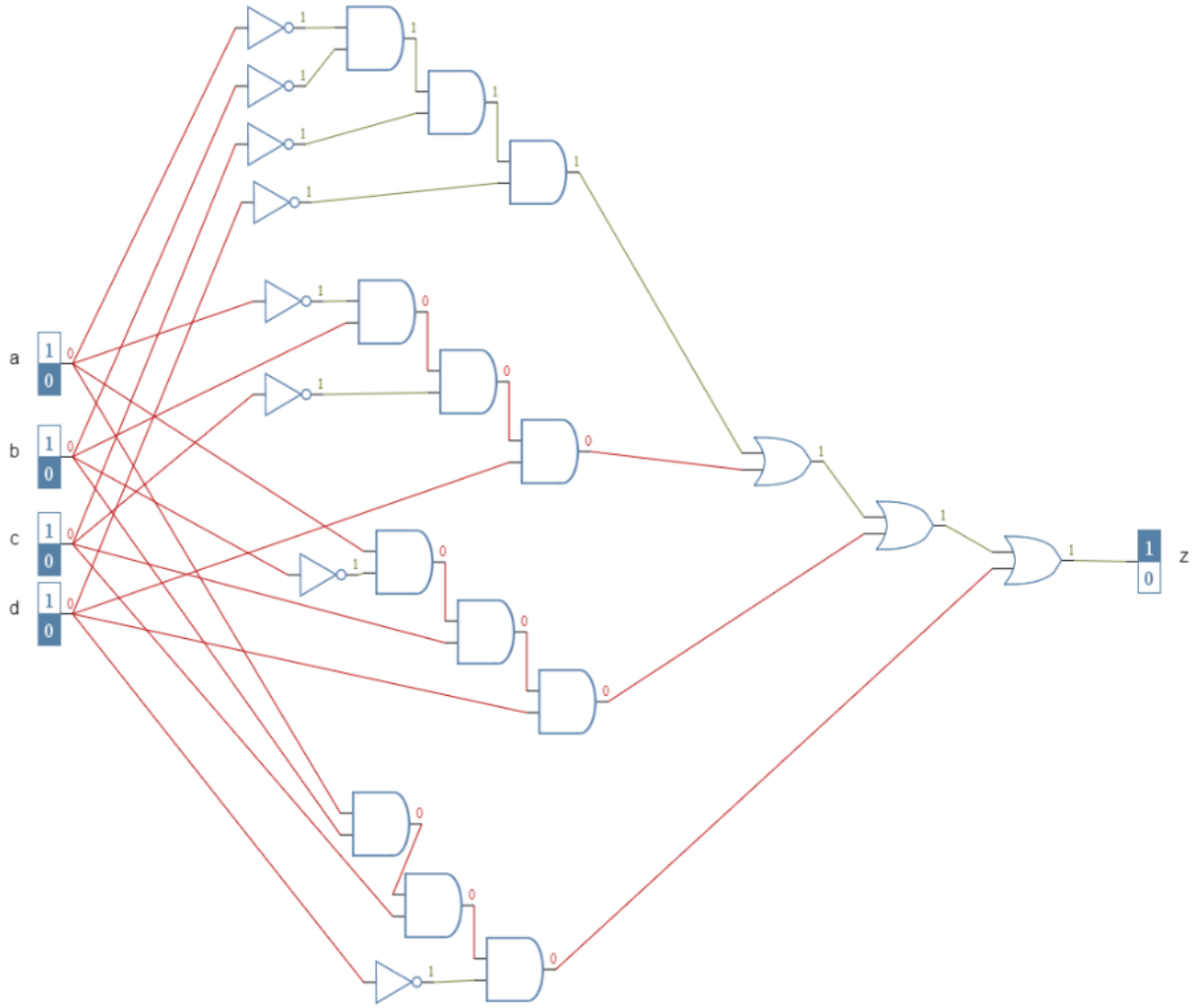
Lab 1

Problem 1:

Gate implementation:



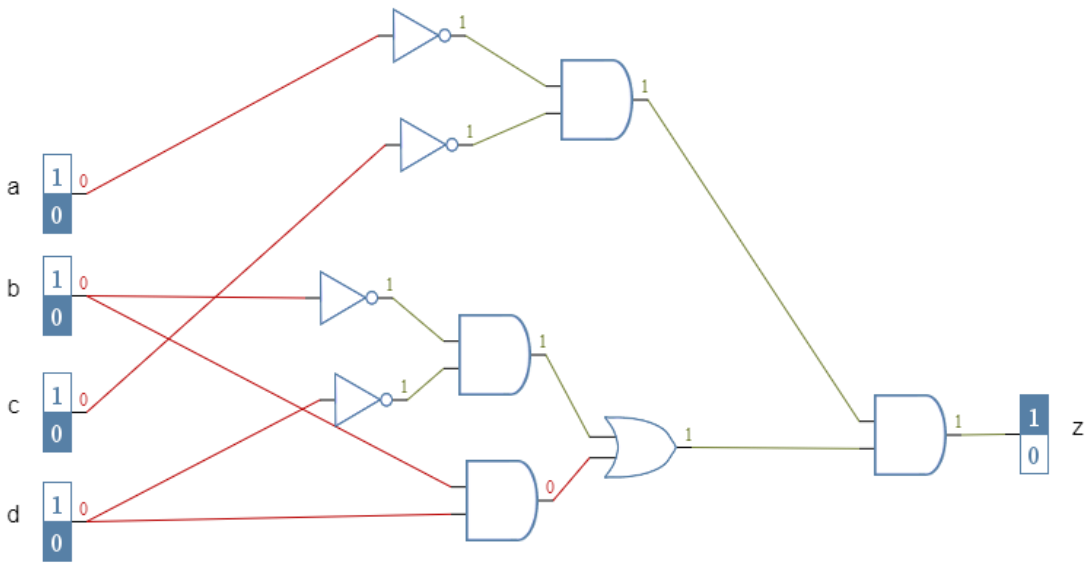
Truth table:

a	b	c	d	a'b'c'd'	a'bc'd	ab'cd	abcd'	Z1
0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	0	0	0
0	0	1	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0
0	1	0	0	0	0	0	0	0
0	1	0	1	0	1	0	0	1
0	1	1	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0
1	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0
1	0	1	0	0	0	0	0	0
1	0	1	1	0	0	1	0	1
1	1	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0
1	1	1	0	0	0	0	1	1
1	1	1	1	0	0	0	0	0

The output for Z1 is HIGH only when a and c are LOW and b and d are either both HIGH or both LOW, or when a and c are HIGH and when only either b or d is HIGH.

Problem 2:

Gate Implementation:



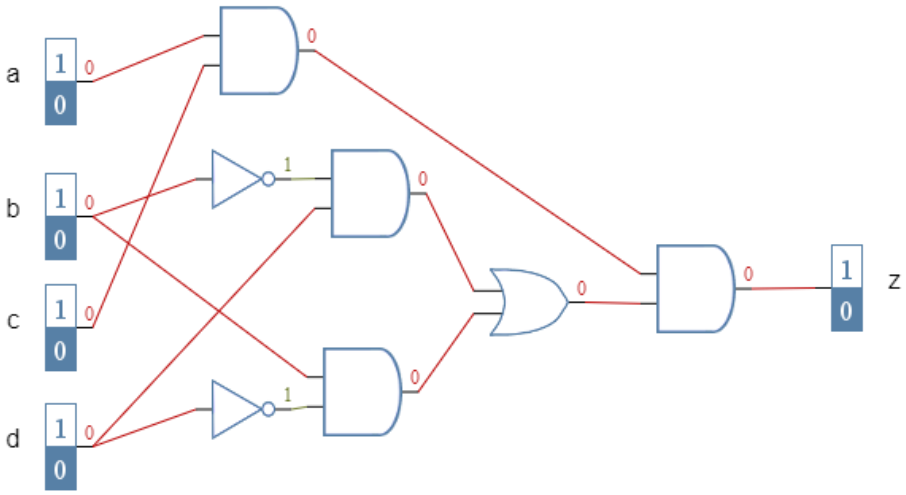
Truth Table:

a	b	c	d	a'c'	b'd'	bd	(b'd'+bd)	Z2
0	0	0	0	1	1	0	1	1
0	0	0	1	1	0	0	0	0
0	0	1	0	0	1	0	1	0
0	0	1	1	0	0	0	0	0
0	1	0	0	1	0	0	0	0
0	1	0	1	1	0	1	1	1
0	1	1	0	0	0	0	0	0
0	1	1	1	0	0	1	1	0
1	0	0	0	0	1	0	1	0
1	0	0	1	0	0	0	0	0
1	0	1	0	0	1	0	1	0
1	0	1	1	0	0	0	0	0
1	1	0	0	0	0	0	0	0
1	1	0	1	0	0	1	1	0
1	1	1	0	0	0	0	0	0
1	1	1	1	0	0	1	1	0

The output for Z2 is HIGH only when a and c are both LOW and either b and d are both LOW or b and d are both HIGH.

Problem 3:

Gate Implementation:



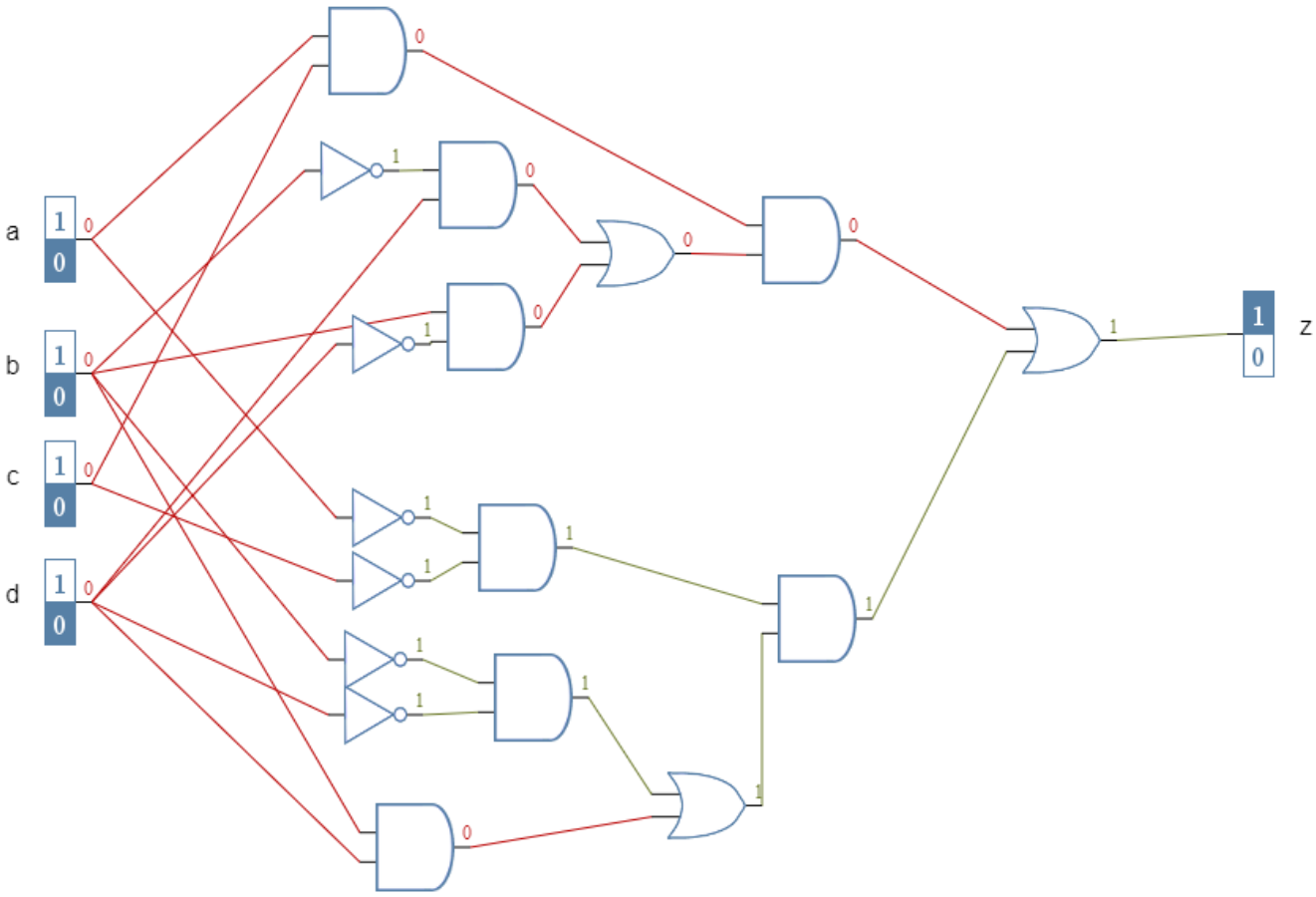
Truth Table:

a	b	c	d	bd’	b’d	bd’+b’d	ac	Z3
0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	1	0	0
0	0	1	0	0	0	0	0	0
0	0	1	1	0	1	1	0	0
0	1	0	0	1	0	1	0	0
0	1	0	1	0	0	0	0	0
0	1	1	0	1	0	1	0	0
0	1	1	1	0	0	0	0	0
1	0	0	0	0	0	0	0	0
1	0	0	1	0	1	1	0	0
1	0	1	0	0	0	0	1	0
1	0	1	1	0	1	1	1	1
1	1	0	0	1	0	1	0	0
1	1	0	1	0	0	0	0	0
1	1	1	0	1	0	1	1	1
1	1	1	1	0	0	0	1	0

The output for Z3 is HIGH only when both a and c are HIGH and only 1 of either b or d is HIGH.

Problem 4:

Gate Implementation:



Truth Table:

a	b	c	d	Z2	Z3	Z2+Z3 =Z4
0	0	0	0	1	0	1
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	0	1	1	0	1
0	1	1	0	0	0	0
0	1	1	1	0	0	0
1	0	0	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	0	0	0
1	0	1	1	0	1	1
1	1	0	0	0	0	0
1	1	0	1	0	0	0
1	1	1	0	0	1	1
1	1	1	1	0	0	0

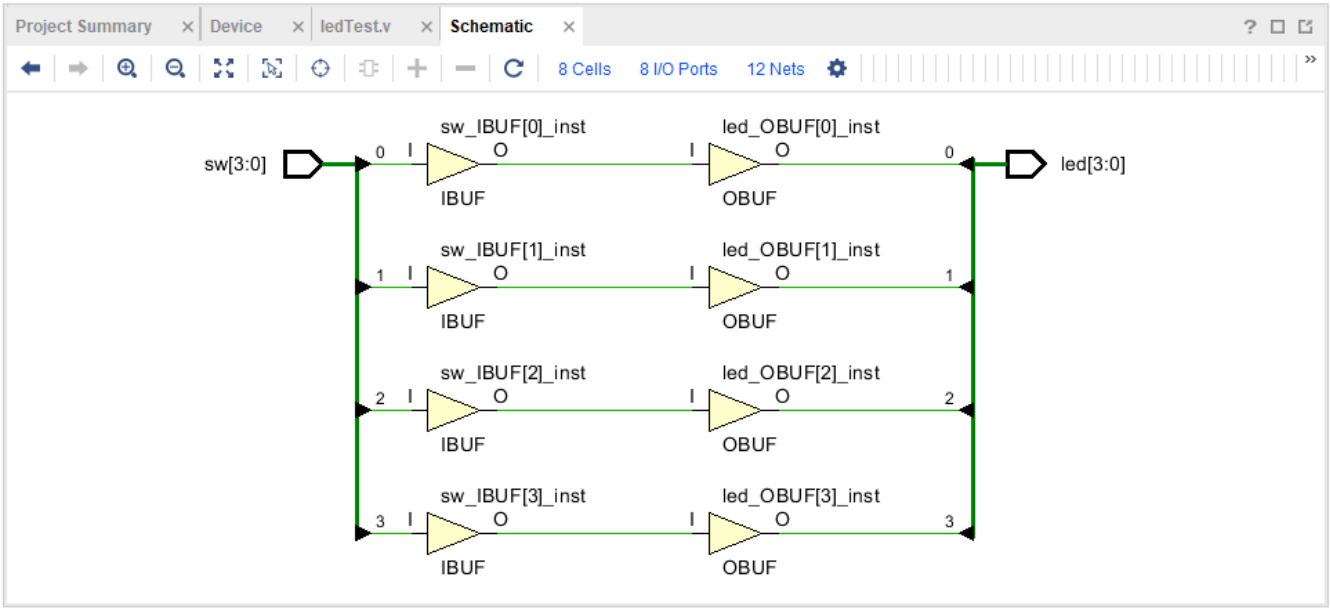
The output for Z4 is HIGH only when if a and c are both LOW and b and d are either both HIGH or LOW, or if a and c are both HIGH and only one of either b or d is HIGH.

Problem 5:

Z1 is equal to Z4 for all possible input values.

Problem 6:

Screen shot of circuit in Viviado:



Pin Assignments:

Inputs	Package Pin	Outputs	Package Pin
sw[0]	U15	led[0]	U14
sw[1]	W14	led[1]	V14
sw[2]	W13	led[2]	V13
sw[3]	W15	led[3]	U16