Jose Andres Melgoza Mendoza

Embedded Systems and FPGA Design Engineer

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Summary

Embedded Systems and FPGA Engineer with 7+ years of experience in software development, hardware acceleration, and FPGA design/verification for safety-critical and space-grade systems. Extensive hands-on experience in C for real-time embedded software, C++ for modular architectures, and Python for automation and tool integration.
Experienced with AUTOSAR, ISO 26262, ASPICE, and ECSS-aligned workflows, with strong capabilities in hardware/software co-design, performance optimization, and robust validation in constrained environments.
Skilled in MCAL, BSW, and complex driver integration in automotive ECUs, and in cross-functional debugging and system-level bring-up. Focused on embedded vision, real-time systems, and dependable low-level engineering.

Technical Skills

Languages: C, C++, Python, VHDL, Bash, SQL
MCUs/SoCs: STM32, MSP430, ARM Cortex-M, Xilinx Zynq, Artix-7
RTOS: FreeRTOS, Zephyr, CMSIS-RTOS
Tools: Vivado, CubeIDE, Keil, IAR, Altium Designer, STM32CubeMX, ModelSim, QuestaSim, Sigasi, Synplify, CANoe, Lauterbach, J-Link, VectorCAST, Coverity, MISRA tools
Protocols: SPI, I2C, UART, CAN, LIN
Linux: Embedded Linux, Yocto, Buildroot, U-Boot, Device Tree
Build Systems: Make, CMake
Advanced: REST API integration, Protocol Buffers
Verification: VHDL testbenches, QuestaSim/ModelSim, UCDB coverage, SystemVerilog Assertions
Requirements & Standards: ECSS standards, IBM DOORS, SUMO requirement tracing
Team/DevOps: Git, GitLab CI, Jenkins, Jira, IBM Rational Team Concert (RTC)
Documentation: LaTeX, IBM DOORS, R4J

Experience

Exceltic, FPGA Design Engineer (Thales Alenia Space – CTEG Project)
Madrid, Spain
Feb 2026 – Present

- Implemented VHDL modules for ADC housekeeping (HK), including telemetry acquisition, monitoring, and reporting.
- Designed PLL scrubbing logic to detect and recover from lock issues for satellite platforms.
- Built unit-level testbenches and simulation checks to validate new VHDL blocks before integration.

Exceltic, FPGA Verification Engineer (Thales Alenia Space – CTEG Project)
Madrid, Spain
May 2025 – Jan 2026

- Verification engineer for the CTEG (Configurable Telecommunication Gateway), a space-grade FPGA-based secure router for satellite communications.
- Developed and executed VHDL testbenches to validate telecommand/telemetry flows, ensuring encryption/decryption compliance with ESU interfaces.
- Performed coverage analysis (QuestaSim/UCDB) and created requirement traceability matrices (DOORS, SUMO) to guarantee full functional verification of FPGA requirements.
- Debugged timing, protocol, and error-handling scenarios (timeouts, busy signals, authentication failures, bit errors) at simulation level.
- Coordinated with cross-site teams (Spain, France, Italy) to align design changes with ECSS standards and project milestones.

Visteon VTCQ, Senior DiApps & BMS Developer — Querétaro, Mexico
Nov 2021 – Sep 2024

- Developed DiApps modules in C for vehicle HMI, including menu navigation, icon rendering, and display personalization based on vehicle state.
- Programmed interaction logic between physical controls (buttons, rotary knobs) and software input handlers using C.
- Maintained and extended BMS communication layers using UDS over CAN, with diagnostics and status reporting logic.
- Wrote and reviewed ASPICE-compliant documentation: SRD, SRS, LLD, HLD.
- Debugged embedded software with Lauterbach (TRACE32) and Vector CANoe across multiple integration stages.
- Participated in software/hardware integration events (SW/HW Bring-up) for pre-production units.
- Worked with cross-functional teams to define ARXML interfaces and signal mappings using Vector tools.
- Collaborated on low-level software configuration using DaVinci Configurator/Developer.

Samsung Electronics, Automation & Vision Systems Engineer — Querétaro, Mexico
Feb 2018 – Mar 2019

- Designed machine vision systems using OpenCV in C++ and Python to detect defects in real-time during manufacturing.
- Developed FPGA-based hardware acceleration for convolutional filters, offloading image preprocessing tasks.
- Trained lightweight convolutional neural networks and deployed them using fixed-point logic in VHDL.
- Integrated HMIs and PLCs to control robotic test benches based on visual classification outcomes.
- Validated end-to-end pipeline from image capture to robotic actuation under tight timing constraints.

Education

M.Sc. **Instituto Tecnológico de Morelia**, Digital Electronics — 2019 – 2021
Thesis: “Neural Network Architectures in FPGA/FPSoC”
Developed VHDL auto-generation from TensorFlow-trained networks.
Focused coursework on digital signal processing, ASIC design, and hardware acceleration techniques.

B.Sc. **Instituto Tecnológico de Morelia**, Electronics Engineering (Embedded Systems) — 2012 – 2018

Certifications

- Udemy: Advanced C Programming
- Vision Technologies and Techniques
- High Voltage Safety and PPE
- 7º Encuentro Regional de Energía Renovable
- XXIV Congreso Internacional TECNOTRONICA

Publications

“FPGA/FPSoC Neural Networks for Performance-Based Design” — 2021
Published at Academia Journals. Presented inference from BNN on Artix-7.

Languages

Spanish: Native **English:** Fluent **German:** Basic

Soft Skills

- Agile/Scrum collaboration
- Mentoring junior developers
- Technical decision-making under pressure
- Fast adaptation to legacy codebases
- Clear technical communication across teams

References

Silvia Ramirez – silvia.ramirez@visteon.com
Dr. Arturo Mendez Patino – arturo.mp@morelia.tecnm.mx