Politecnico di Torino

Microelectronic Systems

DLX Microprocessor: Design & Development

Final Project Report

Master degree in Electronics Engineering
Master degree in Computer Engineering

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CHAPTER 1

Introduction

The aim of the project is to design and synthesize a general purpose, MIPS-based processor. The architecture is RISC (Reduced Instruction Set Computer) and works with words 32-bits long. As a consequence, also the instruction word has the same length and can be of 3 types:

- **R type**: it indicates an instruction that involves two source registers and a destination register. The instruction word is divided as can be seen in figure 1.1

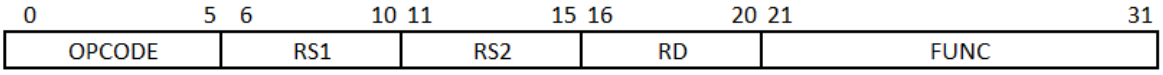

Figure 1.1: R type instruction word.

- **I type**: it indicates an instruction that involves a source register, a destination register and an immediate (i.e. a value specified by the user in the assembly code). The instruction word is divided as can be seen in figure 1.2

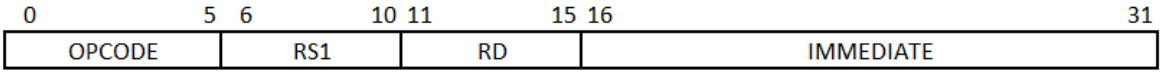

Figure 1.2: I type instruction word.

- **J type**: it indicates an instruction that is used to jump to a given program counter, specified on 26 bits. The instruction word is divided as can be seen in figure 1.3

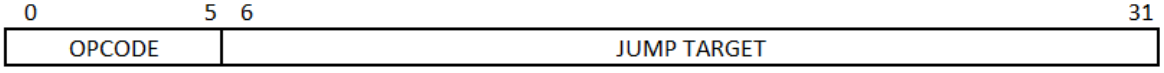

Figure 1.3: J type instruction word.

Knowing how the instructions are encoded is one of the key point in order to be able to perform the decode phase and retrieve the operand of the requested instruction, which can be recognized only if

it is part of the processor ISA (Instruction Set Architecture). The ISA of a processor represent the set of available instructions and it is the design starting point since all the hardware added inside the architecture is in charge of handling a part of one, or more, instruction. The instruction set of this particular processor can be found in figure 1.4

J Type		
Instruction	Opcode	Func
J	0x02	X
JAL	0x03	X

R Type		
Instruction	Opcode	Func
SLL	0x00	0x04
SRL	0x00	0x06
SRA	0x00	0x07
ADD	0x00	0x20
ADDU	0x00	0x21
SUB	0x00	0x22
SUBU	0x00	0x23
AND	0x00	0x24
OR	0x00	0x25
XOR	0x00	0x26
SEQ	0x00	0x28
SNE	0x00	0x29
SLT	0x00	0x2a
SGT	0x00	0x2b
SLE	0x00	0x2c
SGE	0x00	0x2d
SLTU	0x00	0x3a
SGTU	0x00	0x3b
SLEU	0x00	0x3c
SGEU	0x00	0x3d
NAND	0x00	0x3e
NOR	0x00	0x3f
XNOR	0x00	0x40
MUL	0x00	0x41

I Type		
Instruction	Opcode	Func
BEQZ	0x04	X
BNEZ	0x05	X
ADDI	0x08	X
ADDUI	0x09	X
SUBI	0x0a	X
SUBUI	0x0b	X
ANDI	0x0c	X
ORI	0x0d	X
XORI	0x0e	X
LHI	0x0f	X
JR	0x12	X
JALR	0x13	X
SLLI	0x14	X
NOP	0x15	X
SRLI	0x16	X
SRAI	0x17	X
SEQI	0x18	X
SNEI	0x19	X
SLTI	0x1a	X
SGTI	0x1b	X
SLEI	0x1c	X
SGEI	0x1d	X
LB	0x20	X
LH	0x21	X
LW	0x23	X
LBU	0x24	X
LHU	0x25	X
SB	0x28	X
SH	0x29	X
SW	x02b	X
NANDI	0x30	X
NORI	0x31	X
XNORI	0x32	X
MULI	0x33	X
SLTUI	0x3a	X
SGTUI	0x3b	X
SLEUI	0x3c	X
SGEUI	0x3d	X

Figure 1.4: Designed processor ISA.

From an high level point of view, all the architecture hardware can be inserted in two main macro-blocks: the control unit(CU) and the datapath. The former is in charge of driving the datapath units according to the input instruction (see chapter 2) while the latter has to handle all the evolution of the program (see chapter 3). A very basic interconnection between the two units is shown in figure 1.5.

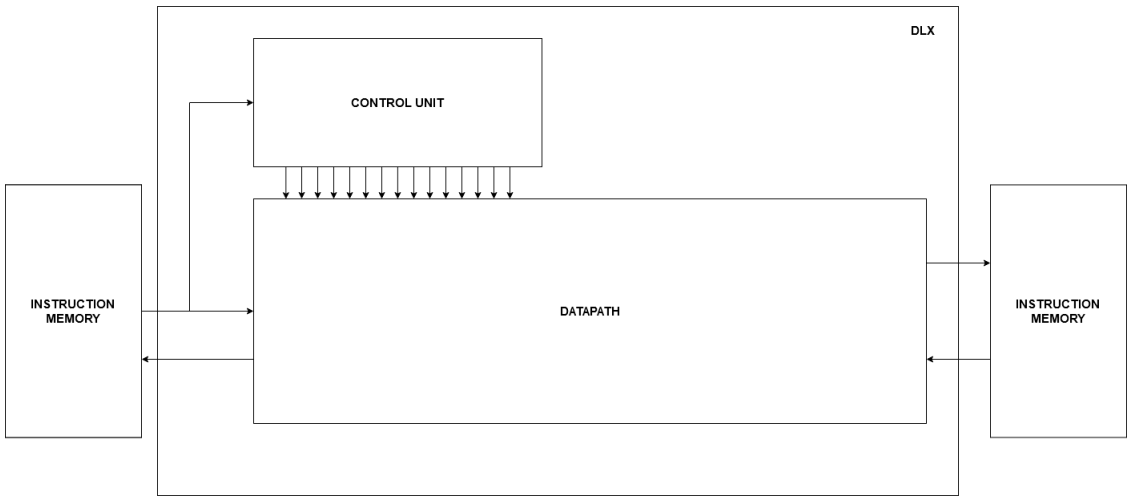

Figure 1.5: Basic interconnections inside the DLX processor and with memories.

In order to increase the performances of the processor, a pipeline has been inserted to divide the datapath in five stages:

- Fetch stage (IF): the instruction is read from memory and the program counter (which stores the address of the next instruction to be fetched) predictions are taken.
- Decode stage (ID): the operands for the requested operation are prepared and the jump, jump register and branch instructions are checked in order to rectify as soon as possible the program counter.
- Execute stage (EX): the requested operation is executed, if the instruction is a load or a store the address of the memory is calculated.
- Memory stage (MEM): interactions with the memory are performed.
- Writeback stage (WB): the result of the requested operation is written back in the register file.

The presence of the pipeline affected also the design of the control unit since it has been necessary to delay part of the control word in order to achieve the correct synchronization.
In the next pages a detailed explanation about how each component inserted in the architecture works and about the design choices that led to that kind of implementation can be found.

Part I

CONTROL LOGIC

CHAPTER 2

Control unit

The control unit is the element of the processor in charge of providing the control signals to all the components inside the datapath in order to correctly manage the execution of the instruction. It has been designed using the hardwired approach, which means that it acts like a decoder that receives as input the OPCODE and the FUNC signal coming from the datapath and produces as output a 34-bits long control word containing all the signals needed to correctly configure the datapath components. This control word is splitted into 2 parts: the 13 most significant bits are directly connected to the ID stage, while the remaining 22 bits are delayed (1 cycle for EX, 2 for MEM and 3 for WB) through a chain of registers in order to synchronize the control signals with the stage in which they must be used.
In order to manage stalls, FILL and SPILL operation, a small logic has been inserted before the input of the first register of the register called ID/EX. It works as follows:

- if there is a stall the ID/EX register receives in input a signal made of all 0. In this way the instruction will be seen by the datapath as a NOP and so a bubble will be created in the pipeline;
- if there is a SPILL operation the instruction is transformed into a STORE which has as target a special section of the DRAM as long as the SPILL signal is asserted;
- if there is a FILL operation the instruction is interpreted as a LOAD from the same memory section of the SPILL operation, until the FILL signal goes to zero.

An architectural level scheme is shown in Figure 2.1.

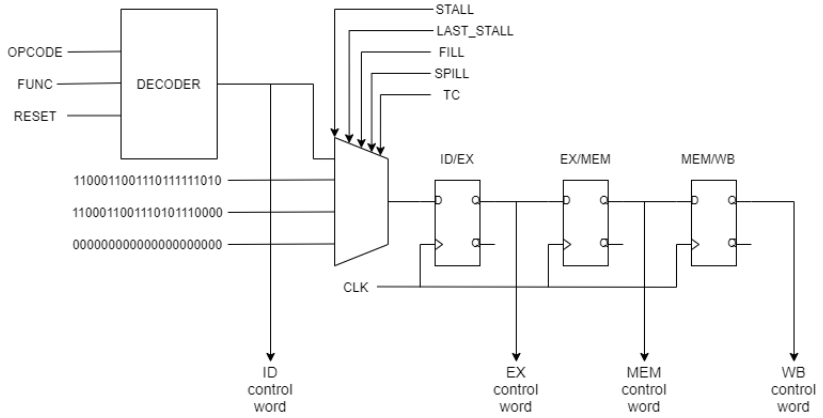

Figure 2.1: Architectural level scheme of the control unit.

Part II

DATAPATH

CHAPTER 3

Datapath introduction

The datapath is the processor macro block in which all the hardware units are inserted. It is in charge of managing the whole execution of the instruction (from the preparation to the saving through the execution). In order to perform such a task in the most performant way, the datapath is divided into the five pipeline stages (see chapter 1). This kind of organization allows to increment the processor throughput (which indicates the amount of instruction executed per time unit) since at each clock cycle a new instruction is performed. On the other hand is important to underline that a new instruction will take 5 clock cycles to be fully committed (1 clock cycle for each pipeline stage). Two consecutive stages are connected together through some pipeline registers whose main role is to preserve the necessary data for continuing the execution, a basic schema is visible in figure 3.1

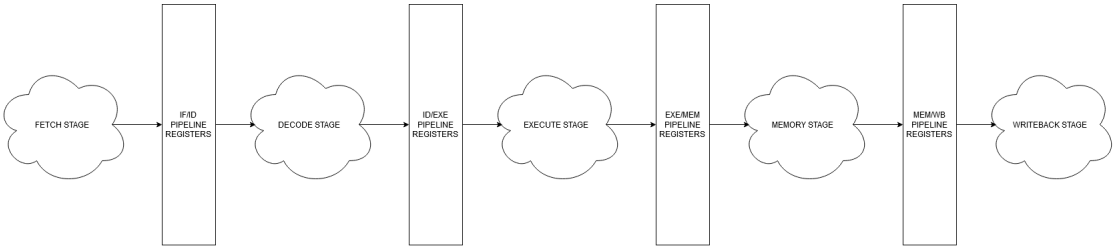

Figure 3.1: Datapath basic schema: the bubbles represent all the logic inserted in the stage.

The following chapters describe each one of the pipeline stages.

CHAPTER 4

Instruction fetch stage

The main goal of the instruction fetch stage is to pick an instruction from the instruction memory (IRAM) and store it into the instruction register that is one of the IF/ID pipeline registers. The address used to access the IRAM is stored into a special register called program counter (PC) that is updated at each clock cycle. The components present in this stage are:

- **Branch target buffer**;
- **Program counter register**;
- **Program counter update logic**;
- **Program counter adder**;
- **Branch recognition logic**;
- **Flush logic**.

An architectural level scheme of this stage is shown in Figure 4.1.

4.1 Branch target buffer

The branch target buffer is one of the dynamic branch prediction techniques. It is a small memory that is used to immediately predict the new program counter in case of a branch instruction. The BTB present inside the DLX (its interface is shown in Figure 4.2) has 256 entries composed of 3 parts: the address of the instruction, the target address where to jump in case the condition of the branch is verified and a bit indicating if the entry is full or empty (see Figure 4.3). Each time an instruction is fetched, its PC is used to access one of the entry of the BTB (since the BTB has 256 entries, the bits from 2 to 9 of the PC are used to address it). If the selected entry is not empty, the target address is given as output and the signal BTB_FOUND is set to 1. When the signal that has just been asserted enters the ID stage, its value is compared with the condition of the branch and if a misprediction is detected the entry of the BTB is deleted and the IF stage of the pipeline flushed. In case the prediction was correct, the processor can continue without needing stalls or flushes. In case the entry accessed by the PC is empty and the condition of the branch gives a *branch taken* as result in the decode stage, the PC and the target address computed by the adder/subtractor in ID are written in the BTB, otherwise nothing happens because the prediction was correct.
The BTB has been synthesized to estimate its area, power consumption and performance. The value obtained from the various reports are shown in appendix B.1.

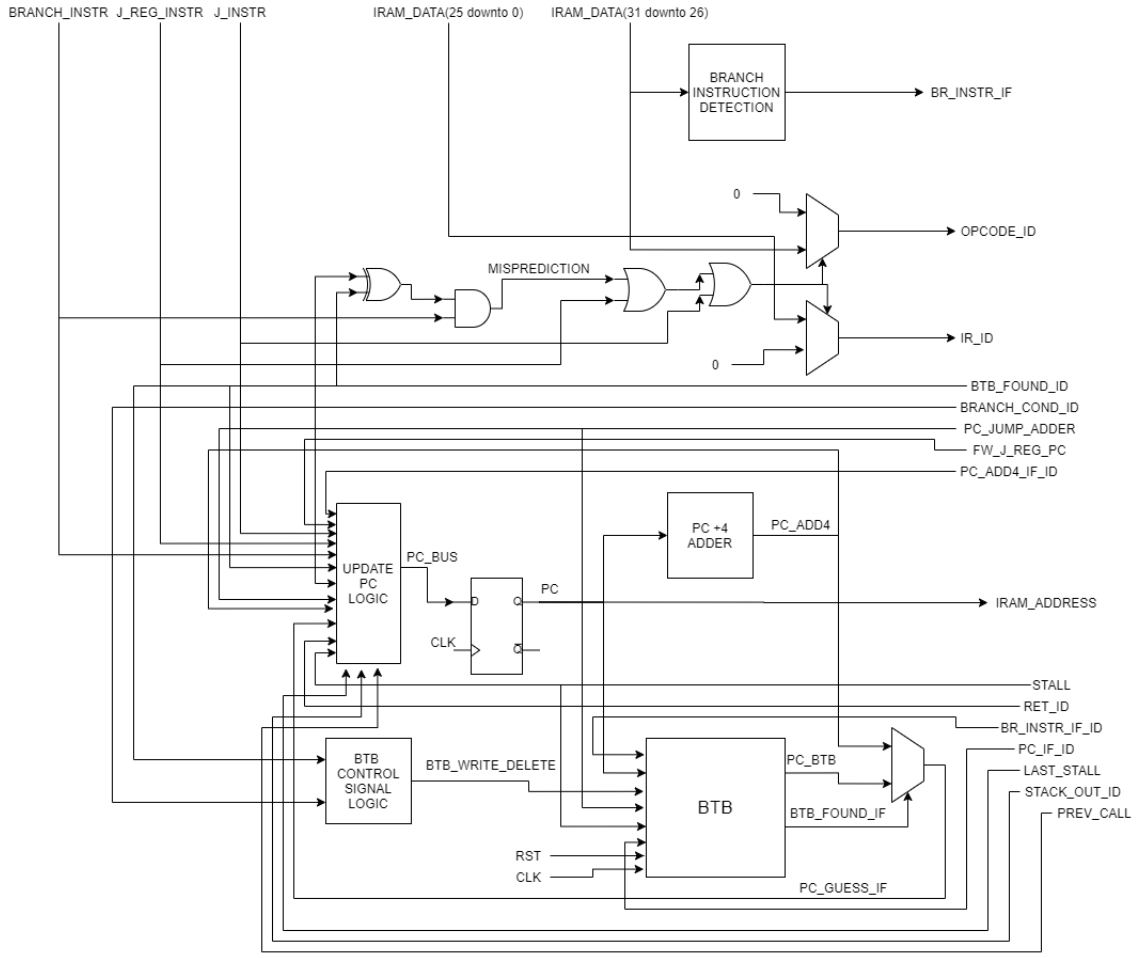

Figure 4.1: Architectural level scheme of the instruction fetch stage.

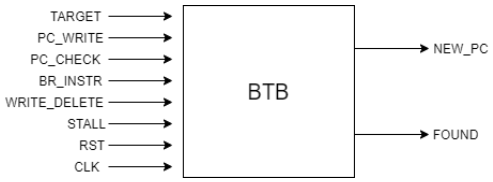

Figure 4.2: Branch target buffer interface

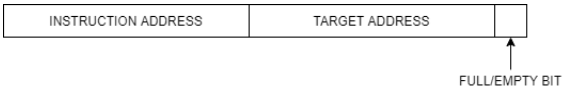

Figure 4.3: Composition of each entry inside the branch target buffer.

4.2 Program counter and update logic

The program counter is a register containing the address of the instruction memory where the instruction to be fetched is stored. It must be updated each clock cycle, with the exception of the stalls during which it must preserve its value.
The logic that computes the next value to be written inside the PC has been designed in order to update at every clock cycle a new value. According to some control signals coming from the decode stage (where branches are evaluated) the update logic behaves as follow:

- if a stall is needed ⇒ the value is not updated;
- if no stall is needed ⇒
  - if the instruction in the ID stage is a J type ⇒ the value is taken from the adder/subtractor in ID stage;
  - if the instruction in the ID stage is a JR or a JALR ⇒
    - when it corresponds to a return from function and no calls preceded it ⇒ the value is taken from the stack;
    - otherwise ⇒ the signal propagated is the FW_J_REG_PC whose meaning will be described in the chapter dedicated to the ID stage;
  - if the instruction in the ID stage is a BRANCH ⇒
    - if the previous PC was found in the BTB but the result of the branch is not taken ⇒ the new value of the PC is taken from the register in the IF/ID pipeline where the previous instruction PC incremented by 4 is stored;
    - if the previous PC was not found in the BTB but the result of the branch is taken ⇒ the new value comes from the adder/subtractor in the ID stage;
    - otherwise ⇒ the value propagated is the one predicted in the current stage (between the output of the BTB and the output of the program counter adder);
  - otherwise ⇒ the value propagated is the one predicted in the current stage.

4.3 Program counter adder

It is an adder described in a behavioral way in the VHDL code that receives as input the value of the PC and increments it by 4. The reason behind this addiction is that the instruction memory has entries of 1 byte and each instruction inside the processor occupies 4 bytes (32 bits), so each instruction starting address inside the memory is a multiple of 4.
The program counter adder has been synthesized to estimate its area, power consumption and performance. The value obtained from the various reports are shown in appendix B.2.

4.4 Branch recognition logic

The branch recognition logic consists in checking if the opcode of the instruction corresponds to a BEQZ or a BNEZ. If a branch is recognized a signal called BR_INSTR_IF is set to 1, otherwise to 0. This signal will be propagated to the ID stage by storing it into a IF/ID pipeline register in order to allow an eventual write/delete in the BTB during the ID stage (because the write/delete is a synchronous operation and has as enable signal the BR_INSTR_IF_ID).

4.5 Flush logic

This logic is used to flush the pipeline in case of a branch misprediction or when the instruction in ID stage is a J, JAL, JALR or JR. This is necessary since both the branch condition check and the computation of the new PC in case of a jump and branch instruction are done in the ID stage, so in the meanwhile a new instruction has been fetched based on the prediction done in the IF stage in the previous clock cycle. That instruction must be flushed (i.e. canceled) because it is not the correct one. In order to perform this task the opcode signal sent to the control unit and the instruction register are set to all 0. In this way the control unit will interpret the instruction as a R-type add instruction whose all operands are all R0 and, therefore, nothing will be written in the register file. The signal that indicates a misprediction is computed using the formula in equation 4.1

$$MISPREDICTION \Leftarrow (BTB\_FOUND\_ID \oplus BRANCH\_COND\_ID) \cdot BRANCH\_INSTR \quad (4.1)$$

CHAPTER 5

Fetch/Decode pipeline registers

There are 6 fetch/decode pipeline registers:

- **BR_INSTR_IF_ID** (1 bit) : stores the information about the type of the current instruction (in particular if it is a branch instruction);
- **BTB_FOUND_ID** (1 bit) : brings to the ID stage the BTB_FOUND signal;
- **PC_IF_ID** (32 bits) : stores current PC;
- **PC_ADD4_IF_ID** (32 bits) : stores the current PC incremented by 4;
- **IR_IF_ID** (26 bits) : stores the instruction word with exception of the opcode;
- **OPCODE** (6 bits) : stores the opcode;

All the registers are enabled by the STALL_IF_ID signal and, therefore, will be always active unless a stall is needed.

CHAPTER 6

Decode Stage

The decode stage is the phase of the pipeline in which the processor starts to configure its units in order to execute the incoming instruction. In particular, according to the informations given by the presence of the control word coming from the control unit, the following oprations are performed:

- The instruction word is read and the various components are extracted (source registers, destination register, immediate, function bits)
- The register file is read and all the operand for the execute stage are prepared and put in the pipeline registers.
- If the instruction is a branch one, it is evaluated in order to correct as soon as possible the program counter picked during the fetch stage. The same happens with jump instructions.
- The presence of hazards is checked and, if necessary, the whole processor is stalled to avoid any kind of errors. All the hazards that could arise will make the instruction stall during the decode stage.

In order to perform such operations, the following units have been included in the design:

- **Instruction register decode unit**
- **Register file**
- **Register file decode unit**
- **Hazard detection unit**
- **Register file bypass unit**
- **Return detection unit**
- **Stack**
- **Jump comparator**
- **Jump adder**

In the following sections each unit is going to be well explained.
The architectural schema of the whole decode stage is showed in figure 6.1.

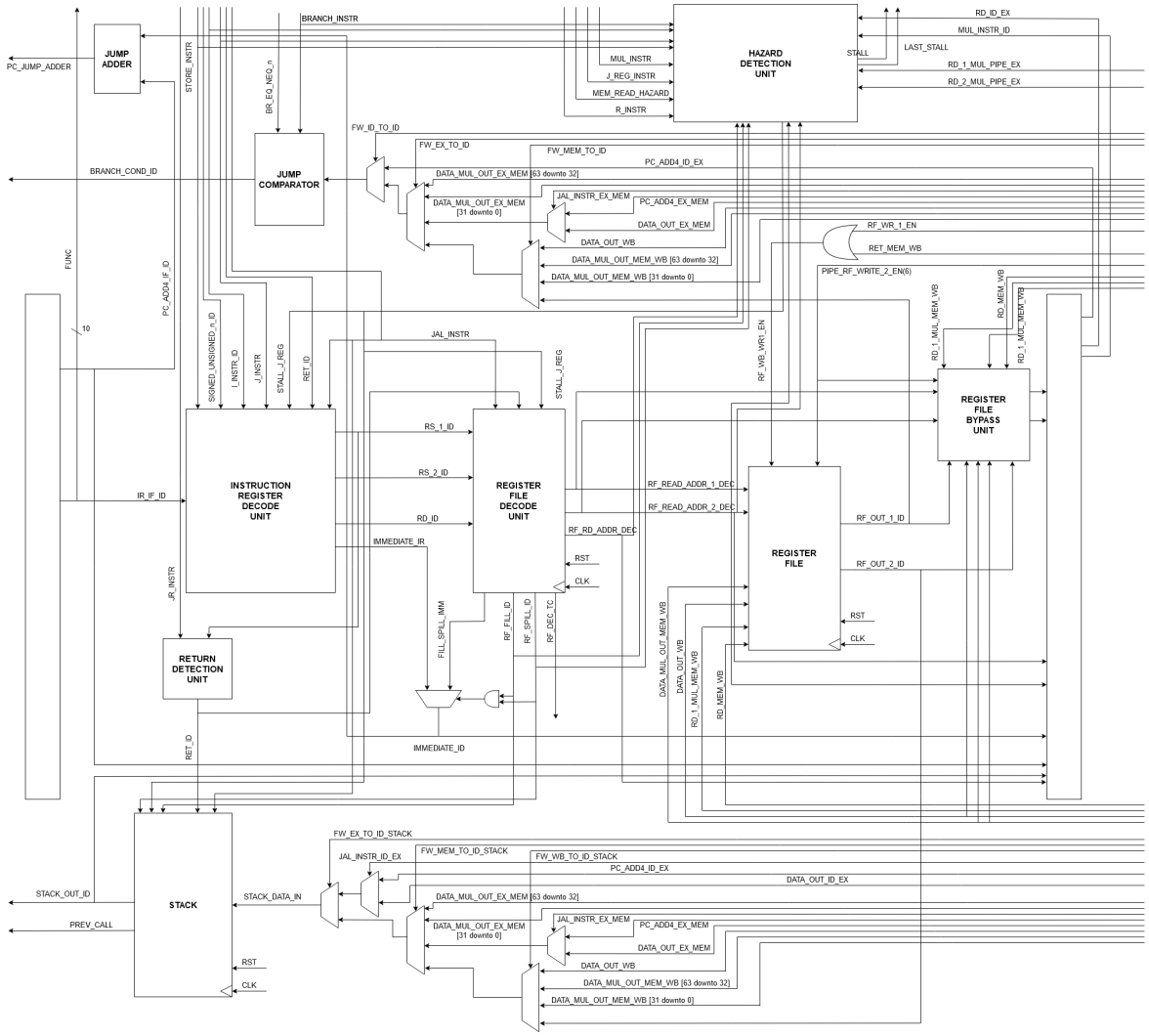

Figure 6.1: Decode stage schematic.

6.1 Instruction register decode unit

It is the combinational logic that is in charge of translating the instruction register into the different information and extending the immediate from 16 bits (or 26 if the instruction is a J type) to 32 bits. In order to perform this task, it takes two signal from the control word to identify the type of the instruction. One of the two signals is asserted when the incoming data is part of a J type instruction, while the other works in the same way but with a I type one (it is assumed to be a R type instruction if both those signals are not at '1'). The RD, RS1, RS2 and the IMMEDIATE signals are then assigned to their values following the two input signals already described.
There are though two particular cases in which the *instruction register decode unit* assigns the values in a different way:

- **Store instructions**: the RD field is assigned to the RS2 signal. This choice has been taken since the RD in this kind of operations indicates the register whose value has to be stored in memory. By performing this simple swap the data is automatically read from the register file.
- **Jump and link instructions**: since in this particular type of jump the actual value of the PC

has to be written inside the Link Register (R31 in this architecture) the RD field is set to point to the 31^{st} register.

Finally to perform correctly the extension of the immediate, a signal that carries the information about the numeric representation that has to be used is needed.
An estimation of area and power has been performed after the synthesis of the component and can be found in appendix C.1

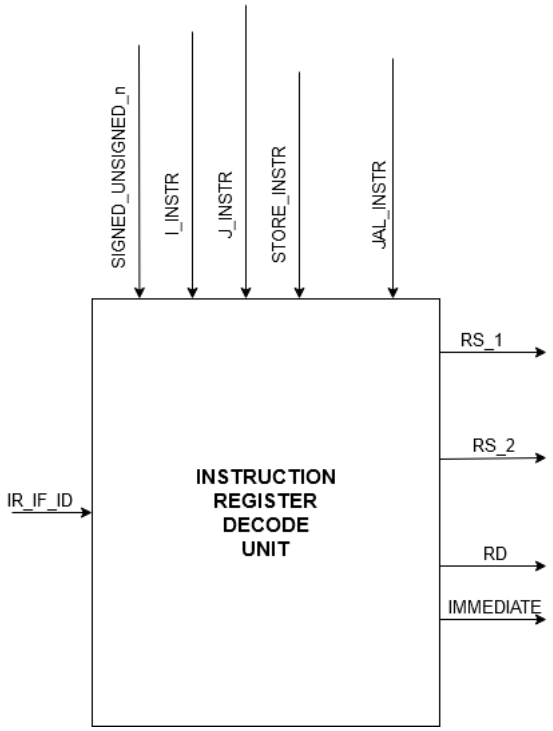

Figure 6.2: Instruction register decode unit entity view.

6.2 Register file

The register file is one of the main components of the processor. It is where all the register are placed and, therefore, where data is stored.
In the architecture of this processor, the register file contains 72 registers. The number of present registers is much bigger than the needed number since the architecture works with 32 registers, but this enhanced number is used in combination with the *register file decode unit* to implement a windowed register file.
In a windowed register file, the total number of register is divided into different windows and only one is used at a time. When a call request is received by the processor, the active window is shifted forward and when a new active window overlaps with one that has already been used the data is firstly saved into memory starting from the address 1023 and then the active window is changed. Similarly, when a return request is received, the window is shifted backward as long as the new active window overlaps with one that has been saved into memory. In this case, before going on the processor starts to take all the data from memory and bring it back into the register file. All this kind of operations are hidden to the user that will keep using the standard 32 registers of the DLX. Every operation related to the windowed register file management is performed by the *register file decode unit* explained in the following section. The design chosen for this register file allows the presence of 7 windows, each

one of them made of 24 registers which are shifted by 16 each time and 8 global registers that stay constant for all the windows (the global registers are the R0 and the registers from R25 to R31 from the user point of view, register with address 0 and registers from address 65 to 71 from the register file point of view).
The register file inserted in this architecture has been designed to support two writing and two reading ports. The two read ports are asynchronous and have been inserted in order to avoid delays during the decode phase and to be able to read the two possible source registers simultaneously. For what concerns the writing, two synchronous ports have been added. This choice has been made in order to avoid any kind of stalls due to the presence of the multiplication as a possible instruction. The second port is dedicated to the result of the multiplication and is configured to write in the register specified by the RD and in the following one (RD + 1) since the value to be written is represented on 64 bits. The two write ports are enabled through two input signals to avoid any undesired data to be saved in the register file.
An estimation of area and power has been performed after the synthesis of the component and can be found in appendix C.2

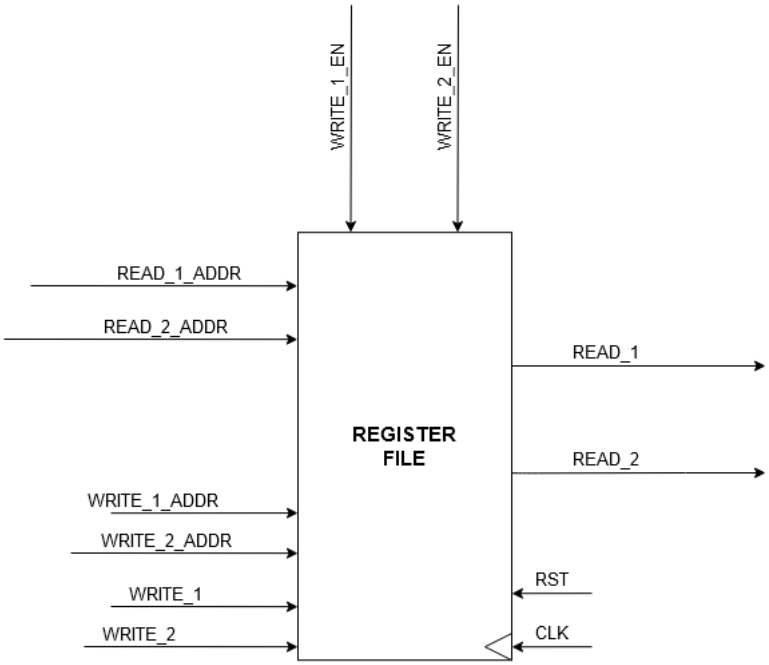

Figure 6.3: Register file entity view.

6.3 Register file decode unit

The *register file decode unit* is a necessary logic that allows to make the windowed register file working. It is in charge of translating the input register addresses accordingly to the active window.
By putting this element right after the *instruction register decoder* it is possible to transform the relative addresses requested by the user into absolute addresses. This additional unit simplifies a lot the rest of the architecture since no more checks have to be done in order to correctly perform the incoming instructions. In addition, the *register file decode unit* is in charge of handling the FILL and SPILL signals, which inform the *hazard detection unit* about the need of stalling in order to perform necessary operations in the register file. Also the immediate needed to correctly address the memory is generated by this unit and then sent in the execute stage.

It is a partially synchronous unit since the translation is done in a combinatory way, but all the logic related to the handling of the SPILL and FILL process is synchronous (there is also a counter that allows to change the read or write address at each clock cycle).
An estimation of area and power has been performed after the synthesis of the component and can be found in appendix C.3

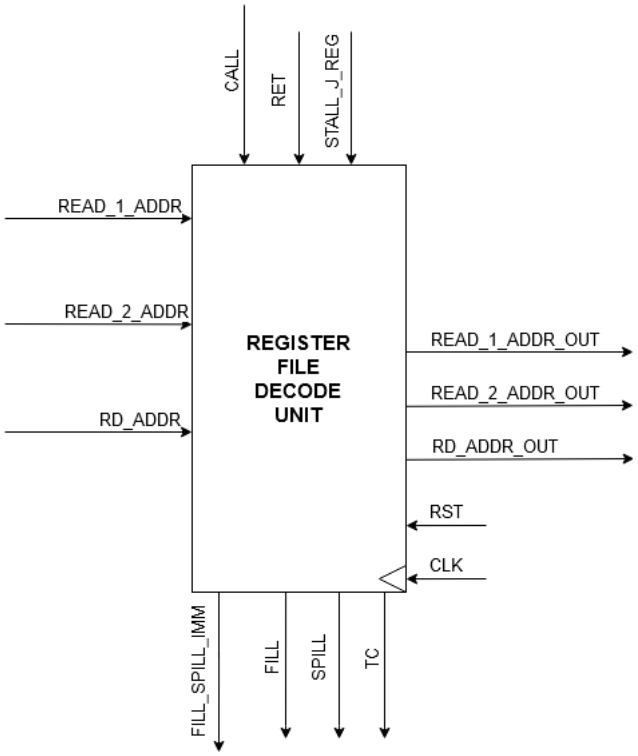

Figure 6.4: Register file decode unit entity view.

6.4 Hazard detection unit

The *hazard detection unit* is the main actor in the process of avoiding errors during the execution of instructions. Its main role is to inform the Control Unit about the presence of a situation that requires a stall, i.e. stop the current instruction in the decode stage for one or more clock cycles.
There are five main type of stalls inside this architecture:

- **Multiplication stall**: due to the fact that the multiplication instruction is executed in a pipelined execution unit and takes 8 clock cycles to complete. If an instruction that follows a multiplication requires the result of the latter as input value, the whole processor stops waiting for the multiplication to finish its execution stage. In particular this detection is possible by checking the presence of the source registers of the instruction in the decode phase, inside the cascade of registers used to delay the arrival of the multiplication destination register.
- **Write After Write (WAW)**: due to the presence of the pipelined multiplication. If an instruction that follows a multiplication writes its result in the same register the multiplication does, the processor has to wait the end of the multiplication otherwise the final result in the register would not be the one expected.

- **Load stall**: it is due to the presence of a load followed by another instruction that requires the value coming from the memory.
- **Branch stall**: since branches are entirely handled during the decode phase, it may be necessary to wait for the result of the execution stage if the register that has to be checked during the branch is modified right before the arrival of the branch instruction.
- **Jump stall**: during a jump instruction that involves a register, it may be necessary to wait for the result of this register to be evaluated in the execution stage or in the memory stage in case of a LOAD instruction.

As it can be seen from figure 6.5, there are two output signals called *STALL_J_REG_OUT* and *LAST_STALL*. The latter is used to make the *stack* and the *register file decode unit* stall (a specific signal is needed since those two elements work aside of the rest of the pipeline but are still synchronous), while the latter is necessary to avoid the delay of one clock cycle due to the fact that the whole pipeline is synchronous (the signal is asserted when the last clock cycle of the stall is reached so that the next clock cycle the processor can start to work again).
Other kind of stalls are avoided thanks to the presence of the *forwarding unit* that, in combination with some multiplexers, is able to take the values stored in the pipeline registers, which contain the updated value for the register specified in the destination register field, and use them as input for the following instructions. Also the presence of a two write port register file is a way to avoid stalls, in particular in the writeback stage.
An estimation of area and power has been performed after the synthesis of the component and can be found in appendix C.4

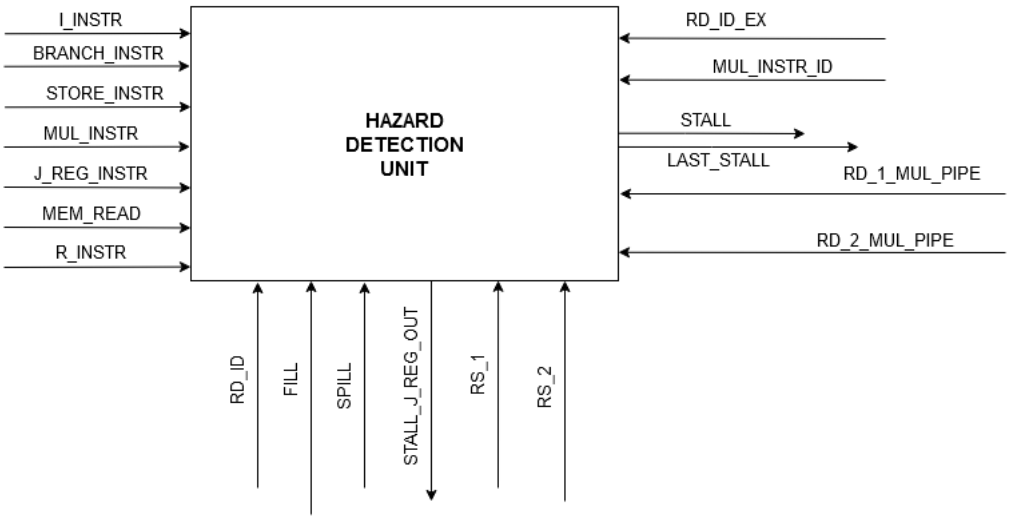

Figure 6.5: Hazard detection unit entity view.

6.5 Register file bypass unit

It is a very simple unit that has been inserted to allow the register file to write data in a register and simultaneously use it as output. In particular, this combinational logic is asserted when one of the two write ports (or both) are active. When active, it checks if one of the two possible source registers is equal to one of the two write addresses (it takes into account the fact that the multiplication writes in two registers at a time) and accordingly chooses the data coming from the register file or the data that is going to be written.

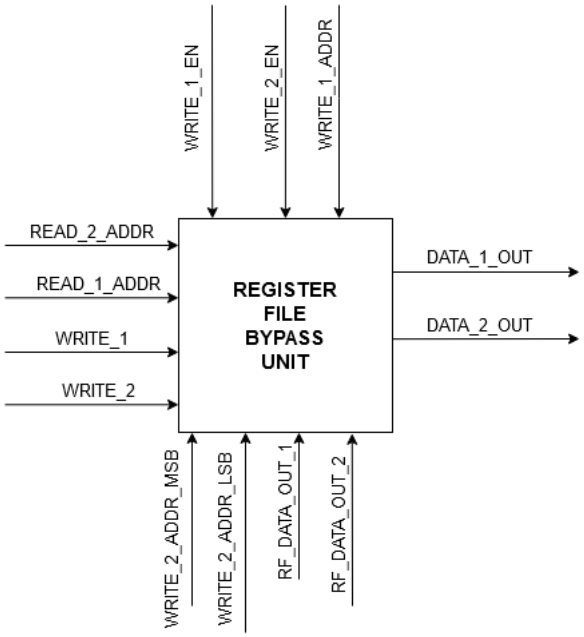

Figure 6.6: Register file bypass unit entity view.

6.6 Return detection unit

This unit is a combinational logic that simply checks if the incoming instruction corresponds to a return. In order to do that it takes a signal from the control word that is asserted when the instruction is a jump register one and takes the register address related to it. If the latter points to the link register (R31) the output is asserted to inform the other units (in particular the *register file decoder unit*).

6.7 Stack

The stack implemented in this architecture is a little memory where the current value of the link register is stored when a call is received by the processor. The memory is very small, 8 words of 32 bits, since the number of consecutive calls supported is given by the number of possible windows of the register file, that are only 7.
When a call is received, the value stored in the link register is saved during the decode phase inside this memory. The write process is synchronous and the value to be written is forwarded in order to avoid possible errors due to the data dependency. On the contrary, when a return is requested by the user the data inside the stack is read asynchronously and written in the link register. Simultaneously the read value is also sent to the program counter in order to correctly fetch the following instruction without having delays. The architecture does not need the presence of a stack pointer since it is integrated inside this unit and no instructions allow the user to interact with the stack (no POP or PUSH instructions).
On account of the need to disable the unit from writing when a FILL or a SPILL of the register file is needed, the *SPILL* and *FILL* signals are inputs of the stack as well as the *STALL_J_REG* signal that prevent the unit from working when a jump register instruction is stalled in decode waiting for the value of its source register to be calculated. The latter feature is possible combining the stack output with the *PREV_CALL* signal that is used to avoid the selection of the stack output if before the return a call was requested (in this case the value where to jump back is written inside the link

register and must be taken from there).
An estimation of area and power has been performed after the synthesis of the component and can be found in appendix C.5

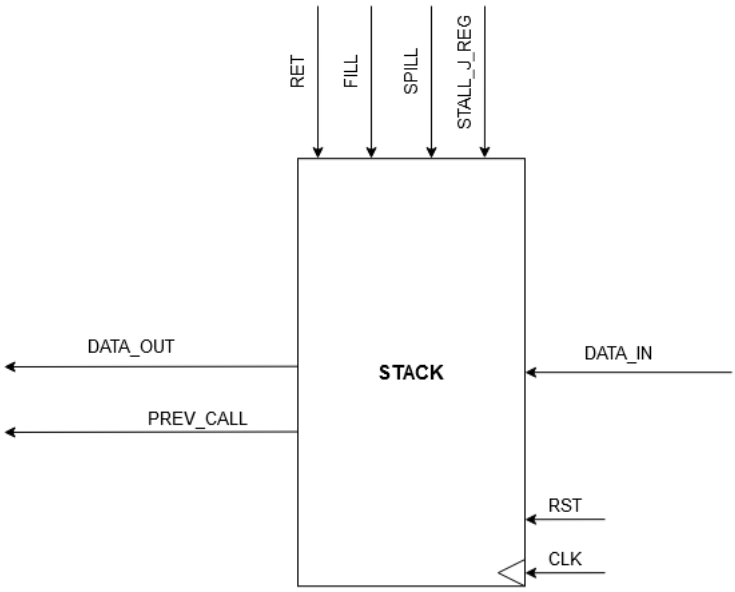

Figure 6.7: Stack entity view.

6.8 Jump comparator

The *jump comparator* is the logic in charge of checking the result of the requested branch. Only one input is necessary since the only two branches that are available in this processor ISA are the branch equal and not equal zero. The single output of this component is asserted when the comparison result is true (the requested branch is the equal zero and the input is a zero), not asserted otherwise.
The output of this component is used in combination with one of the output of the *BTB* to control the correctness of the program counter prediction made during the fetch phase and, eventually, put in the next program counter the valid value.
An estimation of area and power has been performed after the synthesis of the component and can be found in appendix C.7

6.9 Jump adder

This component is a simple adder whose only role is to add to the value of the program counter the offset requested by the user (if the instruction is a jump one). The output is then used to update the value of the program counter.
An estimation of area and power has been performed after the synthesis of the component and can be found in appendix C.6

CHAPTER 7

Decode/Execute pipeline registers

There are 12 decode/execute pipeline registers:

- **FILL_ID_EX** (1 bit) : brings to the execute stage the FILL signal;
- **SPILL_ID_EX** (1 bit) : brings to the execute stage the SPILL signal;
- **RF_OUT_1_ID_EX** (32 bit) : stores the output data of the read port 1 of the register file;
- **RF_OUT_2_ID_EX** (32 bit) : stores the output data of the read port 2 of the register file;
- **IMMEDIATE_ID_EX** (32 bits) : stores the extended immediate;
- **RD_ID_EX** (7 bits) : stores the destination register of the operation;
- **RS_1_ID_EX** (7 bits) : stores the source register 1 of the operation;
- **RS_2_ID_EX** (7 bits) : stores the source register 2 of the operation;
- **PC_ADD4_ID_EX** (32 bits) : stores the PC of the instruction in the ID stage incremented by 4;
- **STACK_OUT_ID_EX** (32 bits) : stores the output of the stack;
- **RET_ID_EX** (1 bit) : brings to the execute stage the RETURN signal;
- **JAL_INSTR_ID_EX** (1 bit) : brings to the execute stage the JAL_INSTR (i.e. call) signal;

All the registers are enabled by the ID_EX_PIPE_EN signal which is asserted by the control unit.

CHAPTER 8

Execute stage

The execute stage is where the instruction is executed, therefore the main computational unit of the processor (ALU) is placed here. In this step of the pipeline, operations in case of R-type instruction and I-type instruction are performed, while for the LOAD and STORE instructions the address for the access in memory is computed.
Going more into the details, the execute stage of the DLX is composed by the following components:

- **ALU**;
- **Forwarding Unit**
- **LHI instruction handler**
- **Destination register handler**
- **2 chains of registers**
- **7 MUX**

The architectural level scheme of this stage is shown in figure 8.1.

8.1 ALU

The Arithmetic and Logic Unit is the main actor in the execution of an instruction since it is able to perform many of the main operations of the processor ISA (the complete list is shown in table 8.1).
In order to be able to handle the high amount of instructions, the ALU can be divided into the following sub-unit:

- **adder/subtactor**;
- **comparator**;
- **logical unit**;
- **shifter**;
- **pipelined multiplier**;

In the following pages the architecture, characteristics and performance of each component that compose the ALU will be described more in details.

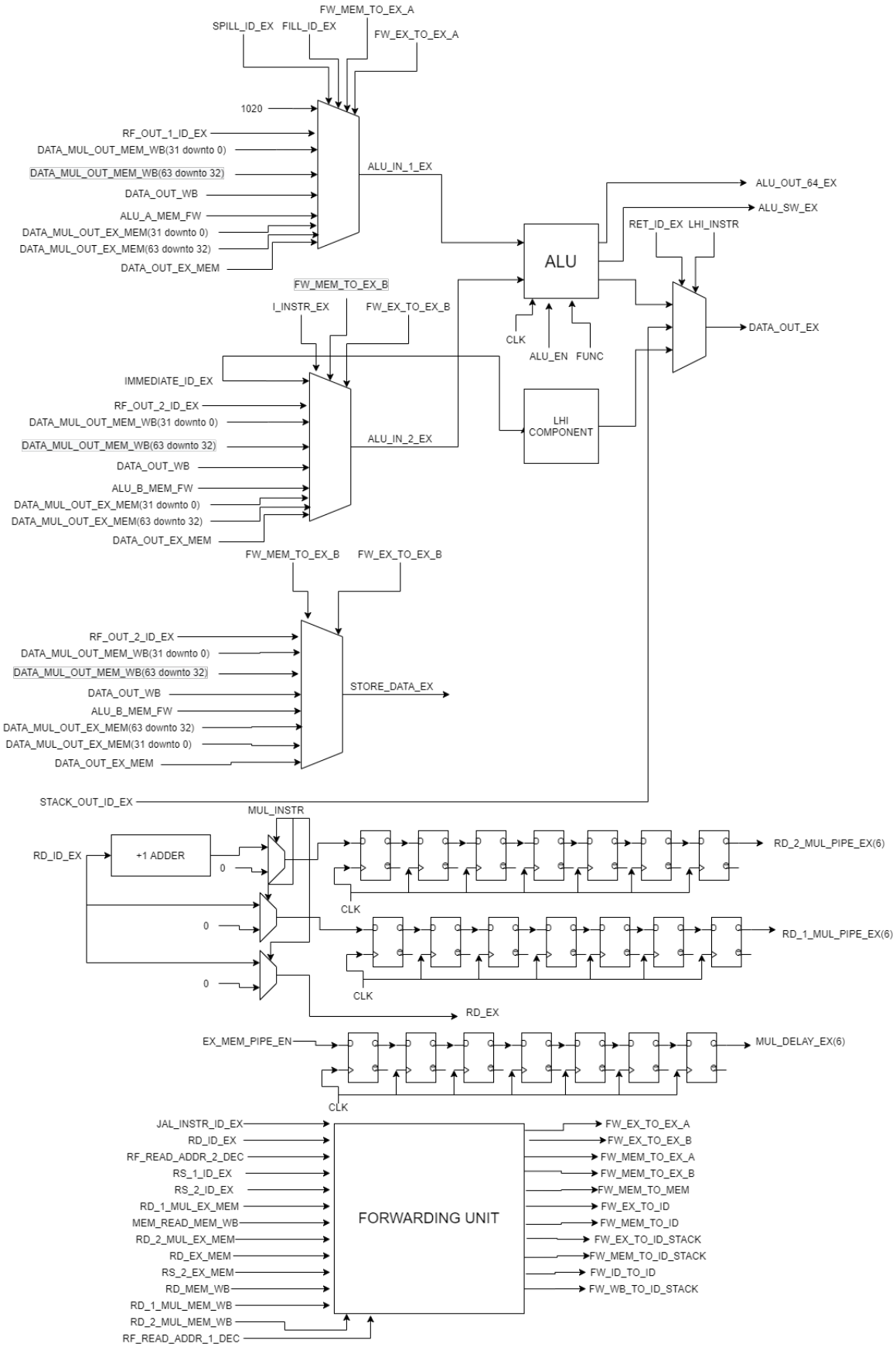

Figure 8.1: Architectural level scheme of the execute stage.

SIGNED	UNSIGNED
ADD	ADDU
SUB	SUBU
SGT	SGTU
SLT	SLTU
SGE	SGEU
SLE	SLEU
SEQ	
SNE	
AND	
OR	
XOR	
NAND	
NOR	
XNOR	
MUL	
SLL	
SRL	
SRA	

Table 8.1: List of the operations that can be performed by the ALU.

To correctly connect the ALU and its internal component to the rest of the processor, the interface reported in figure 8.2 has been designed.
It is composed by 4 input ports:

- **A,B**: 32-bits wide, connected to the two input operands coming from the ID/EX pipeline registers;
- **CLK**: connected to the system clock. This port is used only to manage the pipelined multiplier;
- **ALU_EN**: represent the enable of the component and it is connected to a signal coming from the Control Unit;
- **FUNC**: made of 5 bits, it is used to select the operation that must be performed.

and 3 output ports:

- **SW**: made of 2 bits where the MSB is the overflow flag, while the LSB is the carry flag (the two flags are used to inform about the status of the performed operation);
- **O_32**: 32-bits wide, it contains the result of the ALU operation with the exception of the multiplication;
- **O_64**: made of 64 bits, it represents the result of the multiplication.

For what concerns the internal interconnections, whose scheme is visible in figure 8.3, the inputs of the various units have been multiplexed in order to select between the ALU input signals (A and B) and words made of zeros according to the FUNC signal (which identify uniquely each operation that is supported by the ALU). The main reason for the insertion of this structure is to reduce as much as possible the power losses since in the chosen structure the sub-unit will work on data only when needed. The 32-bit output of the ALU is selected between the output of the inner units, choosing the one that produced data in the current clock cycle (once again FUNC is used as selection signal). The 64-bit output is directly connected to the multiplier one.

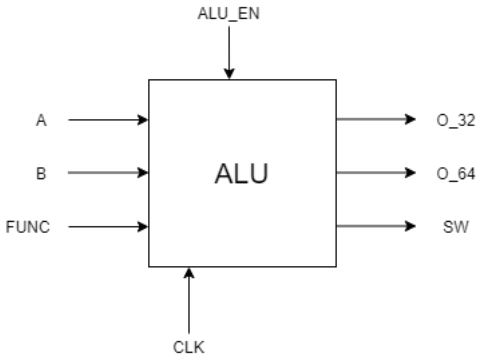

Figure 8.2: ALU interface signals.

The reports obtained during the synthesis are available in appendix D.1.

8.1.1 Adder / Subtractor

The adder/subtractor that has been designed has the same structure of the one present in the P4 processor, the architectural level view is shown in Figure 8.4.
It is composed by 3 main components:

- **PG network**;
- **carry generation block**;
- **sum generation block**.

The PG network receives as input the operands A and B together with the carry in that is used to distinguish a sum from a subtraction (SUM $\Rightarrow$ Cin = 0, SUB $\Rightarrow$ Cin = 1) and produces as output all the propagate and generate signals needed by the carry generation block.
The formulas of the propagate and generate signals are the following:

$$p(i) = A(i) \oplus B(i) \tag{8.1}$$

$$g(i) = A(i) \cdot B(i) \text{ for i from 1 to 31} \tag{8.2}$$

$$g(0) = (A(0) \cdot B(0)) + ((A(0) \oplus B(0)) \cdot C_{in}) \tag{8.3}$$

The carry generator block has been designed as a carry lookahead adder sparse tree. It is composed by two types of blocks that are the G block and PG block whose equations are:

$$G_{i:j} = G_{i:k} + P_{i:k} \cdot G_{k-1:j} \tag{8.4}$$

$$P_{i:j} = P_{i:k} \cdot P_{k-1:j} \tag{8.5}$$

The interconnection between the internal blocks that form the sparse tree is shown in Figure 8.5. The output of the sparse tree is a vector of 9 bits where each bit represents the carry in that goes as input to each one of the eight carry select block (CSB) that compose the sum generator. Each CSB is a simplified version of a carry select adder because the carry in is not given by the previous block but it is directly taken from the carry generator block. An additional feature present in the CSB that computes the MSB of the result is the capability of generating the carry and the overflow flags. The former is obtained connecting directly the last carry out of the sum (equation 8.6), while the latter is calculated with the equation 8.7.

$$C = S(31) \tag{8.6}$$

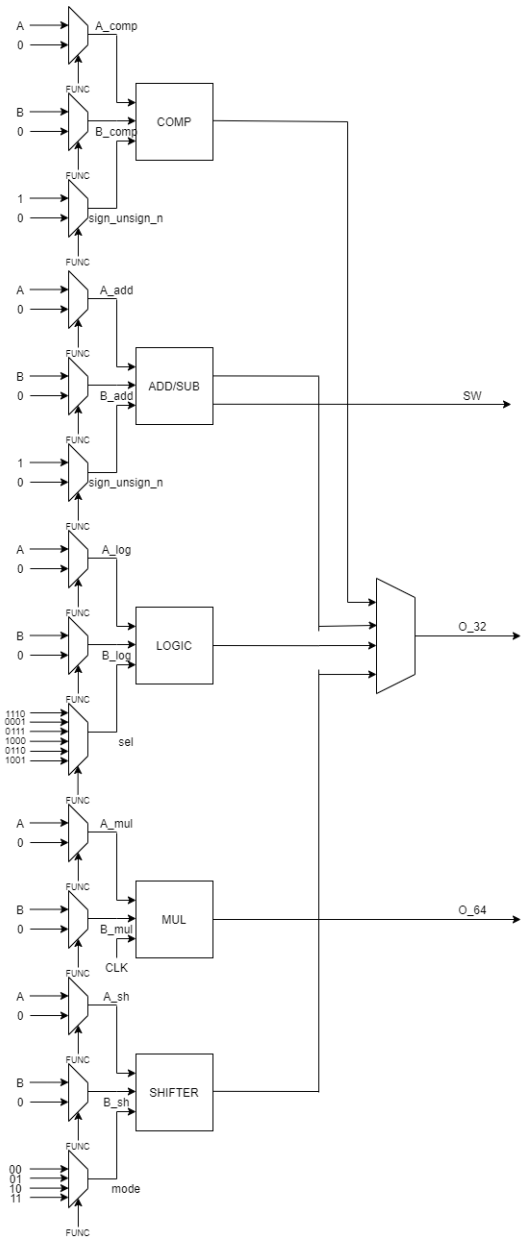

Figure 8.3: High level interconnection scheme of the ALU components. The enable signal is not present in the scheme.

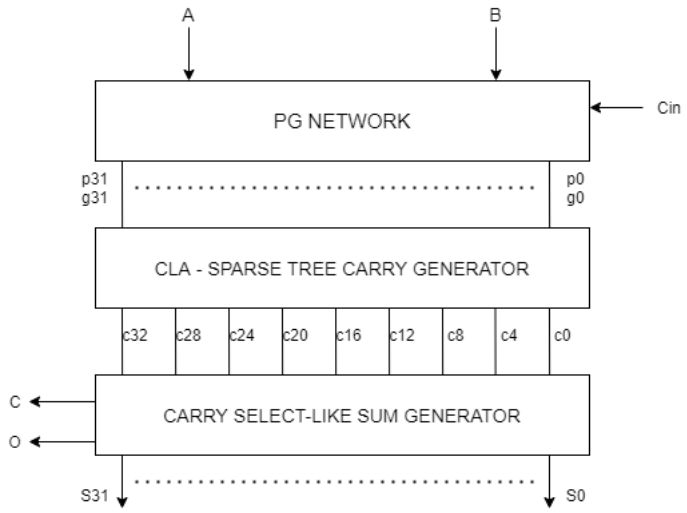

Figure 8.4: Architectural level scheme of the adder/subtractor designed.

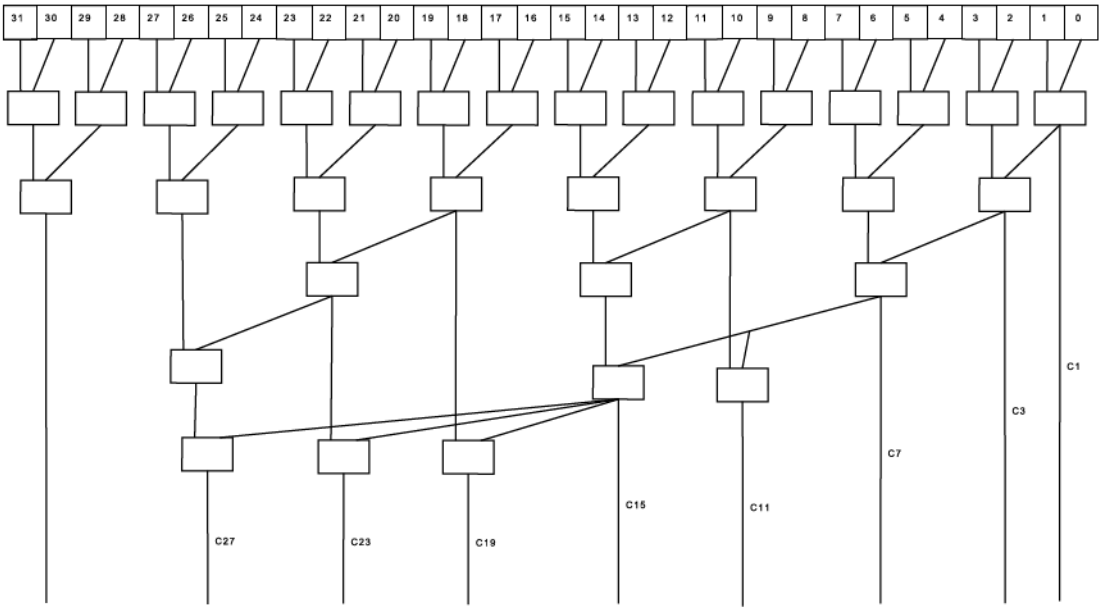

Figure 8.5: Pentium 4 sparse tree carry generator.

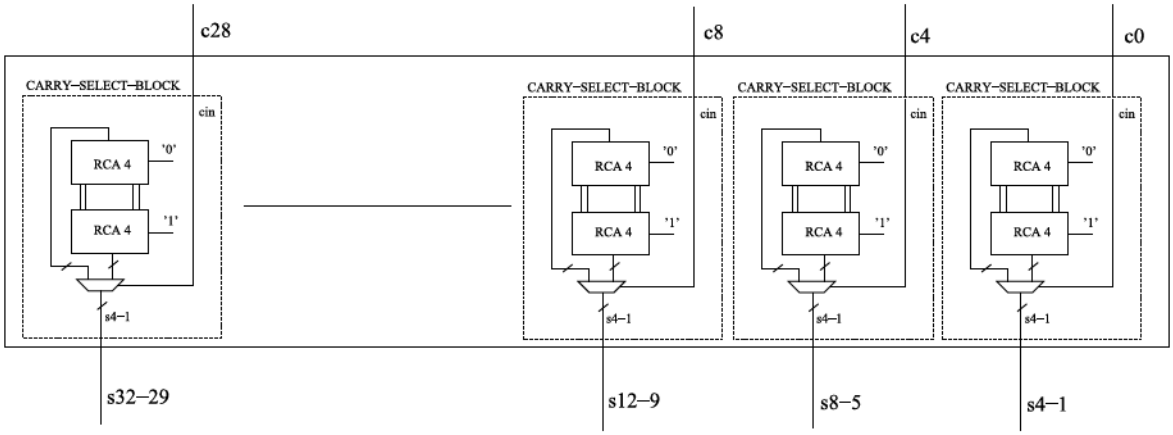

Figure 8.6: Pentium 4 adder sum generator block.

$$O = (S(31) \oplus A(31)) \cdot (A(31) \oplus B(31)) \tag{8.7}$$

The architectural level scheme of the sum generator block is reported in figure 8.6.
The adder has also been synthesized in order to estimate its critical path, area and power consumption. The reports obtained are shown in appendix D.1.1.

8.1.2 Comparator

The comparator inserted in this architecture works by comparing the inputs with bit by bit operations. In particular it has two different logics that allow to handle the signed and unsigned representations. For what concerns the former, the first step is to check the MSB. If the two MSBs are different, the greater number will be the one with MSB equal to 0. If the two bits that have just been checked are equal, the comparator will set two vectors where each bit correspond to a bit of the two inputs. In the first vector a bit will be set at one when the corresponding inputs bits follow the logic expression shown in 8.8. This indicates when the bit of A is higher than the bit of B. The same happens in the second vector, but with the opposite idea. As it can be seen in 8.9, the bit will be set to one when the bit of B is greater than the A one.
The last step is choose the correct couple of bits in the two vectors to generate all the outputs of the unit. It is done by using a priority encoder, whose task is to select the first couple, starting from the MSB, where at least one of the two vectors show a one.

$$A[i] \cdot \overline{B[i]} \tag{8.8}$$

$$\overline{A[i]} \cdot B[i] \tag{8.9}$$

The same procedure is followed with the unsigned numbers, with the exception that the MSB is treated in the same way the other bits are treated in the signed procedure.
The outputs are then obtained applying the following boolean equations:

- **AGB (A Greater than B)**: $vector\_AGB[i]$
- **BGA (B Greater than A)**: $vector\_BGA[i]$
- **AEB (A Equal B)**: $\overline{vector\_AGB[i] + vector\_BGA[i]}$
- **ANEB (A Not Equal B)**: $\overline{AEB}$

- **AGEB (A Greater Equal B)**: $vector\_AGB[i] + AEB$
- **BGEA (B Greater Equal A)**: $vector\_BGA[i] + AEB$

Where i is the index obtained by the priority encoder.
The synthesis reports of the unit are reported in the appendix D.1.2

8.1.3 Logical Unit

The logical unit that has been designed has the same structure of the one inside the OpenSPARC T2 processor. Its logic network is shown in Figure 8.7.

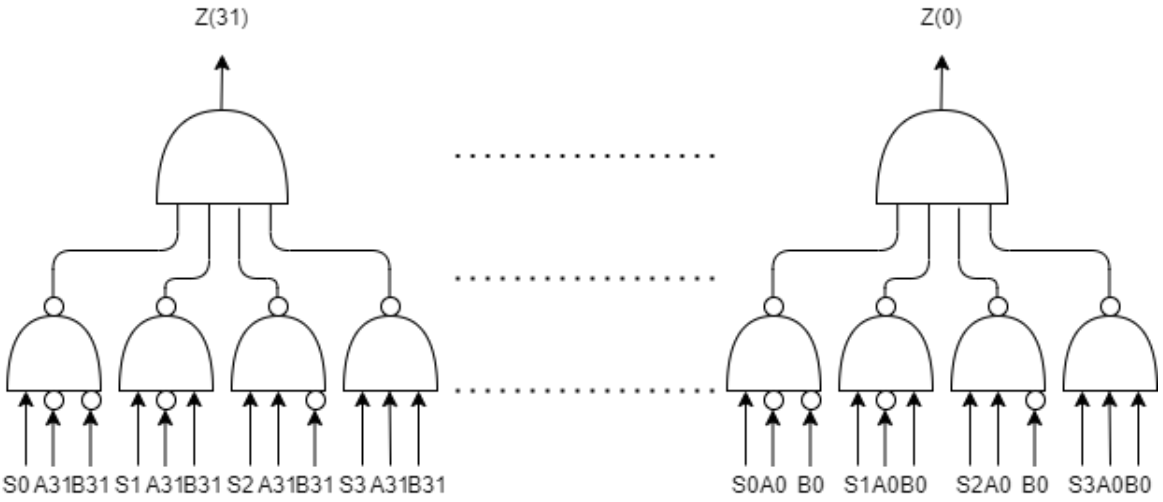

Figure 8.7: Logic circuit of the logical unit

The signals S0, S1, S2 and S3 are used to perform the desired operation. All the possible combinations are visible in Table 8.2.

S0	S1	S2	S3	OPERATION
0	0	0	1	AND
1	1	1	0	NAND
0	1	1	1	OR
1	0	0	0	NOR
0	1	1	0	XOR
1	0	0	1	XNOR

Table 8.2: combinations of the selection signals and the corresponding operation performed by the logical unit.

The logical unit has been synthetized using Synopsys Design vision in order to estimate its performance, area and power consumption. The reports obtained are visible in Appendix D.1.3.

8.1.4 Shifter

The shifter designed for this processor has the same architecture of the one present in the OpenSPARC T2 processor. Its operational behavior can be divided in 3 stages:

- generation of all the masks;

- choice of the correct mask;
- select the correct bits of the chosen mask.

Each operation has his own set of masks and the correct set to use (and so the operation to be performed) is chosen using a signal called MODE. Its possible values and the corresponding operations are shown in Table 8.3.

MODE	OPERATION
00	LOGICAL SHIFT RIGHT
01	ARITHMETIC SHIFT RIGHT
10	LOGIC SHIFT LEFT
11	UNUSED

Table 8.3: values of the MODE signal and the corresponding operation performed.

The masks are 8 bits longer than the operands, and each of them corresponds to the operand A as it is or shifted right or left (depending on the set of mask that is considered) by an amount of bits that is a multiple of 8. Since the operands are 32 bit long, inside the input B, that represents the amount of bits that the operand A should be shifted, the only bits that are relevant are the 6 LSBs. In particular the bits with index from 5 to 3 are used to select the correct mask inside the set, while the bits with index from 2 to 0 are used to select the correct bits inside the mask. The shifter has been synthetized to estimate its area, power consumption and performance. The value obtained from the various reports are shown in Appendix D.1.4.

8.1.5 Multiplier

The multiplier designed for this processor is a pipelined Booth multiplier. The operands are 32 bits long and the result produced is on 64 bits, which means that it will be stored into 2 consecutive registers inside the register file. The pipeline is composed of 8 stages, where each stage consists in 2 successive iterations of the Booth algorithm. Inside each step of the pipeline a mux encoded, that has as selection signal 3 consecutive bits of the operand B and produces in output one of the values visible in Table 8.4, is needed.

B(i+1)	B(i)	B(i-1)	OUTPUT
0	0	0	0
0	0	1	A
0	1	0	A
0	1	1	2A
1	0	0	-2A
1	0	1	-A
1	1	0	-A
1	1	1	0

Table 8.4: output of the mux encoded present in each iteration of the algorithm.

The output of the mux encoded is given as input to a 64 bit adder which sum that value with the result produced by the previous iteration (except for the first iteration of the first stage that sum the value produced by the mux encoded with 0). The data produced by the adder of the second iteration inside each stage is stored inside a pipeline register in order to make it available to the successive stage the next clock cycle. In order to correctly pipeline the multiplier, a register has been added between

each stage to store the partial result produced at the end of the stage and two chains of register with proper length for each stage have been used to correctly delay the arrival of the operands A and B. At the end of each iteration the operand A is multiplied by 4 (obtained shifting it left by 2 positions) and the window of 3 bits of the operand B is shifted left by 2 positions. A schematic vision of the pipeline registers is visible in Figure 8.8, while an architectural level view of each stage is shown in Figure 8.9.

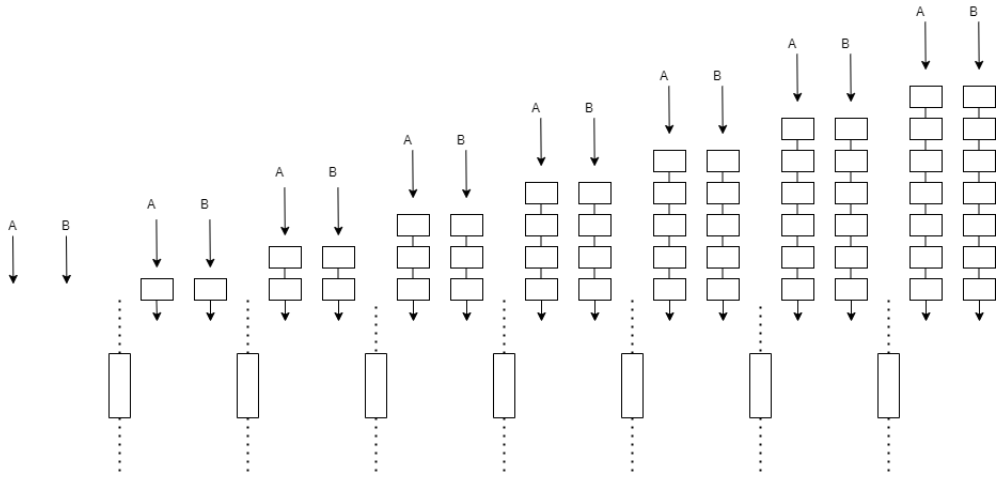

Figure 8.8: Schematic view of the multiplier pipeline registers.

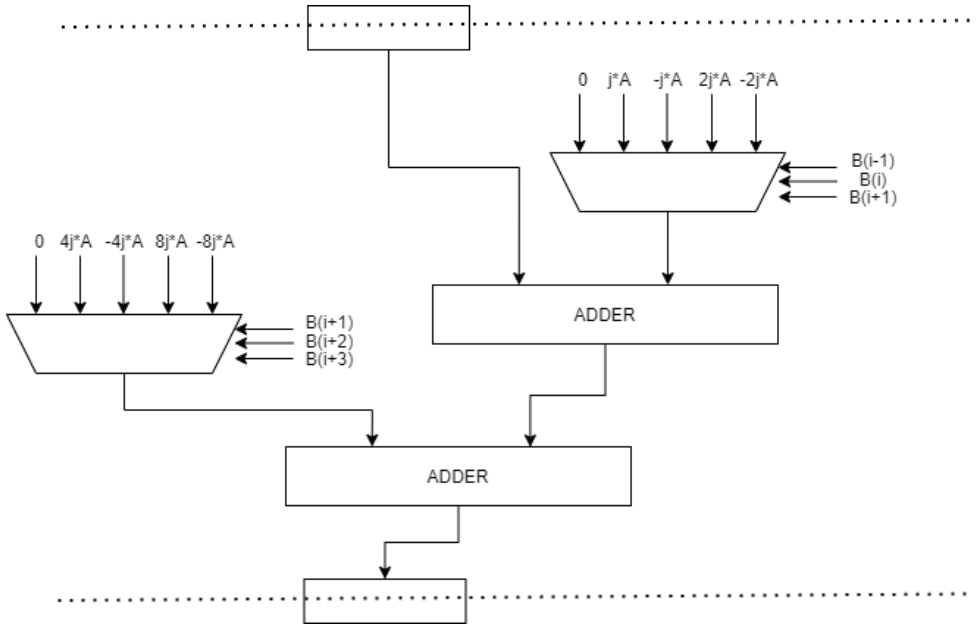

Figure 8.9: Architectural view of a generic multiplier pipeline stage

The multiplier has also been synthetized in order to obtain an estimation of its critical path, area and power consumption. The area,timing and power reports are visible in Appendix D.1.5.

8.2 Forwarding Unit

The forwarding unit is the component dedicated to detect possible data dependencies among the code instructions and to activate some signals that will be used by the various muxes along the datapath to correctly select the value to propagate between the default one and signals coming from successive stages. It is very useful because it allows to avoid a lot of stalls caused by data dependencies. In particular the forwarding unit that has been designed is able to:

- **Forward data from the EX stage to the EX stage**:
  useful to avoid stalls due to RAW hazards caused by two consecutive instruction. In order to perform the task it checks if one of the operands saved in the ID/EX pipeline register (RS_1_ID_EX and RS_2_ID_EX) is equal to the destination register saved in the EX/MEM pipeline register for both MUL and standard operation. Moreover it checks that the operand is different from 0 to avoid considering the STORE instruction (whose RD field is equal to 0). To exclude the case of a LOAD followed by an operation, the bit of the control word of the instruction that will enable the DRAM in the memory stage is checked to be 0.

  The VHDL code is the following:

```
if RS_1_ID_EX=RD_1_MUL_EX_MEM and RS_1_ID_EX/="0000000" then
        FW_EX_TO_EX_A <= "10";
elsif RS_1_ID_EX = RD_2_MUL_EX_MEM and RS_1_ID_EX /= "0000000" then
        FW_EX_TO_EX_A <= "01";
elsif RS_1_ID_EX = RD_EX_MEM and RS_1_ID_EX /= "0000000"
      and MEM_READ_WB = '0' then
        FW_EX_TO_EX_A <= "11";
else
        FW_EX_TO_EX_A <= "00";
end if;

if RS_2_ID_EX = RD_1_MUL_EX_MEM and RS_2_ID_EX /= "0000000" then
        FW_EX_TO_EX_B <= "10";
elsif RS_2_ID_EX = RD_2_MUL_EX_MEM and RS_2_ID_EX /= "0000000" then
        FW_EX_TO_EX_B <= "01";
elsif RS_2_ID_EX = RD_EX_MEM and RS_2_ID_EX /= "0000000"
      and MEM_READ_WB = '0' then
        FW_EX_TO_EX_B <= "11";
else
        FW_EX_TO_EX_B <= "00";
end if;
```

- **Forward data from MEM stage to EX stage**:
  useful to avoid stalls due to RAW hazards caused by two instructions that are separated by another instruction in the between. In this case the unit checks if the operand RS_1_ID_EX or RS_2_ID_EX is equal to the destination register saved in the MEM/WB pipeline stage for both MUL and standard operations.

  The VHDL code is the following:

```
if RS_1_ID_EX = RD_1_MUL_MEM_WB and RS_1_ID_EX /= "0000000" then
        FW_MEM_TO_EX_A <= "10";
elsif RS_1_ID_EX = RD_2_MUL_MEM_WB and RS_1_ID_EX /= "0000000" then
        FW_MEM_TO_EX_A <= "01";
```

```
elsif RS_1_ID_EX = RD_MEM_WB and RS_1_ID_EX /= "0000000" then
        FW_MEM_TO_EX_A <= "11";
else
        FW_MEM_TO_EX_A <= "00";
end if;

if RS_2_ID_EX = RD_1_MUL_MEM_WB and RS_2_ID_EX /= "0000000" then
        FW_MEM_TO_EX_B <= "10";
elsif RS_2_ID_EX = RD_2_MUL_MEM_WB and RS_2_ID_EX /= "0000000" then
        FW_MEM_TO_EX_B <= "01";
elsif RS_2_ID_EX = RD_MEM_WB and RS_2_ID_EX /= "0000000" then
        FW_MEM_TO_EX_B <= "11";
else
        FW_MEM_TO_EX_B <= "00";
end if;
```

- **Forward data from the MEM stage to the MEM stage**:
  prevents to stall the pipeline when there is a LOAD instruction followed by a STORE instruction. In this case the component check if the field RS2 of the STORE (that is in the MEM stage) is equal to the field RD of the LOAD (which is in WB).

  The VHDL code is shown below:

```
if RS_2_EX_MEM = RD_1_MUL_MEM_WB then
        FW_MEM_TO_MEM <= "10";
elsif RS_2_EX_MEM = RD_2_MUL_MEM_WB then
        FW_MEM_TO_MEM <= "01";
elsif RS_2_EX_MEM = RD_MEM_WB then
        FW_MEM_TO_MEM <= "11";
else
        FW_MEM_TO_MEM <= "00";
end if;
```

- **Forward data from the EX stage to the ID stage**:
  dedicated to the case when there is a JAL or a JALR instruction followed by a JR R31 or another JALR R31. In this case it is checked that both the field RD of the instruction in ID and the RD stored in the ID/EX pipeline register are equal to 71 (R31 decoded according to the windowed register file size) and that the instruction that is in the EX stage is a JAL or a JALR instruction. If this forward signal is enabled the value of PC+4 that is in the ID/EX pipeline register is written into the PC.

  The VHDL code is the following:

```
if RS_1_ID=RD_ID_EX and RS_1_ID="1000111" and JAL_INSTR_EX='1' then
        FW_ID_TO_ID <= '1';
else
        FW_ID_TO_ID <= '0';
end if;
```

- **Forward data from the MEM stage to the ID stage**:
  used to manage JR, JALR and BRANCH instructions. In particular it is checked that the field RS1 of the instruction in ID (the JR, JALR or BRANCH) is equal to the field RD present in

the EX/MEM pipeline registers and that those values are different from 0 (which is the reset default value). If this forward signal is enabled the result of the EX stage stored in the EX/MEM pipeline register is forwarded backwards to the ID stage.

The VHDL code is shown below:

```
if RS_1_ID = RD_1_MUL_EX_MEM and RS_1_ID /= "0000000" then
        FW_EX_TO_ID <= "10";
elsif RS_1_ID = RD_2_MUL_EX_MEM and RS_1_ID /= "0000000" then
        FW_EX_TO_ID <= "01";
elsif RS_1_ID = RD_EX_MEM and RS_1_ID /= "0000000" then
        FW_EX_TO_ID <= "11";
else
        FW_EX_TO_ID <= "00";
end if;
```

- **Forward data from WB stage to the ID stage**:
  has the same goal of the previous one, but in this case the value that is forwarded is the one in the WB stage. The VHDL code is the following:

```
if RS_1_ID = RD_1_MUL_MEM_WB and RS_1_ID /= "0000000" then
        FW_MEM_TO_ID <= "10";
elsif RS_1_ID = RD_2_MUL_MEM_WB and RS_1_ID /= "0000000" then
        FW_MEM_TO_ID <= "01";
elsif RS_1_ID = RD_MEM_WB and RS_1_ID /= "0000000" then
        FW_MEM_TO_ID <= "11";
else
        FW_MEM_TO_ID <= "00";
end if;
```

- **Forward data from EX, MEM and WB stage to the stack in ID stage**:
  since in the processor is present a windowed register file, a stack has been inserted to manage nested function calls and the purpose of these forward signals is to detect whether in one of the stage following the ID is present an instruction that has as destination register R31. In this case that value is forwarded backwards when there is a function call in order to be written into the stack. The VHDL code is shown below:

```
if RS_2_ID = RD_ID_EX and RS_2_ID = "1000111" then
        FW_EX_TO_ID_STACK <= '1';
else
        FW_EX_TO_ID_STACK <= '0';
end if;

if RS_2_ID = RD_1_MUL_EX_MEM and RS_2_ID = "1000111" then
        FW_MEM_TO_ID_STACK <= "10";
elsif RS_2_ID = RD_2_MUL_EX_MEM and RS_2_ID = "1000111" then
        FW_MEM_TO_ID_STACK <= "01";
elsif RS_2_ID = RD_EX_MEM and RS_2_ID = "1000111" then
        FW_MEM_TO_ID_STACK <= "11";
else
        FW_MEM_TO_ID_STACK <= "00";
end if;
```

```
if RS_2_ID = RD_1_MUL_MEM_WB and RS_2_ID = "1000111" then
        FW_WB_TO_ID_STACK <= "10";
elsif RS_2_ID = RD_2_MUL_MEM_WB and RS_2_ID = "1000111" then
        FW_WB_TO_ID_STACK <= "01";
elsif RS_2_ID = RD_MEM_WB and RS_2_ID = "1000111" then
        FW_WB_TO_ID_STACK <= "11";
else
        FW_WB_TO_ID_STACK <= "00";
end if;
```

The forward unit has also been synthetized using Synopsys Design vision to estimate its area, performance and power consumption. The reports generated are shown in Appendix D.2.

8.3 LHI instruction handler

It is a component specialized in the execution of the LHI instruction. It takes as input the 16 bits of the immediate and produces as output a 32 bit signal where the bits of the immediate are on the 16 MSB, while the 16 LSB bits are set to 0.

8.4 Destination register handler

It is an adder used to generate the second destination register of the multiplication since it has a result on 64 bits and so the result must be stored into two consecutive registers inside the register file. Therefore it takes as input the value of the ID/EX destination pipeline register and produces as output its value incremented by one.

8.5 Register chains

They are 3 chains of 7 registers: two are made of 7 bit registers and are used to delay the progress in the datapath of the destination register of the multiplication since it takes 8 cycles to complete. Both of them receives as input a significant value (different from 0) only when the instruction that is in the execution stage is a multiplication. In particular one of them receives the value of the ID/EX destination pipeline register, while the other is connected to the output of the destination register handler. The last chain is made by registers of 1 bit and it is used to delay the enable of the EX/MEM pipeline registers dedicated to the multiplication. It receives as input the enable signal for the EX/MEM pipeline registers and produces as output a signal that will be used as the enable for the EX/MEM pipeline registers dedicated for the multiplication.

8.6 Mux

In this stage there are 7 muxes that are used to correctly select the signal that will go in input to each component or in input to the EX/MEM pipeline registers depending on the instruction that is being performed. The role of each mux is described in the following:

- 2 muxes are used to select the operands in input to the ALU.

  The VHDL code that describe their behavior is:

```
mux_a_alu: process(FW_EX_TO_EX_A,FW_MEM_TO_EX_A,RF_OUT_1_ID_EX,
           DATA_OUT_WB,DATA_MUL_OUT_MEM_WB,
           DATA_MUL_OUT_EX_MEM, DATA_OUT_EX_MEM,
           SPILL_ID_EX, FILL_ID_EX)
variable ALU_A_MEM_FW: std_logic_vector(31 downto 0);
  begin
  if SPILL_ID_EX = '1' or FILL_ID_EX = '1' then
        ALU_IN_1_EX <= std_logic_vector(to_unsigned(1020,32));
  else
    case FW_MEM_TO_EX_A is
        when "00" => ALU_A_MEM_FW := RF_OUT_1_ID_EX;
        when "01" => ALU_A_MEM_FW := DATA_MUL_OUT_MEM_WB(31 downto 0);
        when "10" => ALU_A_MEM_FW := DATA_MUL_OUT_MEM_WB(63 downto 32);
        when others => ALU_A_MEM_FW := DATA_OUT_WB;
        end case;

        case FW_EX_TO_EX_A is
        when "00" => ALU_IN_1_EX <= ALU_A_MEM_FW;
        when "01" => ALU_IN_1_EX <= DATA_MUL_OUT_EX_MEM(31 downto 0);
        when "10" => ALU_IN_1_EX <= DATA_MUL_OUT_EX_MEM(63 downto 32);
        when others => ALU_IN_1_EX <= DATA_OUT_EX_MEM;
        end case;
  end if;
end process;
mux_b_alu:process(FW_MEM_TO_EX_B,FW_EX_TO_EX_B,RF_OUT_2_ID_EX,
          DATA_OUT_WB,DATA_MUL_OUT_MEM_WB,I_INSTR_EX,
          IMMEDIATE_ID_EX,DATA_MUL_OUT_EX_MEM,DATA_OUT_EX_MEM,
          SPILL_ID_EX, FILL_ID_EX)
  variable ALU_B_MEM_FW: std_logic_vector(31 downto 0);
  begin
        if I_INSTR_EX = '1' then
                ALU_IN_2_EX <= IMMEDIATE_ID_EX;
        else
          case FW_MEM_TO_EX_B is
            when "00" => ALU_B_MEM_FW := RF_OUT_2_ID_EX;
            when "01" => ALU_B_MEM_FW := DATA_MUL_OUT_MEM_WB(31 downto 0);
            when "10" => ALU_B_MEM_FW := DATA_MUL_OUT_MEM_WB(63 downto 32);
            when others => ALU_B_MEM_FW := DATA_OUT_WB;
          end case;

          case FW_EX_TO_EX_B is
            when "00" => ALU_IN_2_EX <= ALU_B_MEM_FW;
            when "01" => ALU_IN_2_EX <= DATA_MUL_OUT_EX_MEM(31 downto 0);
            when "10" => ALU_IN_2_EX <= DATA_MUL_OUT_EX_MEM(63 downto 32);
            when others => ALU_IN_2_EX <= DATA_OUT_EX_MEM;
          end case;
        end if;
  end process;
```

In case a SPILL or a FILL is being executed, the first mux selects 1020 because it is the starting

address of the DRAM section dedicated to store the windows of the register file, while the other one selects the immediate coming from the ID stage that will contain the offset to be subtracted to 1020 in order to compute the address where to store each of the 16 registers that compose the register file window. In all the other cases the first mux selects the value coming from the ID/EX pipeline register that stores the value read from the register file in the ID stage if there is no data to be forwarded; otherwise it selects the data coming from the EX/MEM pipeline register or the final data in the WB stage giving the priority to the one in the EX/MEM pipeline register because it belongs to a more recent instruction (therefore its value is the most up to date).

The other mux has the same behavior of the first one, but in addiction it distinguishes between a I-type instruction and a R-type instruction because in the first case it selects the immediate, while in the other the output of the second read port of the register file.

- a mux is used to select the value that will be stored in the EX/MEM pipeline register dedicated to the data that, in case of a STORE instruction, will be written in the DRAM. The VHDL code is the following:

```
mux_store_data: process(FW_MEM_TO_EX_B,FW_EX_TO_EX_B,RF_OUT_2_ID_EX,
                DATA_OUT_WB,DATA_MUL_OUT_MEM_WB,DATA_MUL_OUT_EX_MEM,
                DATA_OUT_EX_MEM)
  variable ALU_B_MEM_FW: std_logic_vector(31 downto 0);
  begin
    case FW_MEM_TO_EX_B is
        when "00" => ALU_B_MEM_FW := RF_OUT_2_ID_EX;
        when "01" => ALU_B_MEM_FW := DATA_MUL_OUT_MEM_WB(31 downto 0);
        when "10" => ALU_B_MEM_FW := DATA_MUL_OUT_MEM_WB(63 downto 32);
        when others => ALU_B_MEM_FW := DATA_OUT_WB;
    end case;

    case FW_EX_TO_EX_B is
        when "00" => STORE_DATA_EX <= ALU_B_MEM_FW;
        when "01" => STORE_DATA_EX <= DATA_MUL_OUT_EX_MEM(31 downto 0);
        when "10" => STORE_DATA_EX <= DATA_MUL_OUT_EX_MEM(63 downto 32);
       when others => STORE_DATA_EX <= DATA_OUT_EX_MEM;
    end case;
  end process;
```

In case no data must be forwarded it selects the data coming from the pipeline register storing the value of the second read port of the register file, otherwise it selects the data forwarded from the EX/MEM pipeline register or from the WB stage, giving the priority always to the one coming from the EX/MEM for the same reason explained before.

- another mux is used to select the data that will be stored in EX/MEM pipeline register dedicated to the value to be propagated to the WB stage where it will be written in the register file. It selects the output of the LHI component in case of a LHI instruction, the value of the ID/EX pipeline register containing the output of the stack (that is the value that must be written in the link register in case of nested function calls) in case of JR R31 instruction, otherwise the 32 bit output signal of the ALU.

  The VHDL is shown below:

```
mux_data_out_ex: process(LHI_INSTR,LHI_RESULT,RET_ID_EX,
```

```
                          STACK_OUT_ID_EX,ALU_OUT_32_EX)
begin
    if LHI_INSTR = '1' then
       DATA_OUT_EX <= LHI_RESULT;
    else
        if RET_ID_EX = '1' then
            DATA_OUT_EX <= STACK_OUT_ID_EX;
        else
            DATA_OUT_EX <= ALU_OUT_32_EX;
            end if;
    end if;
end process;
```

- 3 muxes are used to select the destination register to be propagated to the MEM stage (2 are dedicated for the multiplication and 1 for all the other operations). The ones dedicated to the MUL instruction selects respectively the value of RD stored in the ID/EX pipeline register and the output of the destination register handler in case the actual instruction is a MUL, otherwise 0. The other one selects the RD ID/EX pipeline register where the instruction is not a MUL, otherwise 0.

  The VHDL code is the following:

```
RD_1_MUL_MUX_OUT <= RD_ID_EX when MUL_INSTR = '1' else "0000000";
RD_2_MUL_MUX_OUT <= RD_2_MUL_MUX_IN when MUL_INSTR = '1' else "0000000";
RD_EX <= RD_ID_EX when MUL_INSTR = '0' else "0000000";
```

CHAPTER 9

Execute/Memory pipeline registers

There are 11 execute/memory pipeline registers:

- **RD_EX_MEM**(7 bits) : stores the destination register for instructions different from the multiplication;
- **RD_1_MUL_EX_MEM**(7 bits) : stores one of the 2 destination registers of the MUL instruction;
- **RD_2_MUL_EX_MEM**(7 bits) : stores the other destination register of the MUL instruction;
- **RS_2_EX_MEM**(7 bits) : stores the field RS2 of the instruction;
- **DATA_OUT_EX_MEM**(32 bits) : stores the result produced by the execute stage (DATA_OUT_EX signal);
- **DATA_MUL_OUT_EX_MEM**(64 bits) : stores the result of the multiplier;
- **STORE_DATA_EX_MEM**(32 bits) : stores the data to be written in memory in case of a store;
- **PC_ADD4_EX_MEM**(32 bits) : stores the value produced by the +4 adder during the fetch of that instruction;
- **RET_EX_MEM**(1 bit) : stores a signal that indicates if that instruction is a return from function;
- **JAL_INSTR_EX_MEM**(1 bit) : stores a signal that indicates if that instruction is a JAL or a JALR;
- **DRAM_ADDRESS_EX_MEM**(32 bits) : stores the address that will be given in input to the DRAM in the memory stage.

All the registers, with the exception of RD_1_MUL_EX_MEM, RD_2_MUL_EX_MEM and DATA_MUL_OUT_E_MEM which have as enable signal the signal exiting from the chain of registers managing the delay of the MUL instruction control signals, are enabled by the signal coming from the CU called EX_MEM_PIPE_EN.

CHAPTER 10

Memory stage

The memory stage is the part of the pipeline dedicated to access the DRAM, both in reading (LOAD) and in writing (STORE).
The components present in this stage are:

- DRAM;
- 1 mux;
- 1 chain of registers;
- Load Unit.

Their interconnections are shown in the architectural level scheme shown in figure 10.1.

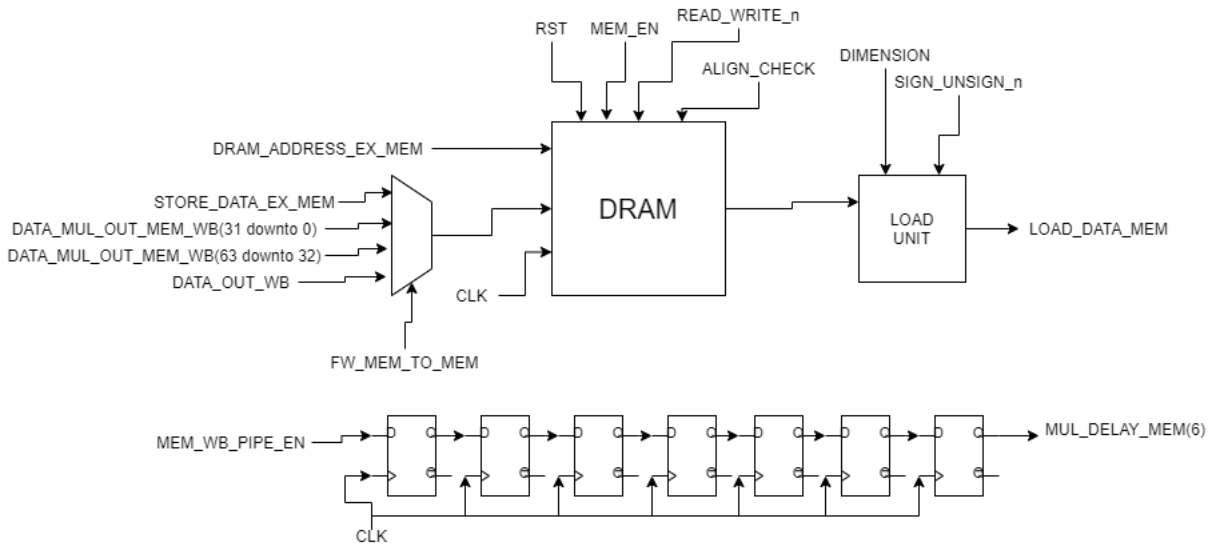

Figure 10.1: Architectural level scheme of the memory stage.

10.1 Mux

The mux is used to correctly select the signal to give as input to the DRAM. It has as selection signal the FW_MEM_TO_MEM signal and as inputs:

- **STORE_DATA_EX_MEM**: will be chosen if there is no need of forward data;
- **DATA_MUL_OUT_EX_MEM(31 downto 0) and DATA_MUL_OUT_EX_MEM(63 downto 32)**: will be chosen if one of the destination MEM/WB pipeline registers dedicated to the MUL is equal to the register that must be written;
- **DATA_OUT_WB**: will be chosen if the destination MEM/WB pipeline register is equal to the register that must be written.

The VHDL code describing this mux is shown below.

```
mux_dram_in : process(FW_MEM_TO_MEM, STORE_DATA_EX_MEM,
                      DATA_MUL_OUT_MEM_WB, DATA_OUT_WB)
begin
        case FW_MEM_TO_MEM is
            when "00" => DRAM_DATA_IN <= STORE_DATA_EX_MEM;
            when "01" => DRAM_DATA_IN <= DATA_MUL_OUT_MEM_WB(31 downto 0);
            when "10" => DRAM_DATA_IN <= DATA_MUL_OUT_MEM_WB(63 downto 32);
            when others => DRAM_DATA_IN <= DATA_OUT_WB;
        end case;
end process;
```

10.2 DRAM

The DRAM is not a real component of the DLX processor, but in order to make the explanation of the memory stage more clear, it will be briefly described. It is a 1 Kbyte read and write memory that has been described in VHDL in a purely behavioral way since it is used only for simulation purpose (it is not synthesized). It is a synchronous in writing and asynchronous in reading memory, with an enable signal, a reset and another signal called ALIGN_CHECK that is used to make the address aligned with the size of the data that has to be read or written. In particular if the data is a byte the address is left unchanged; if the data is an half word, the LSB of the address is cleared (changed to 0); while if it is a word, the 2 LSB are cleared. Moreover, since the processor has a big endian addressing mode, the starting address corresponds with the MSB of the word that will be read or written, while the rest of the word is composed by the memory words pointed by the 3 successive addresses.
For what concerns the LOAD, independently on the size of the data that must be read, the memory produces as output an entire word starting from the memory cell pointed by the address given as input to the memory cell pointed by the address incremented by 3. The value will be then modified by the Load Unit, according to the requested operation.

10.3 Load Unit

The Load Unit has the role of modifying the value produced as output by the DRAM depending on the size of the data that must be read. Its interface, shown in figure 10.2, is composed by the following signals:

- **MEM_OUT**(32 bits) : is the output of the DRAM;
- **DIMENSION**(2 bits) : indicates the size of the data to be read as follow:
  - 00: the unit is disabled, the output is set to all zeros.
  - 01: the read data is a byte.

  - 10: the read data is a half-word.
  - 11: the read data is a full word.

- **SIGN_UNSIGN_n**(1 bit) : indicates if it is a signed or an unsigned instruction;
- **LHU_OUT**(32 bits) : is the read value produced as output by the Load Unit.

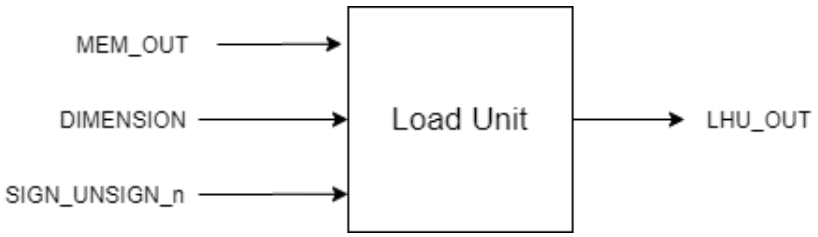

Figure 10.2: Interface of the Load Unit.

The output produced will put the requested word dimension starting from the LSBs. Therefore the expected output will be:

- $(0)^{24}$ ## MEM in case of unsigned load byte;
- $(MEM_7)^{24}$ ## MEM in case of signed load byte;
- $(0)^{16}$ ## MEM in case of unsigned load half-word;
- $(MEM_7)^{16}$ ## MEM in case of signed load half-word;
- MEM in case of load word;

The Load Unit has been synthesized using Synopsys Design Vision to estimate the power consumption, area and performance. The reports generated are visible in Appendix E.1.

10.4 Chain of register

It is a chain of 7 registers made of 1 bit that is used to delay by 7 clock cycles the signal that will be used as enable for the MEM/WB pipeline registers dedicated to the MUL instruction.
The VHDL code is the following:

```
mul_ctrl_sig_pipe_mem: process(CLK, RST)
begin
        if RST = '0' then
                MUL_DELAY_MEM <= (others => '0');
        elsif CLK = '1' and CLK'event then
                for i in 1 to 6 loop
                                MUL_DELAY_MEM(i) <= MUL_DELAY_MEM(i-1);
                end loop;
                MUL_DELAY_MEM(0) <= MEM_WB_PIPE_EN;
        end if;
end process;
```

CHAPTER 11

MEMORY/WRITE BACK PIPELINE REGISTERS

There are 9 memory/write pipeline registers:

- **RD_MEM_WB**(7 bits) : contains the destination register for the instructions different from the MUL;
- **RD_1_MUL_MEM_WB**(7 bits) : stores the first destination register of the MUL instruction;
- **RD_2_MUL_MEM_WB**(7 bits) : contains the second destination register of the MUL instruction;
- **DATA_OUT_MEM_WB**(32 bits) : stores the result computed in the EX stage that has been propagated till the WB;
- **DATA_MUL_OUT_MEM_WB(64 bits)** : contains the result of the MUL instruction computed in EX stage and propagated till the WB stage;
- **DATA_LOAD_MEM_WB**(32 bits) : stores the value produced by the Load Unit;
- **MEM_READ_MEM_WB**(1 bit) : contains the MEM_READ bit coming from the control word in the MEM stage;
- **PC_ADD4_MEM_WB**(32 bits) : stores the value of the program counter of the current instruction +4 produced by the PC adder in IF stage and propagated till the WB stage;
- **RET_MEM_WB**(1 bit) : stores a bit that indicates if the current instruction is a return from function.

CHAPTER 12

Write back stage

The write back stage is dedicated to write some data into a register inside the register file or into the stack in case of a forward. The components present in this stage are:

- **2 muxes**;
- **a chain of registers**.

The architectural level scheme of this stage is shown in Figure 12.1.

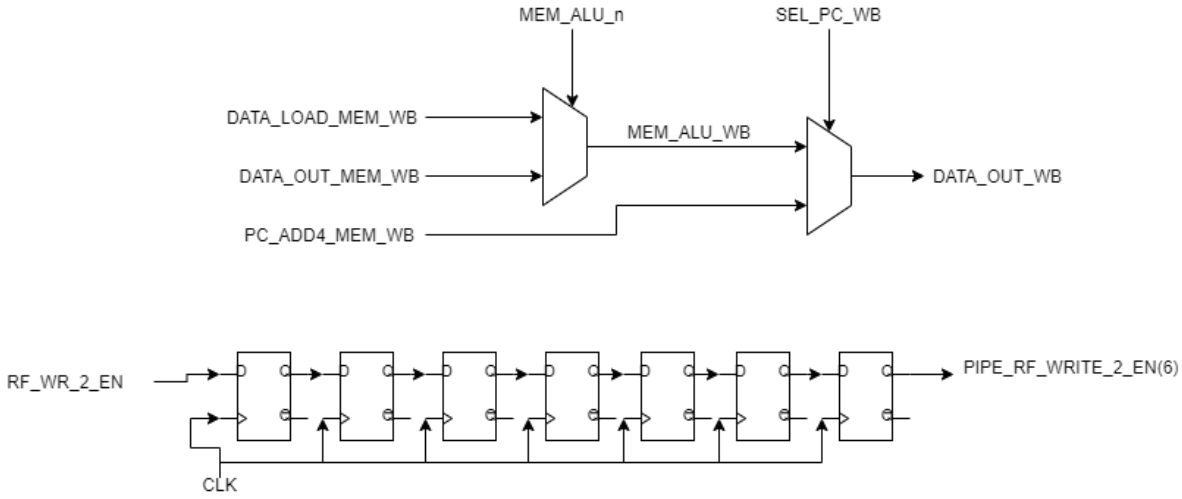

Figure 12.1: Architectural level scheme of the WB stage

12.1 MUX

The first mux is driven by the MEM_ALU_n signal that indicates if the data to propagate is the one coming from the DRAM in the memory stage or is the one of the EX stage propagated to the MEM/WB pipeline registers. The data coming from the DRAM will be selected only if the instruction is a LOAD, otherwise the other signal will be propagated to the next mux. The second mux has as selection signal SEL_PC_WB and as input signals the output of the previous mux and the value of PC+4 computed during the IF stage of the current instruction and propagated through the pipeline registers till here. The PC+4 is selected only if the the current instruction is a JAL or a JALR because

it must be written into the link register (r31 in the register file). The VHDL code describing these muxes is the following.

```
MEM_ALU_WB <= DATA_LOAD_MEM_WB when MEM_ALU_n = '1' else DATA_OUT_MEM_WB;
DATA_OUT_WB <= PC_ADD4_MEM_WB when SEL_PC_WB = '1' else MEM_ALU_WB;
```

12.2 Chain of registers

This chain is composed by 7 registers of 1 bit and is used to delay the enable signal of the write port 2 of the register file, which is the one dedicated to the MUL instruction. The VHDL code that describes it is shown below.

```
wr2_en_pipe: process(CLK)
begin
        if RST = '0' then
                for i in 0 to 6 loop
                        PIPE_RF_WRITE_2_EN(i) <= '0';
                end loop;
        elsif CLK = '1' and CLK'event then
                for i in 1 to 6 loop
                        PIPE_RF_WRITE_2_EN(i) <= PIPE_RF_WRITE_2_EN(i-1);
                end loop;
                PIPE_RF_WRITE_2_EN(0) <= RF_WR_2_EN;
        end if;
end process;
```

Part III

SYNTHESIS AND ROUTING

CHAPTER 13

Synthesis and post-synthesis simulation

After the simulation of the entire processor and the verification of its correct behavior, the synthesis has been performed using *Synopsys Design Vision*. In order to automatize the synthesis, a script has been used and its code is shown in appendix F.1.
To reduce the total dynamic power consumed by the system, during the synthesis the clock gating technique has been applied. In particular the gating element used is shown in figure 13.1. It is composed by a latch active on the negative level of the clock because in this way when the clock is at logic level 1, the output of the latch is stable and so glitches are avoided. Then the output of the latch goes in input to an AND gate together with the clock signal and its output is the clock received by the registers.

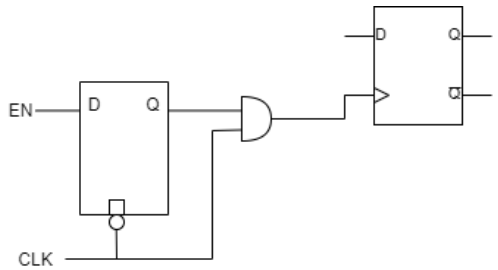

Figure 13.1: Gating element used during the synthesis.

The synthesis has been run several times with the aim of finding the minimum value for both clock period and maximum combinational delay between two synchronous elements or system ports. The value that has been found is 2.3 ns which means that the clock frequency is around 435 MHz. At the end of the synthesis, reports have been produced to estimate the timing of the critical path, the total static and dynamic power consumed and the area occupied by the processors. Those reports are visible in the appendix F.2.
Once the synthesis was completed, a post-synthesis simulation has been performed in order to check that the synthesized design produced by Synopsys behaves in a correct way. In order to do that, a verilog netlist describing the design has been produced by the tool and it has been used in Modelsim as a substitute of the original VHDL code to perform another simulation using the same testbenches used for the behavioral simulation. When the behavior has been verified, the layout design process was started.

CHAPTER 14

Placing and routing

The last step of the design is creating the physical layout of the whole architecture. In order to perform such a task, the commercial tool *Innovus* has been used.
The step that led to the final design are:

- Addition of the power rings and the power stripes that have been mapped to *M9* and *M10* layers.
- Placing of standard cells and of filler
- Pin editing, that have been inserted as follow:
  - top: ALIGN_CHECK, DRAM_ADDRESS, DRAM_DATA_IN, DRAM_ENABLE, DRAM_READ_WRITE_n;
  - right: DRAM_DATA_OUT, IRAM_DATA;
  - bottom: IRAM_ADDRESS;
  - left: CLK, RST;
- Routing
- Post-routing optimization
- Timing extraction and slack violation verification
- RC extraction
- Connectivity and geometry verification

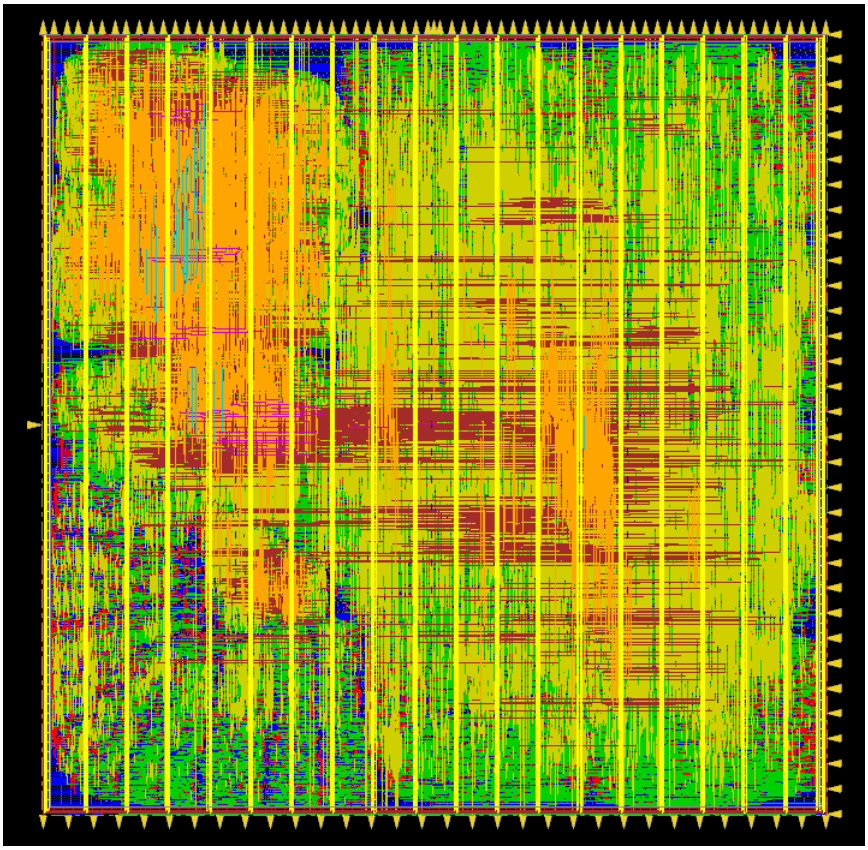

Figure 14.1: Physical layout scheme produced by *Innovus*

Part IV

APPENDICES

APPENDIX A

Components synthesis script

During the design of the whole processor, when an internal unit was completely designed and tested, it was synthesized in order to be able to estimate what would the best achievable clock frequency be. Consequently, the synthesis aim was to minimize as much as possible the timing of the components. The script that has been used to automatize as much as possible the process is here reported and it was run only after the files analysis and the elaboration of the wanted architecture have been performed.

```
# VARIABLES #
set constraint 0.63
set file_name "adder_subtractor"

# SYNTHESIS PROCESS #
set_max_delay -from [all_inputs] -to [all_outputs] $constraint
compile -map_effort high
report_timing > ./reports/${file_name}_timing.txt
report_area > ./reports/${file_name}_area.txt
report_power > ./reports/${file_name}_power.txt
```

Listing A.1: Synthesis script of a non clocked component

```
# VARIABLES #
set constraint 0.63
set file_name "adder_subtractor"

# SYNTHESIS PROCESS #
set_max_delay -from [all_inputs] -to [all_outputs] $constraint
create_clock -name "CLK" -period $constraint CLK
compile -map_effort high
report_timing > ./reports/${file_name}_timing.txt
report_area > ./reports/${file_name}_area.txt
report_power > ./reports/${file_name}_power.txt
```

Listing A.2: Synthesis script of a clocked component

In order to correctly synthesize and save the reports it is necessary to change the first two lines with the wanted constraint and with a relevant name that will be used to save the reports produced by Synopsys.

APPENDIX B

Fetch post synthesis reports

B.1 Branch target buffer

Power report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
BTB                   5K_hvratio_1_1    NangateOpenCellLibrary


Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  = 116.9689 mW   (98%)
  Net Switching Power  =   2.9423 mW    (2%)
                         ---------
Total Dynamic Power    = 119.9113 mW  (100%)

Cell Leakage Power     =   2.1892 mW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %
)  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000            0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000            0.0000  (   0.00%)
register       1.1594e+05            2.0687        1.2940e+06        1.1724e+05  (  96.02%)
sequential         0.0000            0.0000            0.0000            0.0000  (   0.00%)
combinational  1.0276e+03        2.9401e+03        8.9531e+05        4.8632e+03  (   3.98%)
--------------------------------------------------------------------------------------------------
Total          1.1697e+05 uW     2.9422e+03 uW     2.1893e+06 nW     1.2210e+05 uW
```

Area report

```
Number of ports:                          135
Number of nets:                         64218
Number of cells:                        64099
Number of combinational cells:          47458
Number of sequential cells:             16640
Number of macros:                           0
Number of buf/inv:                      19795
Number of references:                      33

Combinational area:       49211.330532
Noncombinational area:    75451.695356
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          124663.025888
Total area:                 undefined
```

Timing report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: full_empty_n_reg[249]
              (rising edge-triggered flip-flop clocked by CLK)
  Endpoint: full_empty_n_reg[249]
            (rising edge-triggered flip-flop clocked by CLK)
  Path Group: CLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  BTB                5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock CLK (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  full_empty_n_reg[249]/CK (SDFFR_X1)      0.00 #     0.00 r
  full_empty_n_reg[249]/Q (SDFFR_X1)       0.07       0.07 f
  U71785/ZN (AOI22_X1)                     0.07       0.14 r
  full_empty_n_reg[249]/SE (SDFFR_X1)      0.01       0.15 r
  data arrival time                                   0.15

  clock CLK (rise edge)                    0.96       0.96
  clock network delay (ideal)              0.00       0.96
  full_empty_n_reg[249]/CK (SDFFR_X1)      0.00       0.96 r
  library setup time                      -0.09       0.87
  data required time                                  0.87
  -----------------------------------------------------------
  data required time                                  0.87
  data arrival time                                  -0.15
  -----------------------------------------------------------
  slack (MET)                                        0.72


  Startpoint: PC_CHECK[2]
              (input port)
  Endpoint: NEW_PC[0] (output port)
  Path Group: default
  Path Type: max
```

```
Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
BTB                5K_hvratio_1_1        NangateOpenCellLibrary

Point                                    Incr       Path
-----------------------------------------------------------
input external delay                     0.00       0.00 r
PC_CHECK[2] (in)                         0.00       0.00 r
U77318/ZN (INV_X1)                       0.02       0.02 f
U79124/ZN (NOR2_X2)                      0.10       0.12 r
U45396/ZN (AND2_X1)                      0.08       0.20 r
U77172/ZN (NAND2_X1)                     0.04       0.24 f
U35861/Z (BUF_X1)                        0.05       0.29 f
U36535/ZN (INV_X2)                       0.08       0.37 r
U36226/ZN (NAND2_X1)                     0.04       0.42 f
U36228/ZN (AND3_X1)                      0.04       0.46 f
U36013/ZN (AND4_X1)                      0.04       0.50 f
U36010/ZN (AND4_X1)                      0.04       0.55 f
U79888/ZN (NAND4_X1)                     0.03       0.58 r
eq_30_2/A[20] (BTB_DW01_cmp6_0)          0.00       0.58 r
eq_30_2/U31/ZN (XNOR2_X1)                0.05       0.63 r
eq_30_2/U29/ZN (AND4_X1)                 0.06       0.70 r
eq_30_2/U48/ZN (AND4_X1)                 0.06       0.76 r
eq_30_2/U39/ZN (AND4_X2)                 0.06       0.82 r
eq_30_2/EQ (BTB_DW01_cmp6_0)             0.00       0.82 r
U77237/ZN (AND2_X2)                      0.05       0.88 r
U77257/ZN (INV_X1)                       0.04       0.92 f
U79984/ZN (NOR2_X1)                      0.04       0.96 r
NEW_PC[0] (out)                          0.00       0.96 r
data arrival time                                   0.96

max_delay                                0.96       0.96
output external delay                    0.00       0.96
data required time                                  0.96
-----------------------------------------------------------
data required time                                  0.96
data arrival time                                  -0.96
-----------------------------------------------------------
slack (MET)                                         0.00
```

B.2 Program counter adder

Power report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
ADDER_PC               5K_hvratio_1_1    NangateOpenCellLibrary


Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  =  19.1711 uW   (78%)
  Net Switching Power  =   5.4436 uW   (22%)
                         ---------
Total Dynamic Power    =  24.6147 uW  (100%)

Cell Leakage Power     =   2.5710 uW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %
)  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000            0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000            0.0000  (   0.00%)
register           0.0000            0.0000            0.0000            0.0000  (   0.00%)
sequential         0.0000            0.0000            0.0000            0.0000  (   0.00%)
combinational     19.1711            5.4436        2.5710e+03           27.1857  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total             19.1711 uW         5.4436 uW     2.5710e+03 nW        27.1857 uW
```

Area report

```
Number of ports:                           64
Number of nets:                            67
Number of cells:                            1
Number of combinational cells:              0
Number of sequential cells:                 0
Number of macros:                           0
Number of buf/inv:                          0
Number of references:                       1

Combinational area:        124.487998
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)
```

```
Total cell area:          124.487998
Total area:                undefined
```

Timing report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: PC[2] (input port)
  Endpoint: NEW_PC[28] (output port)
  Path Group: default
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  ADDER_PC           5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                                   Incr       Path
  ---------------------------------------------------------------------------
  input external delay                                    0.00       0.00 r
  PC[2] (in)                                              0.00       0.00 r
  add_14/A[2] (ADDER_PC_DW01_add_2)                       0.00       0.00 r
  add_14/U15/ZN (NAND3_X1)                                0.04       0.04 f
  add_14/U17/ZN (NOR2_X1)                                 0.04       0.08 r
  add_14/U18/ZN (AND4_X2)                                 0.07       0.14 r
  add_14/U25/ZN (AND2_X2)                                 0.05       0.20 r
  add_14/U112/ZN (NAND2_X1)                               0.03       0.23 f
  add_14/U97/ZN (XNOR2_X1)                                0.05       0.28 f
  add_14/SUM[28] (ADDER_PC_DW01_add_2)                    0.00       0.28 f
  NEW_PC[28] (out)                                        0.00       0.28 f
  data arrival time                                                  0.28

  max_delay                                               0.28       0.28
  output external delay                                   0.00       0.28
  data required time                                                 0.28
  ---------------------------------------------------------------------------
  data required time                                                 0.28
  data arrival time                                                 -0.28
  ---------------------------------------------------------------------------
  slack (MET)                                                        0.00
```

APPENDIX C

Decode post synthesis reports

C.1 Instruction register decode unit

Power report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
DECODE_IMM_EXT         5K_hvratio_1_1    NangateOpenCellLibrary


Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  =  17.2071 uW   (55%)
  Net Switching Power  =  13.8568 uW   (45%)
                         ---------
Total Dynamic Power    =  31.0639 uW  (100%)

Cell Leakage Power     =   1.9396 uW

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %
)  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000            0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000            0.0000  (   0.00%)
register           0.0000            0.0000            0.0000            0.0000  (   0.00%)
sequential         0.0000            0.0000            0.0000            0.0000  (   0.00%)
combinational     17.2071           13.8568        1.9396e+03           33.0035  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total             17.2071 uW        13.8568 uW     1.9396e+03 nW        33.0035 uW
```

Area report

```
Number of ports:                           78
Number of nets:                           110
Number of cells:                           79
Number of combinational cells:             79
Number of sequential cells:                 0
Number of macros:                           0
Number of buf/inv:                         30
Number of references:                      14

Combinational area:         73.416000
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:            73.416000
Total area:                 undefined
```

Timing report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: J_INSTR (input port)
  Endpoint: RD[0] (output port)
  Path Group: default
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  DECODE_IMM_EXT     5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 f
  J_INSTR (in)                             0.00       0.00 f
  U403/ZN (INV_X1)                         0.04       0.04 r
  U401/ZN (NAND3_X1)                       0.04       0.08 f
  U400/Z (BUF_X1)                          0.05       0.14 f
  U413/ZN (OAI221_X1)                      0.06       0.20 r
  RD[0] (out)                              0.00       0.20 r
  data arrival time                                   0.20

  max_delay                                0.20       0.20
  output external delay                    0.00       0.20
  data required time                                  0.20
  -----------------------------------------------------------
  data required time                                  0.20
  data arrival time                                  -0.20
  -----------------------------------------------------------
  slack (MET)                                         0.00
```

C.2 Register file

Power report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
WRF_M8_N8_F4_N_bit32   5K_hvratio_1_1    NangateOpenCellLibrary


Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  =  34.5628 mW   (91%)
  Net Switching Power  =   3.2870 mW    (9%)
                         ---------
Total Dynamic Power    =  37.8497 mW  (100%)

Cell Leakage Power     = 563.3884 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %
)  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000            0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000            0.0000  (   0.00%)
register       3.3778e+04          61.7015          1.8131e+05        3.4021e+04  (  88.57%)
sequential         0.0000           0.0000              0.0000            0.0000  (   0.00%)
combinational    784.6436        3.2253e+03          3.8208e+05        4.3919e+03  (  11.43%)
--------------------------------------------------------------------------------------------------
Total          3.4563e+04 uW     3.2870e+03 uW     5.6339e+05 nW     3.8413e+04 uW
```

Area report

```
Number of ports:                          192
Number of nets:                         13738
Number of cells:                        12009
Number of combinational cells:           9737
Number of sequential cells:              2272
Number of macros:                           0
Number of buf/inv:                       2302
Number of references:                      22

Combinational area:       12792.205961
Noncombinational area:    12087.040390
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          24879.246351
```

```
Total area:                 undefined
```

Timing report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: phy_reg_reg[71][1]
              (rising edge-triggered flip-flop clocked by CLK)
  Endpoint: phy_reg_reg[71][1]
            (rising edge-triggered flip-flop clocked by CLK)
  Path Group: CLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  WRF_M8_N8_F4_N_bit32
                     5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock CLK (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  phy_reg_reg[71][1]/CK (DFFR_X1)          0.00 #     0.00 r
  phy_reg_reg[71][1]/Q (DFFR_X1)           0.09       0.09 f
  U20140/ZN (AOI22_X1)                     0.05       0.14 r
  U20139/ZN (OAI221_X1)                    0.05       0.19 f
  phy_reg_reg[71][1]/D (DFFR_X1)           0.01       0.20 f
  data arrival time                                   0.20

  clock CLK (rise edge)                    0.48       0.48
  clock network delay (ideal)              0.00       0.48
  phy_reg_reg[71][1]/CK (DFFR_X1)          0.00       0.48 r
  library setup time                      -0.05       0.43
  data required time                                  0.43
  -----------------------------------------------------------
  data required time                                  0.43
  data arrival time                                  -0.20
  -----------------------------------------------------------
  slack (MET)                                        0.24


  Startpoint: READ_2_ADDR[3]
              (input port)
  Endpoint: READ_2[0] (output port)
  Path Group: default
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  WRF_M8_N8_F4_N_bit32
                     5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 f
  READ_2_ADDR[3] (in)                      0.00       0.00 f
  U25553/ZN (INV_X1)                       0.05       0.05 r
  U26256/ZN (NOR3_X1)                      0.03       0.08 f
  U26425/ZN (AND2_X1)                      0.04       0.12 f
  U17843/Z (BUF_X1)                        0.06       0.19 f
```

```
U24575/ZN (AOI222_X1)                    0.11       0.30 r
U26385/ZN (OAI221_X1)                    0.05       0.35 f
U25138/ZN (NOR4_X1)                      0.08       0.44 r
U26066/ZN (NAND4_X1)                     0.04       0.48 f
READ_2[0] (out)                          0.00       0.48 f
data arrival time                                   0.48

max_delay                                0.48       0.48
output external delay                    0.00       0.48
data required time                                  0.48
-----------------------------------------------------------
data required time                                  0.48
data arrival time                                  -0.48
-----------------------------------------------------------
slack (MET)                                         0.00
```

C.3 Register file decode unit

Power report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
RF_DECODER_M8_N8_F4_N_bit32
                      5K_hvratio_1_1    NangateOpenCellLibrary


Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  = 190.8235 uW   (75%)
  Net Switching Power  =  65.1032 uW   (25%)
                         ---------
Total Dynamic Power    = 255.9267 uW  (100%)

Cell Leakage Power     =   6.8605 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %
)  Attrs
-----------------------------------------------------------------------------------------------
io_pad             0.0000            0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000            0.0000  (   0.00%)
register         140.6452           11.8149          900.2835          153.3604  (  58.36%)
sequential         0.0000            0.0000            0.0000            0.0000  (   0.00%)
combinational     50.1783           53.2882        5.9602e+03          109.4267  (  41.64%)
-----------------------------------------------------------------------------------------------
Total            190.8235 uW        65.1032 uW     6.8605e+03 nW       262.7871 uW
```

Area report

```
Number of ports:                          76
Number of nets:                          298
Number of cells:                         244
Number of combinational cells:           233
Number of sequential cells:               11
Number of macros:                          0
Number of buf/inv:                        64
Number of references:                     33

Combinational area:        252.434001
Noncombinational area:      55.860000
Net Interconnect area:      undefined  (Wire load has zero net area)
```

```
Total cell area:          308.294001
Total area:                undefined
```

Timing report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: CUR_CNT_reg[0]
              (rising edge-triggered flip-flop clocked by CLK)
  Endpoint: CUR_CNT_reg[4]
            (rising edge-triggered flip-flop clocked by CLK)
  Path Group: CLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  RF_DECODER_M8_N8_F4_N_bit32
                     5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock CLK (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  CUR_CNT_reg[0]/CK (DFF_X1)               0.00       0.00 r
  CUR_CNT_reg[0]/QN (DFF_X1)               0.07       0.07 f
  U838/ZN (AND2_X1)                        0.05       0.11 f
  U860/ZN (AND4_X2)                        0.06       0.17 f
  U871/ZN (AOI211_X1)                      0.11       0.28 r
  U853/ZN (INV_X1)                         0.05       0.33 f
  U784/ZN (NAND3_X1)                       0.06       0.39 r
  U814/ZN (INV_X1)                         0.03       0.42 f
  U852/ZN (AOI21_X1)                       0.04       0.46 r
  U872/ZN (OAI21_X1)                       0.03       0.49 f
  CUR_CNT_reg[4]/D (DFF_X1)                0.01       0.50 f
  data arrival time                                   0.50

  clock CLK (rise edge)                    0.55       0.55
  clock network delay (ideal)              0.00       0.55
  CUR_CNT_reg[4]/CK (DFF_X1)               0.00       0.55 r
  library setup time                      -0.04       0.51
  data required time                                  0.51
  -----------------------------------------------------------
  data required time                                  0.51
  data arrival time                                  -0.50
  -----------------------------------------------------------
  slack (MET)                                         0.01


  Startpoint: RET (input port)
  Endpoint: FILL_SPILL_IMM[8]
            (output port)
  Path Group: default
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  RF_DECODER_M8_N8_F4_N_bit32
                     5K_hvratio_1_1        NangateOpenCellLibrary
```

```
Point                                   Incr       Path
-----------------------------------------------------------
input external delay                    0.00       0.00 r
RET (in)                                0.00       0.00 r
U671/ZN (NAND3_X1)                      0.05       0.05 f
U731/ZN (INV_X1)                        0.07       0.12 r
U736/ZN (NAND2_X1)                      0.06       0.17 f
U718/ZN (NOR2_X1)                       0.05       0.22 r
U717/Z (BUF_X1)                         0.07       0.29 r
U724/ZN (AOI21_X1)                      0.05       0.35 f
U723/ZN (INV_X1)                        0.02       0.37 r
FILL_SPILL_IMM[8] (out)                 0.00       0.37 r
data arrival time                                  0.37

max_delay                               0.55       0.55
output external delay                   0.00       0.55
data required time                                 0.55
-----------------------------------------------------------
data required time                                 0.55
data arrival time                                 -0.37
-----------------------------------------------------------
slack (MET)                                        0.18
```

C.4 Hazard detection unit

Power report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
HAZARD_UNIT            5K_hvratio_1_1    NangateOpenCellLibrary


Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  = 217.2625 uW   (62%)
  Net Switching Power  = 131.4604 uW   (38%)
                         ---------
Total Dynamic Power    = 348.7228 uW  (100%)

Cell Leakage Power     =  17.5185 uW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %
)  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000             0.0000  (   0.00%)
register           0.0000           0.0000            0.0000             0.0000  (   0.00%)
sequential         0.0000           0.0000            0.0000             0.0000  (   0.00%)
combinational    217.2626         131.4604        1.7519e+04           366.2414  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total            217.2626 uW       131.4604 uW     1.7519e+04 nW       366.2414 uW
```

Area report

```
Number of ports:                          139
Number of nets:                           692
Number of cells:                          556
Number of combinational cells:            556
Number of sequential cells:                 0
Number of macros:                           0
Number of buf/inv:                         39
Number of references:                      20

Combinational area:        790.019992
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)
```

```
Total cell area:          790.019992
Total area:                undefined
```

Timing report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: RD_ID_EX[0]
              (input port)
  Endpoint: STALL (output port)
  Path Group: default
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  HAZARD_UNIT        5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 r
  RD_ID_EX[0] (in)                         0.00       0.00 r
  U1437/ZN (AND4_X1)                       0.07       0.07 r
  U1679/ZN (NAND2_X1)                      0.03       0.09 f
  U1435/ZN (XNOR2_X1)                      0.07       0.16 f
  U1678/ZN (INV_X1)                        0.04       0.20 r
  U1657/Z (XOR2_X1)                        0.06       0.26 r
  U1654/ZN (AND4_X1)                       0.07       0.32 r
  U1675/ZN (NAND4_X1)                      0.04       0.37 f
  U1669/ZN (AOI21_X1)                      0.05       0.42 r
  U1668/ZN (NOR3_X1)                       0.02       0.44 f
  U1672/ZN (OAI22_X1)                      0.05       0.49 r
  U1671/ZN (OAI21_X1)                      0.04       0.53 f
  U1670/ZN (NAND4_X1)                      0.03       0.56 r
  STALL (out)                              0.00       0.56 r
  data arrival time                                   0.56

  max_delay                                0.60       0.60
  output external delay                    0.00       0.60
  data required time                                  0.60
  -----------------------------------------------------------
  data required time                                  0.60
  data arrival time                                  -0.56
  -----------------------------------------------------------
  slack (MET)                                         0.04
```

C.5 Stack

Power report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
STACK                 5K_hvratio_1_1    NangateOpenCellLibrary


Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  =   3.8687 mW   (94%)
  Net Switching Power  = 247.7316 uW    (6%)
                         ---------
Total Dynamic Power    =   4.1164 mW  (100%)

Cell Leakage Power     =  52.0804 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %
)  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000            0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000            0.0000  (   0.00%)
register       3.7762e+03          19.4409          2.3277e+04        3.8189e+03  (  91.61%)
sequential         0.0000           0.0000              0.0000            0.0000  (   0.00%)
combinational     92.4521          228.2911          2.8803e+04          349.5461  (   8.39%)
--------------------------------------------------------------------------------------------------
Total          3.8687e+03 uW       247.7320 uW     5.2080e+04 nW     4.1685e+03 uW
```

Area report

```
Number of ports:                           72
Number of nets:                          1303
Number of cells:                         1169
Number of combinational cells:            876
Number of sequential cells:               291
Number of macros:                           0
Number of buf/inv:                        340
Number of references:                      25

Combinational area:       1193.010008
Noncombinational area:    1547.322050
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          2740.332057
```

```
Total area:                 undefined
```

Timing report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: address_reg[2]
              (rising edge-triggered flip-flop clocked by CLK)
  Endpoint: address_reg[22]
            (rising edge-triggered flip-flop clocked by CLK)
  Path Group: CLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  STACK              5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock CLK (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  address_reg[2]/CK (DFFR_X1)              0.00       0.00 r
  address_reg[2]/QN (DFFR_X1)              0.07       0.07 f
  U1435/ZN (INV_X2)                        0.06       0.13 r
  add_56/A[2] (STACK_DW01_inc_1)           0.00       0.13 r
  add_56/U117/ZN (NAND2_X1)                0.04       0.18 f
  add_56/U113/ZN (NOR2_X1)                 0.05       0.23 r
  add_56/U14/ZN (AND4_X2)                  0.07       0.30 r
  add_56/U110/ZN (NAND2_X1)                0.04       0.34 f
  add_56/U50/ZN (NOR2_X1)                  0.04       0.39 r
  add_56/U118/ZN (XNOR2_X1)                0.03       0.42 f
  add_56/SUM[22] (STACK_DW01_inc_1)        0.00       0.42 f
  U2201/ZN (AOI22_X1)                      0.05       0.47 r
  U1430/ZN (NAND2_X1)                      0.03       0.50 f
  address_reg[22]/D (DFFR_X1)              0.01       0.51 f
  data arrival time                                   0.51

  clock CLK (rise edge)                    0.55       0.55
  clock network delay (ideal)              0.00       0.55
  address_reg[22]/CK (DFFR_X1)             0.00       0.55 r
  library setup time                      -0.04       0.51
  data required time                                  0.51
  -----------------------------------------------------------
  data required time                                  0.51
  data arrival time                                  -0.51
  -----------------------------------------------------------
  slack (MET)                                         0.00


  Startpoint: RET (input port)
  Endpoint: DATA_OUT[0]
            (output port)
  Path Group: default
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  STACK              5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                    Incr       Path
```

```
-------------------------------------------------------------
input external delay                     0.00       0.00 f
RET (in)                                 0.00       0.00 f
U1724/ZN (INV_X1)                        0.04       0.04 r
U2254/ZN (NOR3_X4)                       0.07       0.10 f
U1680/ZN (NAND2_X1)                      0.04       0.15 r
U1497/Z (BUF_X1)                         0.09       0.24 r
U1536/ZN (OAI22_X1)                      0.05       0.29 f
U1730/ZN (AOI221_X1)                     0.09       0.38 r
U1728/ZN (NAND2_X1)                      0.03       0.40 f
DATA_OUT[0] (out)                        0.00       0.41 f
data arrival time                                   0.41

max_delay                                0.55       0.55
output external delay                    0.00       0.55
data required time                                  0.55
-------------------------------------------------------------
data required time                                  0.55
data arrival time                                  -0.41
-------------------------------------------------------------
slack (MET)                                         0.14
```

C.6 Jump comparator

Power report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
JUMP_COMPARATOR        5K_hvratio_1_1    NangateOpenCellLibrary


Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  =   3.5053 uW   (57%)
  Net Switching Power  =   2.5977 uW   (43%)
                         ---------
Total Dynamic Power    =   6.1030 uW  (100%)

Cell Leakage Power     = 603.0745 nW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %
)  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000            0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000            0.0000  (   0.00%)
register           0.0000            0.0000            0.0000            0.0000  (   0.00%)
sequential         0.0000            0.0000            0.0000            0.0000  (   0.00%)
combinational      3.5053            2.5977          603.0744            6.7061  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total              3.5053 uW         2.5977 uW       603.0744 nW         6.7061 uW
```

Area report

```
Number of ports:                           35
Number of nets:                            66
Number of cells:                           32
Number of combinational cells:             32
Number of sequential cells:                 0
Number of macros:                           0
Number of buf/inv:                          1
Number of references:                       6

Combinational area:         26.865999
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)
```

```
Total cell area:            26.865999
Total area:                 undefined
```

Timing report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: A[22] (input port)
  Endpoint: COND (output port)
  Path Group: default
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  JUMP_COMPARATOR    5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 f
  A[22] (in)                               0.00       0.00 f
  U68/ZN (NOR2_X1)                         0.04       0.04 r
  U69/ZN (NAND2_X1)                        0.03       0.07 f
  U61/ZN (NOR2_X1)                         0.04       0.11 r
  U56/ZN (NAND4_X1)                        0.05       0.16 f
  U57/ZN (XNOR2_X1)                        0.06       0.21 f
  U73/ZN (AND2_X1)                         0.03       0.25 f
  COND (out)                               0.00       0.25 f
  data arrival time                                   0.25

  max_delay                                0.25       0.25
  output external delay                    0.00       0.25
  data required time                                  0.25
  -----------------------------------------------------------
  data required time                                  0.25
  data arrival time                                  -0.25
  -----------------------------------------------------------
  slack (MET)                                         0.00
```

C.7 Jump adder

Power report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
JUMP_ADDER             5K_hvratio_1_1    NangateOpenCellLibrary


Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  =  98.0584 uW   (57%)
  Net Switching Power  =  75.3085 uW   (43%)
                         ---------
Total Dynamic Power    = 173.3669 uW  (100%)

Cell Leakage Power     =   7.7445 uW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %
)  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000            0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000            0.0000  (   0.00%)
register           0.0000            0.0000            0.0000            0.0000  (   0.00%)
sequential         0.0000            0.0000            0.0000            0.0000  (   0.00%)
combinational     98.0584           75.3085        7.7445e+03          181.1115  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total             98.0584 uW        75.3085 uW     7.7445e+03 nW       181.1115 uW
```

Area report

```
Number of ports:                          96
Number of nets:                           97
Number of cells:                           1
Number of combinational cells:             0
Number of sequential cells:                0
Number of macros:                          0
Number of buf/inv:                         0
Number of references:                      1

Combinational area:        308.027997
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)
```

```
Total cell area:           308.027997
Total area:                 undefined
```

Timing report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: A[2] (input port)
  Endpoint: S[15] (output port)
  Path Group: default
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  JUMP_ADDER         5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                                   Incr       Path
  ---------------------------------------------------------------------------
  input external delay                                    0.00       0.00 f
  A[2] (in)                                               0.00       0.00 f
  add_14/A[2] (JUMP_ADDER_DW01_add_2)                     0.00       0.00 f
  add_14/U152/ZN (INV_X1)                                 0.03       0.03 r
  add_14/U151/ZN (NAND2_X1)                               0.03       0.05 f
  add_14/U150/ZN (NAND2_X1)                               0.03       0.09 r
  add_14/U148/ZN (NAND3_X1)                               0.04       0.12 f
  add_14/U149/ZN (NAND3_X1)                               0.04       0.16 r
  add_14/U178/Z (BUF_X1)                                  0.03       0.19 r
  add_14/U184/ZN (OAI21_X1)                               0.04       0.23 f
  add_14/U126/ZN (AOI21_X1)                               0.06       0.30 r
  add_14/U176/ZN (OAI21_X1)                               0.04       0.33 f
  add_14/U301/ZN (NAND2_X1)                               0.03       0.37 r
  add_14/U300/ZN (NAND2_X1)                               0.03       0.40 f
  add_14/U229/ZN (AOI21_X1)                               0.05       0.44 r
  add_14/U105/ZN (XNOR2_X1)                               0.05       0.50 r
  add_14/SUM[15] (JUMP_ADDER_DW01_add_2)                  0.00       0.50 r
  S[15] (out)                                             0.00       0.50 r
  data arrival time                                                  0.50

  max_delay                                               0.50       0.50
  output external delay                                   0.00       0.50
  data required time                                                 0.50
  ---------------------------------------------------------------------------
  data required time                                                 0.50
  data arrival time                                                 -0.50
  ---------------------------------------------------------------------------
  slack (MET)                                                        0.00
```

APPENDIX D

Execute post synthesis reports

D.1 ALU

Power report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
ALU                   5K_hvratio_1_1    NangateOpenCellLibrary


Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  = 551.5435 uW   (58%)
  Net Switching Power  = 391.5703 uW   (42%)
                         ---------
Total Dynamic Power    = 943.1137 uW  (100%)

Cell Leakage Power     = 278.6212 uW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %
)  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000            0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000            0.0000  (   0.00%)
register           0.0000            0.0000            0.0000            0.0000  (   0.00%)
sequential       334.8367            2.4044        7.0455e+04          407.6974  (  33.37%)
combinational    216.7056          389.1673        2.0816e+05          814.0356  (  66.63%)
--------------------------------------------------------------------------------------------------
Total            551.5422 uW       391.5717 uW     2.7862e+05 nW     1.2217e+03 uW
```

Area report

```
Number of ports:                          169
Number of nets:                           845
Number of cells:                          612
Number of combinational cells:            607
Number of sequential cells:                 0
Number of macros:                           0
Number of buf/inv:                        166
Number of references:                      29

Combinational area:       12038.362064
Noncombinational area:    4178.327848
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          16216.689912
Total area:                 undefined
```

Timing report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: func[0] (input port)
  Endpoint: O_32[26] (output port)
  Path Group: default
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  ALU                5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 f
  func[0] (in)                             0.00       0.00 f
  U668/ZN (INV_X1)                         0.04       0.04 r
  U689/ZN (INV_X1)                         0.03       0.07 f
  U1142/ZN (NAND2_X1)                      0.04       0.11 r
  U1104/ZN (NAND4_X1)                      0.07       0.18 f
  U850/Z (BUF_X1)                          0.09       0.27 f
  U598/ZN (NOR2_X1)                        0.11       0.39 r
  shift/B[1] (SHIFTER)                     0.00       0.39 r
  shift/U597/ZN (INV_X1)                   0.06       0.45 f
  shift/U682/ZN (NOR3_X4)                  0.18       0.62 r
  shift/U318/ZN (INV_X1)                   0.04       0.66 f
  shift/U133/Z (BUF_X1)                    0.04       0.71 f
  shift/U34/Z (BUF_X1)                     0.07       0.78 f
  shift/U436/ZN (NOR2_X2)                  0.16       0.94 r
  shift/U105/ZN (INV_X1)                   0.05       0.99 f
  shift/U447/ZN (OAI222_X1)                0.07       1.06 r
  shift/U446/ZN (AOI221_X1)                0.04       1.10 f
  shift/U308/ZN (OAI211_X1)                0.05       1.15 r
  shift/U362/ZN (AOI22_X1)                 0.04       1.19 f
  shift/U360/ZN (AOI21_X1)                 0.04       1.23 r
  shift/Z[26] (SHIFTER)                    0.00       1.23 r
  U766/ZN (AOI222_X1)                      0.04       1.27 f
  U765/ZN (INV_X1)                         0.03       1.30 r
  O_32[26] (out)                           0.00       1.30 r
  data arrival time                                   1.30

  max_delay                                1.30       1.30
```

```
output external delay                    0.00        1.30
data required time                                   1.30
-----------------------------------------------------------
data required time                                   1.30
data arrival time                                   -1.30
-----------------------------------------------------------
slack (MET)                                          0.00
```

D.1.1 Adder/subtractor

Power report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
P4_ADDER_GEN_N32_M4    5K_hvratio_1_1    NangateOpenCellLibrary


Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  = 223.7685 uW   (54%)
  Net Switching Power  = 192.3326 uW   (46%)
                         ---------
Total Dynamic Power    = 416.1012 uW  (100%)

Cell Leakage Power     =  12.3353 uW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %
)  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000            0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000            0.0000  (   0.00%)
register           0.0000            0.0000            0.0000            0.0000  (   0.00%)
sequential         0.0000            0.0000            0.0000            0.0000  (   0.00%)
combinational    223.7685          192.3326        1.2335e+04          428.4363  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total            223.7685 uW       192.3326 uW     1.2335e+04 nW       428.4363 uW
```

Area report

```
Number of ports:                          100
Number of nets:                           158
Number of cells:                           53
Number of combinational cells:             51
Number of sequential cells:                 0
Number of macros:                           0
Number of buf/inv:                         15
Number of references:                       9

Combinational area:        515.773996
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:           515.773996
```

```
Total area:                 undefined
```

Timing report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: sub_add_n (input port)
  Endpoint: S[24] (output port)
  Path Group: default
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  P4_ADDER_GEN_N32_M4
                     5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                                    Incr       Path
  -----------------------------------------------------------------------------
  input external delay                                     0.00       0.00 f
  sub_add_n (in)                                           0.00       0.00 f
  U195/Z (BUF_X2)                                          0.06       0.06 f
  U160/Z (XOR2_X1)                                         0.08       0.14 f
  carry_gen/B[23] (P4_CARRY_GEN_N32_M4)                    0.00       0.14 f
  carry_gen/PG_NET/B[23] (PG_NETWORK_GEN_N32)              0.00       0.14 f
  carry_gen/PG_NET/U53/Z (XOR2_X1)                         0.08       0.21 f
  carry_gen/PG_NET/p[23] (PG_NETWORK_GEN_N32)              0.00       0.21 f
  carry_gen/PG_L1_1_24/Pik (PG_BLOCK_17)                   0.00       0.21 f
  carry_gen/PG_L1_1_24/U4/ZN (AOI21_X1)                    0.04       0.26 r
  carry_gen/PG_L1_1_24/U3/ZN (INV_X1)                      0.02       0.28 f
  carry_gen/PG_L1_1_24/Gij (PG_BLOCK_17)                   0.00       0.28 f
  carry_gen/PG_B_n_2_24_21/Gik (PG_BLOCK_8)                0.00       0.28 f
  carry_gen/PG_B_n_2_24_21/U2/ZN (AOI21_X1)                0.05       0.33 r
  carry_gen/PG_B_n_2_24_21/U1/ZN (INV_X1)                  0.02       0.36 f
  carry_gen/PG_B_n_2_24_21/Gij (PG_BLOCK_8)                0.00       0.36 f
  carry_gen/PG_B_n_3_24_17/Gik (PG_BLOCK_4)                0.00       0.36 f
  carry_gen/PG_B_n_3_24_17/U3/ZN (AOI21_X1)                0.05       0.41 r
  carry_gen/PG_B_n_3_24_17/U2/ZN (INV_X1)                  0.03       0.43 f
  carry_gen/PG_B_n_3_24_17/Gij (PG_BLOCK_4)                0.00       0.43 f
  carry_gen/G_B_n_5_24/Gik (G_BLOCK_3)                     0.00       0.43 f
  carry_gen/G_B_n_5_24/U2/ZN (AOI21_X1)                    0.05       0.49 r
  carry_gen/G_B_n_5_24/U1/ZN (INV_X1)                      0.03       0.52 f
  carry_gen/G_B_n_5_24/Gij (G_BLOCK_3)                     0.00       0.52 f
  carry_gen/C[5] (P4_CARRY_GEN_N32_M4)                     0.00       0.52 f
  sum_gen/Cin[6] (P4_SUM_GEN_N32_M4)                       0.00       0.52 f
  sum_gen/CSB_i_7/Cin (CSB_GEN_N4_1)                       0.00       0.52 f
  sum_gen/CSB_i_7/U3/ZN (INV_X1)                           0.04       0.57 r
  sum_gen/CSB_i_7/U31/Z (XOR2_X1)                          0.06       0.63 r
  sum_gen/CSB_i_7/S[0] (CSB_GEN_N4_1)                      0.00       0.63 r
  sum_gen/S[24] (P4_SUM_GEN_N32_M4)                        0.00       0.63 r
  S[24] (out)                                              0.00       0.63 r
  data arrival time                                                   0.63

  max_delay                                                0.63       0.63
  output external delay                                    0.00       0.63
  data required time                                                  0.63
  -----------------------------------------------------------------------------
  data required time                                                  0.63
  data arrival time                                                  -0.63
  -----------------------------------------------------------------------------
  slack (MET)                                                         0.00
```

D.1.2 Comparator

Power report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
COMPARATOR             5K_hvratio_1_1    NangateOpenCellLibrary


Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  =  81.9194 uW   (52%)
  Net Switching Power  =  75.5070 uW   (48%)
                         ---------
Total Dynamic Power    = 157.4264 uW  (100%)

Cell Leakage Power     =   6.9900 uW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %
)  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000            0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000            0.0000  (   0.00%)
register           0.0000            0.0000            0.0000            0.0000  (   0.00%)
sequential         0.0000            0.0000            0.0000            0.0000  (   0.00%)
combinational     81.9194           75.5070        6.9900e+03          164.4164  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total             81.9194 uW        75.5070 uW     6.9900e+03 nW       164.4164 uW
```

Area report

```
Number of ports:                          71
Number of nets:                          346
Number of cells:                         281
Number of combinational cells:           281
Number of sequential cells:                0
Number of macros:                          0
Number of buf/inv:                        76
Number of references:                     26

Combinational area:        291.003998
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:           291.003998
```

```
Total area:                 undefined
```

Timing report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: B[9] (input port)
  Endpoint: ANEB (output port)
  Path Group: default
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  COMPARATOR         5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 r
  B[9] (in)                                0.00       0.00 r
  U494/ZN (XNOR2_X1)                       0.05       0.05 r
  U493/ZN (AND2_X1)                        0.04       0.10 r
  U492/ZN (NAND2_X1)                       0.02       0.12 f
  U490/ZN (NOR2_X1)                        0.04       0.16 r
  U491/Z (CLKBUF_X1)                       0.04       0.20 r
  U600/ZN (NAND2_X1)                       0.03       0.23 f
  U391/ZN (OAI33_X1)                       0.08       0.31 r
  U566/ZN (AOI22_X1)                       0.03       0.35 f
  U557/ZN (NAND3_X1)                       0.04       0.39 r
  U455/ZN (AOI21_X1)                       0.03       0.42 f
  U528/ZN (OAI21_X1)                       0.05       0.47 r
  U423/Z (BUF_X1)                          0.05       0.52 r
  U579/ZN (OR2_X1)                         0.05       0.57 r
  U542/ZN (OAI222_X1)                      0.04       0.61 f
  U541/ZN (AOI221_X1)                      0.09       0.70 r
  U508/ZN (OAI222_X1)                      0.06       0.76 f
  U535/ZN (INV_X1)                         0.04       0.79 r
  U505/ZN (OAI221_X1)                      0.04       0.84 f
  U622/ZN (OR2_X1)                         0.06       0.90 f
  ANEB (out)                               0.00       0.90 f
  data arrival time                                   0.90

  max_delay                                0.90       0.90
  output external delay                    0.00       0.90
  data required time                                  0.90
  -----------------------------------------------------------
  data required time                                  0.90
  data arrival time                                  -0.90
  -----------------------------------------------------------
  slack (MET)                                         0.00
```

D.1.3 Logical unit

Power report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
LOGICAL               5K_hvratio_1_1    NangateOpenCellLibrary


Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  =  37.2237 uW   (58%)
  Net Switching Power  =  27.0318 uW   (42%)
                         ---------
Total Dynamic Power    =  64.2555 uW  (100%)

Cell Leakage Power     =   4.9585 uW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %
)  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000            0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000            0.0000  (   0.00%)
register           0.0000            0.0000            0.0000            0.0000  (   0.00%)
sequential         0.0000            0.0000            0.0000            0.0000  (   0.00%)
combinational     37.2237           27.0318        4.9585e+03           69.2140  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total             37.2237 uW        27.0318 uW     4.9585e+03 nW        69.2140 uW
```

Area report

```
Number of ports:                          100
Number of nets:                           292
Number of cells:                          224
Number of combinational cells:             64
Number of sequential cells:                 0
Number of macros:                           0
Number of buf/inv:                         64
Number of references:                     161

Combinational area:        212.800003
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:           212.800003
```

```
Total area:                 undefined
```

Timing report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: B[0] (input port)
  Endpoint: Z[0] (output port)
  Path Group: default
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  LOGICAL            5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 f
  B[0] (in)                                0.00       0.00 f
  U417/ZN (INV_X1)                         0.03       0.03 r
  N2_0/C (NAND3_126)                       0.00       0.03 r
  N2_0/U1/ZN (NAND3_X1)                    0.04       0.07 f
  N2_0/Z (NAND3_126)                       0.00       0.07 f
  N4_0/C (NAND4_0)                         0.00       0.07 f
  N4_0/U1/ZN (NAND4_X1)                    0.03       0.10 r
  N4_0/Z (NAND4_0)                         0.00       0.10 r
  Z[0] (out)                               0.00       0.10 r
  data arrival time                                   0.10

  max_delay                                0.10       0.10
  output external delay                    0.00       0.10
  data required time                                  0.10
  -----------------------------------------------------------
  data required time                                  0.10
  data arrival time                                  -0.10
  -----------------------------------------------------------
  slack (MET)                                         0.00
```

D.1.4 Shifter

Power report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
SHIFTER               5K_hvratio_1_1    NangateOpenCellLibrary


Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  = 185.0148 uW   (45%)
  Net Switching Power  = 225.6546 uW   (55%)
                         ---------
Total Dynamic Power    = 410.6694 uW  (100%)

Cell Leakage Power     =  25.0016 uW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %
)  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000            0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000            0.0000  (   0.00%)
register           0.0000            0.0000            0.0000            0.0000  (   0.00%)
sequential         0.0000            0.0000            0.0000            0.0000  (   0.00%)
combinational    185.0147          225.6548        2.5002e+04          435.6711  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total            185.0147 uW       225.6548 uW     2.5002e+04 nW       435.6711 uW
```

Area report

```
Number of ports:                          98
Number of nets:                          907
Number of cells:                         867
Number of combinational cells:           867
Number of sequential cells:                0
Number of macros:                          0
Number of buf/inv:                       231
Number of references:                     36

Combinational area:        965.846004
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:           965.846004
```

```
Total area:                 undefined
```

Timing report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: B[4] (input port)
  Endpoint: Z[18] (output port)
  Path Group: default
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  SHIFTER            5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 r
  B[4] (in)                                0.00       0.00 r
  U1522/ZN (INV_X1)                        0.03       0.03 f
  U1589/ZN (AND2_X2)                       0.04       0.07 f
  U1420/Z (BUF_X1)                         0.05       0.12 f
  U1824/Z (BUF_X1)                         0.05       0.17 f
  U1746/ZN (AOI21_X1)                      0.08       0.25 r
  U1810/ZN (AND2_X1)                       0.06       0.31 r
  U1901/ZN (OAI22_X1)                      0.04       0.35 f
  U2026/ZN (AOI222_X1)                     0.11       0.47 r
  U1943/ZN (NAND4_X1)                      0.04       0.51 f
  Z[18] (out)                              0.00       0.51 f
  data arrival time                                   0.51

  max_delay                                0.51       0.51
  output external delay                    0.00       0.51
  data required time                                  0.51
  -----------------------------------------------------------
  data required time                                  0.51
  data arrival time                                  -0.51
  -----------------------------------------------------------
  slack (MET)                                         0.00
```

D.1.5 multiplier

Power report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
BOOTHMUL               5K_hvratio_1_1    NangateOpenCellLibrary


Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  =   6.2764 mW   (63%)
  Net Switching Power  =   3.6963 mW   (37%)
                         ---------
Total Dynamic Power    =   9.9727 mW  (100%)

Cell Leakage Power     = 366.1673 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %
)  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000            0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000            0.0000  (   0.00%)
register       3.2499e+03          288.1543        7.3180e+04        3.6113e+03  (  34.93%)
sequential         0.0000            0.0000            0.0000            0.0000  (   0.00%)
combinational  3.0265e+03        3.4081e+03        2.9299e+05        6.7276e+03  (  65.07%)
--------------------------------------------------------------------------------------------------
Total          6.2764e+03 uW     3.6963e+03 uW     3.6617e+05 nW     1.0339e+04 uW
```

Area report

```
Number of ports:                          129
Number of nets:                          3699
Number of cells:                         1259
Number of combinational cells:            303
Number of sequential cells:               924
Number of macros:                           0
Number of buf/inv:                        303
Number of references:                      38

Combinational area:       13425.285981
Noncombinational area:    4179.391849
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          17604.677830
Total area:                 undefined
```

Timing report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: reg_B76_reg[23]
              (rising edge-triggered flip-flop clocked by CLK)
  Endpoint: reg_p78_reg[58]
            (rising edge-triggered flip-flop clocked by CLK)
  Path Group: CLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  BOOTHMUL           5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                                    Incr       Path
  ---------------------------------------------------------------------------
  clock CLK (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  reg_B76_reg[23]/CK (DFF_X1)                              0.00       0.00 r
  reg_B76_reg[23]/Q (DFF_X1)                               0.09       0.09 f
  M13_6_0/sel[0] (MUX_ENCODED_4)                           0.00       0.09 f
  M13_6_0/U15/Z (XOR2_X1)                                  0.08       0.17 f
  M13_6_0/U16/ZN (AND2_X1)                                 0.05       0.22 f
  M13_6_0/U74/ZN (AOI22_X1)                                0.05       0.27 r
  M13_6_0/U75/ZN (NAND2_X1)                                0.03       0.30 f
  M13_6_0/output[1] (MUX_ENCODED_4)                        0.00       0.30 f
  ADD13_6_0/A[1] (ADDER_4)                                 0.00       0.30 f
  ADD13_6_0/add_1_root_add_20_2/A[1] (ADDER_4_DW01_add_2)
                                                           0.00       0.30 f
  ADD13_6_0/add_1_root_add_20_2/U27/ZN (NAND2_X1)          0.04       0.34 r
  ADD13_6_0/add_1_root_add_20_2/U23/ZN (NAND2_X1)          0.03       0.38 f
  ADD13_6_0/add_1_root_add_20_2/U20/ZN (NOR2_X1)           0.05       0.43 r
  ADD13_6_0/add_1_root_add_20_2/U22/ZN (OAI21_X1)          0.03       0.46 f
  ADD13_6_0/add_1_root_add_20_2/U48/ZN (NAND2_X1)          0.03       0.49 r
  ADD13_6_0/add_1_root_add_20_2/U47/ZN (AOI21_X1)          0.03       0.51 f
  ADD13_6_0/add_1_root_add_20_2/U36/ZN (OAI21_X1)          0.05       0.56 r
  ADD13_6_0/add_1_root_add_20_2/U37/ZN (NAND2_X1)          0.04       0.60 f
  ADD13_6_0/add_1_root_add_20_2/U161/Z (BUF_X1)            0.04       0.64 f
  ADD13_6_0/add_1_root_add_20_2/U502/ZN (NAND2_X1)         0.03       0.67 r
  ADD13_6_0/add_1_root_add_20_2/U2/ZN (AND2_X2)            0.04       0.72 r
  ADD13_6_0/add_1_root_add_20_2/U223/ZN (OAI21_X1)         0.03       0.74 f
  ADD13_6_0/add_1_root_add_20_2/U374/ZN (NAND2_X1)         0.03       0.77 r
  ADD13_6_0/add_1_root_add_20_2/U373/ZN (NAND2_X1)         0.03       0.80 f
  ADD13_6_0/add_1_root_add_20_2/U371/ZN (XNOR2_X1)         0.06       0.86 f
  ADD13_6_0/add_1_root_add_20_2/SUM[19] (ADDER_4_DW01_add_2)
                                                           0.00       0.86 f
  ADD13_6_0/S[19] (ADDER_4)                                0.00       0.86 f
  ADD14_6_1/B[19] (ADDER_3)                                0.00       0.86 f
  ADD14_6_1/add_1_root_add_20_2/B[19] (ADDER_3_DW01_add_2)
                                                           0.00       0.86 f
  ADD14_6_1/add_1_root_add_20_2/U131/ZN (OR2_X1)           0.06       0.91 f
  ADD14_6_1/add_1_root_add_20_2/U583/ZN (NAND3_X1)         0.03       0.95 r
  ADD14_6_1/add_1_root_add_20_2/U372/ZN (NAND2_X1)         0.03       0.97 f
  ADD14_6_1/add_1_root_add_20_2/U204/ZN (NAND2_X1)         0.03       1.01 r
  ADD14_6_1/add_1_root_add_20_2/U91/ZN (AOI21_X1)          0.03       1.04 f
  ADD14_6_1/add_1_root_add_20_2/U486/ZN (OAI21_X1)         0.04       1.08 r
  ADD14_6_1/add_1_root_add_20_2/U179/ZN (NAND3_X1)         0.03       1.11 f
  ADD14_6_1/add_1_root_add_20_2/U171/ZN (AND2_X1)          0.04       1.15 f
  ADD14_6_1/add_1_root_add_20_2/U518/ZN (NAND3_X1)         0.03       1.18 r
  ADD14_6_1/add_1_root_add_20_2/U514/ZN (NAND3_X1)         0.04       1.22 f
  ADD14_6_1/add_1_root_add_20_2/U119/ZN (NAND2_X1)         0.04       1.25 r
```

```
ADD14_6_1/add_1_root_add_20_2/U137/ZN (NAND2_X1)        0.03       1.29 f
ADD14_6_1/add_1_root_add_20_2/U164/ZN (NAND2_X1)        0.03       1.31 r
ADD14_6_1/add_1_root_add_20_2/U165/ZN (AND2_X1)         0.04       1.35 r
ADD14_6_1/add_1_root_add_20_2/U492/ZN (NAND2_X1)        0.03       1.38 f
ADD14_6_1/add_1_root_add_20_2/U62/Z (BUF_X1)            0.04       1.42 f
ADD14_6_1/add_1_root_add_20_2/U267/ZN (NAND2_X1)        0.03       1.45 r
ADD14_6_1/add_1_root_add_20_2/U266/ZN (NAND2_X1)        0.03       1.48 f
ADD14_6_1/add_1_root_add_20_2/U317/ZN (XNOR2_X1)        0.05       1.53 f
ADD14_6_1/add_1_root_add_20_2/SUM[58] (ADDER_3_DW01_add_2)
                                                        0.00       1.53 f
ADD14_6_1/S[58] (ADDER_3)                               0.00       1.53 f
reg_p78_reg[58]/D (DFF_X1)                              0.01       1.54 f
data arrival time                                                  1.54

clock CLK (rise edge)                                   1.58       1.58
clock network delay (ideal)                             0.00       1.58
reg_p78_reg[58]/CK (DFF_X1)                             0.00       1.58 r
library setup time                                     -0.04       1.54
data required time                                                 1.54
-----------------------------------------------------------------------------
data required time                                                 1.54
data arrival time                                                 -1.54
-----------------------------------------------------------------------------
slack (MET)                                                        0.00
```

D.2 Forwarding unit

Power report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
FWU                   5K_hvratio_1_1    NangateOpenCellLibrary


Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  = 121.9357 uW   (66%)
  Net Switching Power  =  61.4367 uW   (34%)
                         ---------
Total Dynamic Power    = 183.3724 uW  (100%)

Cell Leakage Power     =  10.3504 uW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %
)  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000            0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000            0.0000  (   0.00%)
register           0.0000            0.0000            0.0000            0.0000  (   0.00%)
sequential         0.0000            0.0000            0.0000            0.0000  (   0.00%)
combinational    121.9357           61.4367        1.0350e+04          193.7229  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total            121.9357 uW        61.4367 uW     1.0350e+04 nW       193.7229 uW
```

Area report

```
Number of ports:                          106
Number of nets:                           452
Number of cells:                          366
Number of combinational cells:            366
Number of sequential cells:                 0
Number of macros:                           0
Number of buf/inv:                         41
Number of references:                      21

Combinational area:        475.341993
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)
```

```
Total cell area:           475.341993
Total area:                 undefined
```

Timing report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: RS_1_ID_EX[1]
              (input port)
  Endpoint: FW_MEM_TO_EX_A[0]
            (output port)
  Path Group: default
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  FWU                5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 f
  RS_1_ID_EX[1] (in)                       0.00       0.00 f
  U1035/ZN (INV_X1)                        0.03       0.03 r
  U1036/Z (XOR2_X1)                        0.07       0.10 r
  U1125/ZN (AND4_X1)                       0.06       0.16 r
  U1161/ZN (AND4_X1)                       0.06       0.22 r
  U1189/ZN (AOI211_X1)                     0.02       0.25 f
  FW_MEM_TO_EX_A[0] (out)                  0.00       0.25 f
  data arrival time                                   0.25

  max_delay                                0.25       0.25
  output external delay                    0.00       0.25
  data required time                                  0.25
  -----------------------------------------------------------
  data required time                                  0.25
  data arrival time                                  -0.25
  -----------------------------------------------------------
  slack (MET)                                         0.00
```

APPENDIX E

Fetch post synthesis reports

E.1 Load unit

Power report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
LHU                   5K_hvratio_1_1    NangateOpenCellLibrary


Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  =  19.4795 uW   (49%)
  Net Switching Power  =  20.3063 uW   (51%)
                         ---------
Total Dynamic Power    =  39.7858 uW  (100%)

Cell Leakage Power     =   2.5505 uW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %
)  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000            0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000            0.0000            0.0000            0.0000  (   0.00%)
register           0.0000            0.0000            0.0000            0.0000  (   0.00%)
sequential         0.0000            0.0000            0.0000            0.0000  (   0.00%)
combinational     19.4795           20.3063        2.5505e+03           42.3363  ( 100.00%)
--------------------------------------------------------------------------------------------------
Total             19.4795 uW        20.3063 uW     2.5505e+03 nW        42.3363 uW
```

Area report

```
Number of ports:                           67
Number of nets:                           129
Number of cells:                           94
Number of combinational cells:             94
Number of sequential cells:                 0
Number of macros:                           0
Number of buf/inv:                         39
Number of references:                      13

Combinational area:         89.110000
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:            89.110000
Total area:                 undefined
```

Timing report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: DIMENSION[0]
              (input port)
  Endpoint: LHU_OUT[8] (output port)
  Path Group: default
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  LHU                5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 f
  DIMENSION[0] (in)                        0.00       0.00 f
  U217/ZN (INV_X1)                         0.03       0.03 r
  U161/ZN (NOR2_X1)                        0.02       0.06 f
  U165/ZN (NAND2_X1)                       0.03       0.09 r
  U208/Z (BUF_X1)                          0.05       0.13 r
  U219/ZN (OAI221_X1)                      0.04       0.17 f
  LHU_OUT[8] (out)                         0.00       0.18 f
  data arrival time                                   0.18

  max_delay                                0.18       0.18
  output external delay                    0.00       0.18
  data required time                                  0.18
  -----------------------------------------------------------
  data required time                                  0.18
  data arrival time                                  -0.18
  -----------------------------------------------------------
  slack (MET)                                         0.00
```

APPENDIX F

DLX synthesis

In this appendix the synthesis script that has been used to synthesize the whole DLX processor and the produced reports can be found.

F.1 Synthesis script

```
remove_design -all
set files {{"01 - REG_GEN.vhd"} {"02 - MY_PACKAGE.vhd"} {"03 - LOG2.vhd"} {"04 - REG1.
    vhd"} {"a.a - CU.vhd"}
      {"a.b.c.a - ADDER_PC.vhd"} {"a.b.c.b - BTB.vhd"} {"a.b.d.a - ADD_SUB.vhd"} {"a.b
          .d.b - DECODE_IMM_EXT.vhd"} {"a.b.d.c - HAZARD_UNIT.vhd"}
      {"a.b.d.d - JUMP_COMPARATOR.vhd"} {"a.b.d.e - RF_DECODER.vhd"} {"a.b.d.f - STACK
          .vhd"} {"a.b.d.g - WRF.vhd"} {"a.b.e.a.a.a - nand4.vhd"}
      {"a.b.e.a.a.a - nand3.vhd"} {"a.b.e.a.a - LOGICAL.vhd"} {"a.b.e.a.b.c -
          pg_network_gen.vhd"} {"a.b.e.a.b.c - g_block.vhd"} {"a.b.e.a.b.c - pg_block.
          vhd"}
      {"a.b.e.a.b.c - csb_ovf_gen.vhd"} {"a.b.e.a.b.c - csb_gen.vhd"} {"a.b.e.a.b.c -
          P4_carry_gen.vhd"} {"a.b.e.a.b.c - P4_SUM_GEN.vhd"} {"a.b.e.a.b - P4_ADDER.
          vhd"}
      {"a.b.e.a.d.a - mux_encoded.vhd"} {"a.b.e.a.d.a - adder.vhd"} {"a.b.e.a.d -
          MUL_8.vhd"} {"a.b.e.a.f - SHIFTER.vhd"} {"a.b.e.a.c - COMPARATOR.vhd"}
      {"a.b.e.a - ALU.vhd"} {"a.b.e.b - FWU.vhd"} {"a.b.f - LHU.vhd"} {"a.b - DATAPATH
          .vhd"} {"a - DLX.vhd"}}
foreach file $files {
  analyze -library WORK -format VHDL $file
}
elaborate DLX -architecture STRUCTURAL -library WORK
create_clock -name "CLK" -period 2.3 CLK
set_max_delay -from [all_inputs] -to [all_outputs] 2.3
set_clock_gating_style -minimum_bitwidth 1 -max_fanout 1024 -positive_edge_logic {
    latch and} -control_point before
compile -exact_map -gate_clock
report_timing > DLX_timing.txt
report_power > DLX_power.txt
report_area > DLX_area.txt
report_clock_gating > DLX_clock_gating.txt
write -hierarchy -format verilog -output /home/ms20.3/DLX_SYN/DLX_2_3.v
```

F.2 DLX synthesis reports

Power report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
DLX                   5K_hvratio_1_1    NangateOpenCellLibrary


Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  =   6.9017 mW   (80%)
  Net Switching Power  =   1.6937 mW   (20%)
                         ---------
Total Dynamic Power    =   8.5954 mW  (100%)

Cell Leakage Power     =   2.8626 mW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %
)  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000            0.0000  (   0.00%)
clock_network  1.4483e+03         300.9426          4.1056e+04        1.7903e+03  (  15.62%)
register       4.7624e+03          47.6908          1.6637e+06        6.4737e+03  (  56.50%)
sequential         0.0000           0.0000              0.0000            0.0000  (   0.00%)
combinational    691.0439        1.3451e+03          1.1580e+06        3.1941e+03  (  27.88%)
--------------------------------------------------------------------------------------------------
Total          6.9017e+03 uW     1.6938e+03 uW     2.8627e+06 nW     1.1458e+04 uW
```

Area report

```
Number of ports:                          166
Number of nets:                           220
Number of cells:                            2
Number of combinational cells:              0
Number of sequential cells:                 0
Number of macros:                           0
Number of buf/inv:                          0
Number of references:                       2

Combinational area:       51529.786371
Noncombinational area:    100119.737828
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          151649.524199
Total area:                 undefined
```

Timing report

```
Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: datapath_inst/opcd/OUT_DATA_reg[0]
              (rising edge-triggered flip-flop clocked by CLK)
  Endpoint: datapath_inst/btb_inst/clk_gate_full_empty_n_reg_79/latch
            (negative level-sensitive latch clocked by CLK)
  Path Group: CLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  DLX                5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                                          Incr       Path
  ---------------------------------------------------------------------------
  clock CLK (rise edge)                                          0.00       0.00
  clock network delay (ideal)                                    0.00       0.00
  datapath_inst/opcd/OUT_DATA_reg[0]/CK (DFFR_X1)                0.00       0.00 r
  datapath_inst/opcd/OUT_DATA_reg[0]/QN (DFFR_X1)                0.06       0.06 f
  datapath_inst/opcd/U7/ZN (INV_X1)                              0.04       0.10 r
  datapath_inst/opcd/OUT_DATA[0] (REG_GEN_N6)                    0.00       0.10 r
  datapath_inst/OPCODE[0] (DATAPATH)                             0.00       0.10 r
  cu_inst/OPCODE[0] (CU)                                         0.00       0.10 r
  cu_inst/U59/ZN (INV_X1)                                        0.03       0.13 f
  cu_inst/U167/ZN (NAND2_X1)                                     0.03       0.16 r
  cu_inst/U186/ZN (NAND2_X1)                                     0.03       0.19 f
  cu_inst/U64/ZN (AND2_X1)                                       0.04       0.22 f
  cu_inst/U69/ZN (AND2_X2)                                       0.04       0.26 f
  cu_inst/J_INSTR (CU)                                           0.00       0.26 f
  datapath_inst/J_INSTR (DATAPATH)                               0.00       0.26 f
  datapath_inst/decode_IR/J_INSTR (DECODE_IMM_EXT)               0.00       0.26 f
  datapath_inst/decode_IR/U79/ZN (NOR2_X1)                       0.06       0.32 r
  datapath_inst/decode_IR/RS_1[0] (DECODE_IMM_EXT)               0.00       0.32 r
  datapath_inst/rf_dec/READ_1_ADDR[0] (RF_DECODER_M8_N8_F4_N_bit32)
                                                                 0.00       0.32 r
  datapath_inst/rf_dec/U87/ZN (AND2_X1)                          0.05       0.37 r
  datapath_inst/rf_dec/U100/ZN (NAND2_X1)                        0.03       0.40 f
  datapath_inst/rf_dec/U103/ZN (NAND3_X1)                        0.04       0.44 r
  datapath_inst/rf_dec/U123/ZN (NAND2_X1)                        0.03       0.47 f
  datapath_inst/rf_dec/U93/ZN (NAND3_X1)                         0.04       0.51 r
  datapath_inst/rf_dec/U117/ZN (NAND2_X1)                        0.03       0.54 f
  datapath_inst/rf_dec/U120/ZN (NAND3_X1)                        0.03       0.57 r
  datapath_inst/rf_dec/r377/U1_4/CO (FA_X1)                      0.07       0.64 r
  datapath_inst/rf_dec/U12/ZN (AND2_X2)                          0.05       0.69 r
  datapath_inst/rf_dec/U227/ZN (XNOR2_X1)                        0.06       0.74 r
  datapath_inst/rf_dec/U113/ZN (NAND2_X1)                        0.03       0.77 f
  datapath_inst/rf_dec/U112/ZN (XNOR2_X1)                        0.06       0.83 f
  datapath_inst/rf_dec/U95/ZN (NAND2_X1)                         0.04       0.87 r
  datapath_inst/rf_dec/U89/ZN (NAND3_X2)                         0.08       0.95 f
  datapath_inst/rf_dec/READ_1_ADDR_OUT[6] (RF_DECODER_M8_N8_F4_N_bit32)
                                                                 0.00       0.95 f
  datapath_inst/reg_file/READ_1_ADDR[6] (WRF_M8_N8_F4_N_bit32)
                                                                 0.00       0.95 f
  datapath_inst/reg_file/U239/Z (CLKBUF_X1)                      0.05       1.00 f
  datapath_inst/reg_file/U6958/ZN (AND2_X1)                      0.04       1.05 f
  datapath_inst/reg_file/U238/Z (BUF_X2)                         0.06       1.11 f
  datapath_inst/reg_file/U6299/ZN (AOI22_X1)                     0.06       1.17 r
  datapath_inst/reg_file/U6077/ZN (OAI221_X1)                    0.05       1.22 f
  datapath_inst/reg_file/U6074/ZN (NOR4_X1)                      0.08       1.30 r
  datapath_inst/reg_file/U6934/ZN (NAND4_X1)                     0.05       1.35 f
```

```
datapath_inst/reg_file/READ_1[29] (WRF_M8_N8_F4_N_bit32)
                                                  0.00       1.35 f
datapath_inst/U1328/ZN (INV_X1)                   0.03       1.38 r
datapath_inst/U1327/ZN (OAI22_X1)                 0.03       1.42 f
datapath_inst/U1948/ZN (NOR2_X1)                  0.04       1.45 r
datapath_inst/U330/ZN (NAND3_X1)                  0.03       1.49 f
datapath_inst/U223/ZN (NAND2_X1)                  0.03       1.52 r
datapath_inst/U225/ZN (NAND2_X1)                  0.03       1.54 f
datapath_inst/jump_comp/A[29] (JUMP_COMPARATOR)   0.00       1.54 f
datapath_inst/jump_comp/U10/ZN (NOR4_X1)          0.09       1.64 r
datapath_inst/jump_comp/U14/ZN (NAND4_X1)         0.05       1.68 f
datapath_inst/jump_comp/U13/ZN (NOR2_X1)          0.05       1.73 r
datapath_inst/jump_comp/U11/ZN (XNOR2_X1)         0.06       1.79 r
datapath_inst/jump_comp/U3/ZN (AND2_X1)           0.05       1.83 r
datapath_inst/jump_comp/COND (JUMP_COMPARATOR)    0.00       1.83 r
datapath_inst/U2108/ZN (INV_X1)                   0.02       1.86 f
datapath_inst/U425/ZN (AND2_X1)                   0.04       1.89 f
datapath_inst/btb_inst/WRITE_DELETE[0] (BTB)      0.00       1.89 f
datapath_inst/btb_inst/U15452/ZN (INV_X1)         0.04       1.93 r
datapath_inst/btb_inst/U15451/ZN (NAND2_X1)       0.03       1.96 f
datapath_inst/btb_inst/U15450/ZN (OAI21_X1)       0.04       2.00 r
datapath_inst/btb_inst/U302/ZN (AND2_X1)          0.07       2.07 r
datapath_inst/btb_inst/U15429/ZN (NAND2_X1)       0.05       2.12 f
datapath_inst/btb_inst/U307/Z (CLKBUF_X1)         0.06       2.17 f
datapath_inst/btb_inst/U15169/ZN (NOR2_X1)        0.04       2.22 r
datapath_inst/btb_inst/clk_gate_full_empty_n_reg_79/EN (SNPS_CLOCK_GATE_HIGH_BTB_432)
                                                  0.00       2.22 r
datapath_inst/btb_inst/clk_gate_full_empty_n_reg_79/test_or/ZN (OR2_X1)
                                                  0.03       2.25 r
datapath_inst/btb_inst/clk_gate_full_empty_n_reg_79/latch/D (DLL_X1)
                                                  0.01       2.26 r
data arrival time                                            2.26

clock CLK (fall edge)                             1.15       1.15
clock network delay (ideal)                       0.00       1.15
datapath_inst/btb_inst/clk_gate_full_empty_n_reg_79/latch/GN (DLL_X1)
                                                  0.00       1.15 f
time borrowed from endpoint                       1.11       2.26
data required time                                           2.26
-------------------------------------------------------------------------
data required time                                           2.26
data arrival time                                           -2.26
-------------------------------------------------------------------------
slack (MET)                                                  0.00

Time Borrowing Information
-----------------------------------------------------------
CLK pulse width                                   1.15
library setup time                               -0.03
-----------------------------------------------------------
max time borrow                                   1.12
actual time borrow                                1.11
-----------------------------------------------------------
```

Clock gating report

Clock Gating Summary

Number of Clock gating elements	636
Number of Gated registers	19908 (94.71%)
Number of Ungated registers	1113 (5.29%)
Total number of registers	21021