# MC14001B Series

# B-Suffix Series CMOS Gates

## MC14001B, MC14011B, MC14023B, MC14025B, MC14071B, MC14073B, MC14081B, MC14082B

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

### Features

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range.
- Double Diode Protection on All Inputs Except: Triple Diode Protection on MC14011B and MC14081B
- Pin–for–Pin Replacements for Corresponding CD4000 Series B Suffix Devices
- Pb–Free Packages are Available*

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$)

| Symbol | Parameter | Value | Unit |
|--------|-----------|-------|------|
| $V_{DD}$ | DC Supply Voltage Range | −0.5 to +18.0 | V |
| $V_{in}$, $V_{out}$ | Input or Output Voltage Range (DC or Transient) | −0.5 to $V_{DD}$ + 0.5 | V |
| $I_{in}$, $I_{out}$ | Input or Output Current (DC or Transient) per Pin | ±10 | mA |
| $P_D$ | Power Dissipation, per Package (Note 1) | 500 | mW |
| $T_A$ | Ambient Temperature Range | −55 to +125 | °C |
| $T_{stg}$ | Storage Temperature Range | −65 to +150 | °C |
| $T_L$ | Lead Temperature (8–Second Soldering) | 260 | °C |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.
1. Temperature Derating:
   Plastic "P and D/DW" Packages: − 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$). Unused outputs must be left open.
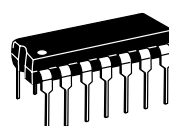
*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
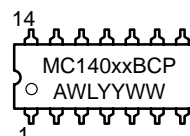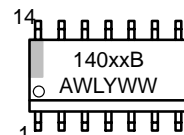
### MARKING DIAGRAMS

PDIP−14
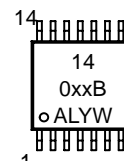P SUFFIX
CASE 646

```
14
MC140xxBCP
AWLYYWW
1
```

SOIC−14
D SUFFIX
CASE 751A

```
14
140xxB
AWLYWW
1
```

TSSOP−14
DT SUFFIX
CASE 948G

```
14
14
0xxB
ALYW
1
```

SOEIAJ−14
F SUFFIX
CASE 965

```
14
MC140xxB
AWLYWW
1
```
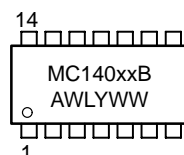
| | |
|---|---|
| xx | = Specific Device Code |
| A | = Assembly Location |
| WL, L | = Wafer Lot |
| YY, Y | = Year |
| WW, W | = Work Week |

### DEVICE INFORMATION

| Device | Description |
|--------|-------------|
| MC14001B | Quad 2–Input NOR Gate |
| MC14011B | Quad 2–Input NAND Gate |
| MC14023B | Triple 3–Input NAND Gate |
| MC14025B | Triple 3–Input NOR Gate |
| MC14071B | Quad 2–Input OR Gate |
| MC14073B | Triple 3–Input AND Gate |
| MC14081B | Quad 2–Input AND Gate |
| MC14082B | Dual 4–Input AND Gate |

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.
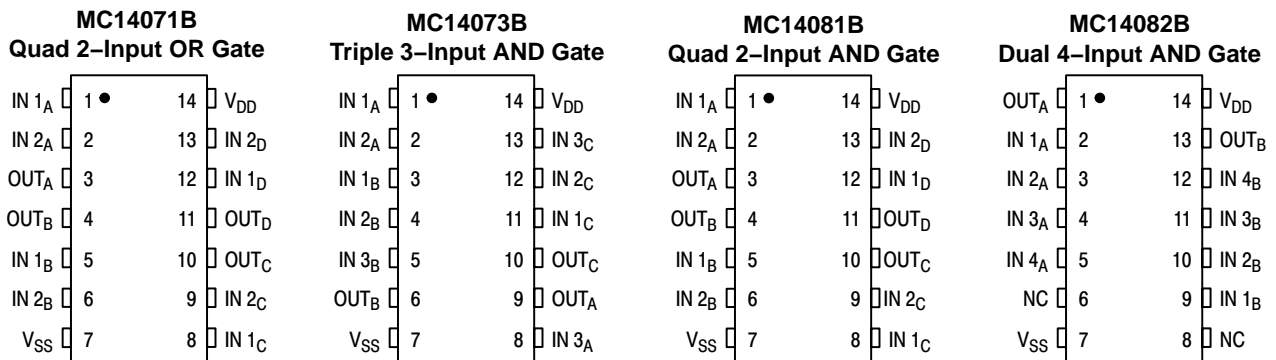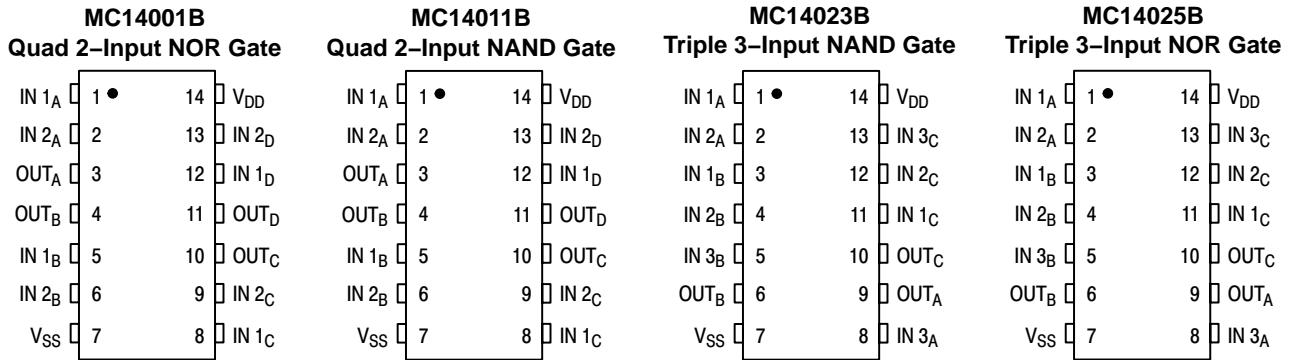
# MC14001B Series

## LOGIC DIAGRAMS

| NOR | NAND | OR | AND |
|---|---|---|---|

### MC14001B
**Quad 2–Input NOR Gate**

### MC14011B
**Quad 2–Input NAND Gate**

### MC14071B
**Quad 2–Input OR Gate**

### MC14081B
**Quad 2–Input AND Gate**

2 INPUT

| | | | |
|---|---|---|---|
| 1, 2 → 3 | 1, 2 → 3 | 1, 2 → 3 | 1, 2 → 3 |
| 5, 6 → 4 | 5, 6 → 4 | 5, 6 → 4 | 5, 6 → 4 |
| 8, 9 → 10 | 8, 9 → 10 | 8, 9 → 10 | 8, 9 → 10 |
| 12, 13 → 11 | 12, 13 → 11 | 12, 13 → 11 | 12, 13 → 11 |

### MC14025B
**Triple 3–Input NOR Gate**

### MC14023B
**Triple 3–Input NAND Gate**

### MC14073B
**Triple 3–Input AND Gate**

### MC14082B
**Dual 4–Input AND Gate**

3 INPUT

| | | | |
|---|---|---|---|
| 1, 2, 8 → 9 | 1, 2, 8 → 9 | 1, 2, 8 → 9 | 2, 3, 4, 5 → 1 |
| 3, 4, 5 → 6 | 3, 4, 5 → 6 | 3, 4, 5 → 6 | 9, 10, 11, 12 → 13 |
| 11, 12, 13 → 10 | 11, 12, 13 → 10 | 11, 12, 13 → 10 | NC = 6, 8 |

$V_{DD}$ = PIN 14
$V_{SS}$ = PIN 7
FOR ALL DEVICES

## PIN ASSIGNMENTS

### MC14001B
**Quad 2–Input NOR Gate**

| | | | |
|---|---|---|---|
| IN $1_A$ | 1 • | 14 | $V_{DD}$ |
| IN $2_A$ | 2 | 13 | IN $2_D$ |
| $OUT_A$ | 3 | 12 | IN $1_D$ |
| $OUT_B$ | 4 | 11 | $OUT_D$ |
| IN $1_B$ | 5 | 10 | $OUT_C$ |
| IN $2_B$ | 6 | 9 | IN $2_C$ |
| $V_{SS}$ | 7 | 8 | IN $1_C$ |

### MC14011B
**Quad 2–Input NAND Gate**

| | | | |
|---|---|---|---|
| IN $1_A$ | 1 • | 14 | $V_{DD}$ |
| IN $2_A$ | 2 | 13 | IN $2_D$ |
| $OUT_A$ | 3 | 12 | IN $1_D$ |
| $OUT_B$ | 4 | 11 | $OUT_D$ |
| IN $1_B$ | 5 | 10 | $OUT_C$ |
| IN $2_B$ | 6 | 9 | IN $2_C$ |
| $V_{SS}$ | 7 | 8 | IN $1_C$ |

### MC14023B
**Triple 3–Input NAND Gate**

| | | | |
|---|---|---|---|
| IN $1_A$ | 1 • | 14 | $V_{DD}$ |
| IN $2_A$ | 2 | 13 | IN $3_C$ |
| IN $1_B$ | 3 | 12 | IN $2_C$ |
| IN $2_B$ | 4 | 11 | IN $1_C$ |
| IN $3_B$ | 5 | 10 | $OUT_C$ |
| $OUT_B$ | 6 | 9 | $OUT_A$ |
| $V_{SS}$ | 7 | 8 | IN $3_A$ |

### MC14025B
**Triple 3–Input NOR Gate**

| | | | |
|---|---|---|---|
| IN $1_A$ | 1 • | 14 | $V_{DD}$ |
| IN $2_A$ | 2 | 13 | IN $3_C$ |
| IN $1_B$ | 3 | 12 | IN $2_C$ |
| IN $2_B$ | 4 | 11 | IN $1_C$ |
| IN $3_B$ | 5 | 10 | $OUT_C$ |
| $OUT_B$ | 6 | 9 | $OUT_A$ |
| $V_{SS}$ | 7 | 8 | IN $3_A$ |

### MC14071B
**Quad 2–Input OR Gate**

| | | | |
|---|---|---|---|
| IN $1_A$ | 1 • | 14 | $V_{DD}$ |
| IN $2_A$ | 2 | 13 | IN $2_D$ |
| $OUT_A$ | 3 | 12 | IN $1_D$ |
| $OUT_B$ | 4 | 11 | $OUT_D$ |
| IN $1_B$ | 5 | 10 | $OUT_C$ |
| IN $2_B$ | 6 | 9 | IN $2_C$ |
| $V_{SS}$ | 7 | 8 | IN $1_C$ |

### MC14073B
**Triple 3–Input AND Gate**

| | | | |
|---|---|---|---|
| IN $1_A$ | 1 • | 14 | $V_{DD}$ |
| IN $2_A$ | 2 | 13 | IN $3_C$ |
| IN $1_B$ | 3 | 12 | IN $2_C$ |
| IN $2_B$ | 4 | 11 | IN $1_C$ |
| IN $3_B$ | 5 | 10 | $OUT_C$ |
| $OUT_B$ | 6 | 9 | $OUT_A$ |
| $V_{SS}$ | 7 | 8 | IN $3_A$ |

### MC14081B
**Quad 2–Input AND Gate**

| | | | |
|---|---|---|---|
| IN $1_A$ | 1 • | 14 | $V_{DD}$ |
| IN $2_A$ | 2 | 13 | IN $2_D$ |
| $OUT_A$ | 3 | 12 | IN $1_D$ |
| $OUT_B$ | 4 | 11 | $OUT_D$ |
| IN $1_B$ | 5 | 10 | $OUT_C$ |
| IN $2_B$ | 6 | 9 | IN $2_C$ |
| $V_{SS}$ | 7 | 8 | IN $1_C$ |

### MC14082B
**Dual 4–Input AND Gate**

| | | | |
|---|---|---|---|
| $OUT_A$ | 1 • | 14 | $V_{DD}$ |
| IN $1_A$ | 2 | 13 | $OUT_B$ |
| IN $2_A$ | 3 | 12 | IN $4_B$ |
| IN $3_A$ | 4 | 11 | IN $3_B$ |
| IN $4_A$ | 5 | 10 | IN $2_B$ |
| NC | 6 | 9 | IN $1_B$ |
| $V_{SS}$ | 7 | 8 | NC |

NC = NO CONNECTION

# MC14001B Series

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to $V_{SS}$)

| Characteristic | Symbol | $V_{DD}$ Vdc | – 55°C | | 25°C | | | 125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Typ [2] | Max | Min | Max | |
| Output Voltage "0" Level<br>$V_{in}$ = $V_{DD}$ or 0 | $V_{OL}$ | 5.0<br>10<br>15 | –<br>–<br>– | 0.05<br>0.05<br>0.05 | –<br>–<br>– | 0<br>0<br>0 | 0.05<br>0.05<br>0.05 | –<br>–<br>– | 0.05<br>0.05<br>0.05 | Vdc |
| "1" Level<br>$V_{in}$ = 0 or $V_{DD}$ | $V_{OH}$ | 5.0<br>10<br>15 | 4.95<br>9.95<br>14.95 | –<br>–<br>– | 4.95<br>9.95<br>14.95 | 5.0<br>10<br>15 | –<br>–<br>– | 4.95<br>9.95<br>14.95 | –<br>–<br>– | Vdc |
| Input Voltage "0" Level<br>($V_O$ = 4.5 or 0.5 Vdc)<br>($V_O$ = 9.0 or 1.0 Vdc)<br>($V_O$ = 13.5 or 1.5 Vdc) | $V_{IL}$ | 5.0<br>10<br>15 | –<br>–<br>– | 1.5<br>3.0<br>4.0 | –<br>–<br>– | 2.25<br>4.50<br>6.75 | 1.5<br>3.0<br>4.0 | –<br>–<br>– | 1.5<br>3.0<br>4.0 | Vdc |
| "1" Level<br>($V_O$ = 0.5 or 4.5 Vdc)<br>($V_O$ = 1.0 or 9.0 Vdc)<br>($V_O$ = 1.5 or 13.5 Vdc) | $V_{IH}$ | 5.0<br>10<br>15 | 3.5<br>7.0<br>11 | –<br>–<br>– | 3.5<br>7.0<br>11 | 2.75<br>5.50<br>8.25 | –<br>–<br>– | 3.5<br>7.0<br>11 | –<br>–<br>– | Vdc |
| Output Drive Current<br>($V_{OH}$ = 2.5 Vdc)   Source<br>($V_{OH}$ = 4.6 Vdc)<br>($V_{OH}$ = 9.5 Vdc)<br>($V_{OH}$ = 13.5 Vdc) | $I_{OH}$ | 5.0<br>5.0<br>10<br>15 | – 3.0<br>– 0.64<br>– 1.6<br>– 4.2 | –<br>–<br>–<br>– | – 2.4<br>– 0.51<br>– 1.3<br>– 3.4 | – 4.2<br>– 0.88<br>– 2.25<br>– 8.8 | –<br>–<br>–<br>– | – 1.7<br>– 0.36<br>– 0.9<br>– 2.4 | –<br>–<br>–<br>– | mAdc |
| ($V_{OL}$ = 0.4 Vdc)   Sink<br>($V_{OL}$ = 0.5 Vdc)<br>($V_{OL}$ = 1.5 Vdc) | $I_{OL}$ | 5.0<br>10<br>15 | 0.64<br>1.6<br>4.2 | –<br>–<br>– | 0.51<br>1.3<br>3.4 | 0.88<br>2.25<br>8.8 | –<br>–<br>– | 0.36<br>0.9<br>2.4 | –<br>–<br>– | mAdc |
| Input Current | $I_{in}$ | 15 | – | ± 0.1 | – | ±0.00001 | ± 0.1 | – | ± 1.0 | µAdc |
| Input Capacitance<br>($V_{in}$ = 0) | $C_{in}$ | – | – | – | – | 5.0 | 7.5 | – | – | pF |
| Quiescent Current<br>(Per Package) | $I_{DD}$ | 5.0<br>10<br>15 | –<br>–<br>– | 0.25<br>0.5<br>1.0 | –<br>–<br>– | 0.0005<br>0.0010<br>0.0015 | 0.25<br>0.5<br>1.0 | –<br>–<br>– | 7.5<br>15<br>30 | µAdc |
| Total Supply Current [3] [4]<br>(Dynamic plus Quiescent,<br>Per Gate, $C_L$ = 50 pF) | $I_T$ | 5.0<br>10<br>15 | | | $I_T$ = (0.3 µA/kHz) f + $I_{DD}$/N<br>$I_T$ = (0.6 µA/kHz) f + $I_{DD}$/N<br>$I_T$ = (0.9 µA/kHz) f + $I_{DD}$/N | | | | | µAdc |

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: $I_T$ is in µA (per package), $C_L$ in pF, V = ($V_{DD}$ – $V_{SS}$) in volts, f in kHz is input frequency, and k = 0.001 x the number of exercised gates per package.

## B–SERIES GATE SWITCHING TIMES

**SWITCHING CHARACTERISTICS** [5] ($C_L$ = 50 pF, $T_A$ = 25°C)

| Characteristic | Symbol | $V_{DD}$ Vdc | Min | Typ [6] | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise Time, All B–Series Gates | $t_{TLH}$ | | | | | ns |
| $\quad t_{TLH}$ = (1.35 ns/pF) $C_L$ + 33 ns | | 5.0 | – | 100 | 200 | |
| $\quad t_{TLH}$ = (0.60 ns/pF) $C_L$ + 20 ns | | 10 | – | 50 | 100 | |
| $\quad t_{TLH}$ = (0.40 ns/PF) $C_L$ + 20 ns | | 15 | – | 40 | 80 | |
| Output Fall Time, All B–Series Gates | $t_{THL}$ | | | | | ns |
| $\quad t_{THL}$ = (1.35 ns/pF) $C_L$ + 33 ns | | 5.0 | – | 100 | 200 | |
| $\quad t_{THL}$ = (0.60 ns/pF) $C_L$ + 20 ns | | 10 | – | 50 | 100 | |
| $\quad t_{THL}$ = (0.40 ns/pF) $C_L$ + 20 ns | | 15 | – | 40 | 80 | |
| Propagation Delay Time | $t_{PLH}$, $t_{PHL}$ | | | | | ns |
| $\quad$ MC14001B, MC14011B only | | | | | | |
| $\quad\quad t_{PLH}, t_{PHL}$ = (0.90 ns/pF) $C_L$ + 80 ns | | 5.0 | – | 125 | 250 | |
| $\quad\quad t_{PLH}, t_{PHL}$ = (0.36 ns/pF) $C_L$ + 32 ns | | 10 | – | 50 | 100 | |
| $\quad\quad t_{PLH}, t_{PHL}$ = (0.26 ns/pF) $C_L$ + 27 ns | | 15 | – | 40 | 80 | |
| $\quad$ All Other 2, 3, and 4 Input Gates | | | | | | |
| $\quad\quad t_{PLH}, t_{PHL}$ = (0.90 ns/pF) $C_L$ + 115 ns | | 5.0 | – | 160 | 300 | |
| $\quad\quad t_{PLH}, t_{PHL}$ = (0.36 ns/pF) $C_L$ + 47 ns | | 10 | – | 65 | 130 | |
| $\quad\quad t_{PLH}, t_{PHL}$ = (0.26 ns/pF) $C_L$ + 37 ns | | 15 | – | 50 | 100 | |
| $\quad$ 8–Input Gates (MC14068B, MC14078B) | | | | | | |
| $\quad\quad t_{PLH}, t_{PHL}$ = (0.90 ns/pF) $C_L$ + 155 ns | | 5.0 | – | 200 | 350 | |
| $\quad\quad t_{PLH}, t_{PHL}$ = (0.36 ns/pF) $C_L$ + 62 ns | | 10 | – | 80 | 150 | |
| $\quad\quad t_{PLH}, t_{PHL}$ = (0.26 ns/pF) $C_L$ + 47 ns | | 15 | – | 60 | 110 | |

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
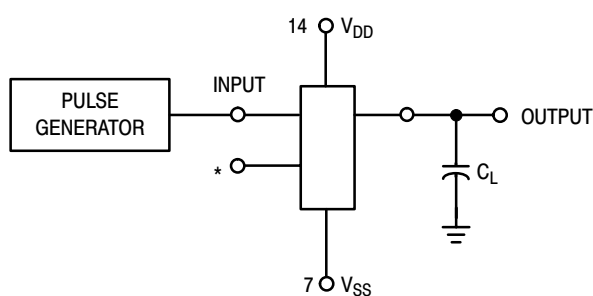


*All unused inputs of AND, NAND gates must be connected to $V_{DD}$.
All unused inputs of OR, NOR gates must be connected to $V_{SS}$.
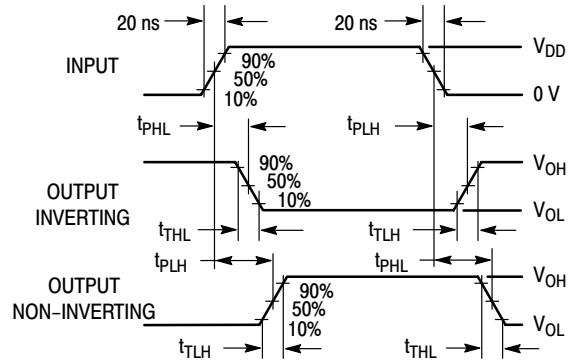
**Figure 1. Switching Time Test Circuit and Waveforms**

# MC14001B Series

## CIRCUIT SCHEMATIC
## NOR, OR GATES

### MC14001B, MC14071B
### One of Four Gates Shown

V_DD

1, 6, 8, 13

2, 5, 9, 12

14  V_DD

3, 4, 10, 11

V_SS

7  V_SS
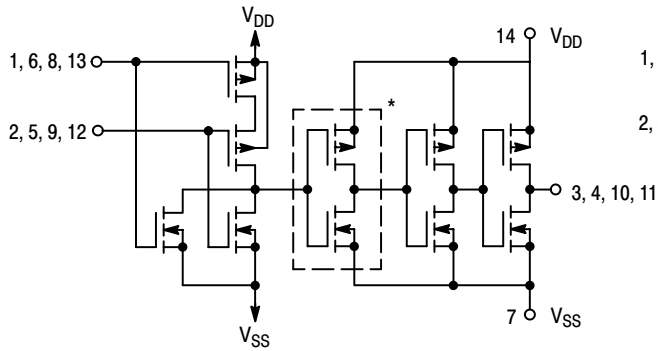
*Inverter omitted in MC14001B

### MC14025B
### One of Three Gates Shown

V_DD

1, 3, 11

2, 4, 12

V_SS

V_DD

8, 5, 13

V_SS

14  V_DD

9, 6, 10

7  V_SS
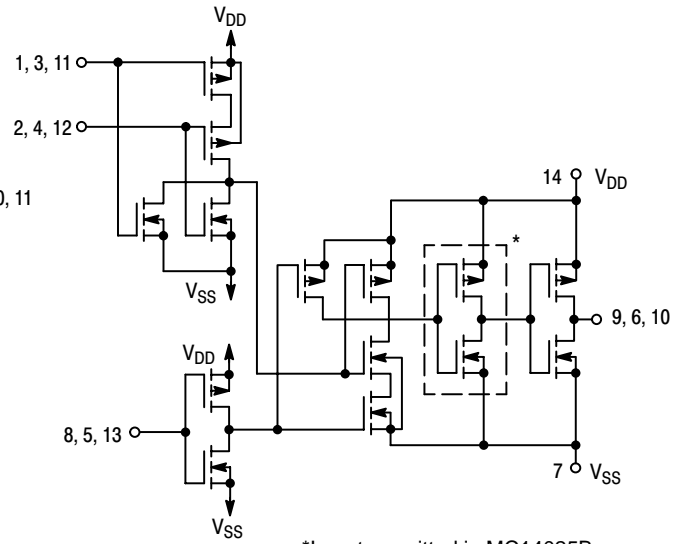
*Inverter omitted in MC14025B

## CIRCUIT SCHEMATIC
## NAND, AND GATES

### MC14023B, MC14073B
### One of Three Gates Shown

V_DD

2, 4, 12

1, 3, 11

V_SS

V_DD

8, 5, 13

V_SS

14  V_DD

9, 6, 10

7  V_SS
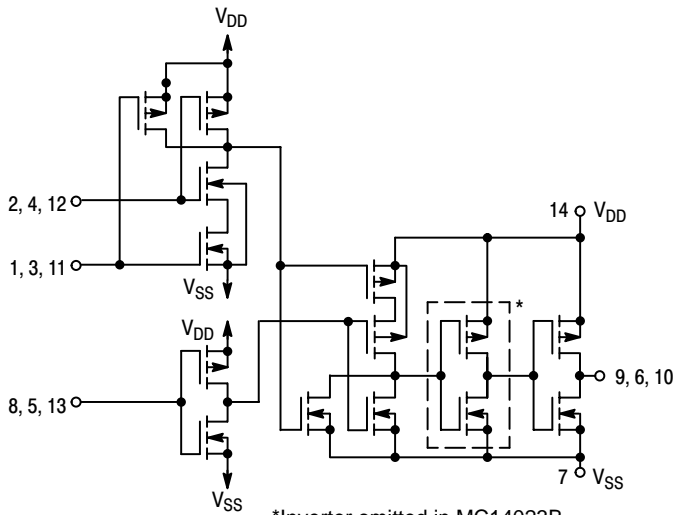
*Inverter omitted in MC14023B

### MC14011B, MC14081B
### One of Four Gates Shown

14  V_DD

3, 4, 10, 11

2, 5, 9, 12

1, 6, 8, 13

7  V_SS
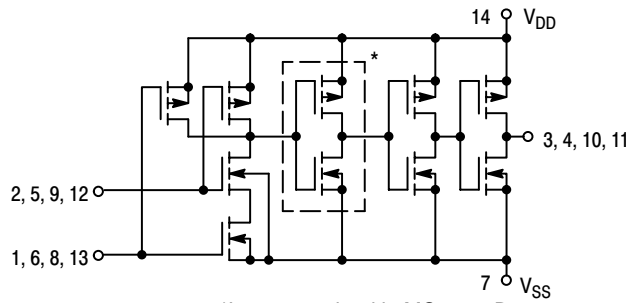
*Inverter omitted in MC14011B

## TYPICAL B–SERIES GATE CHARACTERISTICS

### N–CHANNEL DRAIN CURRENT (SINK)



**Figure 2. V$_{GS}$ = 5.0 Vdc**
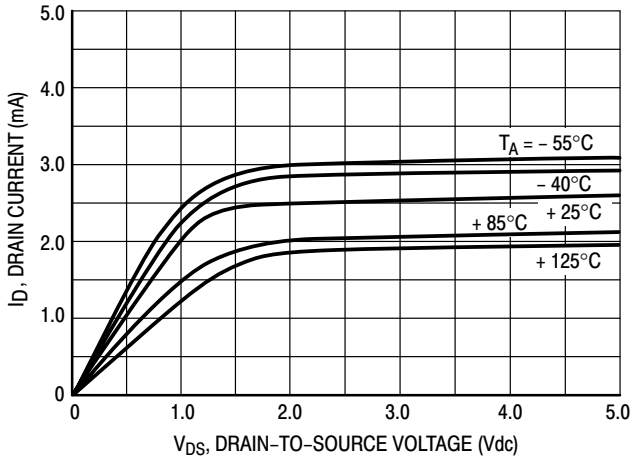


**Figure 4. V$_{GS}$ = 10 Vdc**



**Figure 6. V$_{GS}$ = 15 Vdc**

### P–CHANNEL DRAIN CURRENT (SOURCE)



**Figure 3. V$_{GS}$ = – 5.0 Vdc**
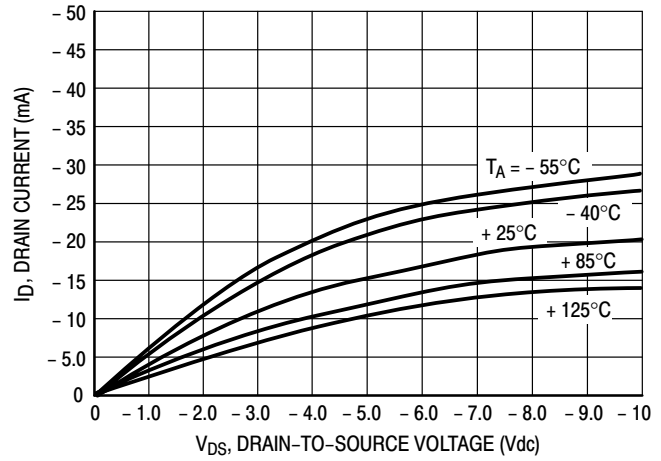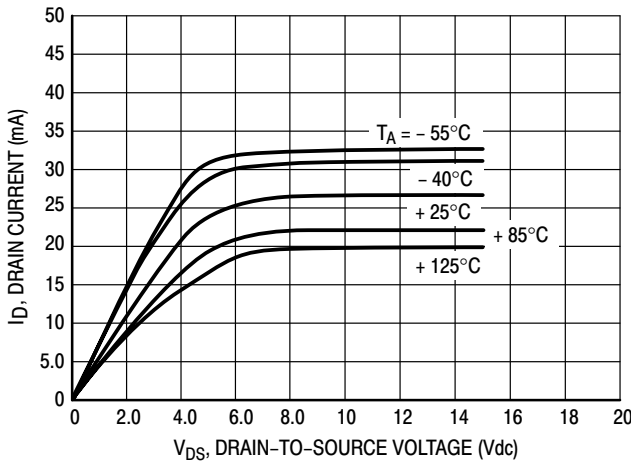


**Figure 5. V$_{GS}$ = – 10 Vdc**
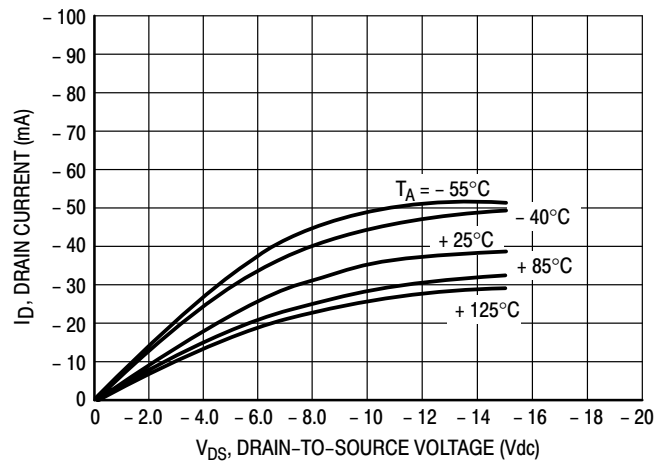


**Figure 7. V$_{GS}$ = – 15 Vdc**

These typical curves are not guarantees, but are design aids.
Caution: The maximum rating for output current is 10 mA per pin.

## TYPICAL B–SERIES GATE CHARACTERISTICS (cont'd)

### VOLTAGE TRANSFER CHARACTERISTICS
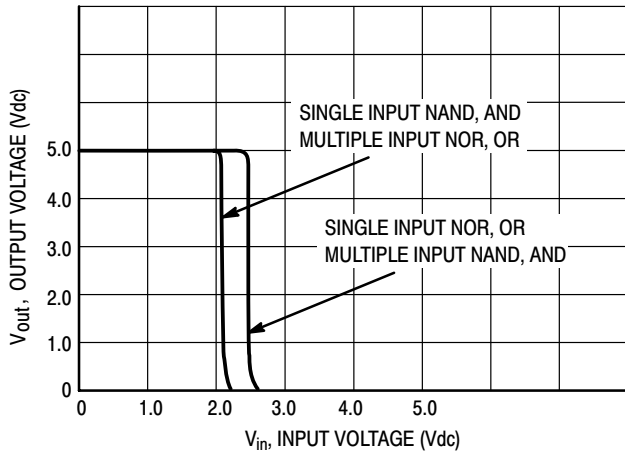


**Figure 8. $V_{DD}$ = 5.0 Vdc**
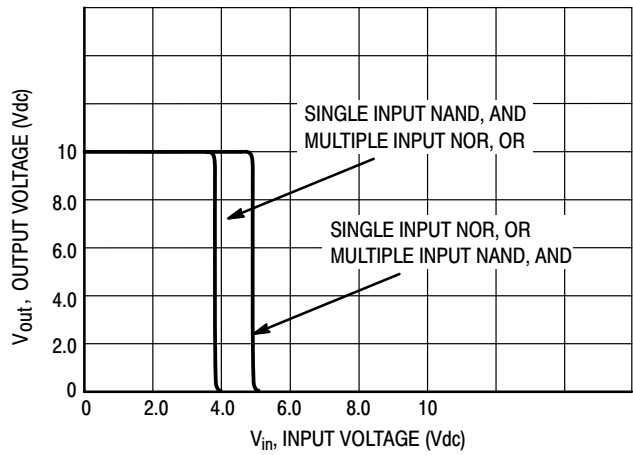


**Figure 9. $V_{DD}$ = 10 Vdc**
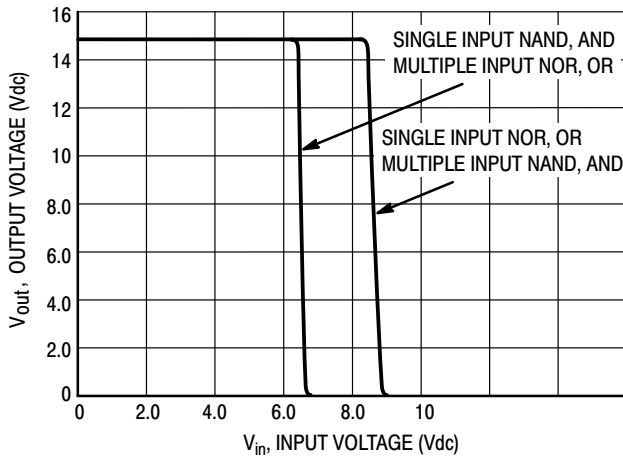


**Figure 10. $V_{DD}$ = 15 Vdc**

### DC NOISE MARGIN

The DC noise margin is defined as the input voltage range from an ideal "1" or "0" input level which does not produce output state change(s). The typical and guaranteed limit values of the input values $V_{IL}$ and $V_{IH}$ for the output(s) to be at a fixed voltage $V_O$ are given in the Electrical Characteristics table. $V_{IL}$ and $V_{IH}$ are presented graphically in Figure 11.

Guaranteed minimum noise margins for both the "1" and "0" levels =

    1.0 V with a   5.0 V supply
    2.0 V with a 10.0 V supply
    2.5 V with a 15.0 V supply
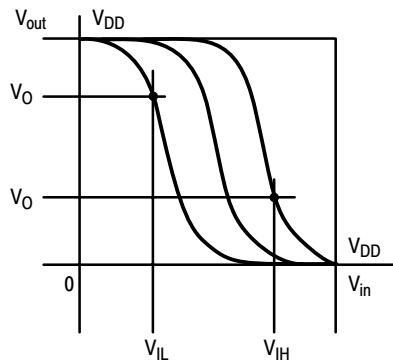


**(a) Inverting Function**
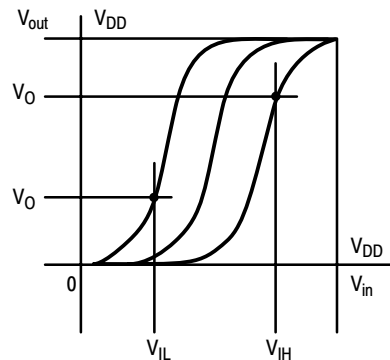
**(b) Non–Inverting Function**

$V_{SS}$ = 0 VOLTS DC

**Figure 11. DC Noise Immunity**

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| MC14001BCP | PDIP–14 | 2000 Units / Box |
| MC14001BCPG | PDIP–14 (Pb–Free) | 2000 Units / Box |
| MC14001BD | SOIC–14 | 2750 Units / Box |
| MC14001BDR2 | SOIC–14 | 2500 Units / Tape & Reel |
| MC14001BDR2G | SOIC–14 (Pb–Free) | 2500 Units / Tape & Reel |
| MC14001BDTR2 | TSSOP–14* | 2500 Units / Tape & Reel |
| MC14001BFEL | SOEIAJ–14 | 2000 Units / Tape & Reel |
| MC14001BFELG | SOEIAJ–14 (Pb–Free) | 2000 Units / Tape & Reel |
| | | |
| MC14011BCP | PDIP–14 | 2000 Units / Box |
| MC14011BCPG | PDIP–14 (Pb–Free) | 2000 Units / Box |
| MC14011BD | SOIC–14 | 2750 Units / Box |
| MC14011BDR2 | SOIC–14 | 2500 Units / Tape & Reel |
| MC14011BDR2G | SOIC–14 (Pb–Free) | 2500 Units / Tape & Reel |
| MC14011BDTR2 | TSSOP–14* | 2500 Units / Tape & Reel |
| MC14011BF | SOEIAJ–14 | 55 Units / Rail |
| MC14011BFEL | SOEIAJ–14 | 2000 Units / Tape & Reel |
| MC14011BFELG | SOEIAJ–14 (Pb–Free) | 2000 Units / Tape & Reel |
| | | |
| MC14023BCP | PDIP–14 | 2000 Units / Box |
| MC14023BCPG | PDIP–14 (Pb–Free) | 2000 Units / Box |
| MC14023BD | SOIC–14 | 2750 Units / Box |
| MC14023BDR2 | SOIC–14 | 2500 Units / Tape & Reel |
| MC14023BDR2G | SOIC–14 (Pb–Free) | 2500 Units / Tape & Reel |
| MC14023BFEL | SOEIAJ–14 | 2000 Units / Tape & Reel |
| | | |
| MC14025BCP | PDIP–14 | 2000 Units / Box |
| MC14025BCPG | PDIP–14 (Pb–Free) | 2000 Units / Box |
| MC14025BD | SOIC–14 | 2750 Units / Box |
| MC14025BDR2 | SOIC–14 | 2500 Units / Tape & Reel |
| MC14025BDR2G | SOIC–14 (Pb–Free) | 2500 Units / Tape & Reel |
| MC14025BFEL | SOEIAJ–14 | 2000 Units / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb–Free.

**ORDERING INFORMATION**

| Device | Package | Shipping[†] |
|---|---|---|
| MC14071BCP | PDIP–14 | 2000 Units / Box |
| MC14071BD | SOIC–14 | 55 Units / Rail |
| MC14071BDR2 | SOIC–14 | 2500 Units / Tape & Reel |
| MC14071BDR2G | SOIC–14 (Pb–Free) | 2500 Units / Tape & Reel |
| MC14071BDT | TSSOP–14* | 96 Units per Rail |
| MC14071BDTR2 | TSSOP–14* | 2500 Units / Tape & Reel |
| MC14071BFEL | SOEIAJ–14 | 2000 Units / Tape & Reel |
| | | |
| MC14073BCP | PDIP–14 | 2000 Units / Box |
| MC14073BCPG | PDIP–14 (Pb–Free) | 2000 Units / Box |
| MC14073BD | SOIC–14 | 55 Units / Rail |
| MC14073BDG | SOIC–14 (Pb–Free) | 55 Units / Rail |
| MC14073BDR2 | SOIC–14 | 2500 Units / Tape & Reel |
| MC14073BDR2G | SOIC–14 (Pb–Free) | 2500 Units / Tape & Reel |
| MC14073BFEL | SOEIAJ–14 | 2000 Units / Tape & Reel |
| | | |
| MC14081BCP | PDIP–14 | 2000 Units / Box |
| MC14081BCPG | PDIP–14 (Pb–Free) | 2000 Units / Box |
| MC14081BD | SOIC–14 | 55 Units / Rail |
| MC14081BDG | SOIC–14 (Pb–Free) | 55 Units / Rail |
| MC14081BDR2 | SOIC–14 | 2500 Units / Tape & Reel |
| MC14081BDR2G | SOIC–14 (Pb–Free) | 2500 Units / Tape & Reel |
| MC14081BDTR2 | TSSOP–14* | 2500 Units / Tape & Reel |
| MC14081BFEL | SOEIAJ–14 | 2000 Units / Tape & Reel |
| MC14081BFELG | SOEIAJ–14 (Pb–Free) | 2000 Units / Tape & Reel |
| | | |
| MC14082BCP | PDIP–14 | 2000 Units / Box |
| MC14082BCPG | PDIP–14 (Pb–Free) | 2000 Units / Box |
| MC14082BD | SOIC–14 | 55 Units / Rail |
| MC14082BDG | SOIC–14 (Pb–Free) | 55 Units / Rail |
| MC14082BDR2 | SOIC–14 | 2500 Units / Tape & Reel |
| MC14082BDR2G | SOIC–14 (Pb–Free) | 2500 Units / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb–Free.

# MC14001B Series

## PACKAGE DIMENSIONS

**P SUFFIX**
PLASTIC DIP PACKAGE
CASE 646–06
ISSUE N
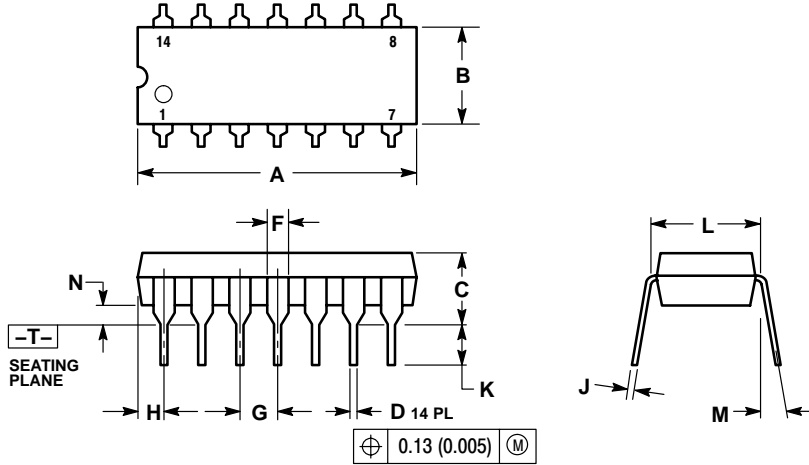


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|--------|-------------|--------|
|     | MIN    | MAX    | MIN         | MAX    |
| A   | 0.715  | 0.770  | 18.16       | 18.80  |
| B   | 0.240  | 0.260  | 6.10        | 6.60   |
| C   | 0.145  | 0.185  | 3.69        | 4.69   |
| D   | 0.015  | 0.021  | 0.38        | 0.53   |
| F   | 0.040  | 0.070  | 1.02        | 1.78   |
| G   | 0.100 BSC | | 2.54 BSC | |
| H   | 0.052  | 0.095  | 1.32        | 2.41   |
| J   | 0.008  | 0.015  | 0.20        | 0.38   |
| K   | 0.115  | 0.135  | 2.92        | 3.43   |
| L   | 0.290  | 0.310  | 7.37        | 7.87   |
| M   | –––    | 10 °   | –––         | 10 °   |
| N   | 0.015  | 0.039  | 0.38        | 1.01   |

**D SUFFIX**
PLASTIC SOIC PACKAGE
CASE 751A–03
ISSUE G
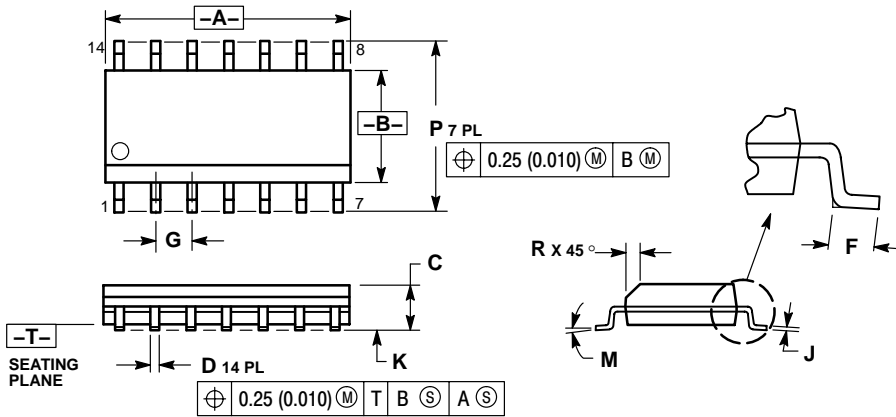


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|--------|--------|--------|
|     | MIN         | MAX    | MIN    | MAX    |
| A   | 8.55        | 8.75   | 0.337  | 0.344  |
| B   | 3.80        | 4.00   | 0.150  | 0.157  |
| C   | 1.35        | 1.75   | 0.054  | 0.068  |
| D   | 0.35        | 0.49   | 0.014  | 0.019  |
| F   | 0.40        | 1.25   | 0.016  | 0.049  |
| G   | 1.27 BSC    |        | 0.050 BSC | |
| J   | 0.19        | 0.25   | 0.008  | 0.009  |
| K   | 0.10        | 0.25   | 0.004  | 0.009  |
| M   | 0 °         | 7 °    | 0 °    | 7 °    |
| P   | 5.80        | 6.20   | 0.228  | 0.244  |
| R   | 0.25        | 0.50   | 0.010  | 0.019  |

## PACKAGE DIMENSIONS

**DT SUFFIX**
PLASTIC TSSOP PACKAGE
CASE 948G–01
ISSUE O
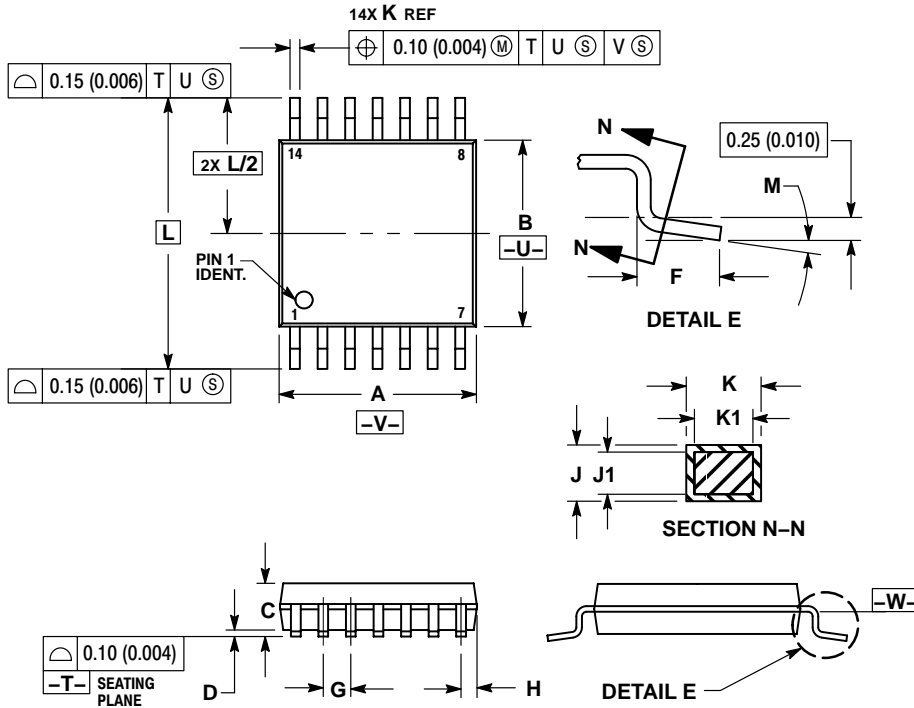
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

| DIM | MILLIMETERS | | INCHES | |
|-----|-----|-----|-----|-----|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | ––– | 1.20 | ––– | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

## PACKAGE DIMENSIONS

**F SUFFIX**
PLASTIC EIAJ SOIC PACKAGE
CASE 965–01
ISSUE O
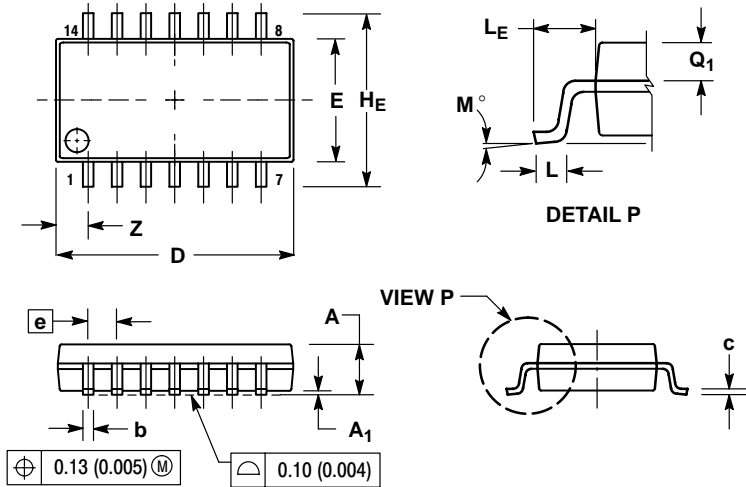


DETAIL P

VIEW P

**NOTES:**
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 ( 0.018).

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| $A_1$ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.18 | 0.27 | 0.007 | 0.011 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| $H_E$ | 7.40 | 8.20 | 0.291 | 0.323 |
| 0.50 | 0.50 | 0.85 | 0.020 | 0.033 |
| $L_E$ | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| $Q_1$ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 1.42 | --- | 0.056 |