CPU

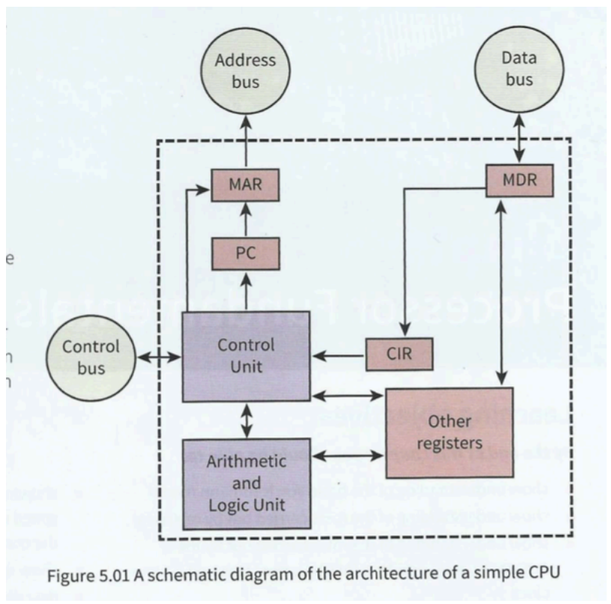

Figure 5.01 A schematic diagram of the architecture of a simple CPU

- ALU
  - Do calculations
- CU
  - Control data flow
  - Ensure program handled correctly
  - Clock
    - Control the cycle of activity
    - Internal — inside
    - System — outside
- Register
  - Accumulator
    - Stores value before and after ALU
Register name	Abbreviation	Register's function
Current instruction register	CIR	Stores the current instruction while it is being decoded and executed
Index register	IX	Stores a value; only used for indexed addressing
Memory address register	MAR	Stores the address of a memory location which is about to have a value read from or written to
Memory data register (memory buffer register)	MDR (MBR)	Stores data that has just been read from memory or is just about to be written to memory
Program counter	PC	Stores the address of where the next instruction is to be read from
Status register	SR	Contains individual bits that are either set or cleared

    Table 5.01 Registers in a simple CPU

System bus

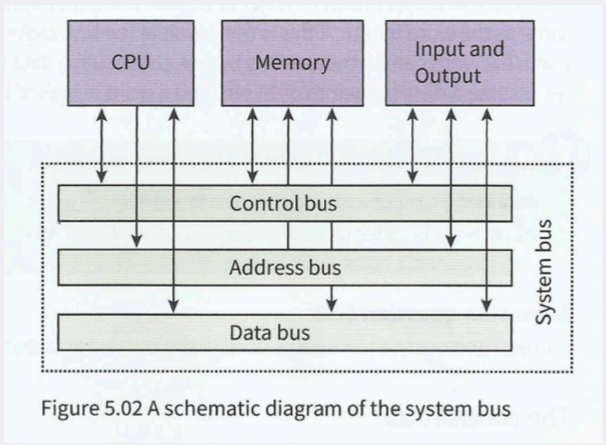

Figure 5.02 A schematic diagram of the system bus

- Parallel transmission device
- Address bus
  - Carry memory addresses
  - One way(cpu to memory)
- Data bus
  - Carry data
    - value
    - address
    - instruction
  - Bus width same as word width
- Word
  - Certain number of bytes
  - Defined in every system
- Control bus
  - Carry signal from control unit to any component
  - Carry timing signals to ensure read/write at the same time
- USB
  - Allow connection of peripheral devices

Fetch and executce

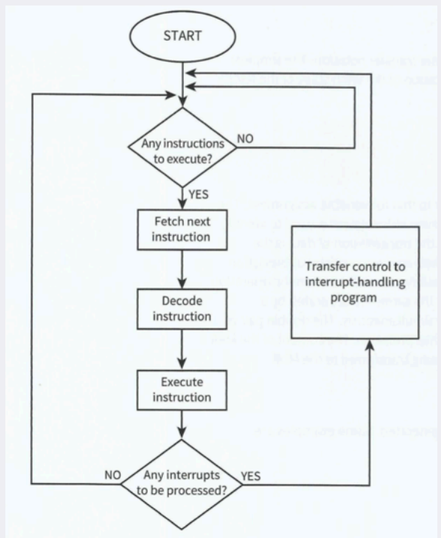

Figure 5.03 Flowchart for the fetch, decode and execute cycle

Registor transfer

```
MAR ← [PC]
PC ← [PC] + 1; MDR ← [[MAR]]
CIR ← [MDR]
```

- Interruption handling
  - Interrupt is detected in each cycle
  - Interruption handling program(interruption service routine is called)
  - When interruption is handled, the program resume