

Logic Testing

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Cs-226: Digital Logic Design



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CADSL

Digital System Realization Process

Customer's need

Determine requirements

Write specifications

ADL

Design synthesis and Verification

Test development

Fabrication

Manufacturing test

① Discrete component
(PCB)

② Integrated circuits
(IC)

Chips to customer

System

2

CADSL



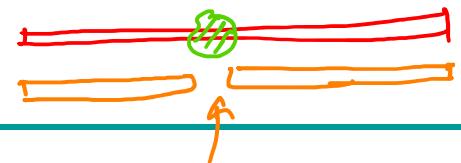
Optimization Parameters

- Area (Cost)
 - No. of gates (switches)
- Performance (delay)
 - No. of switches in signal propagation path (Input to output)
- Power
 - No of gates (indirectly the area as first order model)
- Testability

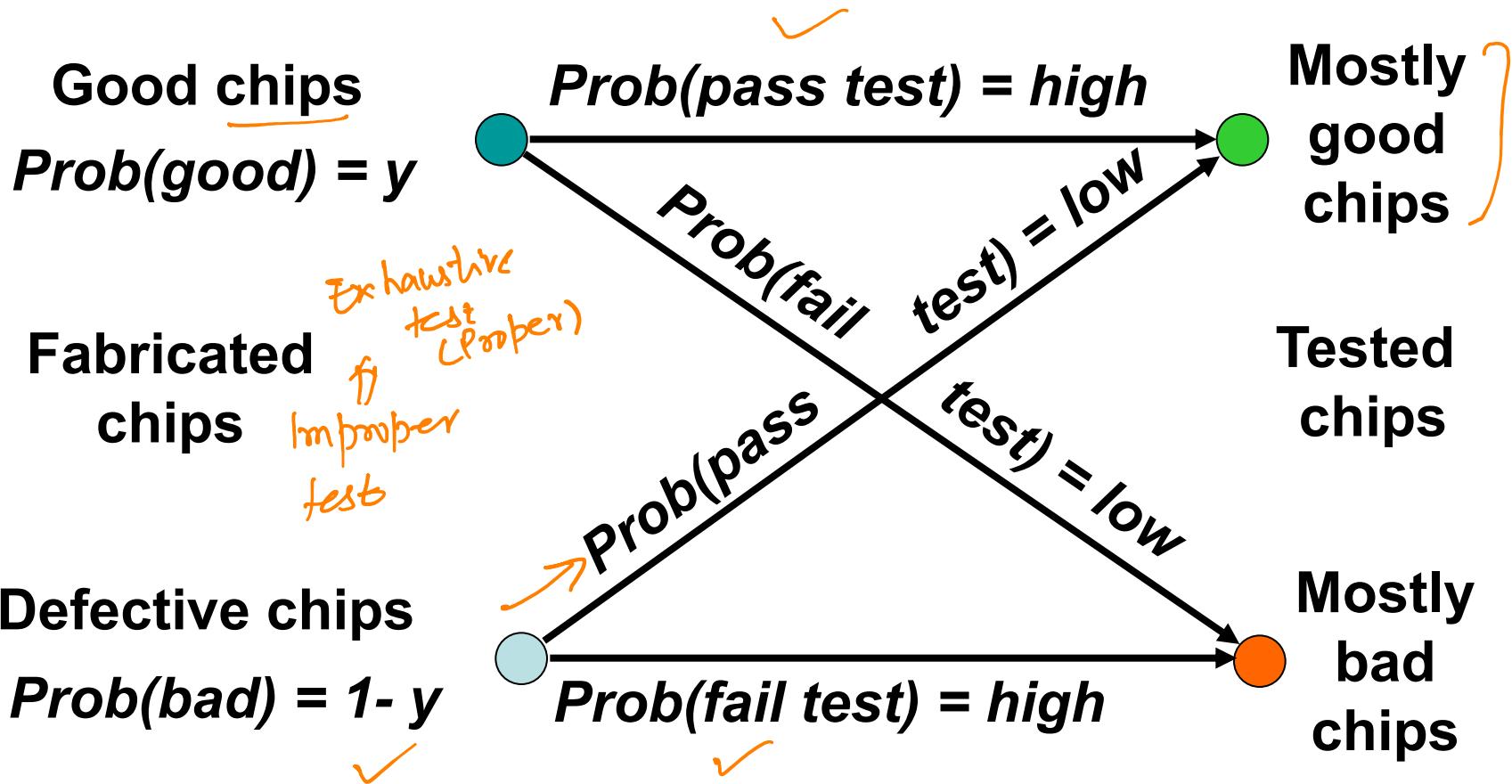


Definitions ✓

- ❖ Design synthesis: Given an I/O function, develop a procedure to manufacture a device using known materials and processes. BA, K-Map, QM ✓
- ❖ Verification: Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given I/O function. ROBDD / SAT ✓
- ❖ Test: A manufacturing step that ensures that the physical device, manufactured from the synthesized design, has no manufacturing defect.



Testing as Filter Process

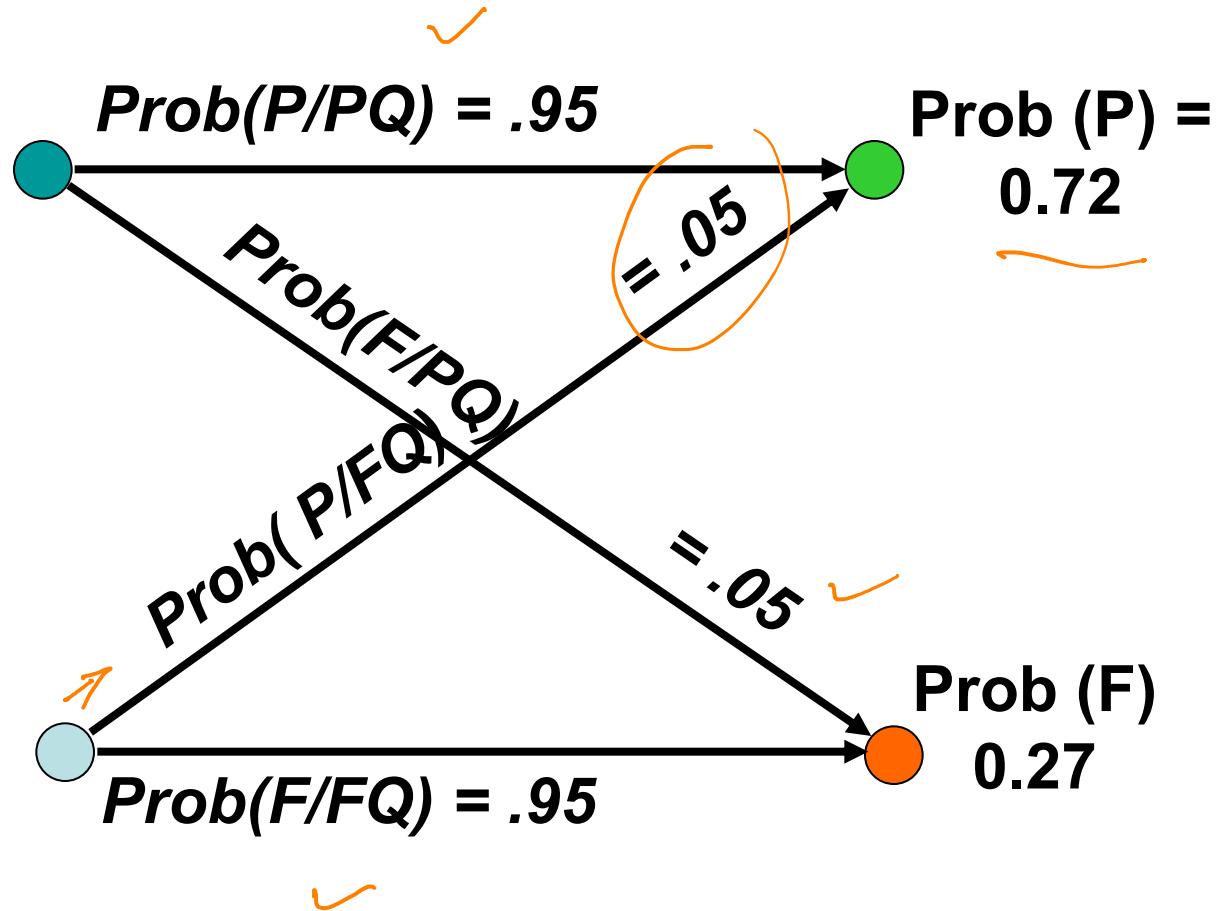


Students Examination

Pass quality
 $\text{Prob}(PQ) = .75$

All
Students

Fail quality
 $\text{Prob}(FQ) = .25$

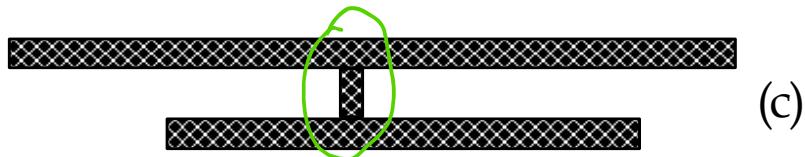
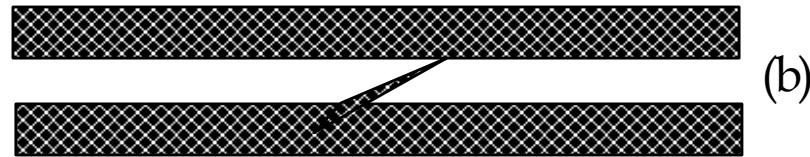


Ideal Tests

- Ideal tests detect all defects produced in the manufacturing process.
- Ideal tests pass all functionally good devices.
- Very large numbers and varieties of possible defects need to be tested..



Defect: Electromigration



(a) Open in a line

(b) Short between two lines (whisker)

(c) Short between lines on different layers (hillock)

Real Tests

- Based on analyzable fault models, which may not map on real defects.
- Incomplete coverage of modeled faults due to high complexity.
- Some good chips are rejected. The fraction (or percentage) of such chips is called the yield loss.
- Some bad chips pass tests. The fraction (or percentage) of bad chips among all passing chips is called the defect level.
 ✓ minimize



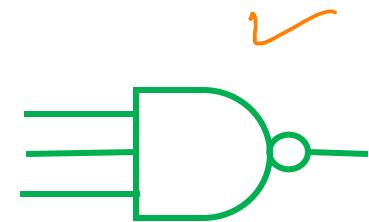
Roles of Testing

- ❖ **Detection:** Determination whether or not the *device under test* (DUT) has some fault. *→ modelled faults*
- ❖ **Diagnosis:** Identification of a specific fault that is present on DUT.
- ❖ Device characterization: Determination and correction of errors in design and/or test procedure.
- ❖ *Failure mode analysis* (FMA): Determination of manufacturing process errors that may have caused defects on the DUT.



IC Testing is a Difficult Problem

- Need $2^3 = 8$ input patterns to exhaustively test a 3-input NAND
- 2^N tests needed for N-input circuit
- Many ICs have > 100 inputs



3-input NAND

$$2^{100} = 1.27 \times 10^{30}$$

$\frac{10^{30}}{10^9} = 10^{21}$

Applying 10^{30} tests at 10^9 per second (1 GHZ) will require 10^{21} secs = 400 billion centuries!

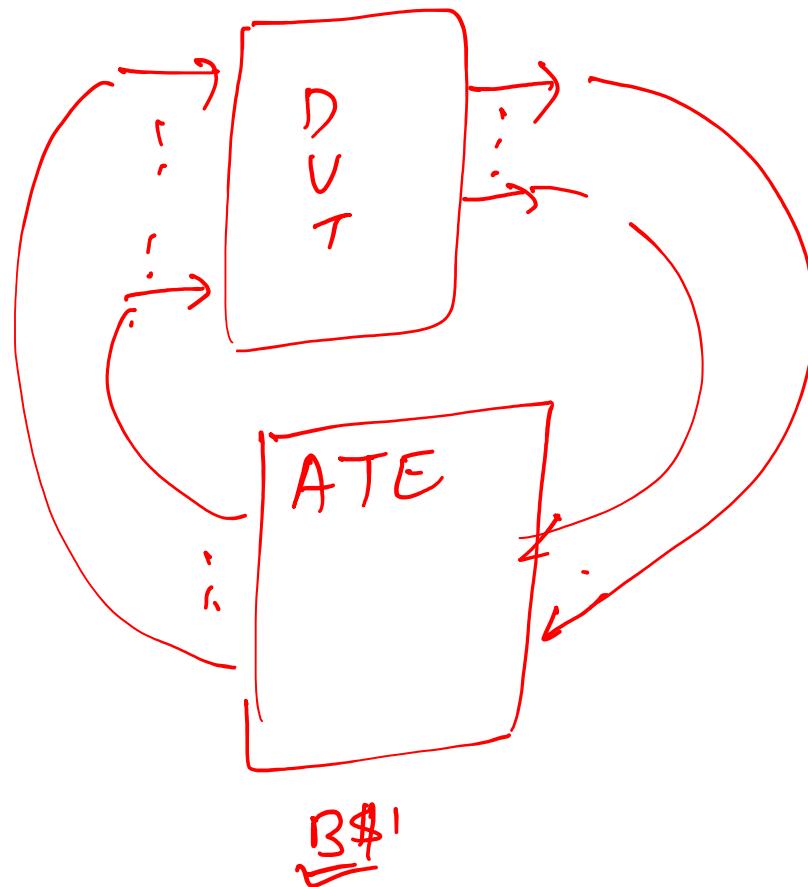
→ impractical

- Only a very few input combinations can be applied in practice

reasonable time ?



Reasonable



₹ 5-6 / sec

1 minute ✓

$$5 \times 60 = \underline{\underline{300}}$$

Reasonable time

↪ few seconds

↓
application



IC Testing in Practice

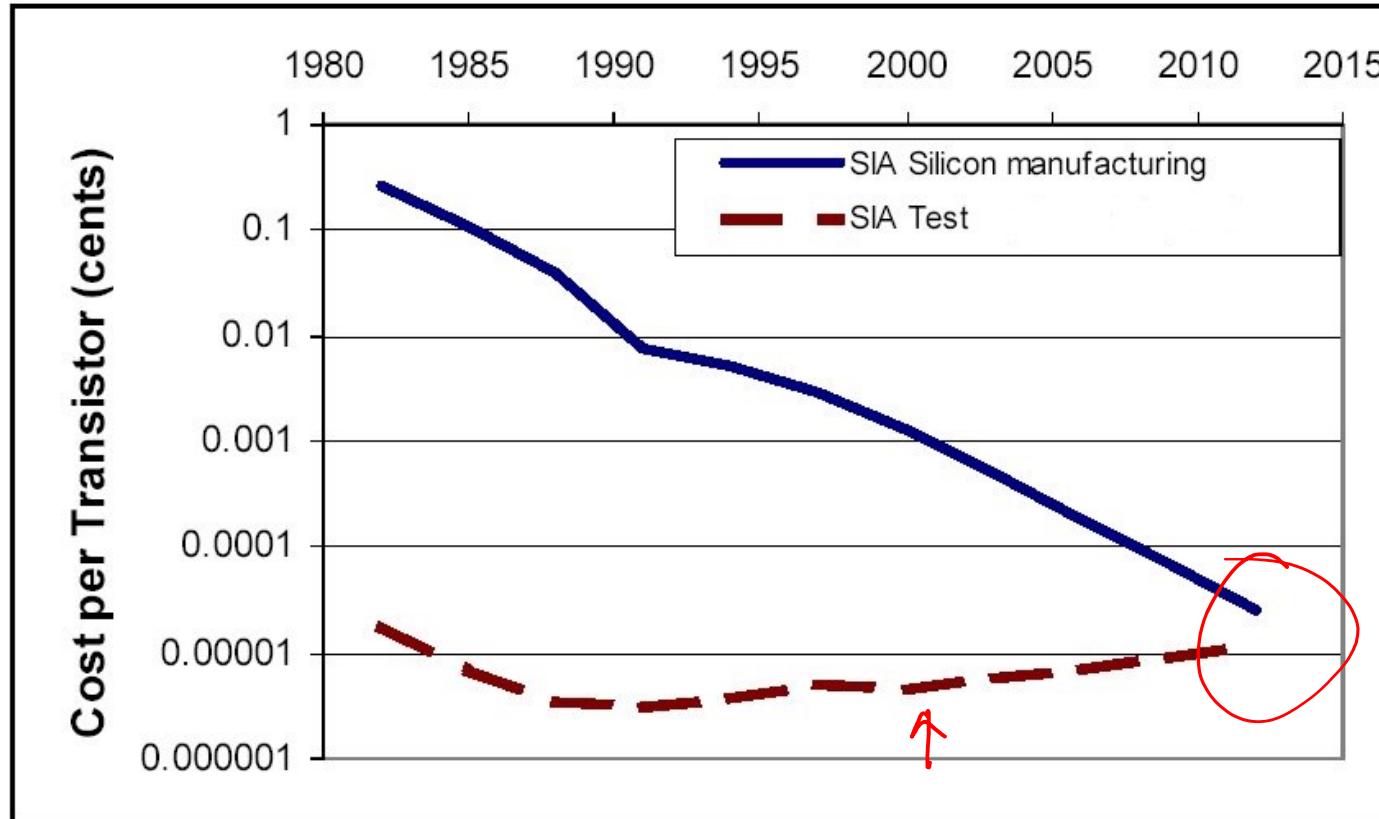
For high end circuits ✓

- A few seconds of test time on very expensive production testers (LATE)
 - Many thousand test patterns applied
 - Test patterns carefully chosen to detect
 - High economic impact
- test costs are approaching manufacturing costs
- Exhaustive
B Years → few secnd.



Microprocessor Cost per Transistor

Cost of testing will *EXCEED* cost of design/manufacturing



(Source: ITR-Semiconductor, 2002)

Definitions

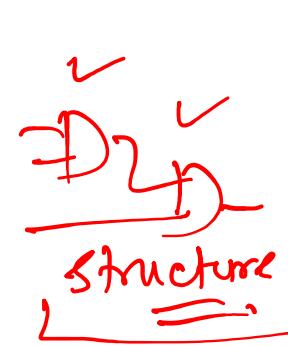
- ❖ **Defect:** A defect in an electronic system is the unintended difference between the implemented hardware and its intended design

 - ❖ **Error:** A wrong output signal produced by defective system is called error. An error is an effect whose cause is some defect] 1/10

 - ❖ **Fault:** A representation of a defect at the abstracted function level is called a fault FAULT
-



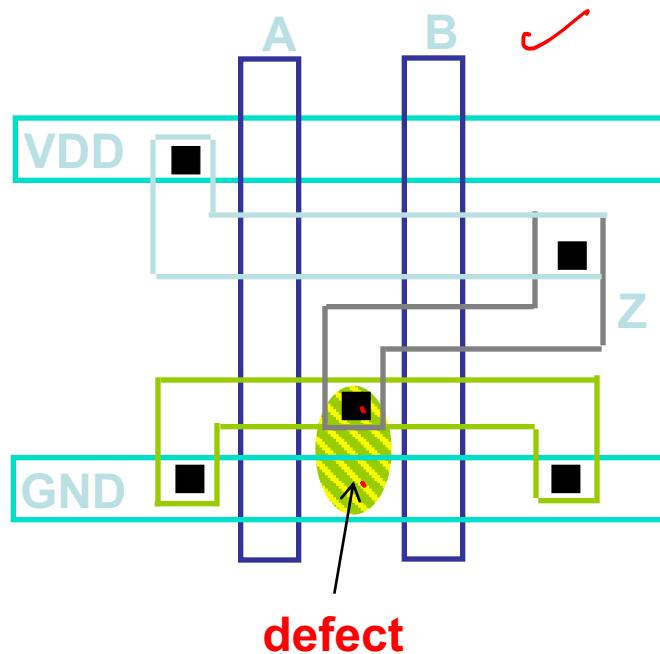
Why Model Faults?

- ❖ I/O function tests inadequate for manufacturing (functionality versus component and interconnect testing)

- ❖ Real defects (often mechanical) too numerous and often not analyzable
- ❖ A fault model identifies targets for testing
- ❖ A fault model makes analysis possible
- ❖ Effectiveness measurable by experiments

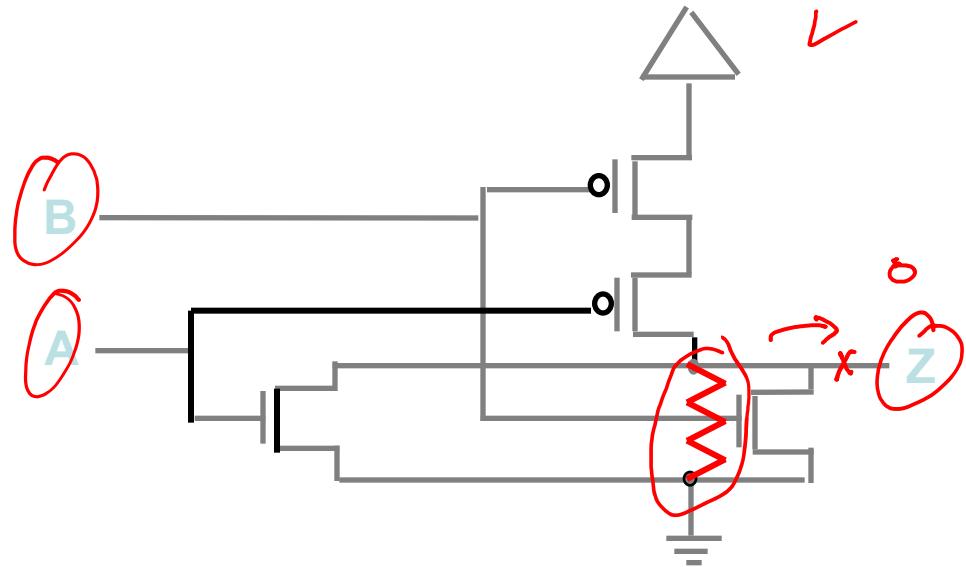


Fault Modeling

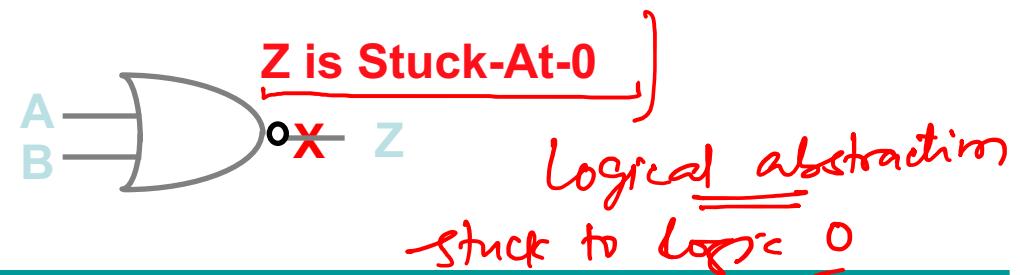
- Physical Model



- Electrical Model



- Logical Model

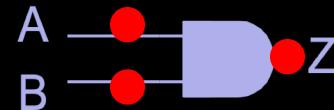


Stuck-At Fault as a Logic Fault

- Stuck-at Fault is a *Functional Fault* on a Boolean (Logic) Function Implementation
- It is not a Physical Defect Model
 - Stuck-at 1 does not imply line is shorted to V_{DD}
 - Stuck-at 0 does not imply line is grounded!
- It is an Abstract fault model
 - A logic stuck-at 1 means when the line is applied a logic 0, it produces a logical error
 - A Logic Error means 0 becomes 1 or vice versa
- It is independent of the underlying technology
 - CMOS, BJT, III-V Semiconductor, Carbon nanotubes etc.



SA Faults



Inputs	FF	Faulty Response						
AB	Response	A/0	B/0	Z/0	A/1	B/1	Z/1	✓

{ 00	0	0	0	0	0	0	1	
	01	0	0	0	1	0	1	✓
	10	0	0	0	0	1	1	
	11	1	0	0	1	1	1	



faults \propto # nets

$$\approx g.(\underline{\text{nets}})$$

fault

no uniqueness

SINGLE
STUCK - AT
FAULT
MODEL

Fault \rightarrow detected by multiple vectors
Vector \rightarrow can detect multiple faults

optimization

Select minimum no. of vectors to detect all possible faults.



Thank You

