CS 254 - Assignment 2

Note: ***For all questions, only structural VHDL code is permitted. (Difference between Structural, Data flow, and Behavioural code were explained in class on 3/02/2021). Also for every question, the top-level entity description is given. It must be used exactly as it is in your code without changing the entity name or any of the port names and the port names must be in the same order. Don't forget to use the ieee.std_logic_1164 library data types. (Bit and bit vector are not permitted.)***

1) Design a 2x1 Multiplexer from basic gates (AND, OR, NOT, etc). i(1) and i(0) are inputs. (MSB and LSB respectively) and 'sel' is the select line. The output is 'z'.

```
entity TwoByOneMux is
        port ( i   : in std_logic_vector(1 downto 0);
               sel : in std_logic;
               z   : out std_logic);
end entity;
```

2) Design a 4x1 Multiplexer using only 2x1 Multiplexers. Vectors 'i' and 'sel' are inputs and select lines respectively and 'z' is the output.

```
entity FourbyOneMux is
        port ( i : in std_logic_vector(3 downto 0):
                 sel: in std_logic_vector(1 downto 0);
                 z : out std_logic);
end entity;
```

3) Design an 8x3 Encoder. Vector 'i' is the input, 'en' is the enable pin and 'z' is the output.

```
entity EightbyThreeEncode is
        port ( i : in std_logic_vector(7 downto 0):
                 en: in std_logic;
                 z : out std_logic_vector(2 downto 0));
end entity;
```

4) Design a 3x8 Decoder. Vector ‘i’ is the input, ‘en’ is the enable pin and ‘z’ is the output.

```
entity ThreebyEightDecode is
        port ( i : in std_logic_vector(2 downto 0):
                en: in std_logic;
                z : out std_logic_vector(7 downto 0));
end entity;
```

Things required in Submission:

1. All VHDL files of top-level and sub-components. (.vhd or .vhdl files)
2. Screenshot of Waveform.

Note: Test bench is not required in submission but create a test bench and use it to test your design before submission. The waveforms generated during your test should be uploaded. No other project files are required. The vhdl files of each question should be kept in a separate folder.