

Logic Testing

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CS-226: Digital Logic Design

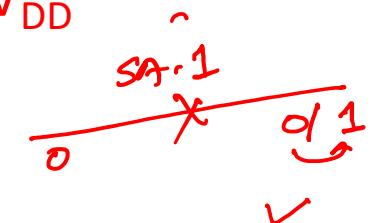


Lecture 32-B: 20 April 2021

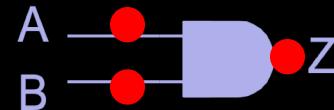
CADSL

Stuck-At Fault as a Logic Fault

- Stuck-at Fault is a *Functional Fault* on a Boolean (Logic) Function Implementation
- It is not a Physical Defect Model
 - Stuck-at 1 does not imply **line is shorted to V_{DD}**
 - Stuck-at 0 does not imply **line is grounded!**
- It is an **Abstract fault model**
 - A logic stuck-at 1 means when the line is applied a logic 0, it produces a logical error
 - A Logic Error means 0 becomes 1 or vice versa
- It is independent of the underlying technology
 - CMOS, BJT, III-V Semiconductor, Carbon nanotubes etc.



SA Faults



Inputs	FF	Faulty Response
AB	Response	A/0 B/0 Z/0 A/1 B/1 Z/1

00	0	0 0 0 0 0 1
01	0	0 0 0 1 0 1
10	0	0 0 0 0 1 1
11	1	0 0 0 1 1 1

Annotations on the left side:

- {B, Z1}
- {A0, B0, Z0}

Annotations on the right side (circled in red):

- 1 (in the row for AB=01)
- 1 (in the row for AB=10)
- 1 (in the row for AB=11)
- 0 (in the row for AB=01)
- 0 (in the row for AB=10)
- 0 (in the row for AB=11)

Fault → detectable by multiple test vectors

Vector → can detect multiple faults

OPTIMIZE

↑ # test vectors

s.t TV_s can cover all
the faults

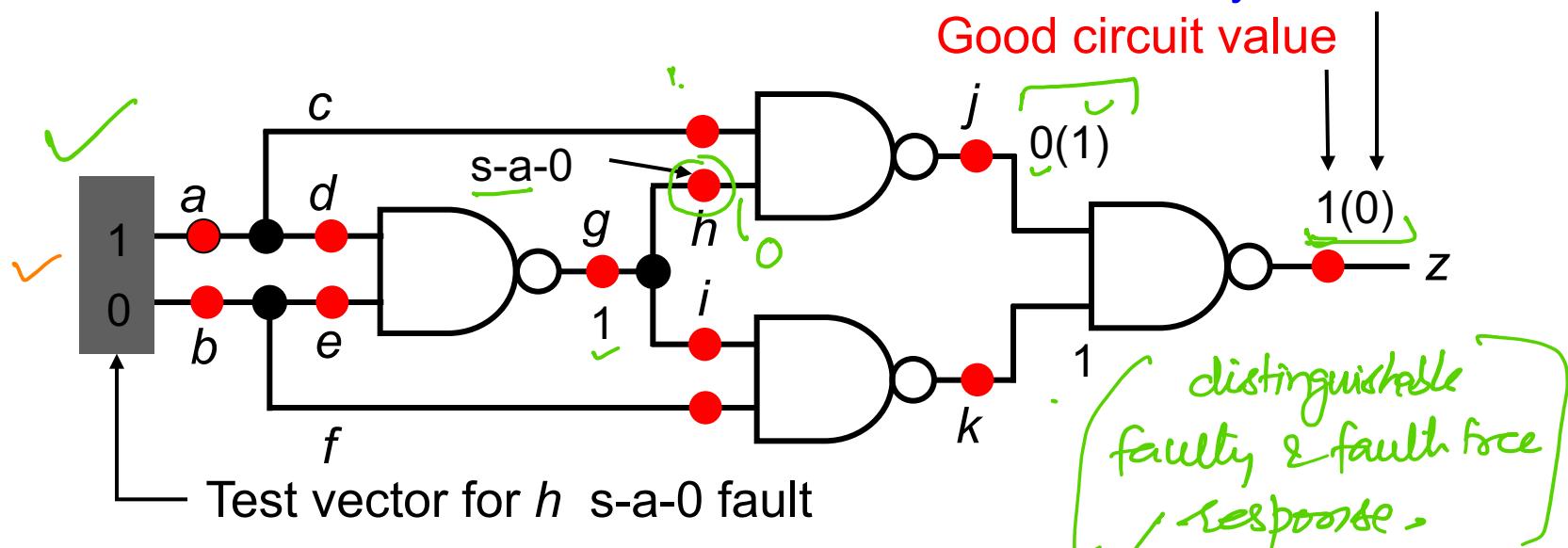
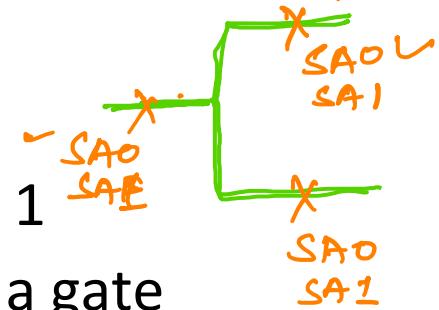
Functional ✗

Structural test ✓



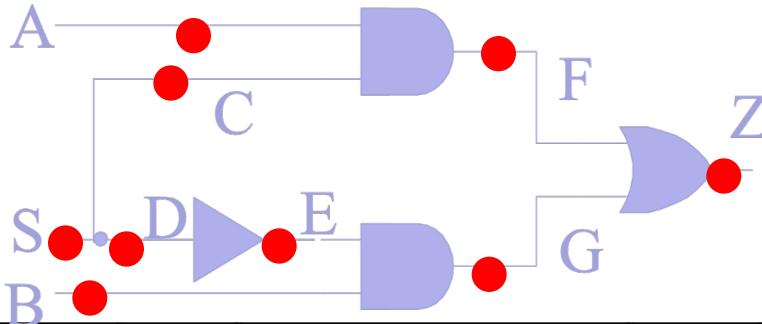
Single Stuck-at Fault

- Three properties define a single stuck-at fault
 - Only one line is faulty
 - The faulty line is permanently set to 0 or 1
 - The fault can be at an input or output of a gate
- Example: XOR circuit has 12 fault sites (●) and 24 single stuck-at faults



SA Faults

MUX



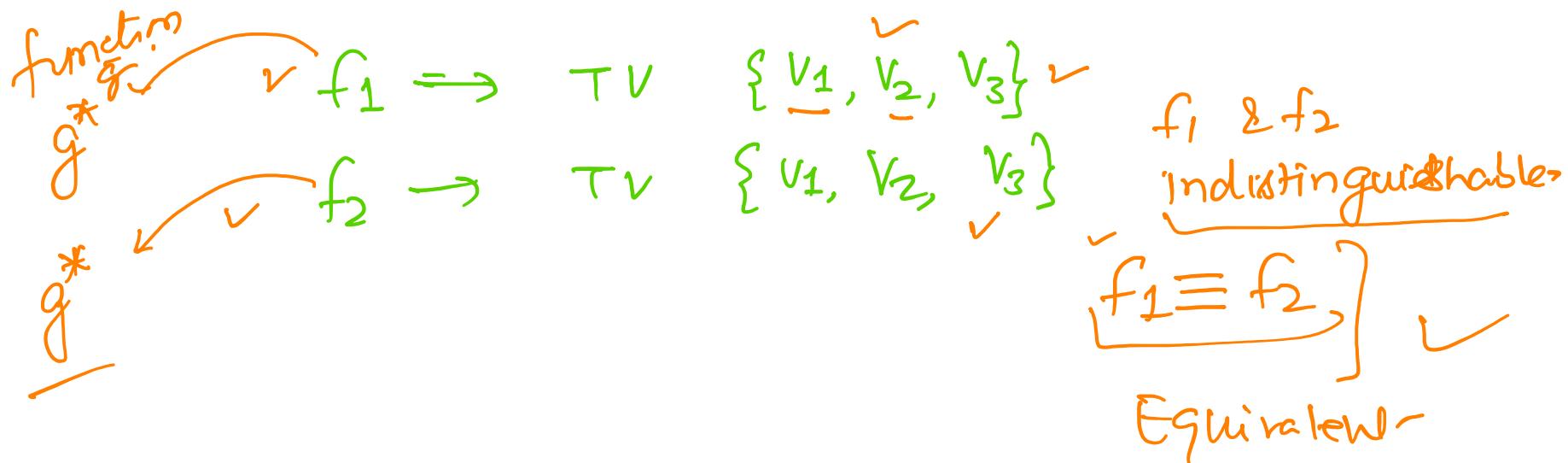
Inp	Response							
	SA	FF	S/0	S/1	C/0	C/1	D/0	D/1
000	000	0	0	0	0	0	0	0
001	001	1	1	0	1	1	1	0
010	010	0	0	1	0	1	0	0
011	011	1	1	1	1	1	1	0
100	100	0	0	0	0	0	0	0
101	101	0	1	0	0	0	1	0
110	110	1	0	1	0	1	1	1
111	111	1	1	1	0	1	1	1



minimum no. of test vectors

Set of faults → take one fault & generate the vector which can detect

$\min \{\# \text{ faults}\}$ → for which we need to generate TV.



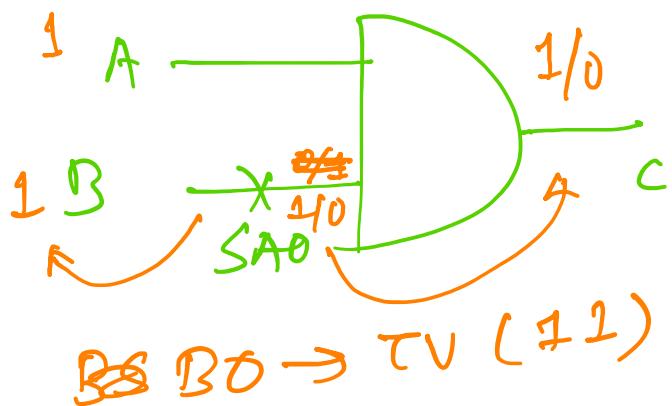
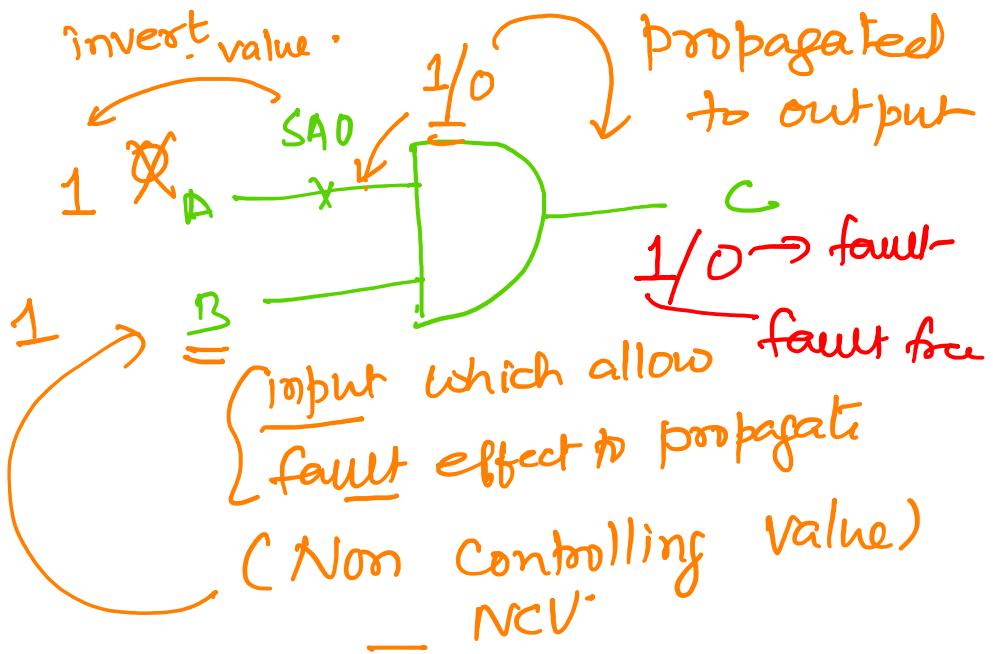
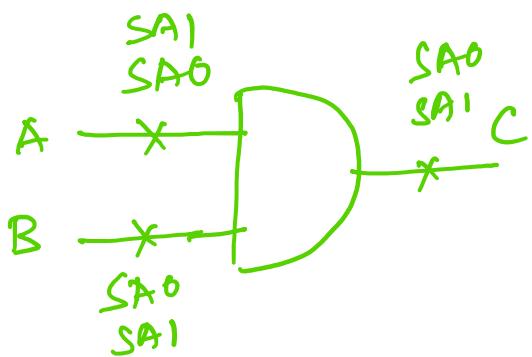
Fault Equivalence

- Number of fault sites in a Boolean gate circuit = $\# \text{PI} + \# \text{gates} + \# (\text{fanout branches})$.
- **Fault equivalence:** Two faults f_1 and f_2 are equivalent if all tests that detect f_1 also detect f_2 .
- If faults f_1 and f_2 are equivalent then the corresponding faulty functions are identical.
- **Fault collapsing:** All single faults of a logic circuit can be divided into disjoint equivalence subsets, where all faults in a subset are mutually equivalent. A collapsed fault set contains one fault from each equivalence subset.

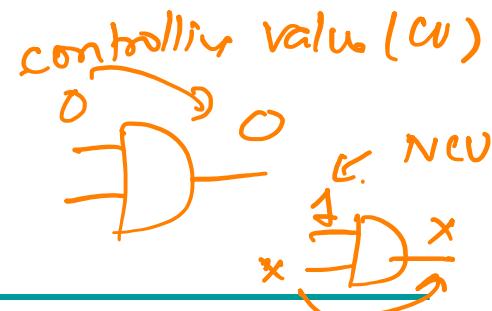
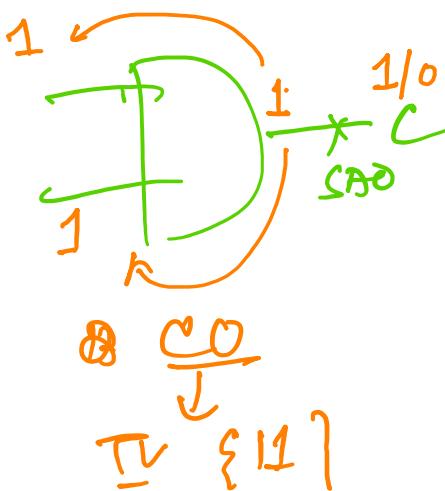
$\{f_1, f_2\}$, $\{f_3, f_5, f_6\}$, $\{f_4, f_8\}$, f_7

target FL = $\{f_1, f_3, f_4, f_7\}$

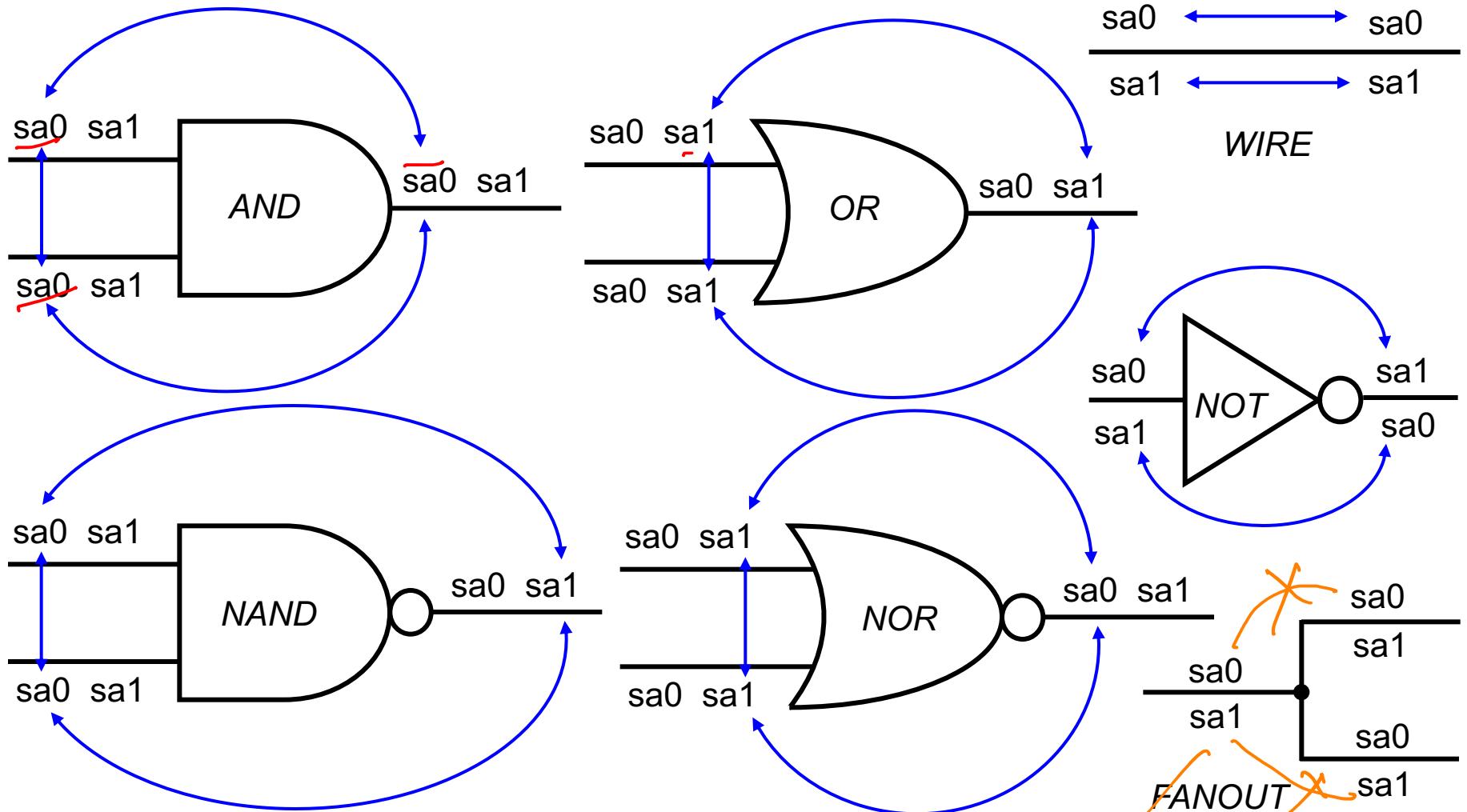




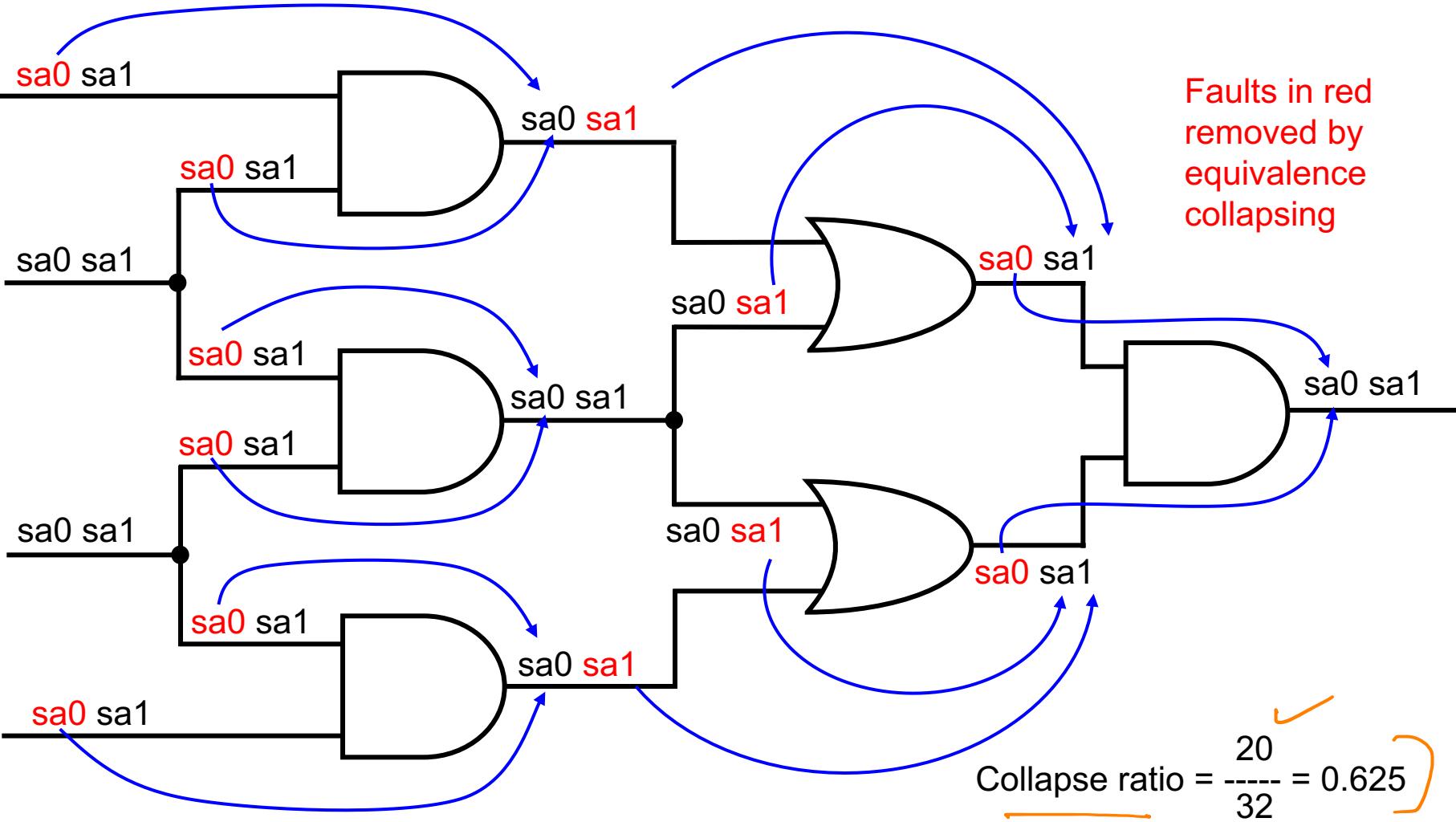
$\{SAO, BO, CO\} \rightarrow TV(11)$

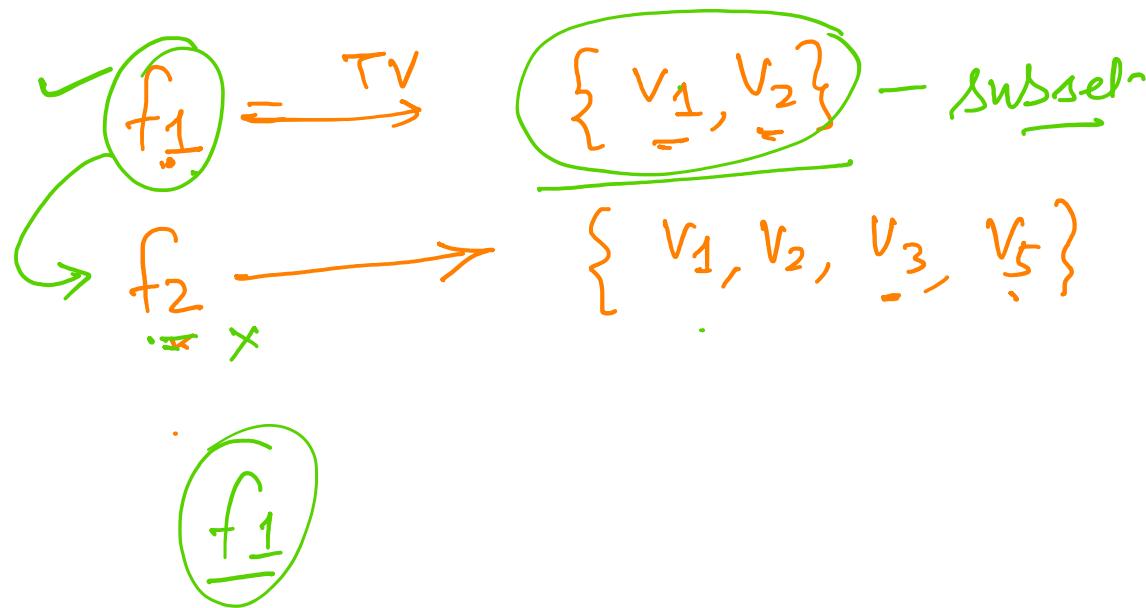


Equivalence Rules



Equivalence Example



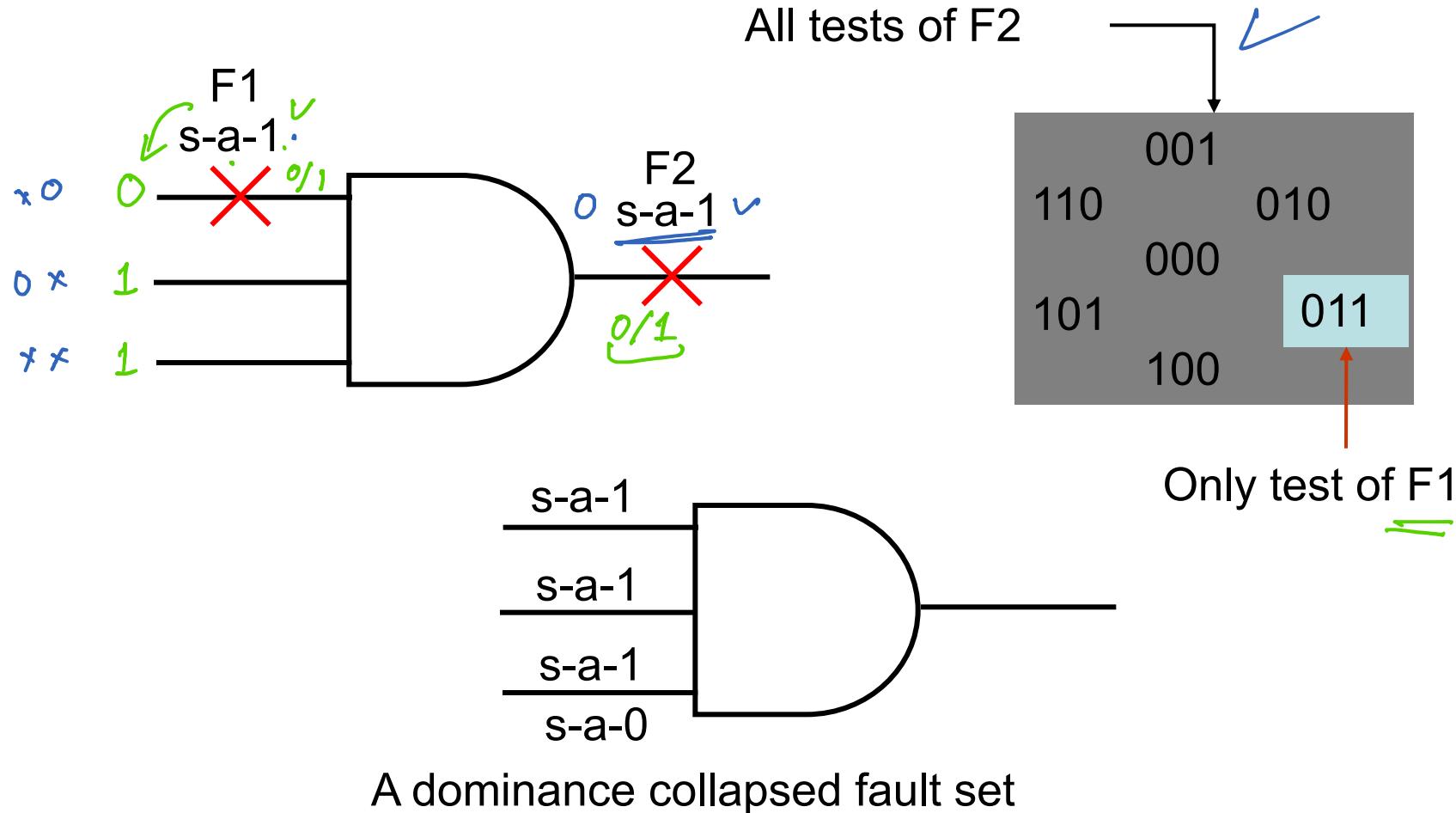


Fault Dominance ✓

- ❖ If all tests of some fault F1 detect another fault F2, then F2 is said to dominate F1.
- ❖ Dominance fault collapsing: If fault F2 dominates F1, then F2 is removed from the fault list.
- ❖ When dominance fault collapsing is used, it is sufficient to consider only the input faults of Boolean gates.
- ❖ In a tree circuit (without fanouts) PI faults form a dominance collapsed fault set.
- ❖ If two faults dominate each other then they are equivalent.



Dominance Example



Test Generation

By using $\underline{FE} \geq \underline{FD}$] reduce the no. of faults

take one by one fault &
generate the test.

Minimize ΣV .



Thank You

