Digital Logic Design Lab
Lab 8

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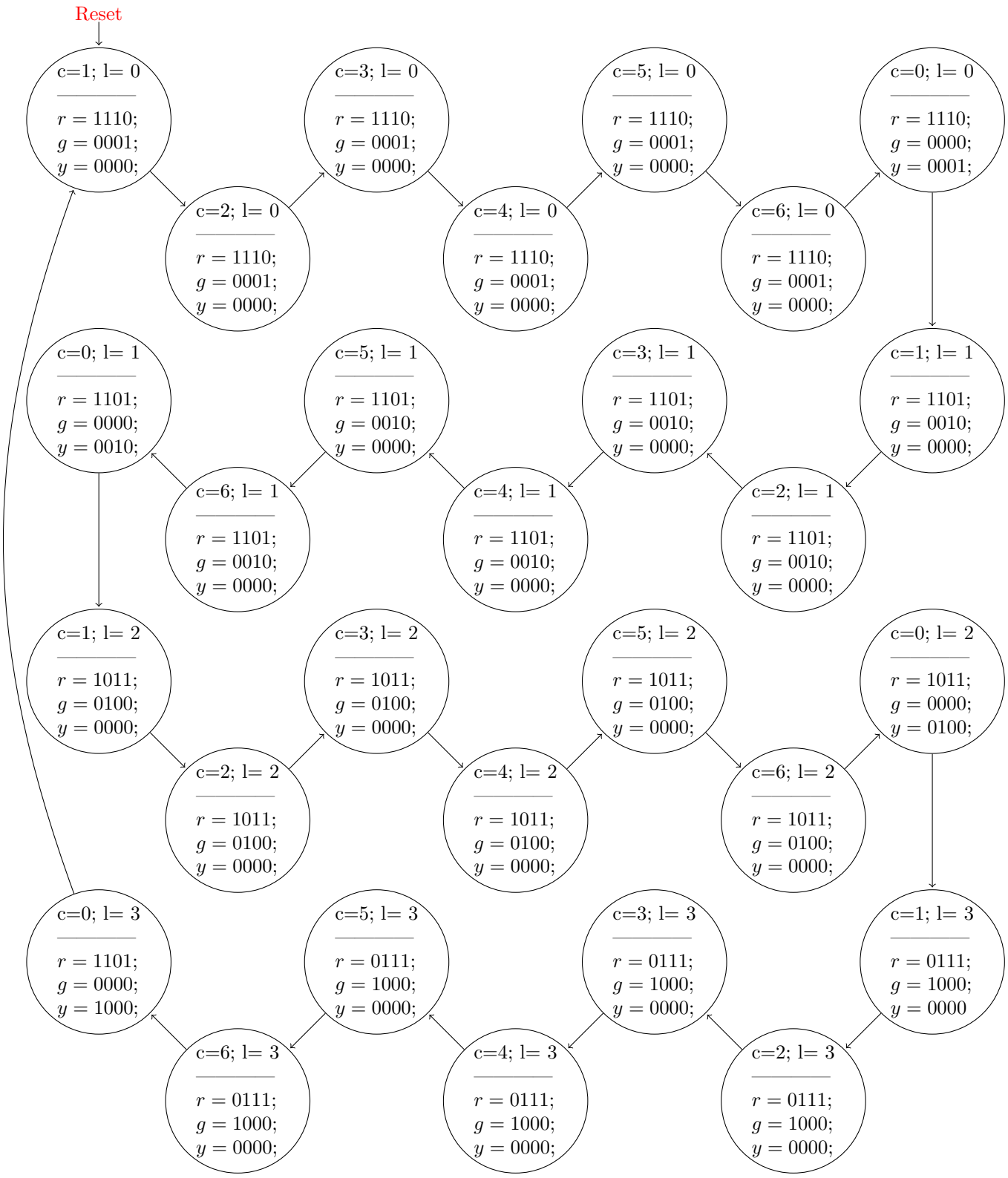

Figure 1: State Diagram for TrafficLightController

In the above state diagram, the variable c represents the (`count` in code) represents the counter for the time intervals/clock cycles completed, whereas the variable l (`lane` in code) represents the lane which is green/yellow (equivalently not red). On each rising clock edge (clock with period 5s), we transition from the current state to the next state. The above state diagram is of a *Moore machine*, therefore output bits for each state is written inside the state itself.

After the reset bit is high, we stay at the state labelled `reset` and wait for it to go low. `reset` goes low just after a rising edge in our testbench, so after reset goes low, we wait for the next rising edge after which we transition to the next state. After this, the states are traversed in a cyclic way i.e after every 35×4s we go back to the initial state.