Arithmetic Circuits

Multiplier

Virendra Singh

Professor

Computer Architecture and Dependable Systems Lab

Department of Electrical Engineering

Indian Institute of Technology Bombay

http://www.ee.iitb.ac.in/~viren/

E-mail: viren@ee.iitb.ac.in

CS-226: Digital Logic Design

Lecture 19-A: 11 March 2021

CADSL

Binary Multiplication (Unsigned)

$1\,0\,0\,0_{two} = 8_{ten}$ — multiplicand

$1\,0\,0\,1_{two} = 9_{ten}$ — multiplier

$n \times n$

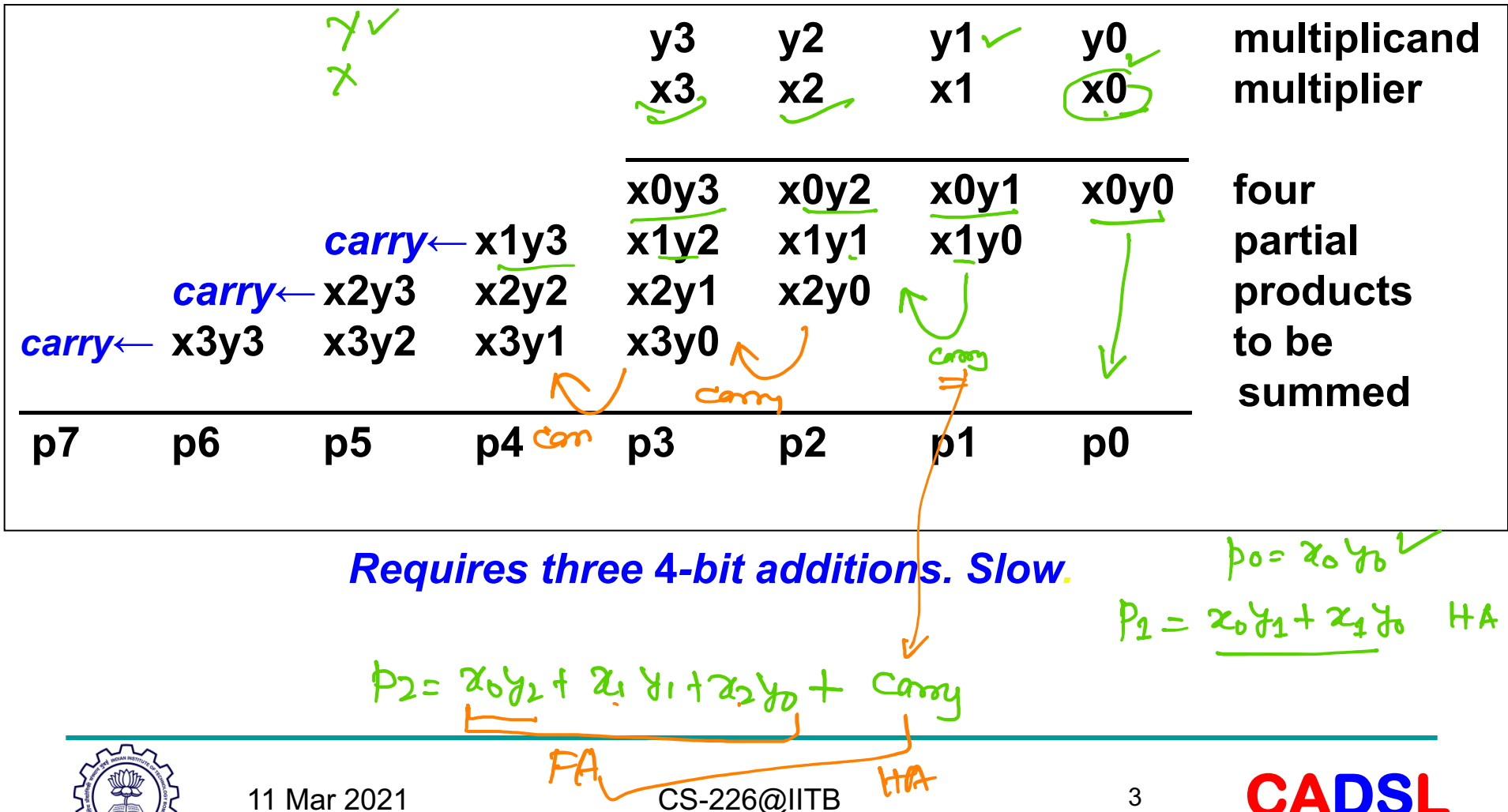
$2n$.

partial products

$$
\begin{array}{r}
1\,0\,0\,0 \\
0\,0\,0\,0 \\
0\,0\,0\,0 \\
1\,0\,0\,0 \\
\hline
1\,0\,0\,1\,0\,0\,0_{two}
\end{array}
\qquad = 72_{ten}
$$

Basic algorithm: For n = 1, 32, only If nth bit of multiplier is 1, then add multiplicand $\times$ 2^{n-1} to product

Adding Partial Products



$$P_3 = x_0y_3 + x_1y_2 + x_2y_1 + x_3y_0 + \text{Carry}$$

FA

FA

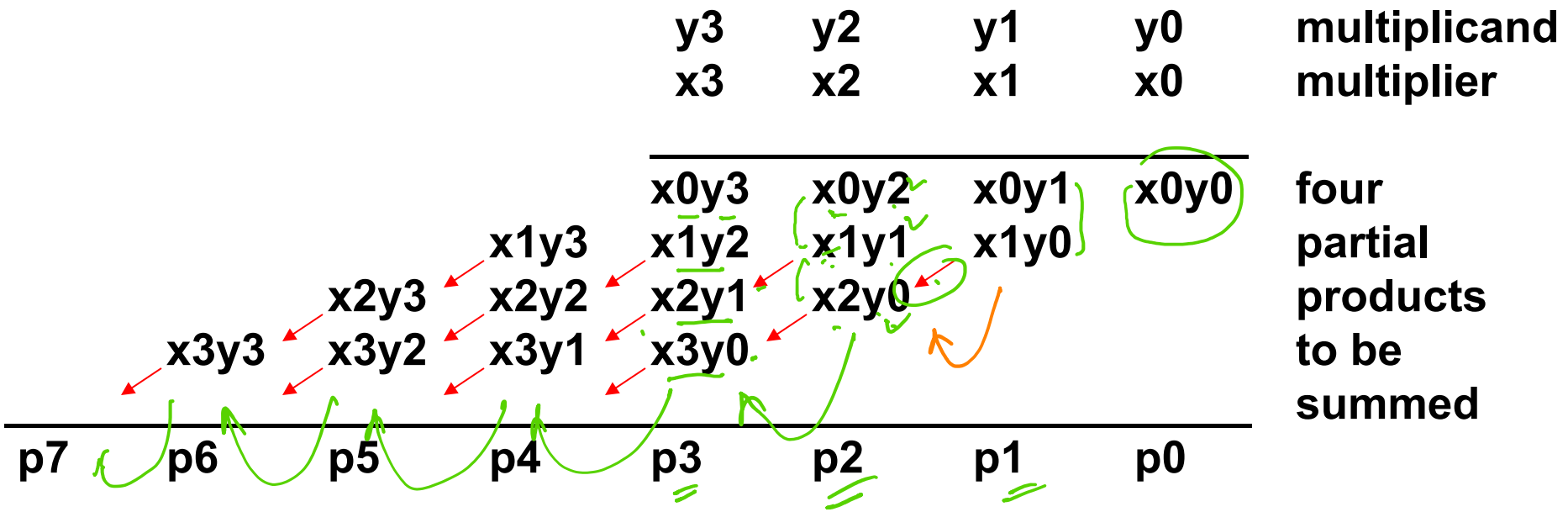
$$P_4 = x_1y_3 + x_2y_2 + x_3y_1 + \text{Carry}$$

FA

HA

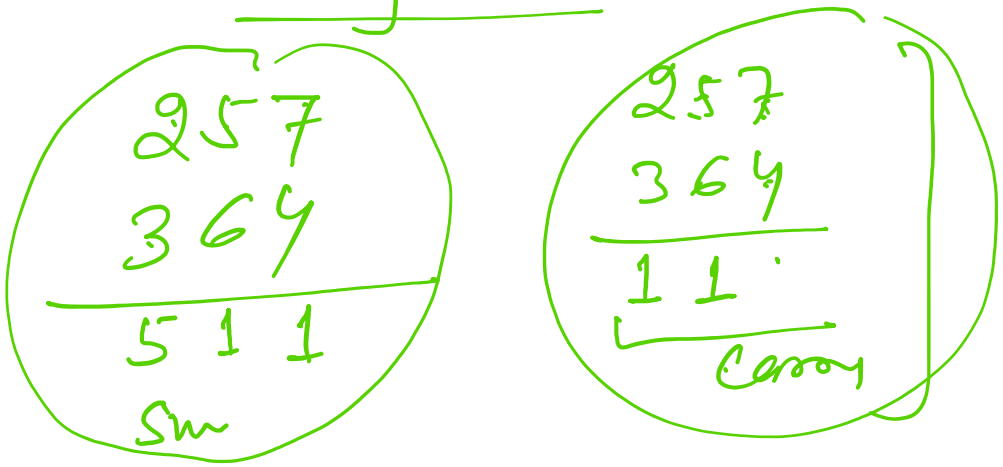
Gates

Array Multiplier: Carry Forward



Note: Carry is added to the next partial product (carry-save addition). Adding the carry from the final stage needs an extra (ripple-carry stage. These additions are faster but we need four stages.

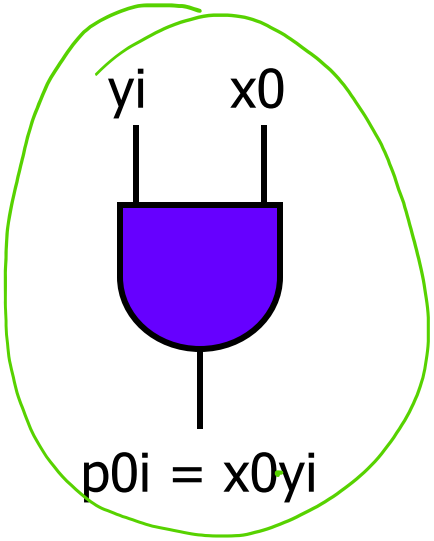
Carry Save Adder



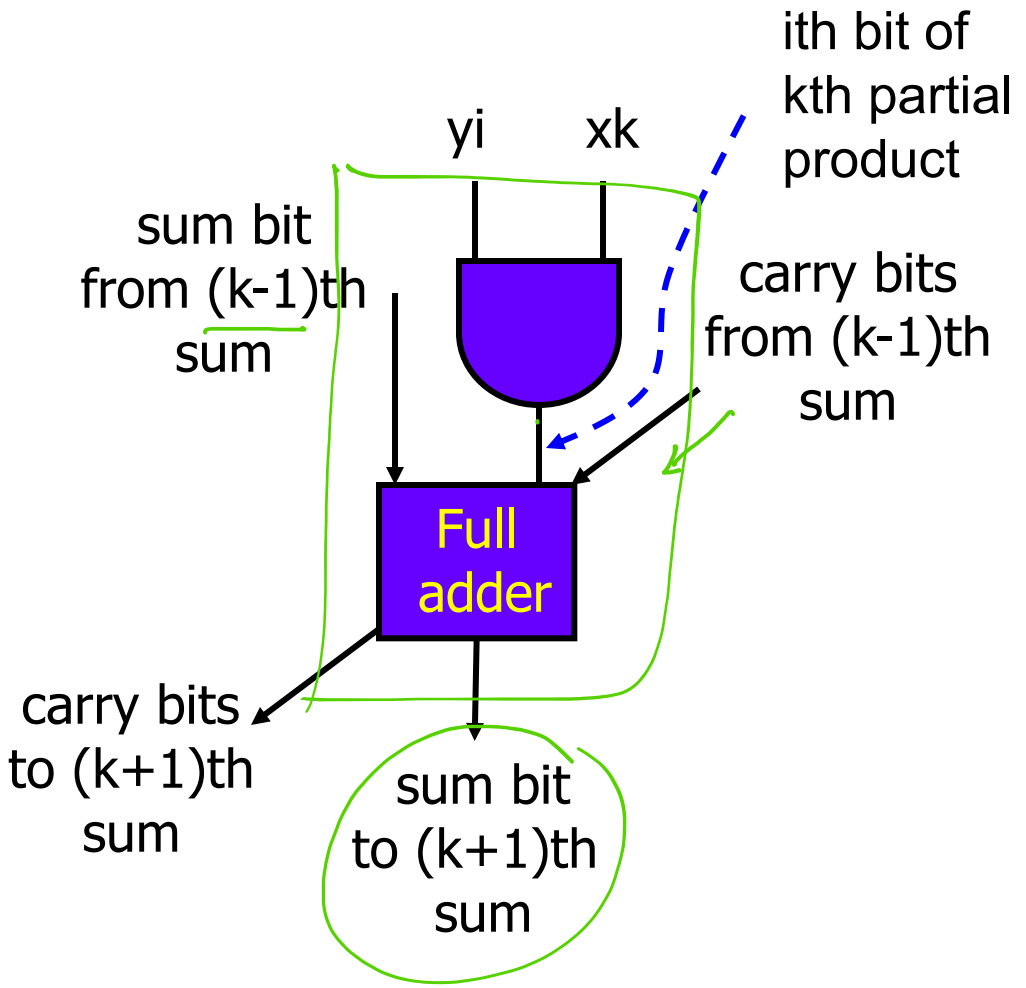
511
110
Addition 621

Basic Building Blocks

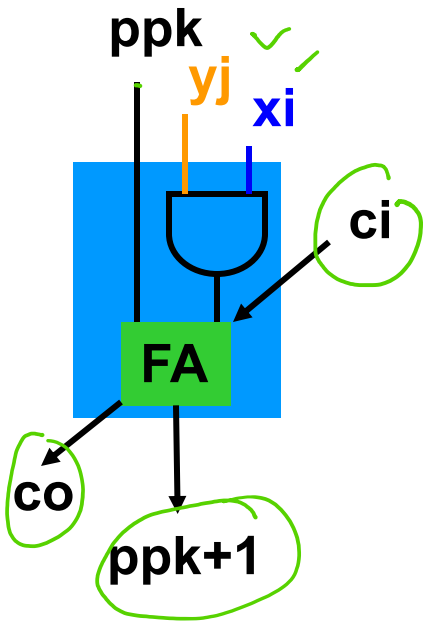
- Two-input AND
- Full-adder



0th partial product



Array Multiplier



Thank You