

CS-226: Digital Design Design

Virendra Singh

Professor

Computer Architecture and Dependable Systems Lab

Department of Electrical Engineering

Indian Institute of Technology Bombay

<http://www.ee.iitb.ac.in/~viren/>

E-mail: viren@ee.iitb.ac.in



Lecture 3: 14 January 2021

CADSL

Digital System



I/O Behaviour: Automobile Ignition

- Engine turns on when
- Ignition key is applied AND
 - Car is in parking gear OR
 - Brake pedal is on
- AND
 - Seat belt is fastened OR
 - Car is in parking gear



Truth Table: Half Adder

X	Y	Binary Sum (C)(S)
0	0	0 0
0	1	0 1
1	0	0 1
1	1	1 0

CARRY

SUM



Truth Table: Full Adder

Z	Y	X	Binary value (C)(S)
0	0	0	0 0
0	0	1	0 1
0	1	0	0 1
0	1	1	1 0
1	0	0	0 1
1	0	1	1 0
1	1	0	1 0
1	1	1	1 1

CARRY SUM



Truth Table: Full Adder

Z	Y	X	Carry C	Sum S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



Truth Tables of logical functions

- Truth tables are used to show/define the relationships between the truth values of
 - the individual propositions and
 - the compound propositions based on them

p	q	$p \cdot q$	$P+q$	$p \oplus q$	$p \Rightarrow q$	$p \Leftrightarrow q$
0	0	0	0	0	1	1
0	1	0	1	1	1	0
1	0	0	1	1	0	0
1	1	1	1	0	1	1



Logic Expressions

Truth Table

X Y Z	F
0 0 0	0
0 0 1	1
0 1 0	0
0 1 1	0
1 0 0	1
1 0 1	1
1 1 0	1
1 1 1	1

Logic Expression

$$F = \bar{X} \cdot \bar{Y} \cdot Z + X \cdot \bar{Y} \cdot \bar{Z} + X \cdot \bar{Y} \cdot Z$$

$$\bar{X} \cdot Y \cdot \bar{Z} + X \cdot Y \cdot Z$$

- Logic expressions, truth tables describe the same function!
- **Truth tables are unique**; expressions are not. This gives flexibility in implementing functions.



How Many Logic Functions?

- Output column of truth table has length 2^n for n input variables.
- It can be arranged in 2^{2^n} ways for n variables.
- Example: $n = 1$, single variable.

Input	Output functions			
	F1(A)	F2(A)	F3(A)	F4(A)
A	0	0	1	1
0	0	0	1	1
1	0	1	0	1



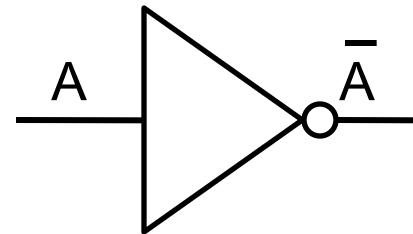
Truth Table: Full Adder

Z	Y	X	Carry C	Sum S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



NOT Gate

Truth Table	
A	\bar{A}
0	1
1	0



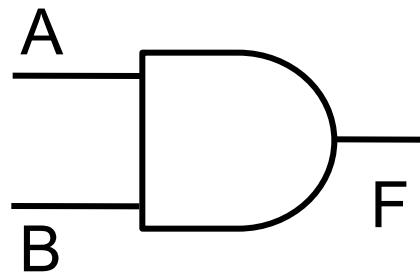
Symbol

Logic Function



AND Gate

Symbol



Logic Function

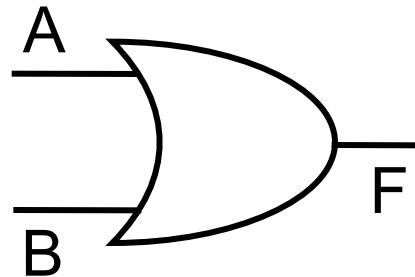
Truth Table

A	B	F
0	0	0
0	1	0
1	0	0
1	1	1



OR Gate

Symbol



Logic Function

Truth Table

A	B	F
0	0	0
0	1	1
1	0	1
1	1	1



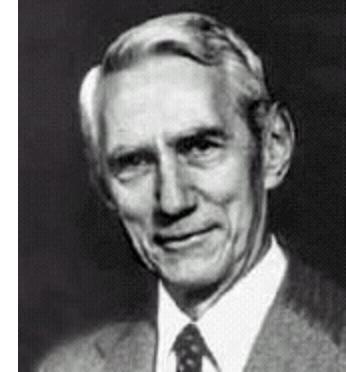
Claude E. Shannon (1916-2001)



http://www.kugelbahn.ch/sesam_e.htm



Shannon's Legacy



- *A Symbolic Analysis of Relay and Switching Circuits*, Master's Thesis, MIT, 1940. Perhaps the most influential master's thesis of the 20th century.
- *An Algebra for Theoretical Genetics*, PhD Thesis, MIT, 1940.
- Founded the field of Information Theory.
- C. E. Shannon and W. Weaver, *The Mathematical Theory of Communication*, University of Illinois Press, 1949. A “must read.”



Logic Function Implementation

- Using Switches

- For inputs:

- logic 1 is switch closed
 - logic 0 is switch open

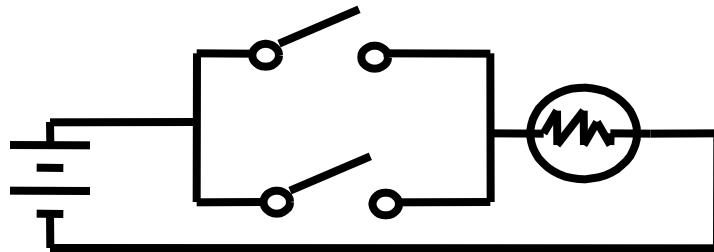
- For outputs:

- logic 1 is light on
 - logic 0 is light off.

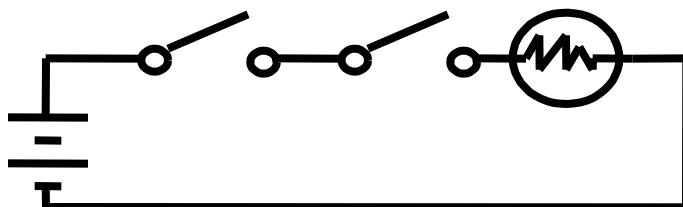
- NOT uses a switch such that:

- logic 1 is switch open
 - logic 0 is switch closed

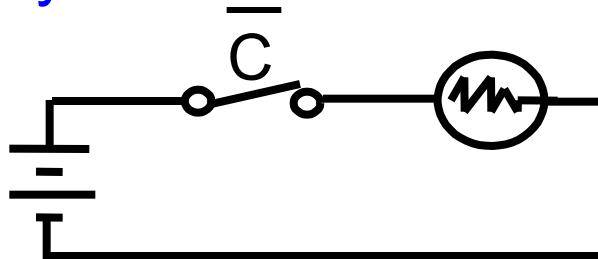
Switches in parallel => OR



Switches in series => AND



Normally-closed switch => NOT



Switching Devices

- Electromechanical relays (1940s)
- Vacuum tubes (1950s)
- Bipolar transistors (1960 - 1980)
- Field effect transistors (1980 -)
- Integrated circuits (1970 -)



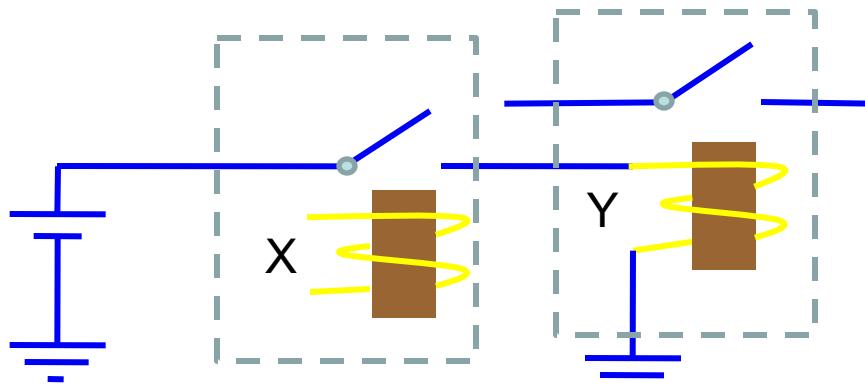
Implementing with Relays

- An electromechanical relay contains:
 - Electromagnet
 - Current source
 - A switch, spring-loaded, normally open or closed
- Switch has two states, open (0) or closed (1).
- The state of switch is controlled by “not applying” or “applying” current to electromagnet.



One Switch Controlling Other

- Switches X and Y are normally open.
- Y cannot close unless a current is applied to X.

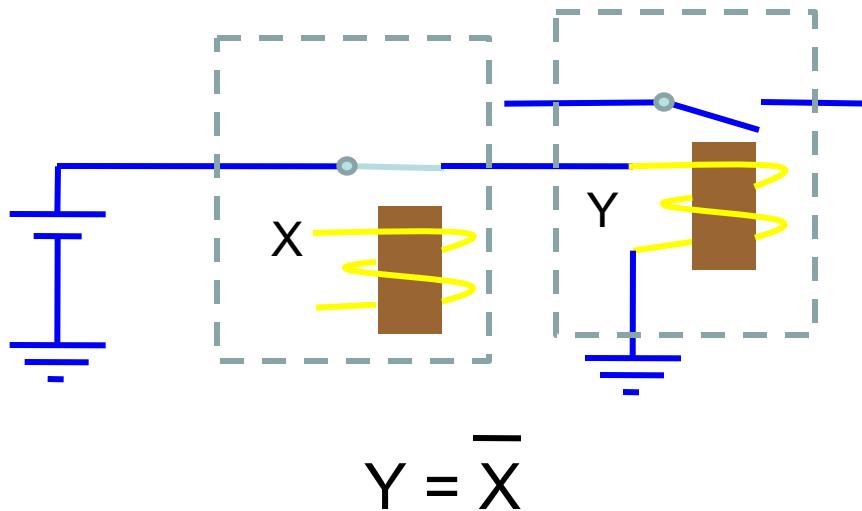


$$Y = X$$



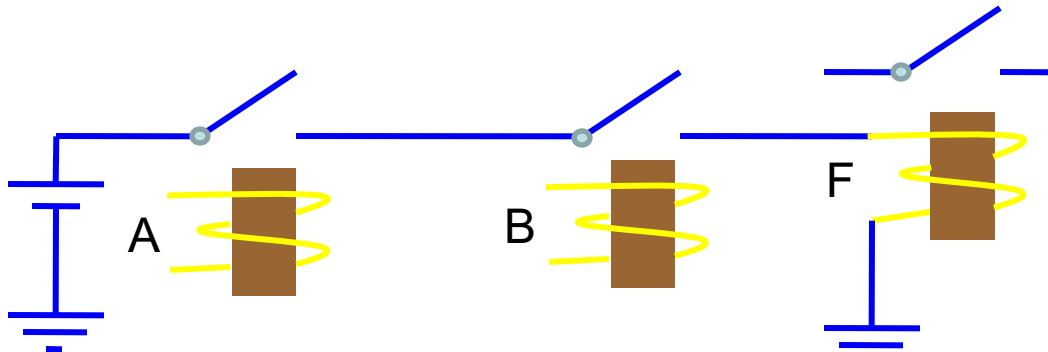
Inverting Switch

- Switch X is normally closed and Y is normally open.
- Y cannot open unless a current is applied to X.

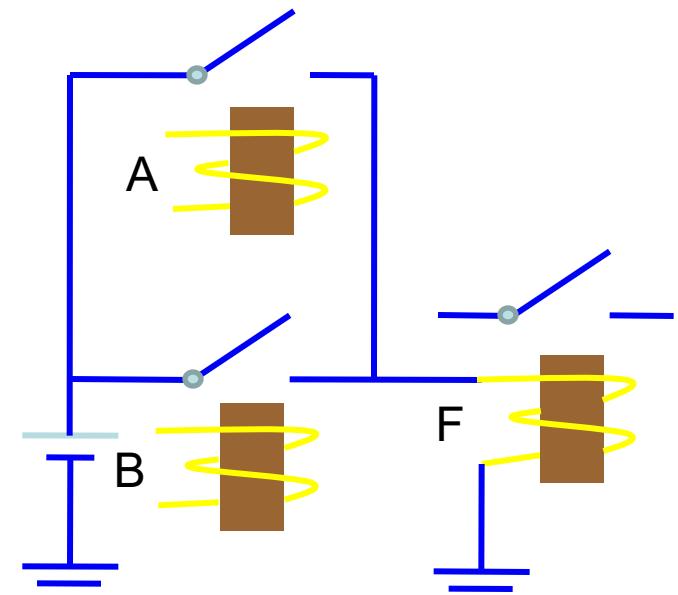


Logic Operations

- AND – Series connected relays.
- OR – Parallel relays.



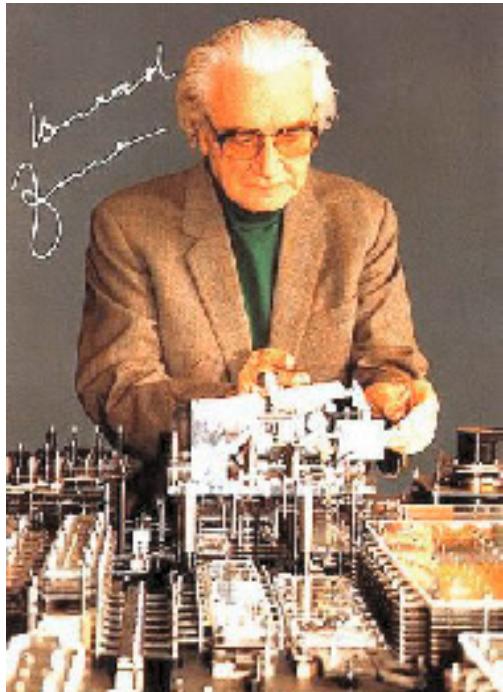
$$F = A B$$



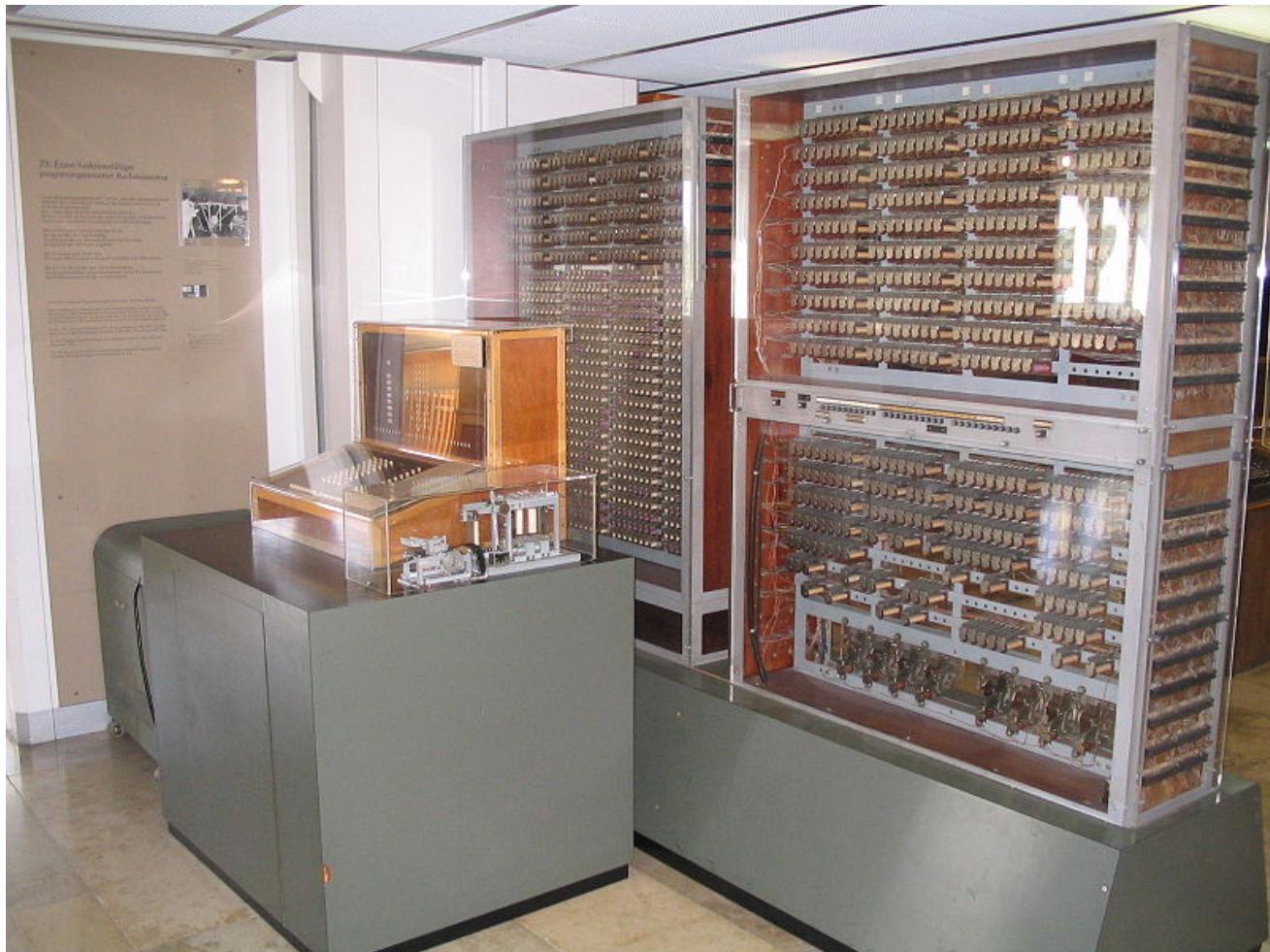
$$F = A + B$$

Relay Computers

Conrad Zuse (1910-1995)

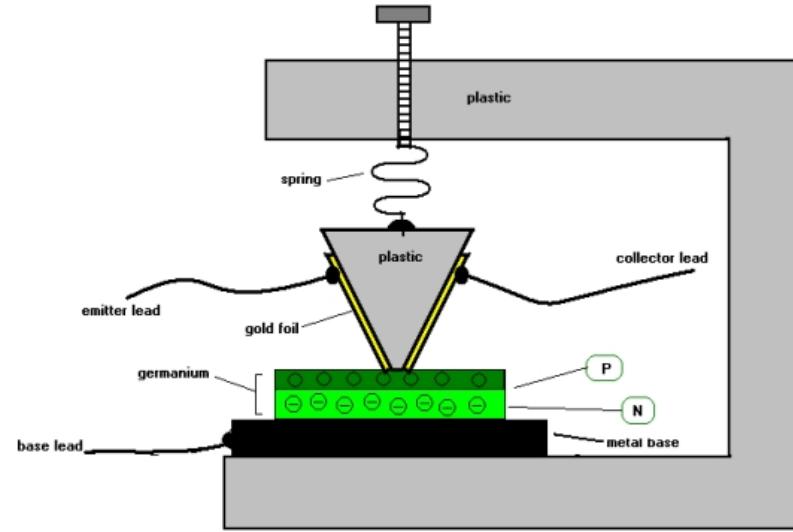
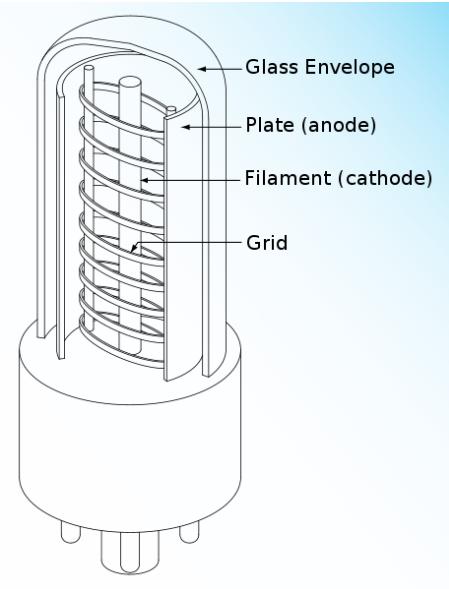


Z1 (1938)



Z3 (1941)

Electronic Switching Devices

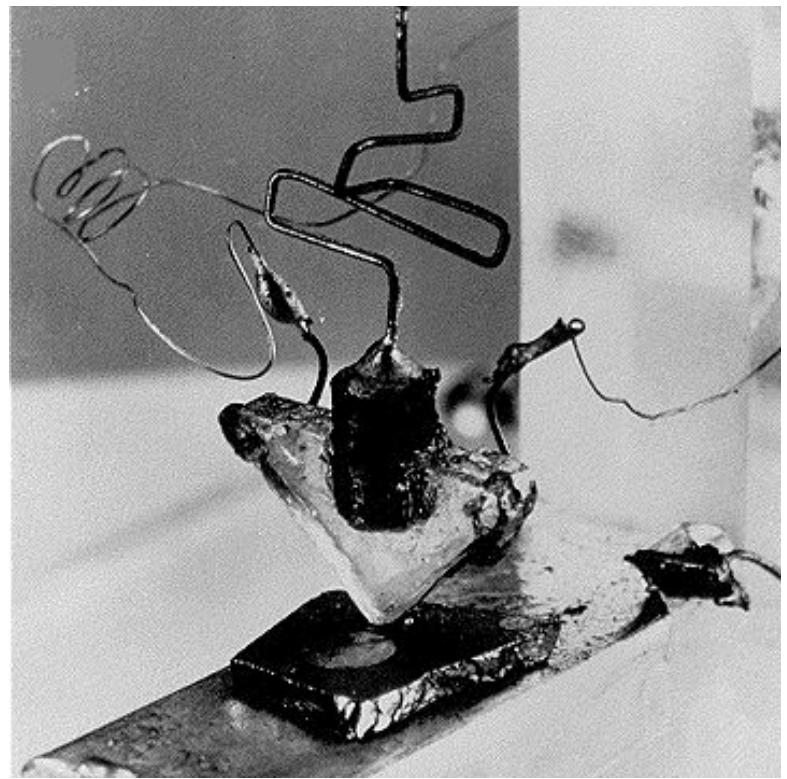
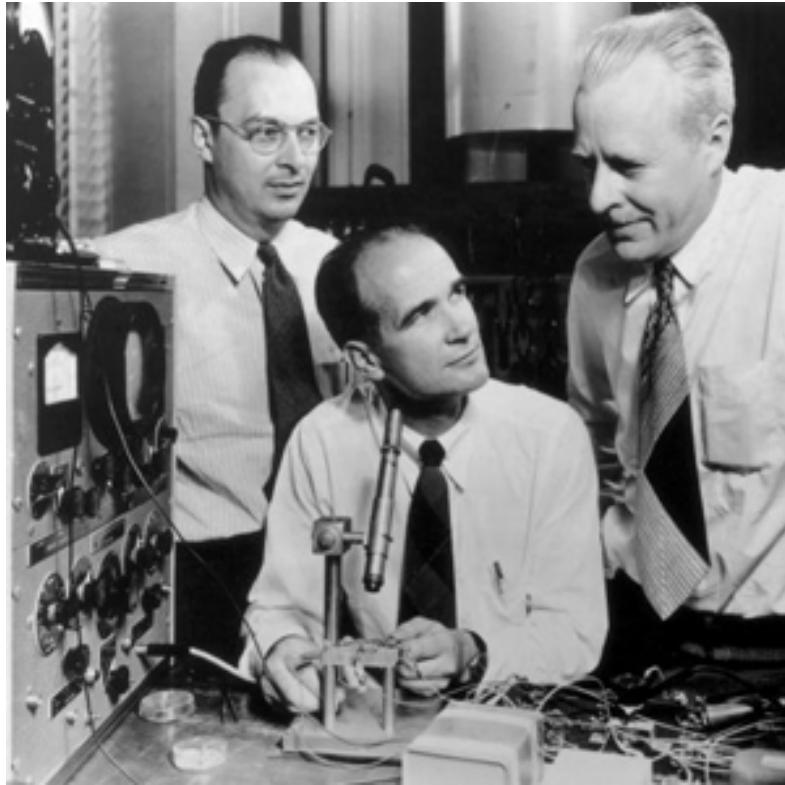


Electron Tube
Fleming, 1904
de Forest, 1906

Point Contact Transistor
Bardeen, Brattain, Shockley, 1948

Transistor, 1948

The thinker, the tinkerer, the visionary and the transistor
John Bardeen, Walter Brattain, William Shockley
Nobel Prize, 1956



Bell Laboratories, Murray Hill, New Jersey



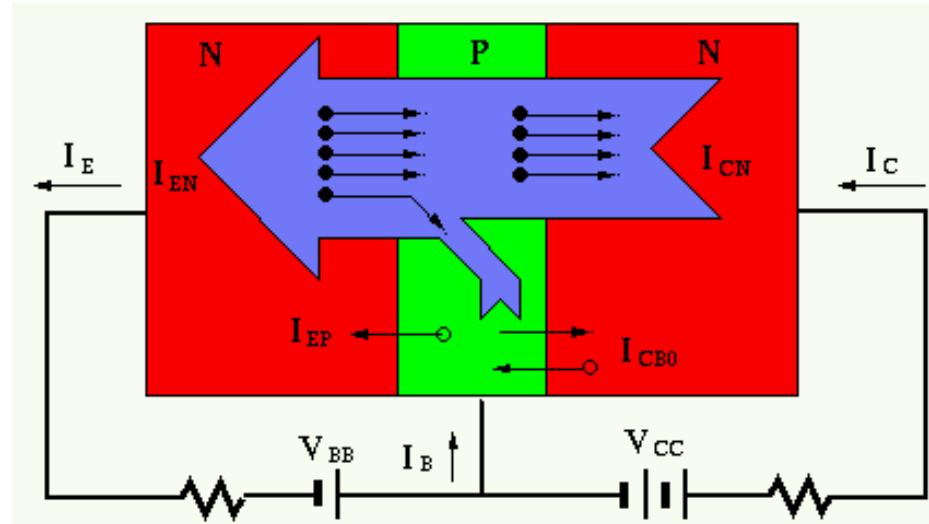
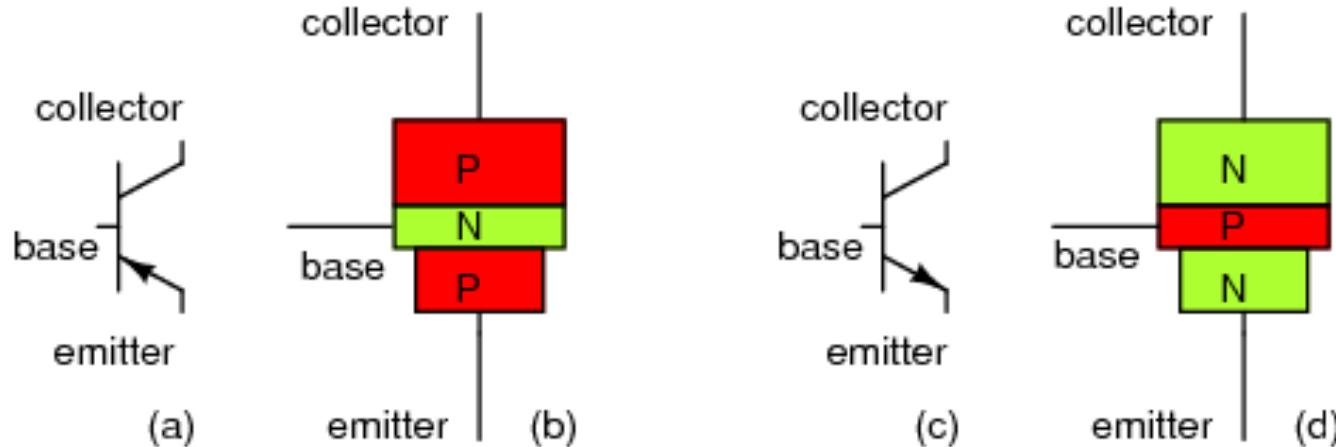
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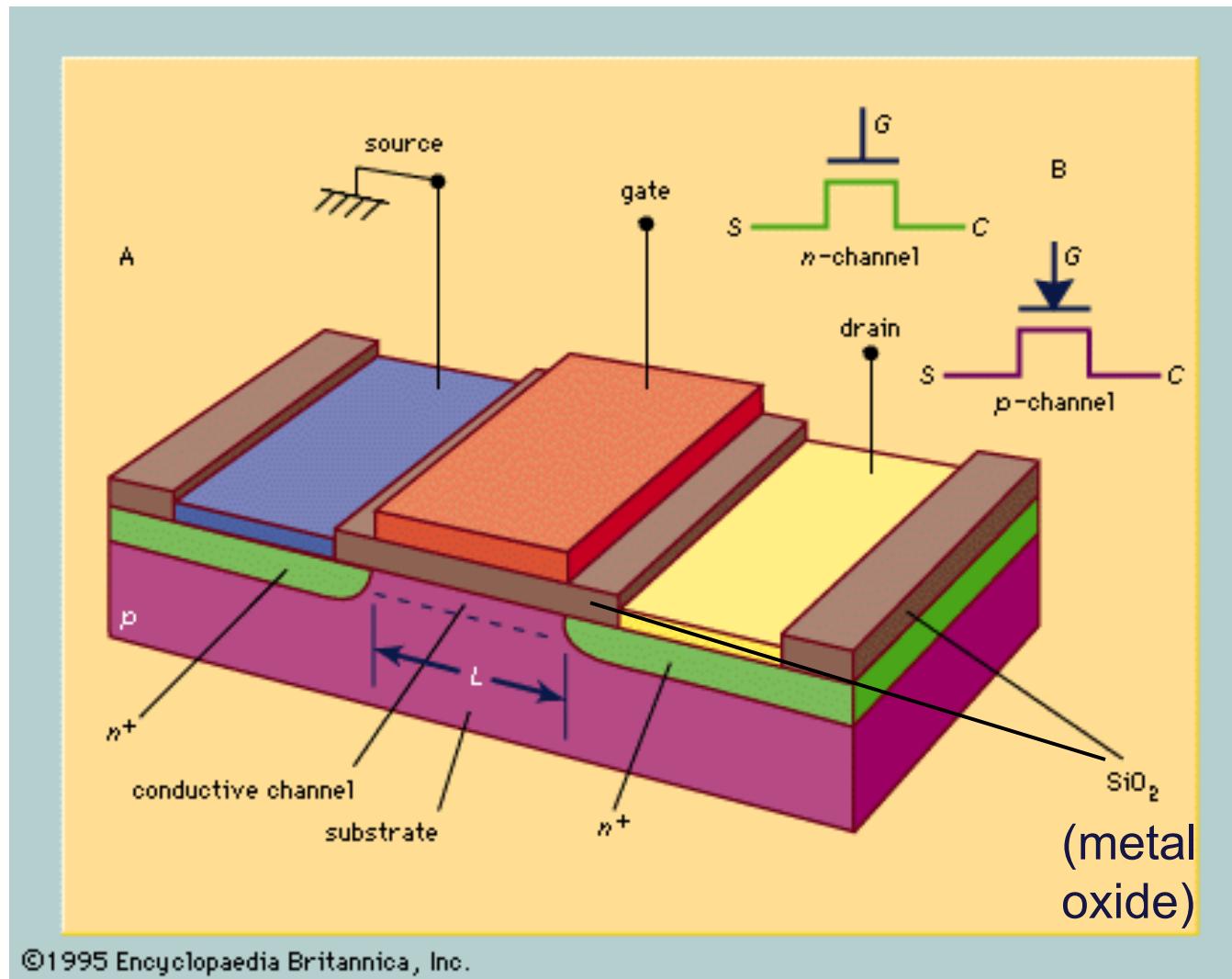
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Bipolar Junction Transistor (BJT)



Field Effect Transistor (FET)

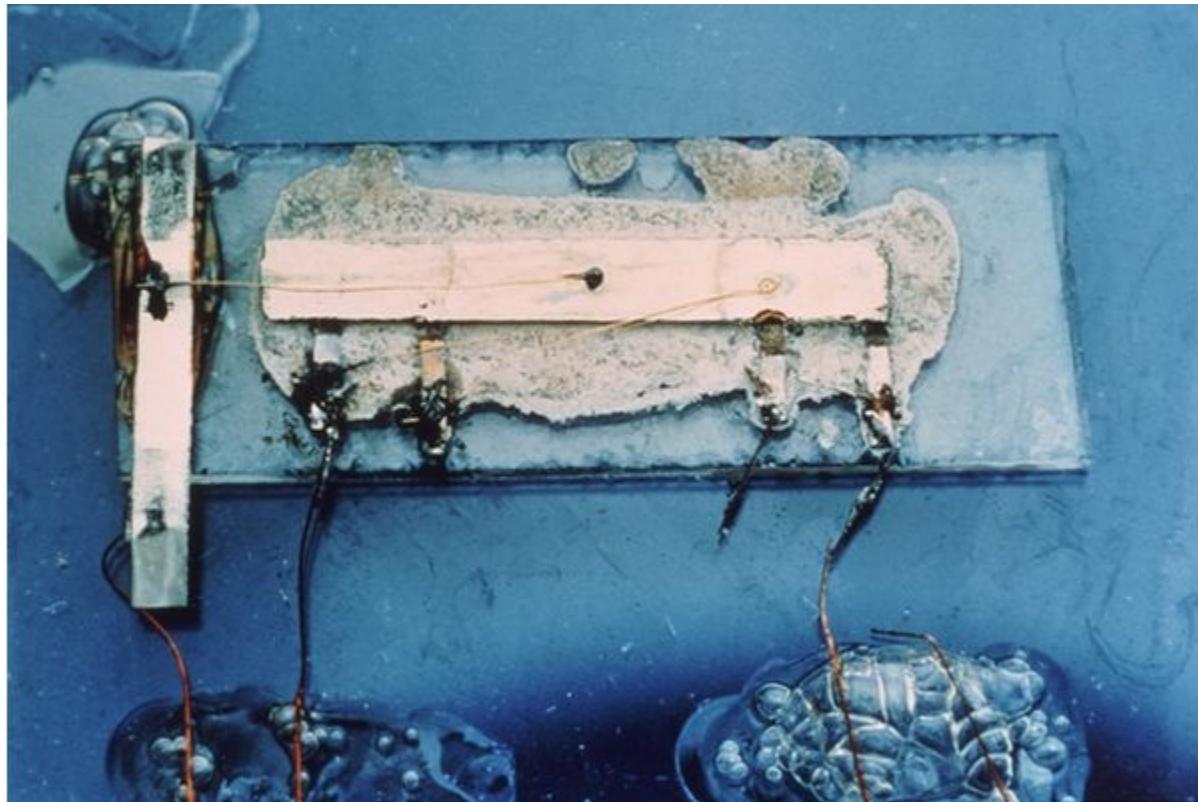
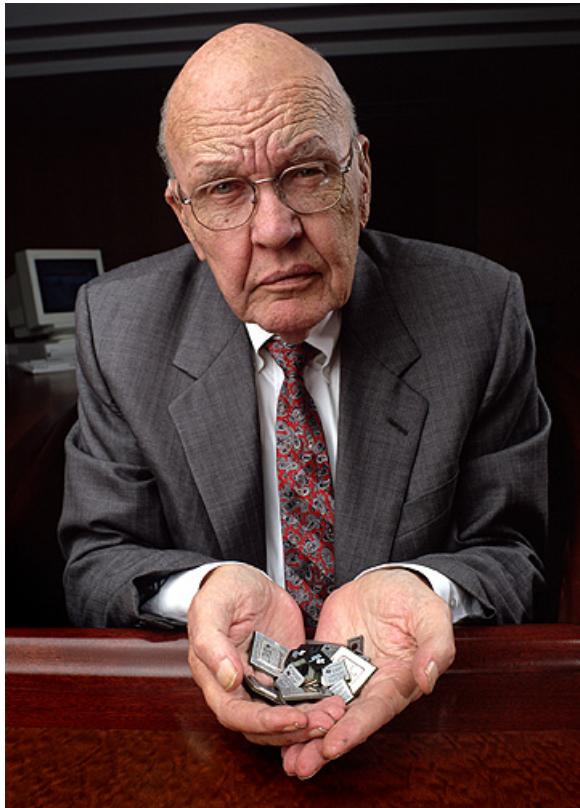
a.k.a.
metal oxide
semiconductor
(MOS) FET.



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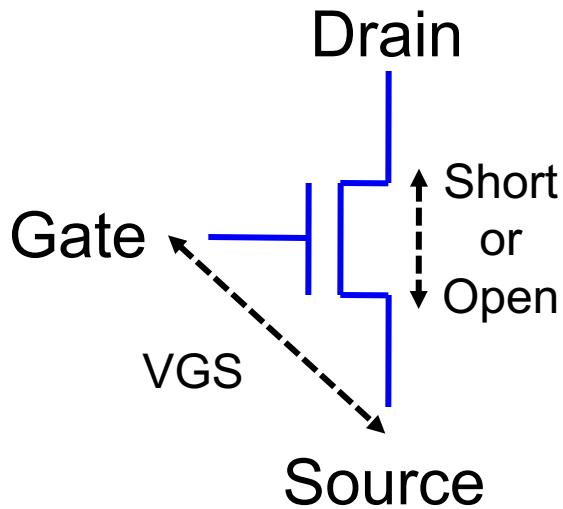
Integrated Circuit (1958)



Jack Kilby (1923-2005), Nobel Prize, 2000

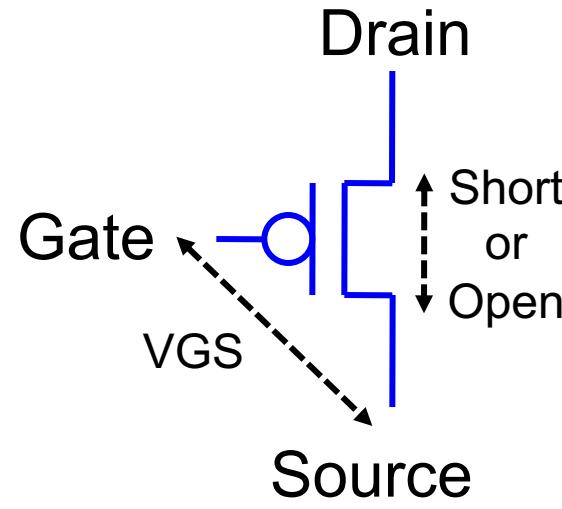


MOSFET (Metal Oxide Semiconductor Field Effect Transistor)



NMOSFET

$V_{GS} = 0$, open
 $V_{GS} = \text{high}$, short



PMOSFET

$V_{GS} = 0$, short
 $V_{GS} = \text{high}$, open

Reference:

R. C. Jaeger and T. N. Blalock, *Microelectronic Circuit Design*,
Third Edition, McGraw Hill.



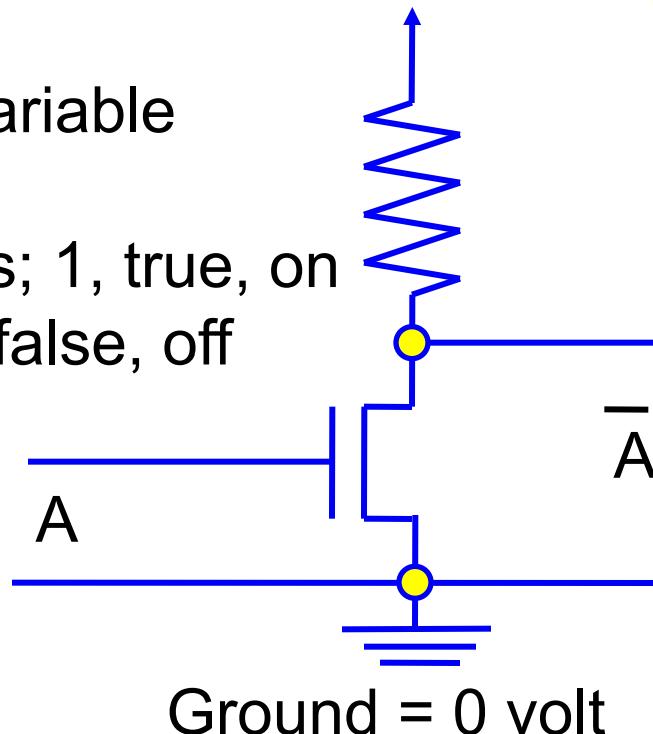
NMOSFET NOT Gate (Early Design)

Power supply
VDD volts
w.r.t. ground

A: Boolean variable

$A = VDD$ volts; 1, true, on

$A = 0$ volt; 0, false, off



Problem: When $A = 1$, current leakage causes power dissipation.

Solution: Complementary MOS design proposed by

F. M. Wanlass and C.-T. Sah,
“Nanowatt Logic Using Field-
Effect Metal-Oxide
Semiconductor Triodes,”
*International Solid State Circuits
Conference Digest of Technical
Papers*, Feb 20, 1963, pp. 32-33.

CMOS Circuit

Dec. 5, 1967

F. M. WANLASS

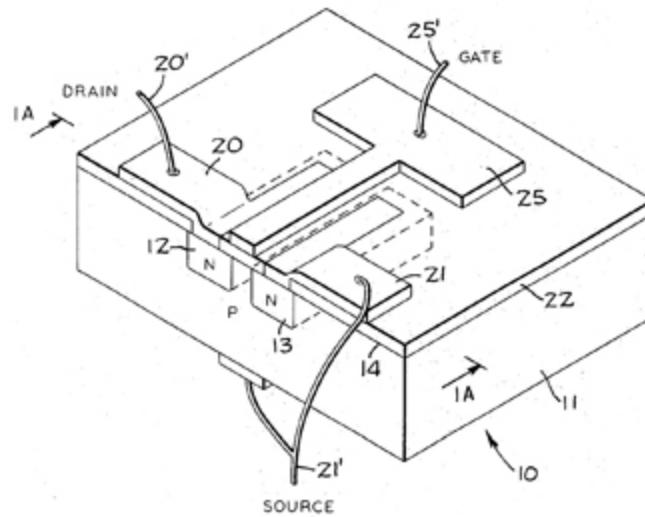
3,356,858

LOW STAND-BY POWER COMPLEMENTARY FIELD EFFECT CIRCUITRY

Filed June 18, 1963

5 Sheets-Sheet 1

FIG. I



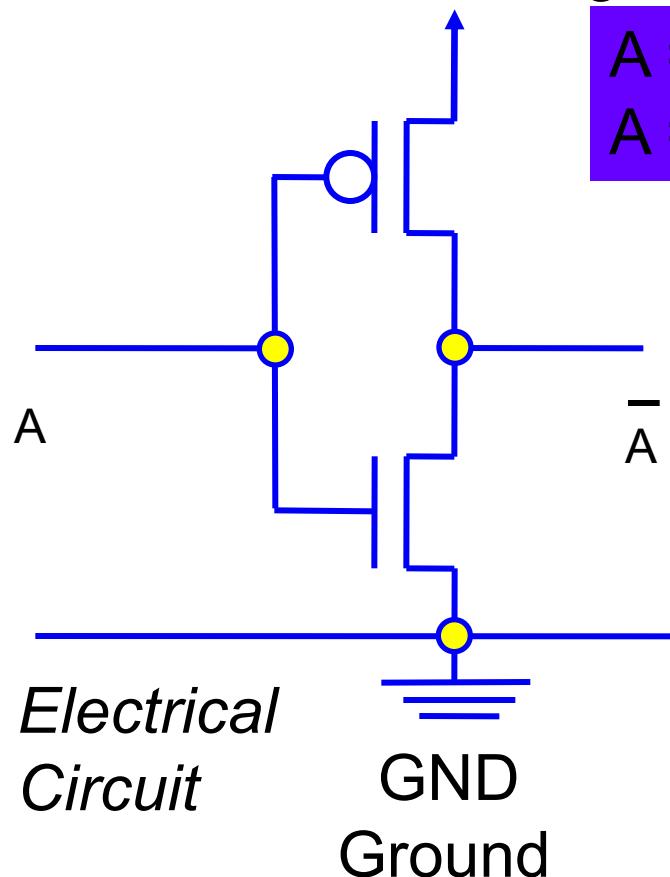
Wanlass, F. M. "Low Stand-By Power Complementary Field Effect Circuitry." U. S. Patent 3,356,858 (Filed June 18, 1963. Issued December 5, 1967).



CMOS NOT Gate (Modern Design)

Power supply

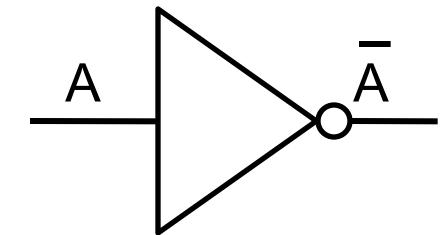
VDD = 1 volt; voltage depends on technology.



A = VDD = 1 volt is state “1”
A = GND = 0 volt is state “0”

Truth Table	
A	\bar{A}
0	1
1	0

Boolean Function



Symbol

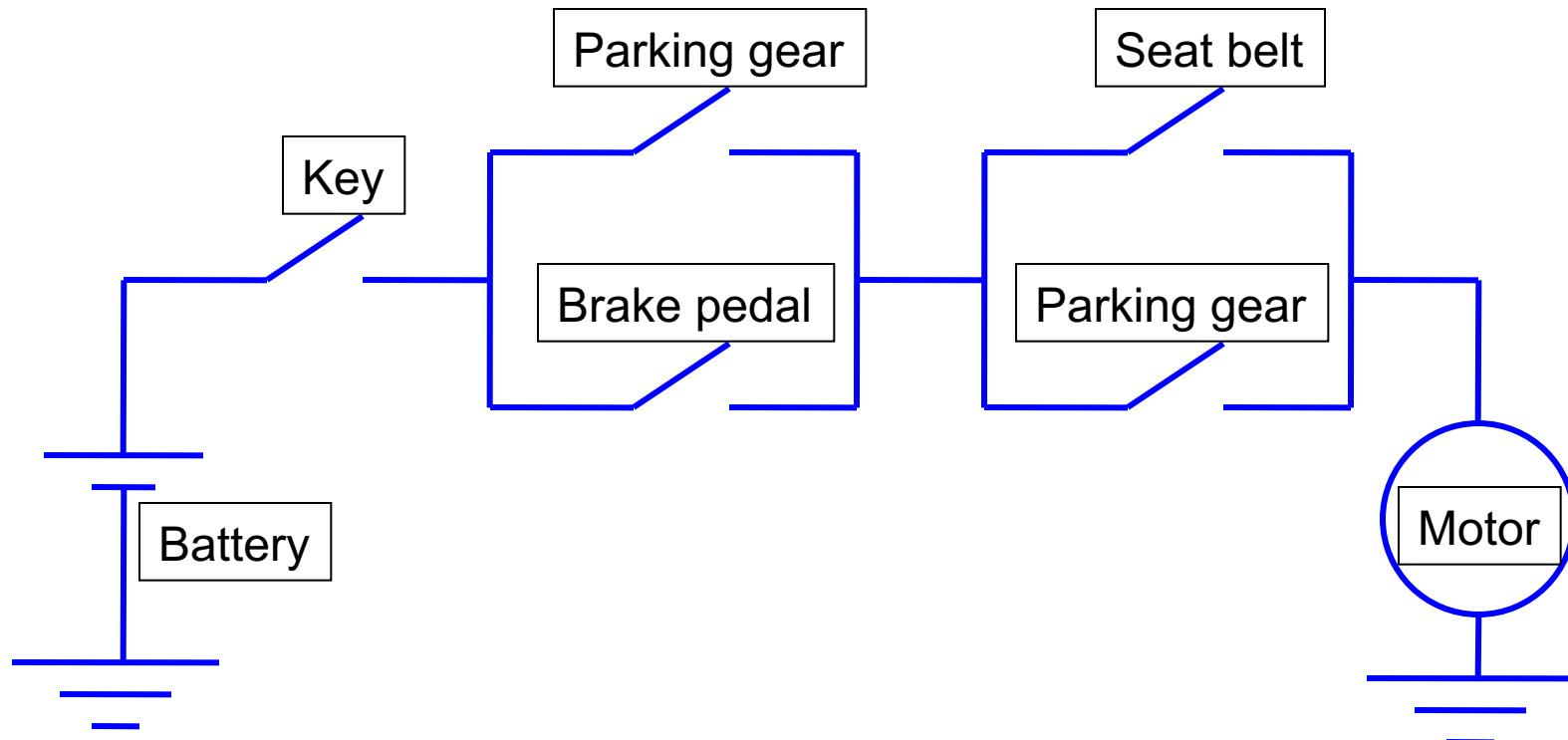


Example: Automobile Ignition

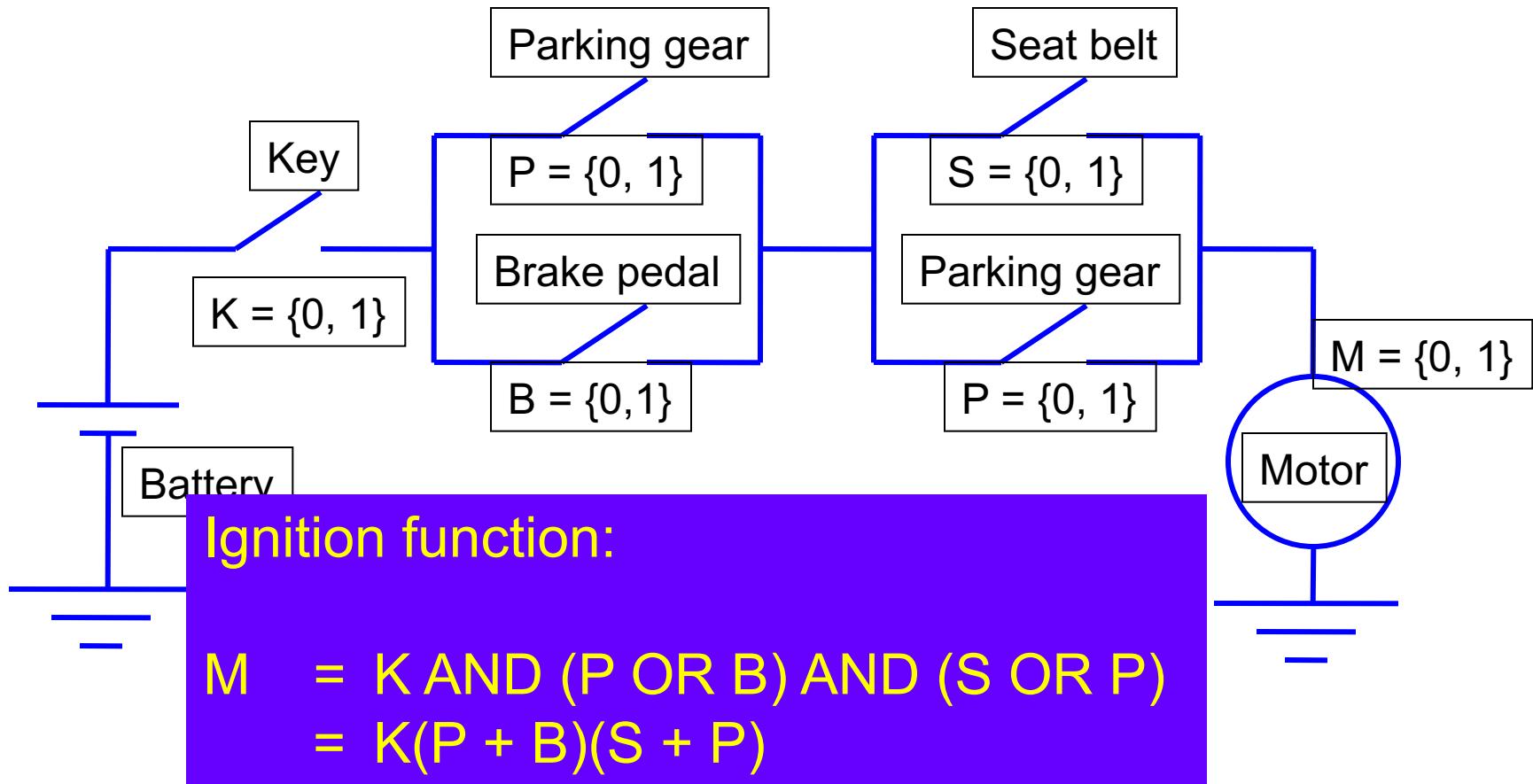
- Engine turns on when
- Ignition key is applied AND
 - Car is in parking gear OR
 - Brake pedal is on
- AND
 - Seat belt is fastened OR
 - Car is in parking gear



Switching logic

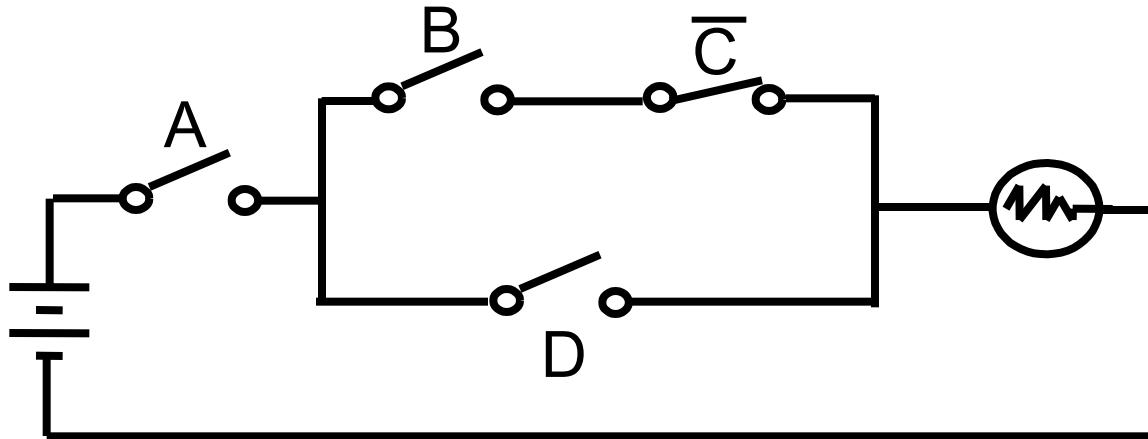


Define Variables



Logic Function Implementation

- Example: Logic Using Switches



- Light is on ($L = 1$) for
$$L(A, B, C, D) = A ((B C') + D) = A B C' + A D$$
and off ($L = 0$), otherwise.
- Useful model for relay circuits and for CMOS gate circuits, the foundation of current digital logic technology

Logic Expression

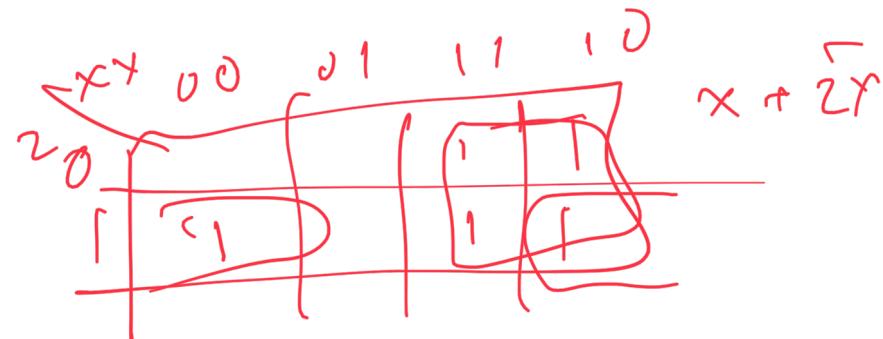
Truth Table

X Y Z	F
0 0 0	0
0 0 1	1
0 1 0	0
0 1 1	0
1 0 0	1
1 0 1	1
1 1 0	1
1 1 1	1

Logic Expression

$$F = \overline{X} \cdot \overline{Y} \cdot Z + X \cdot \overline{Y} \cdot \overline{Z} + X \cdot \overline{Y} \cdot Z$$

$$X \cdot Y \cdot \overline{Z} + X \cdot Y \cdot Z$$



Logic Expressions

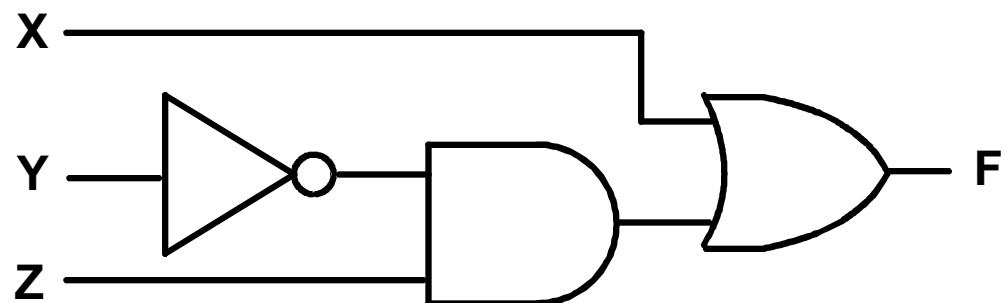
Truth Table

X Y Z	F
0 0 0	0
0 0 1	1
0 1 0	0
0 1 1	0
1 0 0	1
1 0 1	1
1 1 0	1
1 1 1	1

Equation

$$F = X + \bar{Y} Z$$

Logic Diagram



Digital Logic Design

- Express input output relationship using Truth table
- Generate the logical expression by disjunction (OR) terms (conjunction of variables – AND) where system evaluates to true
- Replace all operators by the logic gates
- Replace logic gates by its transistor level circuit



Thank You

