CS 254 - Assignment 5

Rules: ***1) For all questions, only structural VHDL code is permitted.***

2) Only 2 input basic gates are permitted.

3)All the basic gates in this assignment can only be designed using 2x1 muxes.

4)All the entity statements given in the question must be used as it is.

5)Use the ieee.std_logic_1164 library data types. (Bit and bit vector are not permitted.)

1) Design an 8-bit Kogge-Stone unsigned adder-subtractor. This must be designed in a structural way using only 2 input basic gates. The basic gates themselves must be designed using only 2x1 muxes. If 'cin' is given '0' then the circuit should add 'a' and 'b' (a+b). If 'cin' is '1' then the circuit should subtract 'b' from 'a' (a-b).

```
entity EightbitKogStonAddSub is
        port ( a, b : in std_logic_vector (7 downto 0);
        cin: in std_logic;
        sum: out std_logic_vector (7 downto 0);
        cout: out std_logic);
end entity;
```

Bonus: Signed 8-bit Kogge-Stone adder-subtractor. Use the same entity as above.

Things required in Submission:

1. All VHDL files of top-level and sub-components. (.vhd or .vhdl files)
2. Screenshot of Waveform..

Submission rules:

1. The VHDL files of each question should be kept in a **separate folder**.
2. All the VHDL files of one question (both Top-level & sub-components) should be kept in the **same folder**. (It has been observed that some have the habit of putting the sub-components in a separate folder. Please avoid this to speed up our evaluation process.)
3. The final zip file that is submitted on moodle should be named in the following format: **group_<groupnumber>.zip**. For example, the zip file for group 8 should be named group_8.zip