CS 254 - Assignment 6

Rules:

1) D- flipflop vhdl code will be provided.

2) Rest of the code has to be strictly structural.

3) All the entity statements given in the question must be used as it is.

4) Use the ieee.std_logic_1164 library data types. (Bit and bit vector are not permitted.)

1) Design a 2-bit synchronous counter which generates the following periodic sequence: 0 -> 1 -> 2-> 3-> 2-> 1-> 0 ->1 ->2 -> ….. The sequence should start from zero whenever 'rst' is made high.

```
entity TwobitUpCount is
        port ( clk, rst : in std_logic;
        count: out std_logic_vector (1 downto 0));
end entity;
```

2) Design a 3-bit synchronous up/down counter. Whenever 'up' is given '1' the counter should count up. Whenever 'up' is given '0' the counter should count down.

```
entity ThreebitUpDownCount is
        port ( clk, rst, up : in std_logic;
        count : out std_logic_vector (2 downto 0));
end entity;
```

Things required in Submission:

1. All VHDL files of top-level and sub-components. (.vhd or .vhdl files)
2. Screenshot of Waveform.
3. All paperwork: FSM diagrams, state minimizations if any, K-maps if any.

Submission rules:

1. The VHDL files of each question should be kept in a **separate folder**.
2. All the VHDL files of one question (both Top-level & sub-components) should be kept in the **same folder**.
3. The final zip file that is submitted on moodle should be named in the following format: **group_<groupnumber>.zip**. For example, the zip file for group 8 should be named group_8.zip