

Sequential Circuits

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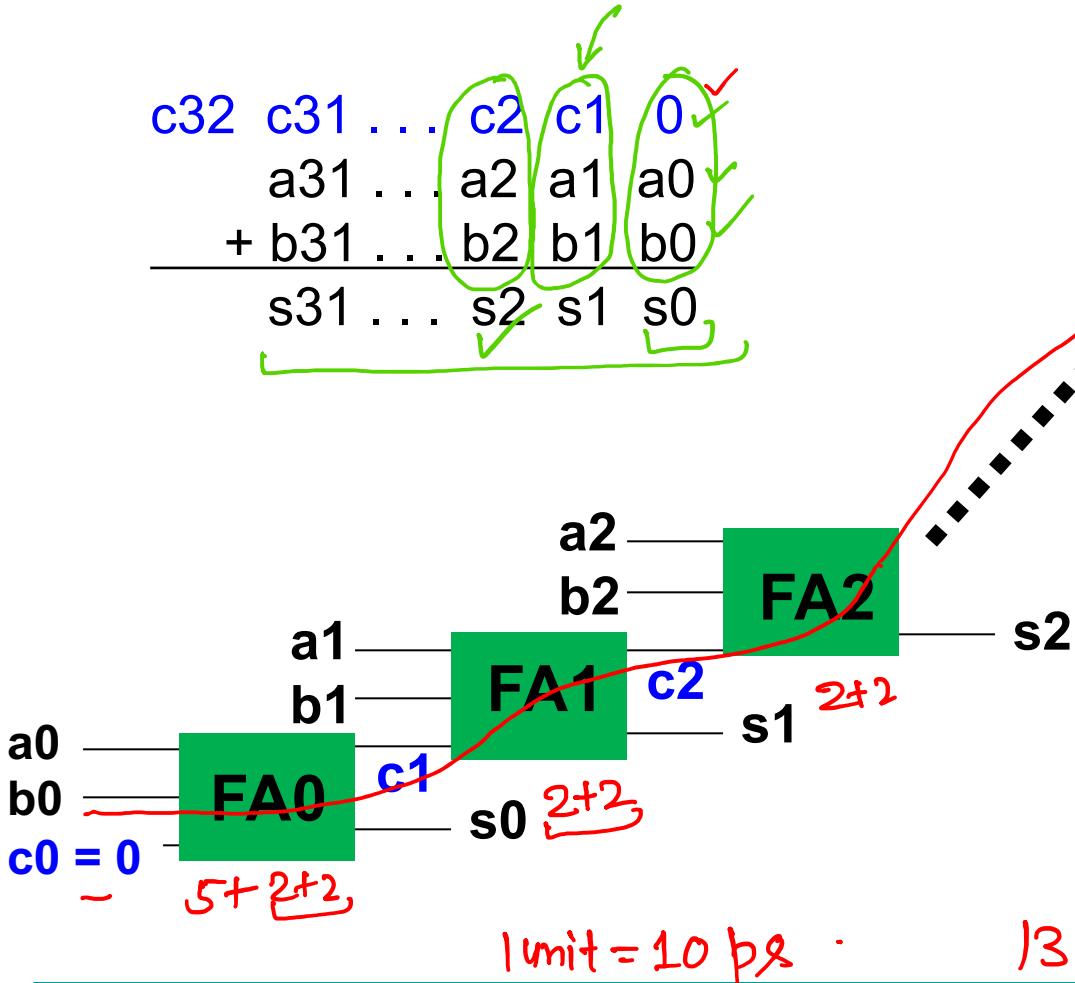
CS-226: Digital Logic Design



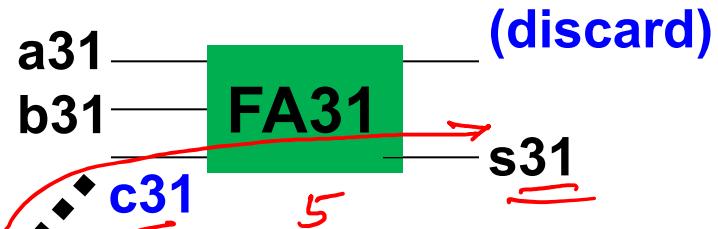
Lecture 20: 15 March 2021

CADSL

32-bit Ripple-Carry Adder



$\text{Area} = \text{Cost} \doteq \text{Cost of } 32 \text{ FA}$
1 FA $\doteq 2 \times \text{OR} + 2 \times \text{AND} + 10R$



delay \propto # Inputs (FA)

$$5 + 5 + (2^{+2})(n-1)$$

delay $\propto n$.

$$\begin{aligned} 4 \times 31 + 10 &= \\ 124 + 10 &= 134 \text{ units} \\ 134 \times 10 &= 1340 \text{ ns} \end{aligned}$$



Full-Adder Circuit

5

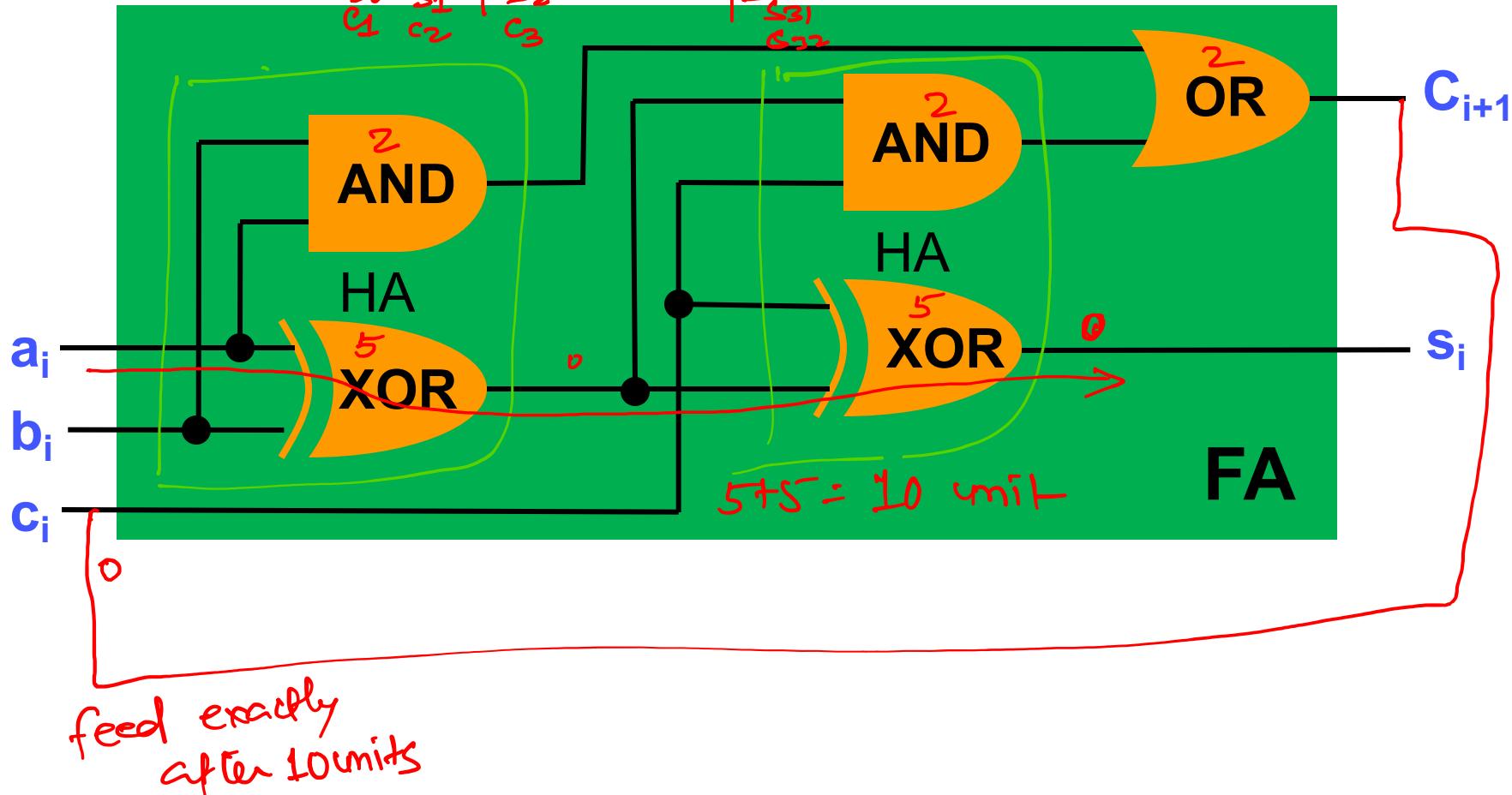
$$1 \text{ unit} = 10 \text{ ps}$$

$$\frac{32 \times 10}{3.2 \text{ ns}} = \underline{\underline{320 \text{ units}}}$$

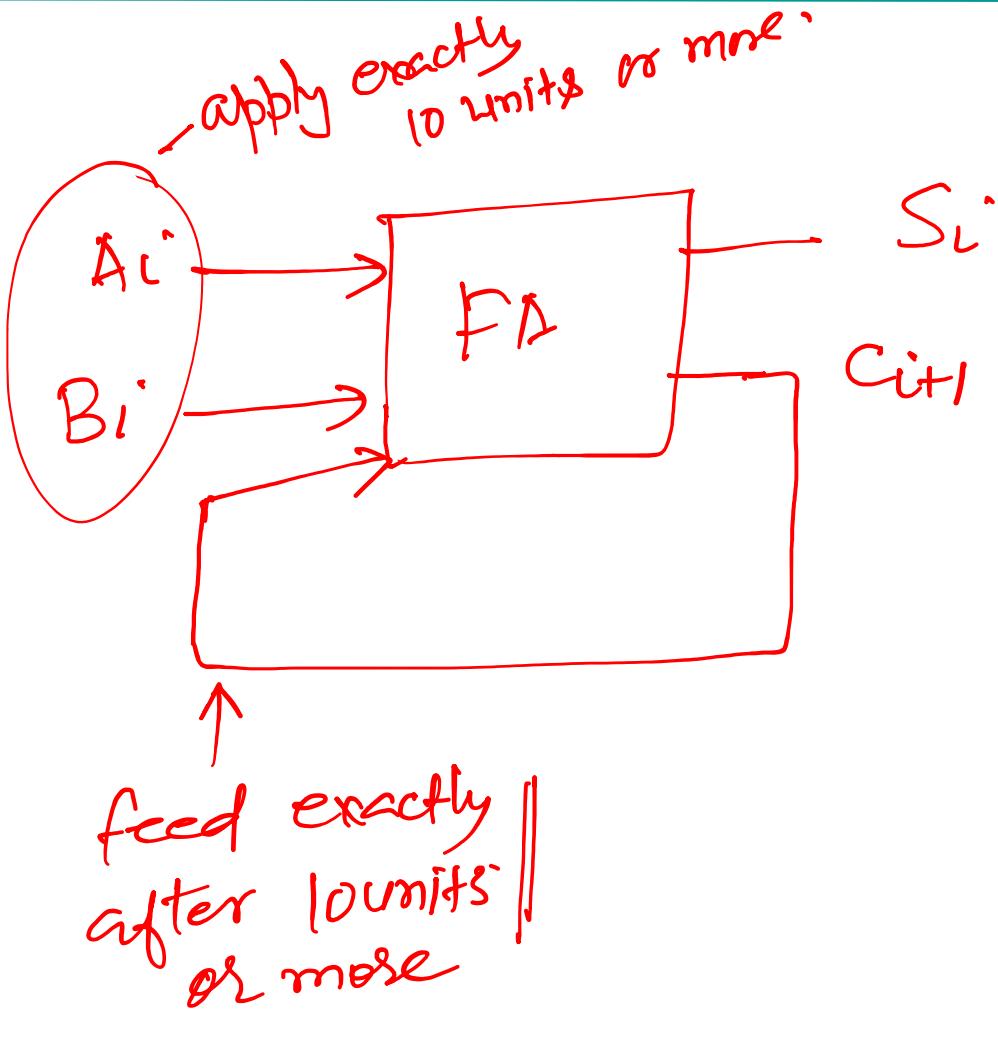
a_0	a_1	a_2	a_{31}
b_0	b_1	b_2	b_{31}
0	0	0	0
s_0	s_1	s_2	s_{31}
c_1	c_2	c_3	c_{32}

FA

a_{31}
b_{31}
c_{31}
s_{31}
c_{32}



Serial Adder



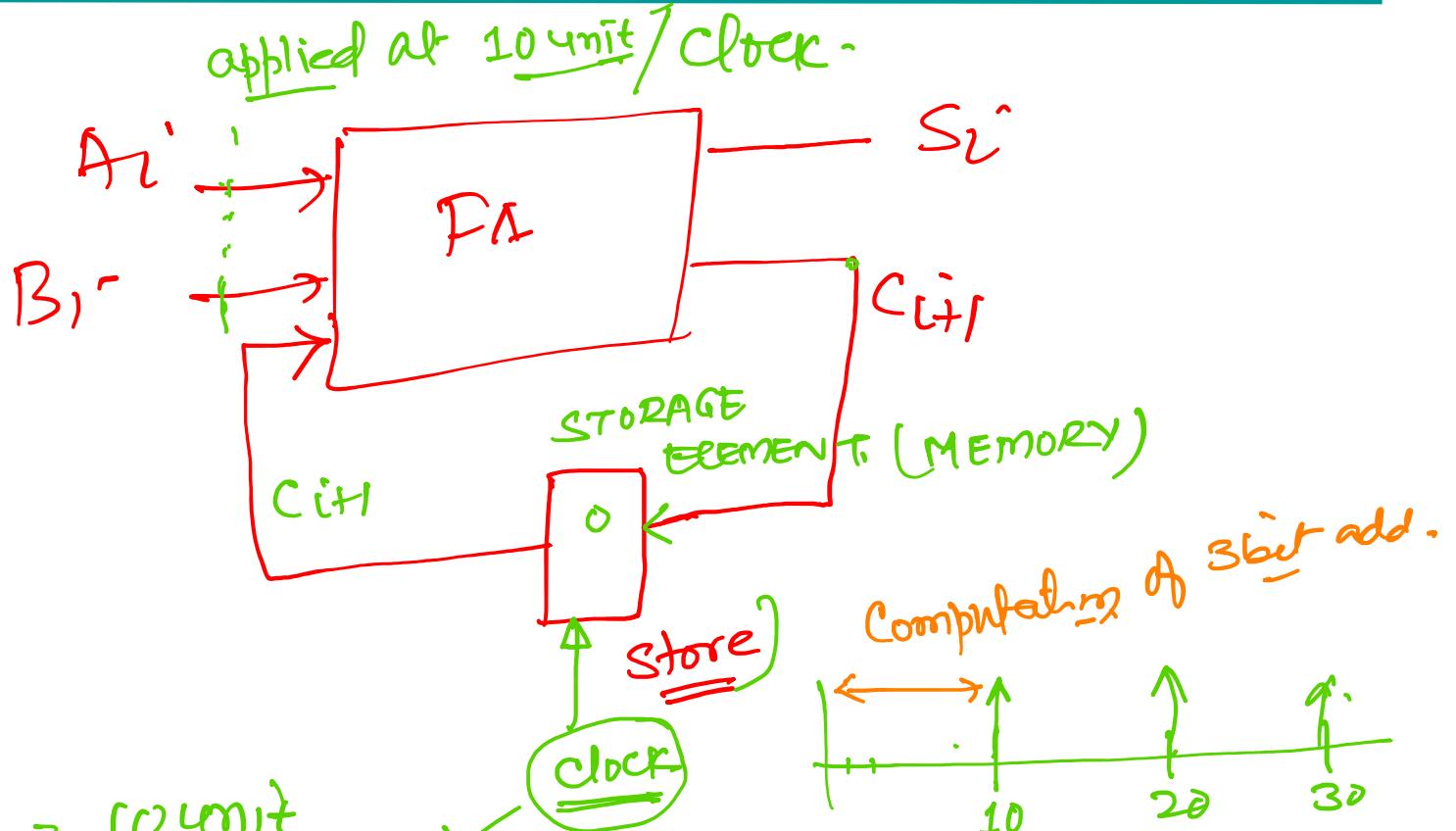
$\frac{32 \times \text{delay of}}{2 \text{ FA}}$
10 units

$\frac{320}{3.2} \text{ n}$

$$\frac{\text{cost}}{1 \text{ FA}}$$



Serial Adder



$$\text{clock} = \frac{\text{10 unit}}{10 \text{ ps}}$$

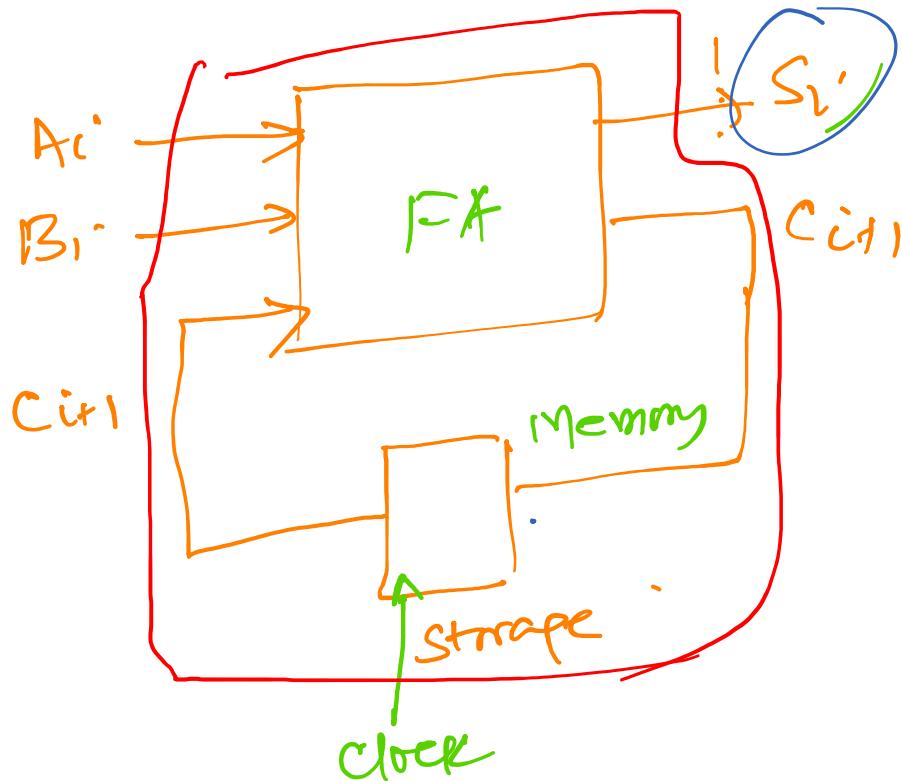
100 ps

$$\frac{1}{100 \times 10^{-12} \text{ Hz}} = \frac{1}{10^{-10}}$$

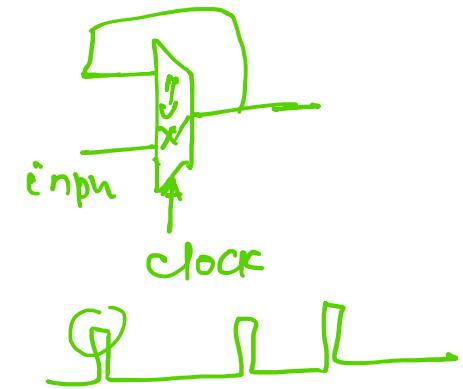
$$= 10^{10} \text{ Hz} = 10 \text{ GHz}$$



Serial Adder



$$\begin{array}{r} \underline{A_i \ B_i} \\ + \underline{B_i} \\ \hline \underline{S_i} \end{array} \quad \text{clock}$$



1 FA + 1 Storage element

Clock to control. (notion of timing)



Serial Adder

A_i	B_i	C_{in}	S_i
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Output is not dependent only on the input but it is also dependent on previous inputs

Sequential circuit

Memory



Serial Adder

Temporal behaviour \rightarrow sequential logic.



STATE OF THE SYSTEM

\hookrightarrow Past behaviour that it has memorized

If can memorize only carry

CARRY = 0
CARRY = 1



Serial Adder

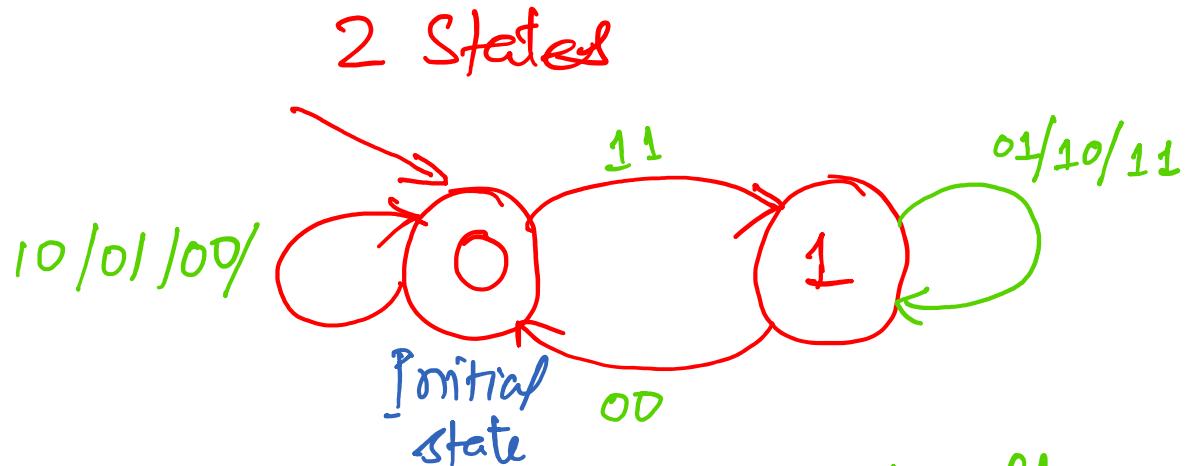
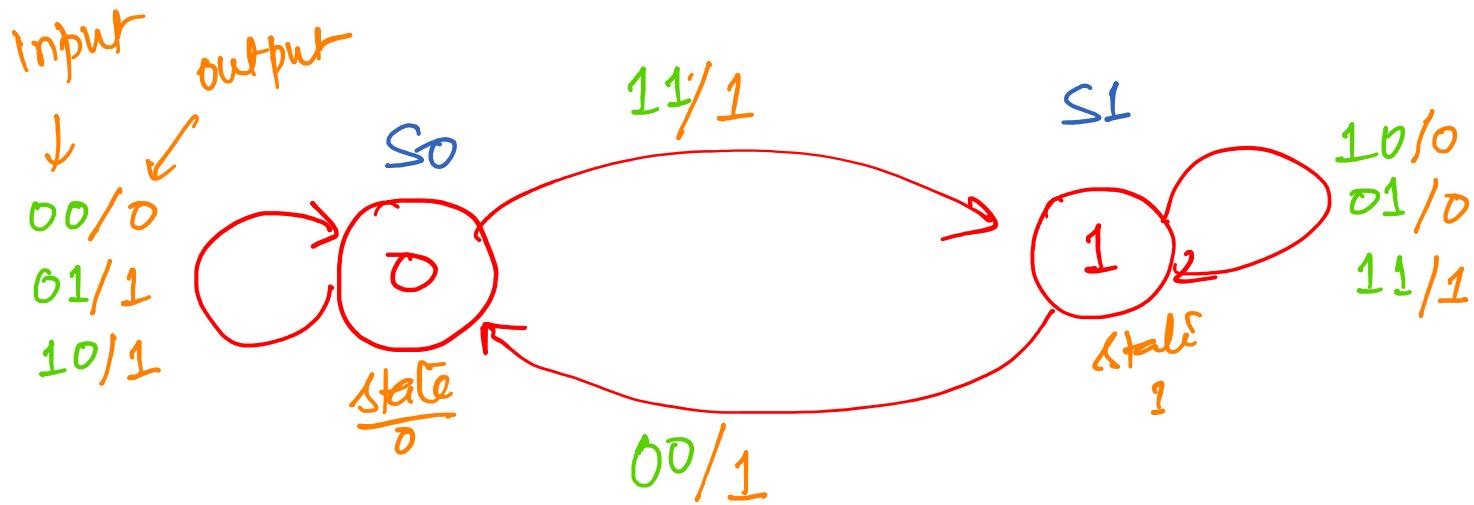


diagram - graphically represent
the transition of state of the system

STG (State Transition Graph)



Serial Adder



State transition Graph (STG)
input / output



<u>A_i</u>	<u>B_i</u>	<u>State</u> <u>C_i</u>	<u>Output</u> <u>S_i</u>	<u>Next State</u> <u>C_{i+1}</u>
0	0	0	0 150	0 150
0	0	1	1 151	0 150
0	1	0	1	0
0	1	1	0	1
1	0	0	1	1
1	0	1	0	0
1	1	0	0	1
1	1	1	1	1

State Transition Table-



Serial Adder

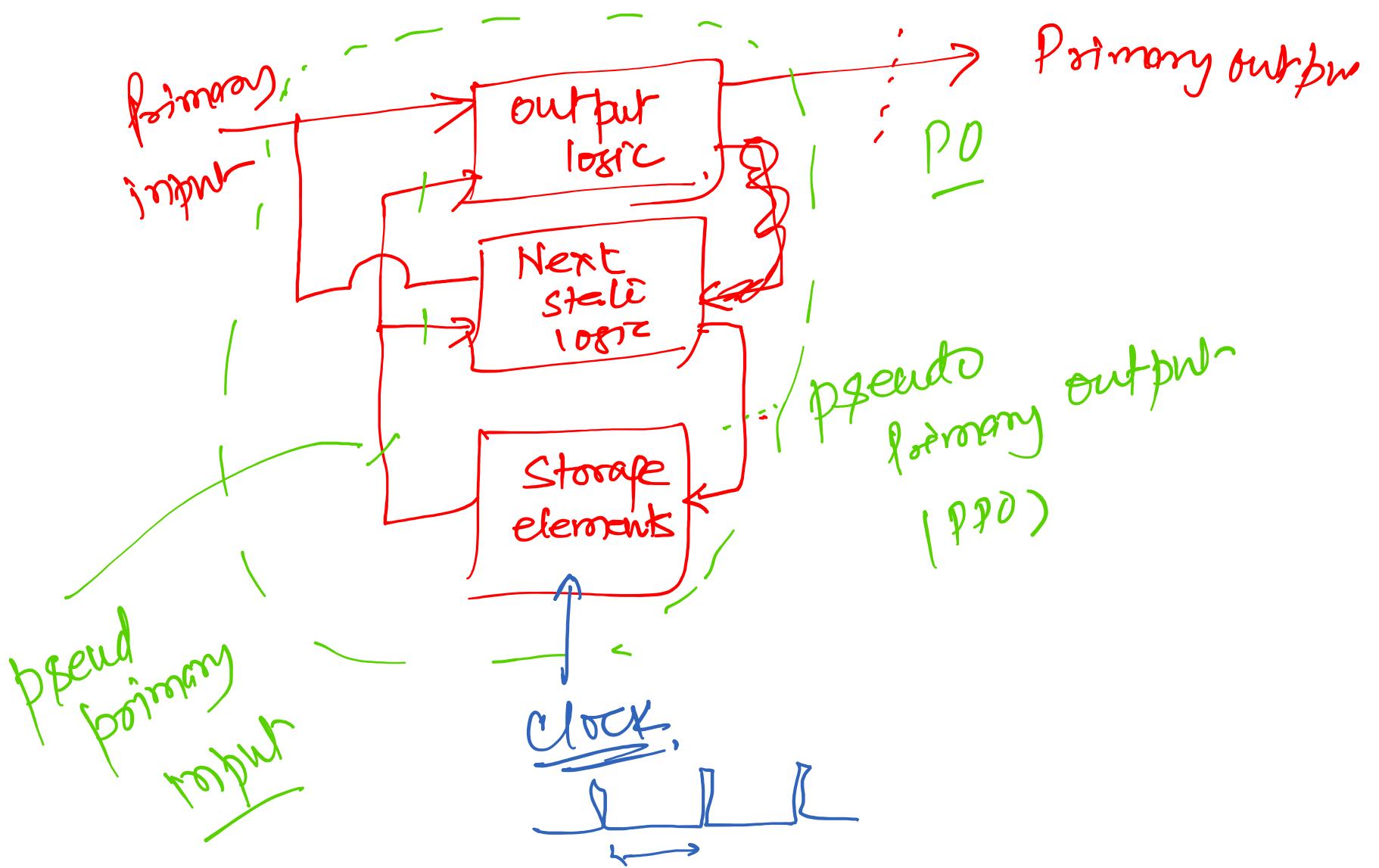
Two logic

→ output logic (produces output based on current input & state)
Combinational logic

→ state transition logic (produces output based on current input & state)
Combinational logic

Storage elements (to store the states) $\leftarrow \log_2 n$





Thank You

