

# Programmable System Design

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*CS-226: Digital Logic Design*

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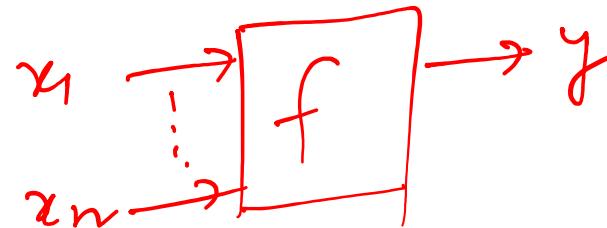


Lecture 28: 12 April 2021

**CADSL**

# Finite State Machine

✓ Combinational



✓ Sequential

A block diagram representing a sequential function. An input vector  $x = [x_1, \dots, x_n]$  enters a block labeled 'f'. The output  $y$  is produced by the function  $y = f(x_1, \dots, x_n, s_1, \dots, s_n)$ , where  $s$  represents the state.

temporal    behaviour

A sequence of states  $S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow \dots \rightarrow S_n$  connected by arrows, illustrating the temporal behavior of the system.



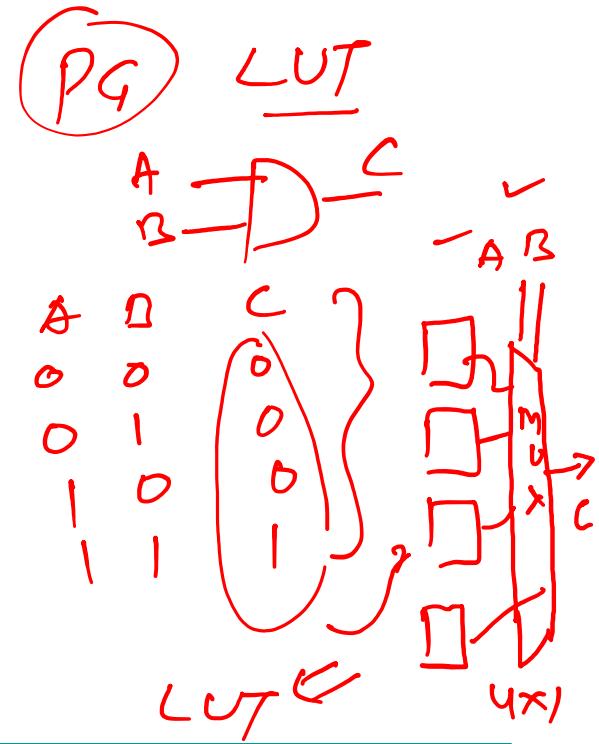
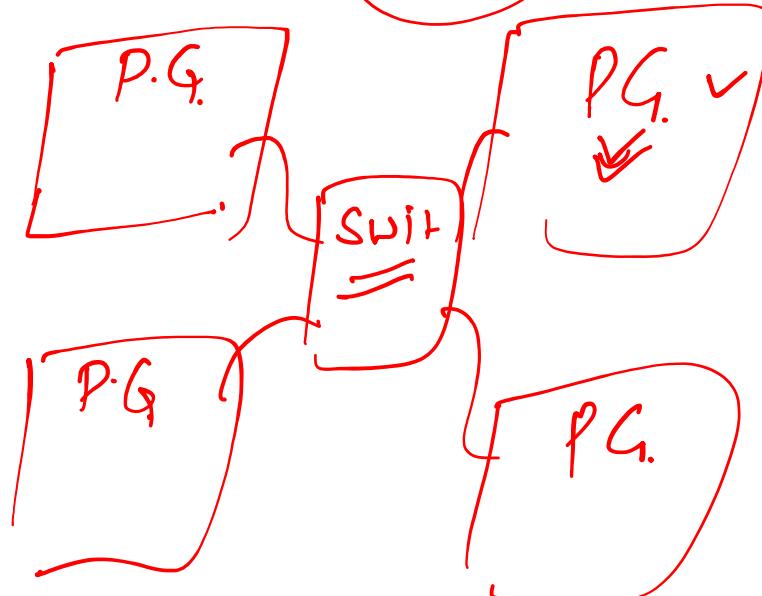
# Flexible System

Implement using flexible fabric

FPGA

Field

Programmable Gate Array



5 input LUT & 6 input LUT.

$$2^5 = 32 \rightarrow 2^2 = 2^{(32)} \quad 2^6 = 64$$

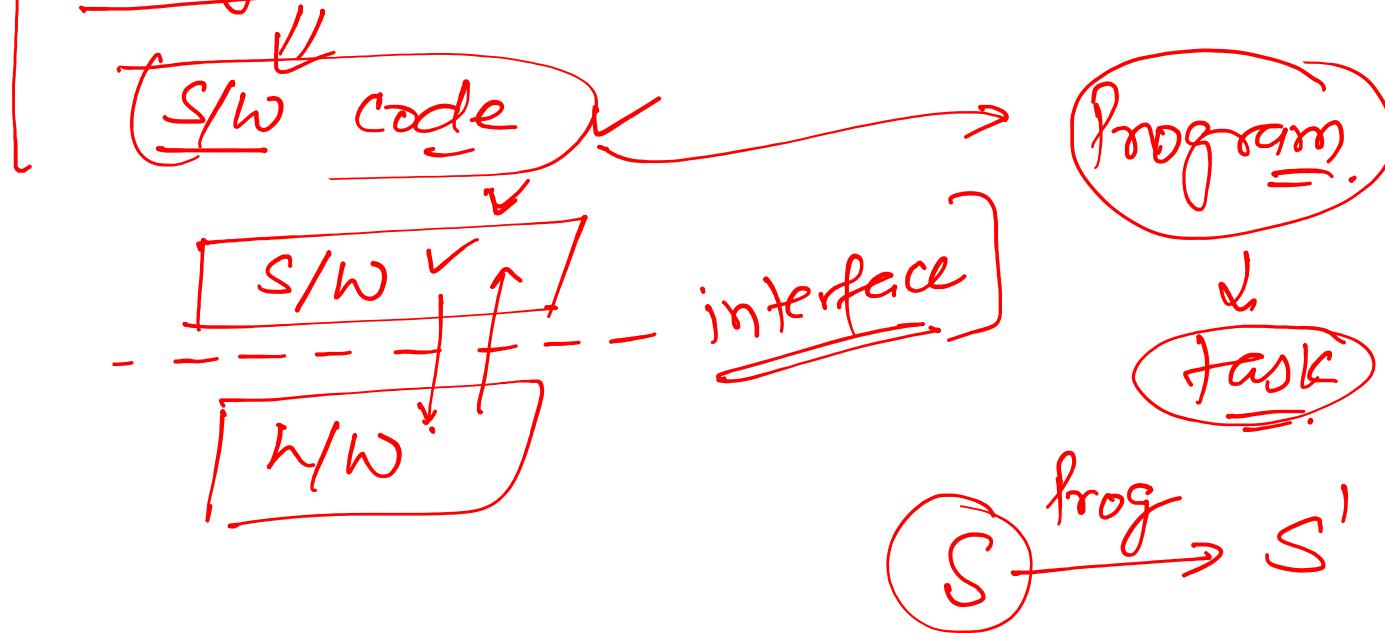
$$\begin{aligned} y_1 &= x_1 x_2 + x_3 x_4 + x_1 x_4 \\ \Rightarrow y_2 &= x_1 + x_2 x_4 \\ y_3 &= x_1 x_3 + x_3 x_4 \neq x_2 \end{aligned}$$

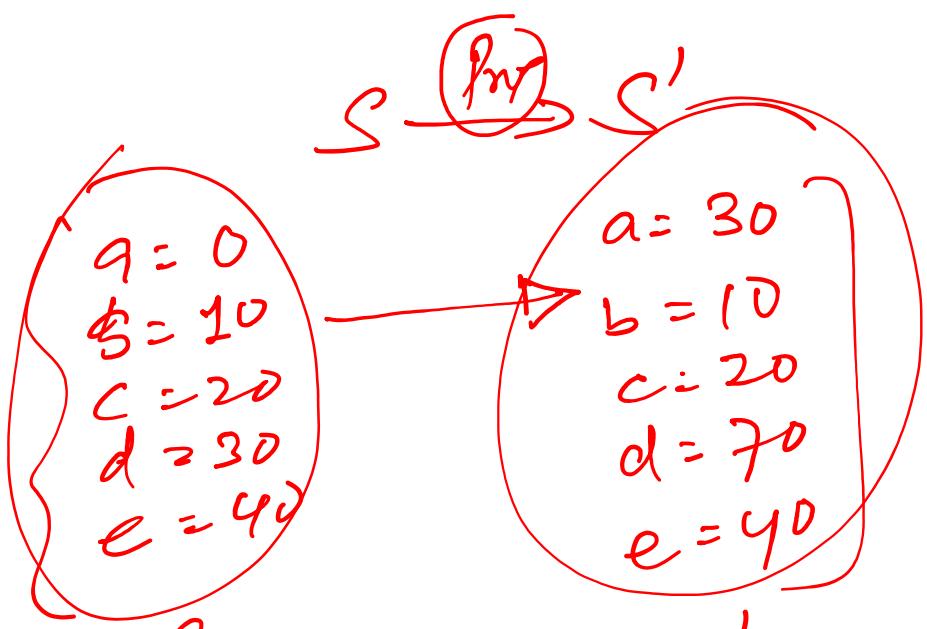
Redesign circuit → Map on FPGA.  
map logic on LUT & interconnect



# Programmable Fabric

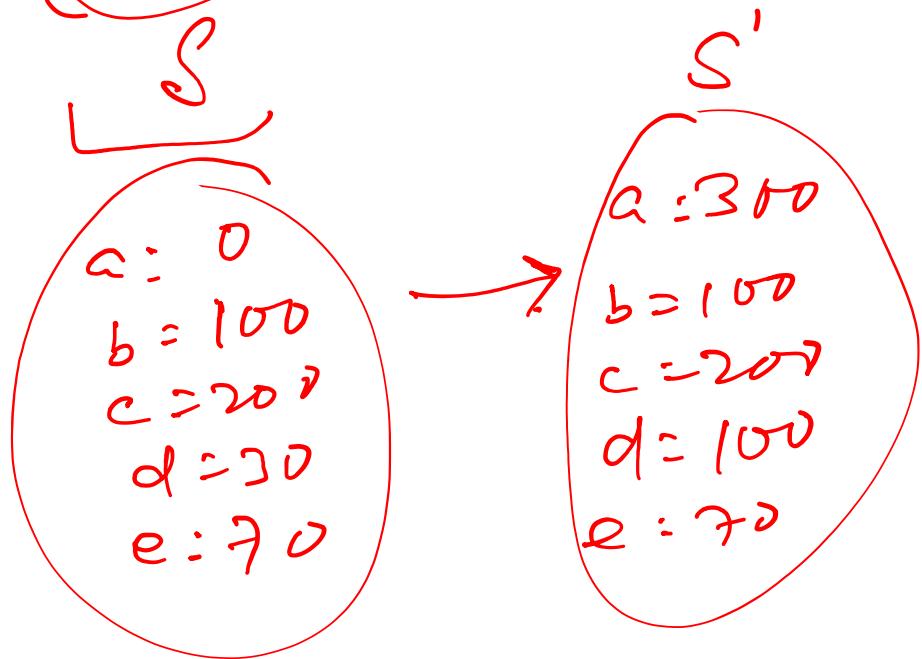
Generic hardware which can be  
programmed as per requirement

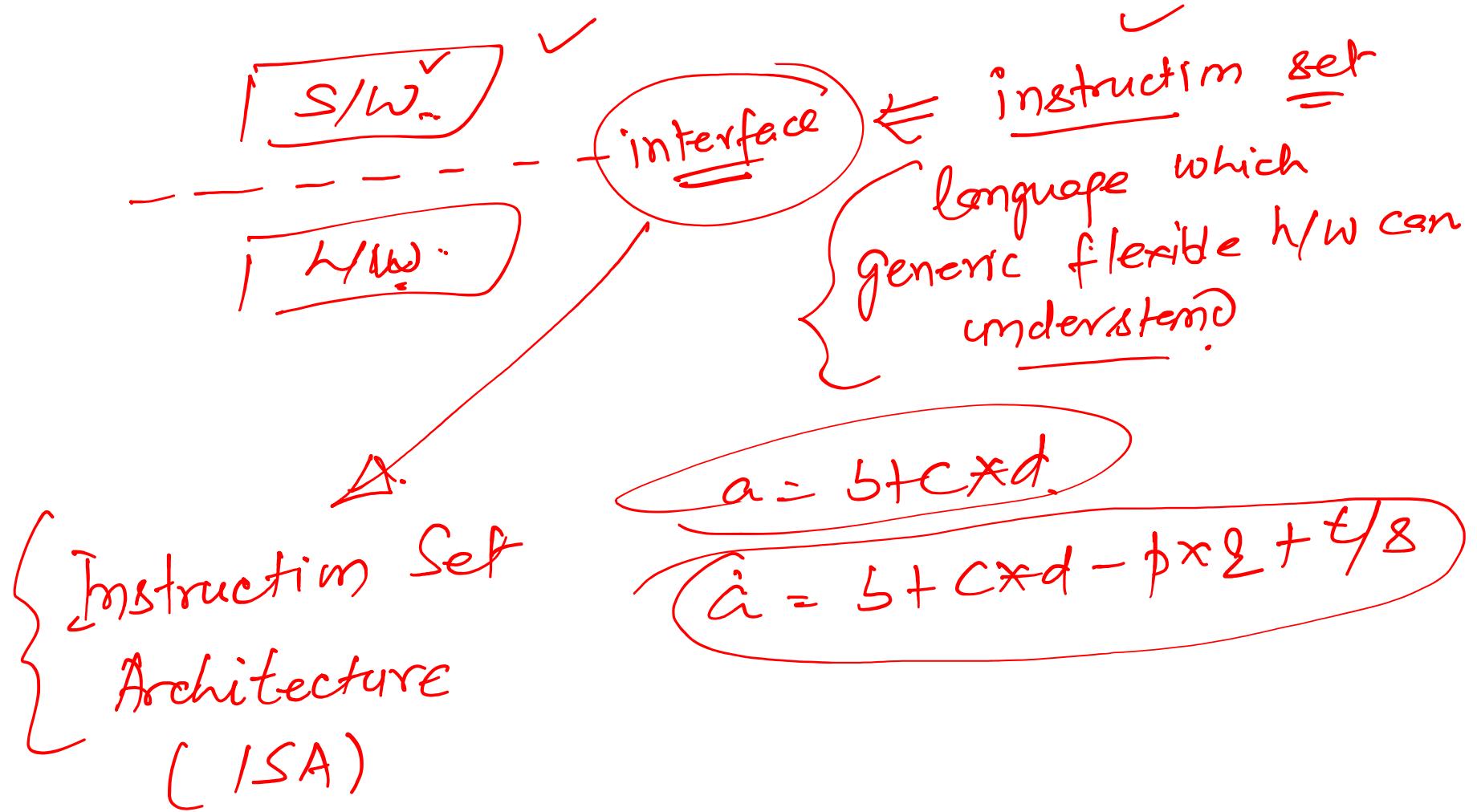




Propom

$a = b+c$   
 $d = d+e$





# Instruction Set Architecture

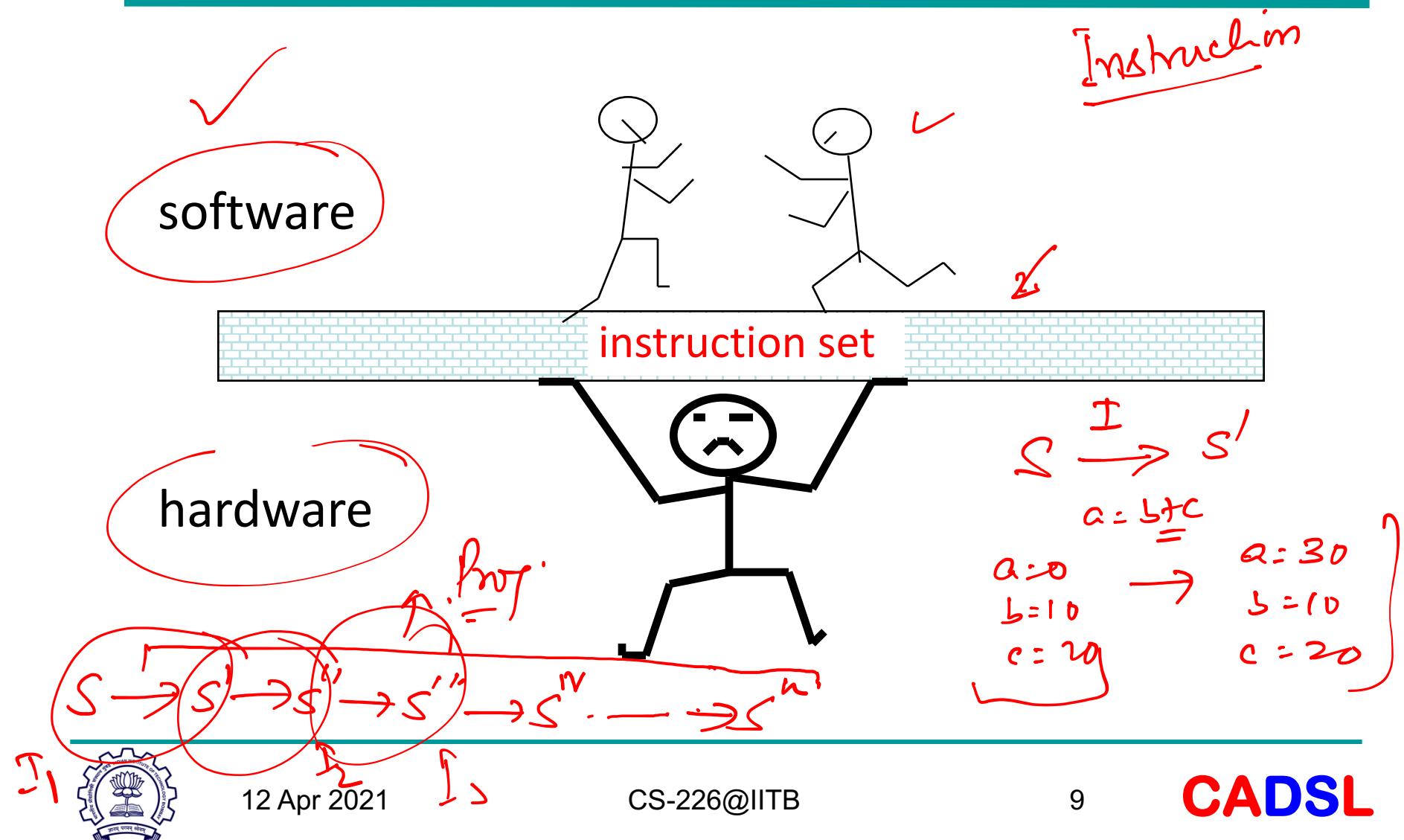
SLW

- Instruction set architecture is the structure of a computer that a machine language programmer must understand to write a correct (timing independent) program for that machine.
- The instruction set architecture is also the machine description that a hardware designer must understand to design a correct implementation of the computer.

{genomic flexible hardware}



# Instruction Set Architecture (ISA)



# Instruction

$\stackrel{+}{=}$  -  $*$ ,  $/$

- C Statement

$$f = (g+h) - (i+j)$$

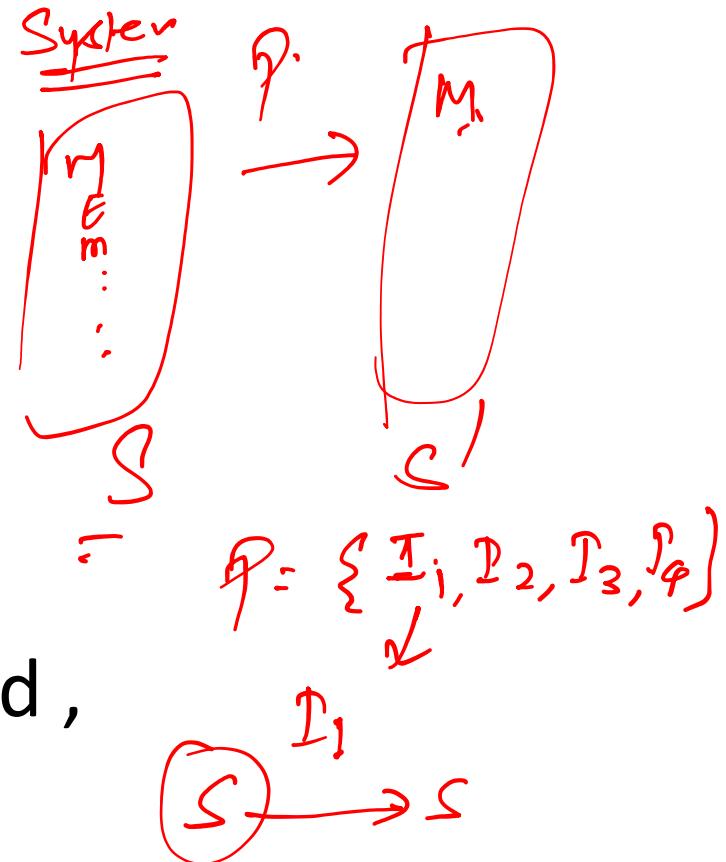
- Assembly instructions

add t0, g, h

add t1, i, j

sub f, t0, t1

- Opcode/mnemonic, operand , source/destination



# Why not Bigger Instructions?

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- Why not “ $f = (g+h) - (i+j)$ ” as one instruction?
- Church’s thesis: A very primitive computer can compute anything that a fancy computer can compute – you need only logical functions, read and write to memory, and data dependent decisions
- Therefore, ISA selection is for practical reasons
  - Performance and cost not computability
- Regularity tends to improve both
  - E.g., H/W to handle arbitrary number of operands is complex and slow, and UNNECESSARY

Primitive computing System



# Instruction

logical

T, {^, v3}

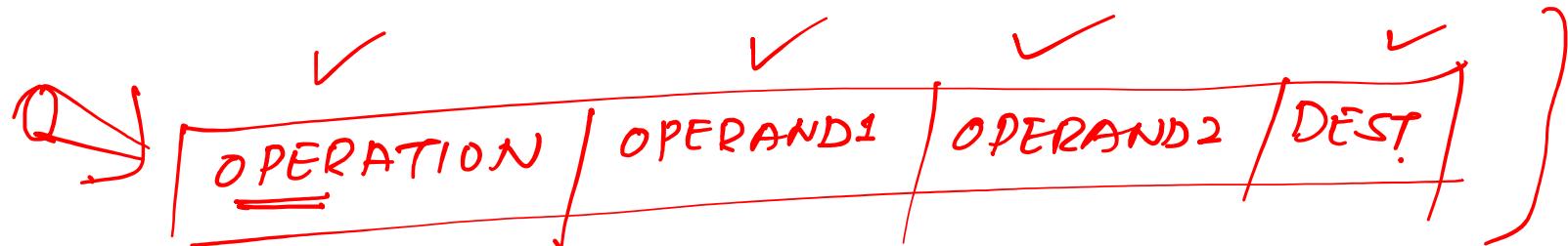
(+)

\*

=

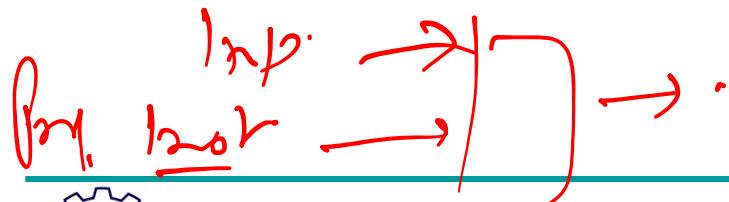
memory read / write

date dependent decision



z = b + c

add b, c, a



| I<sub>1</sub>, I<sub>2</sub>, I<sub>3</sub>, ... , I<sub>n</sub> |



# Thank You

