

Sequential Circuits:

Storage

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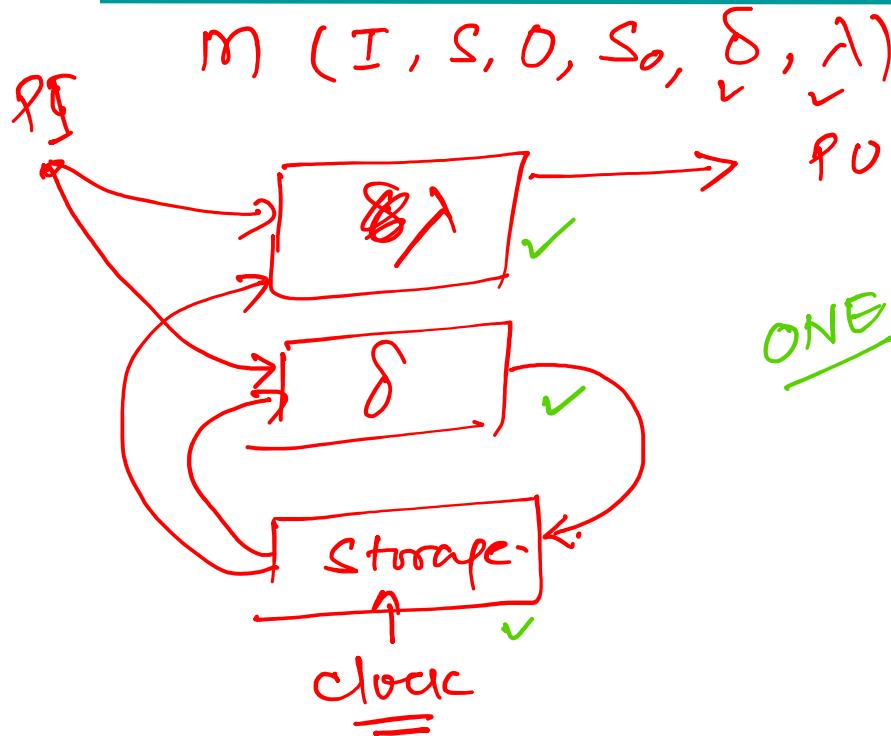
CS-226: Digital Logic Design



Lecture 24: 03 April 2021

CADSL

Finite State Machine



$C \Rightarrow$ longest path
between $(Pf/Pf \& Pd/Pd)$

IM

Q₀

Optimal.
binary encoding -

$$n: \log_2 |S|$$

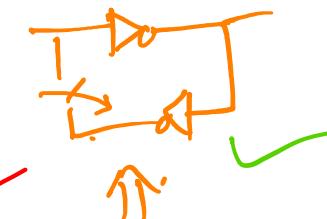
Finite State Machine

STORAGE

- Retain the value -

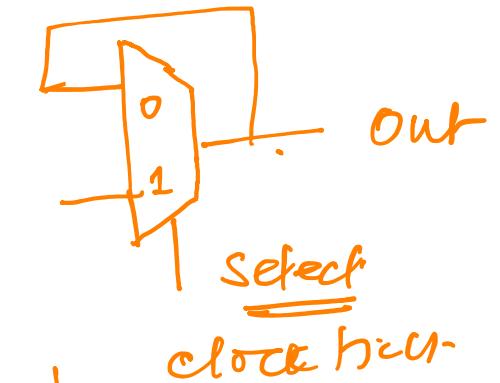
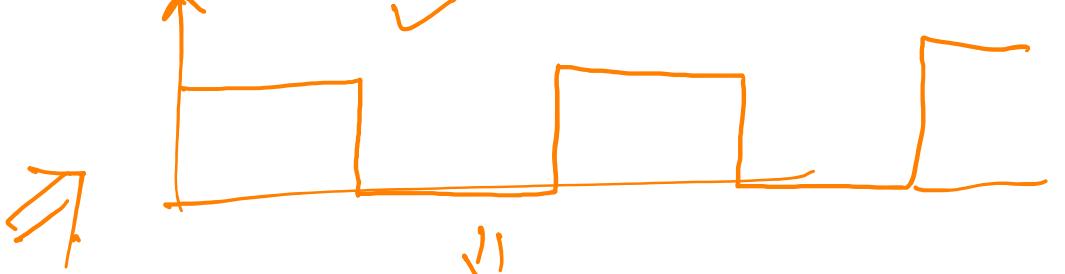
- Change with clock freq

Clock

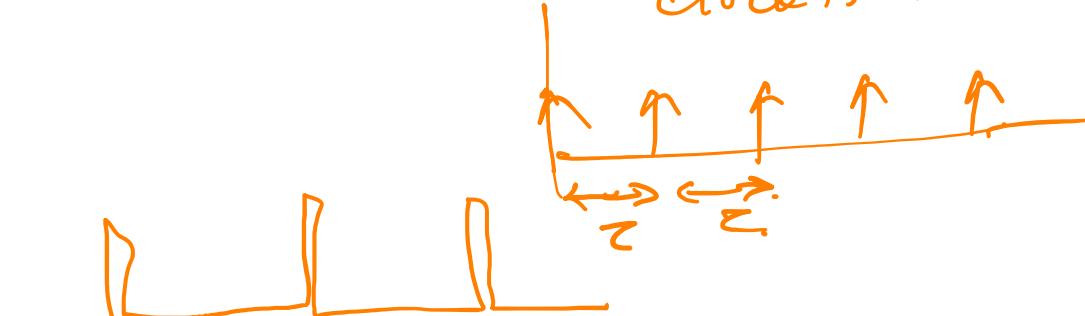


Clock

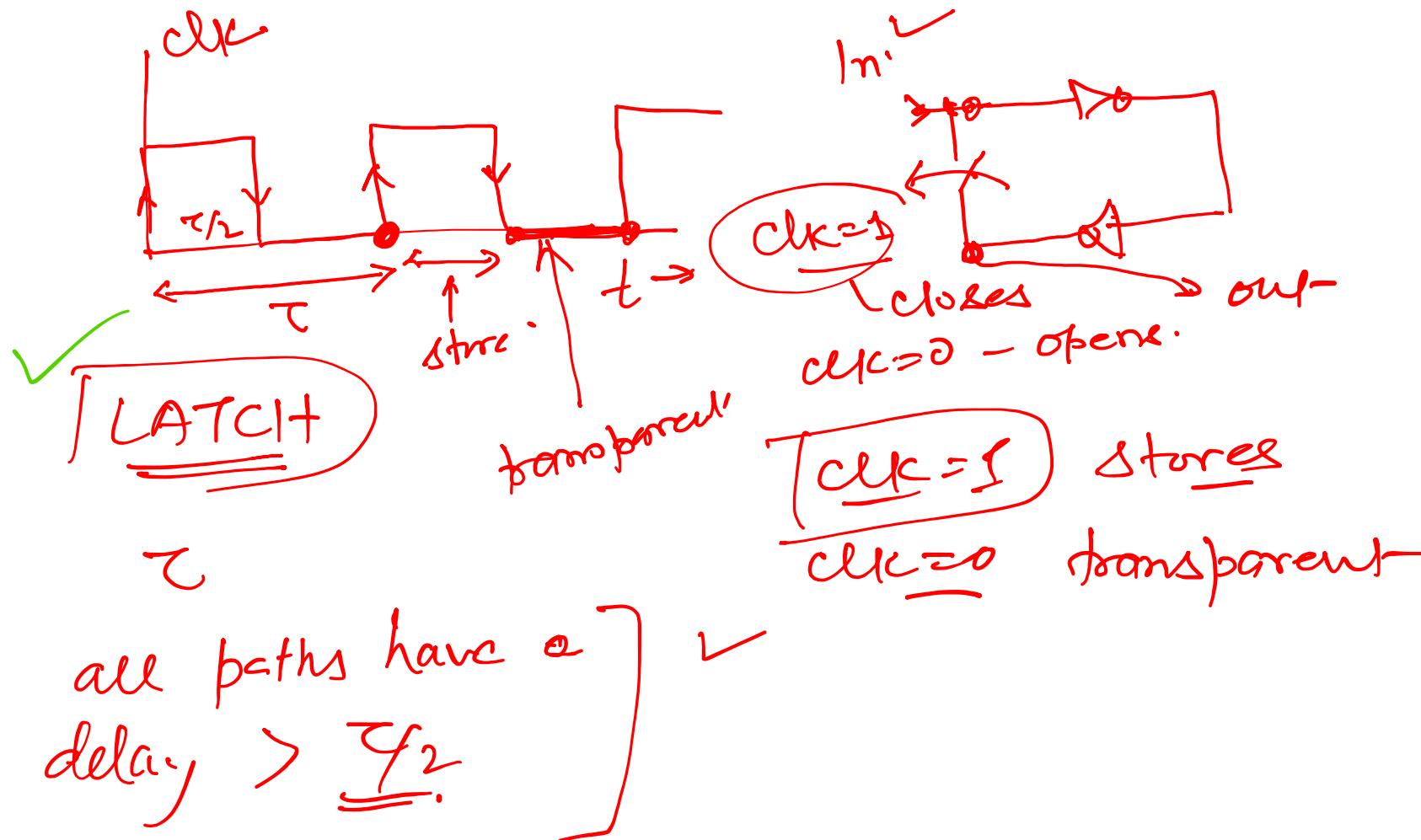
OSCILLATOR



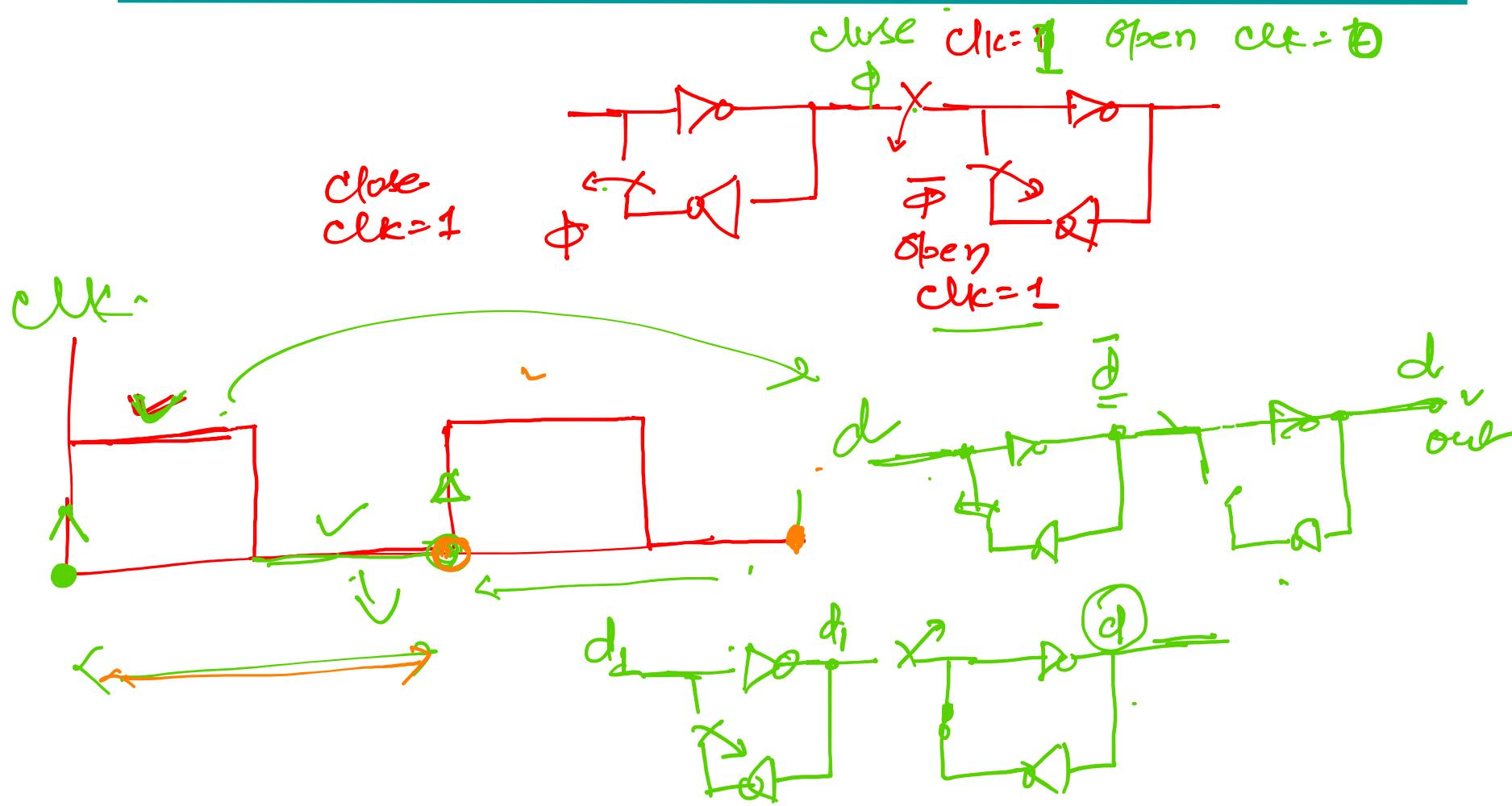
select
clock hz



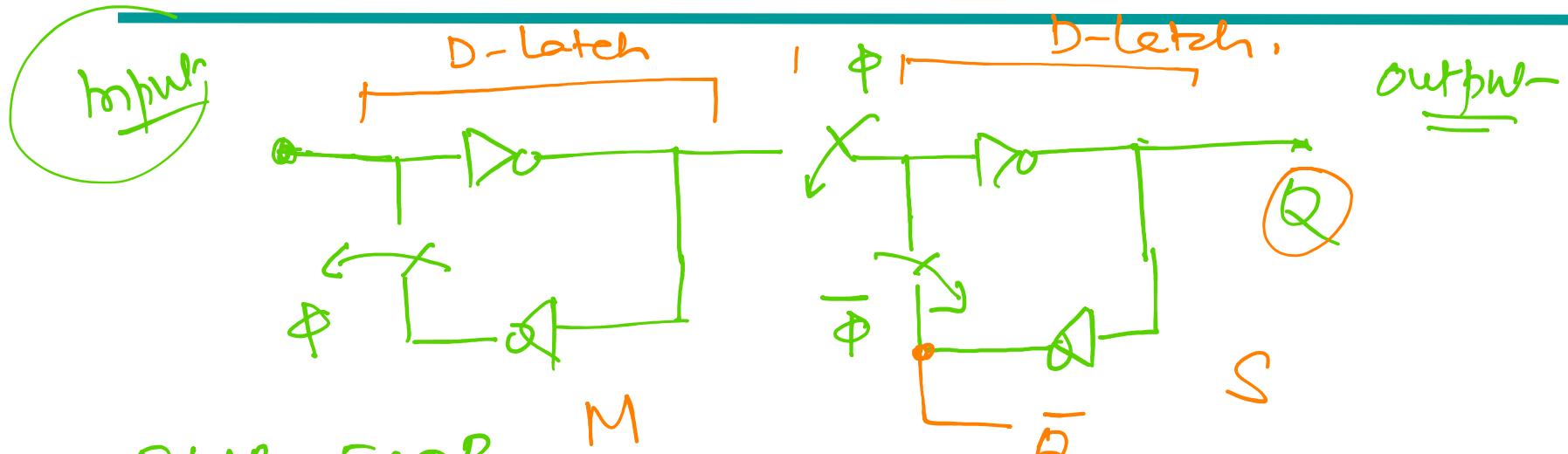
Finite State Machine



Finite State Machine



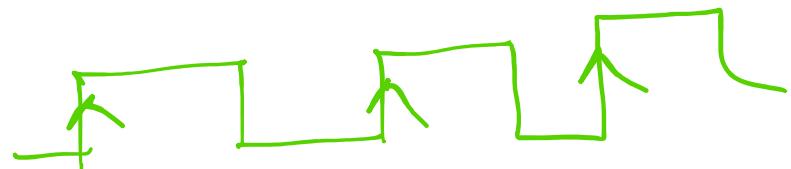
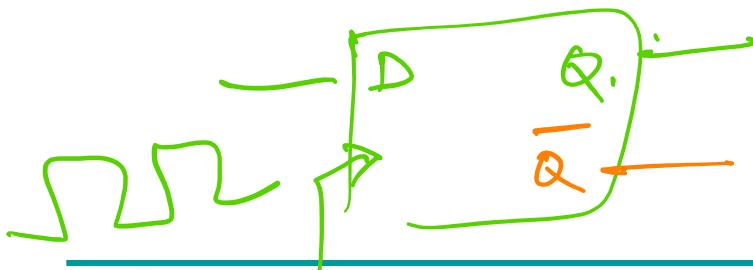
Finite State Machine



PLD - FLIP-FLOP

A:

D - Flip-flop

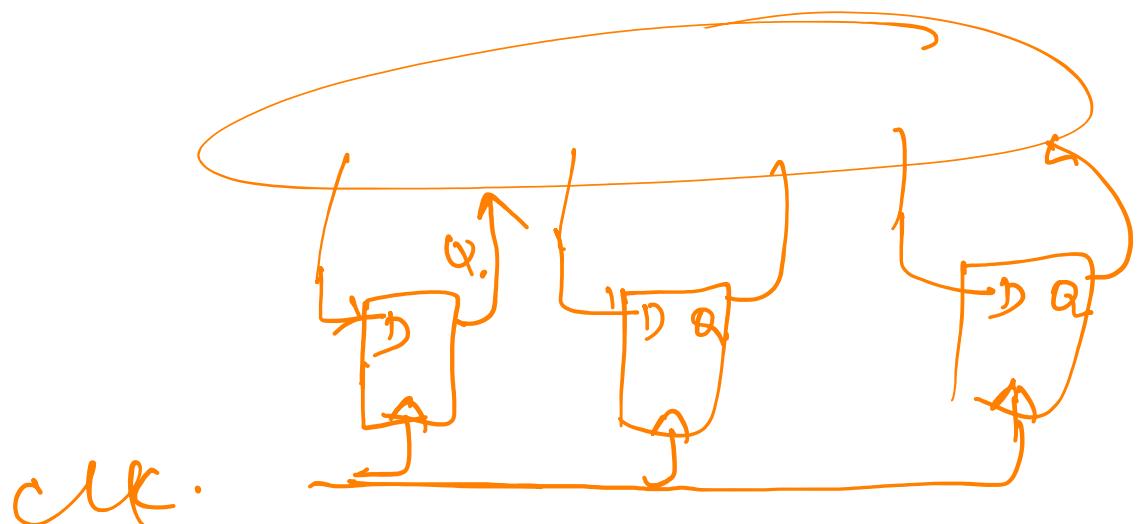
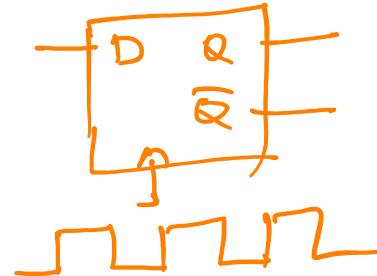


Positive edge triggered

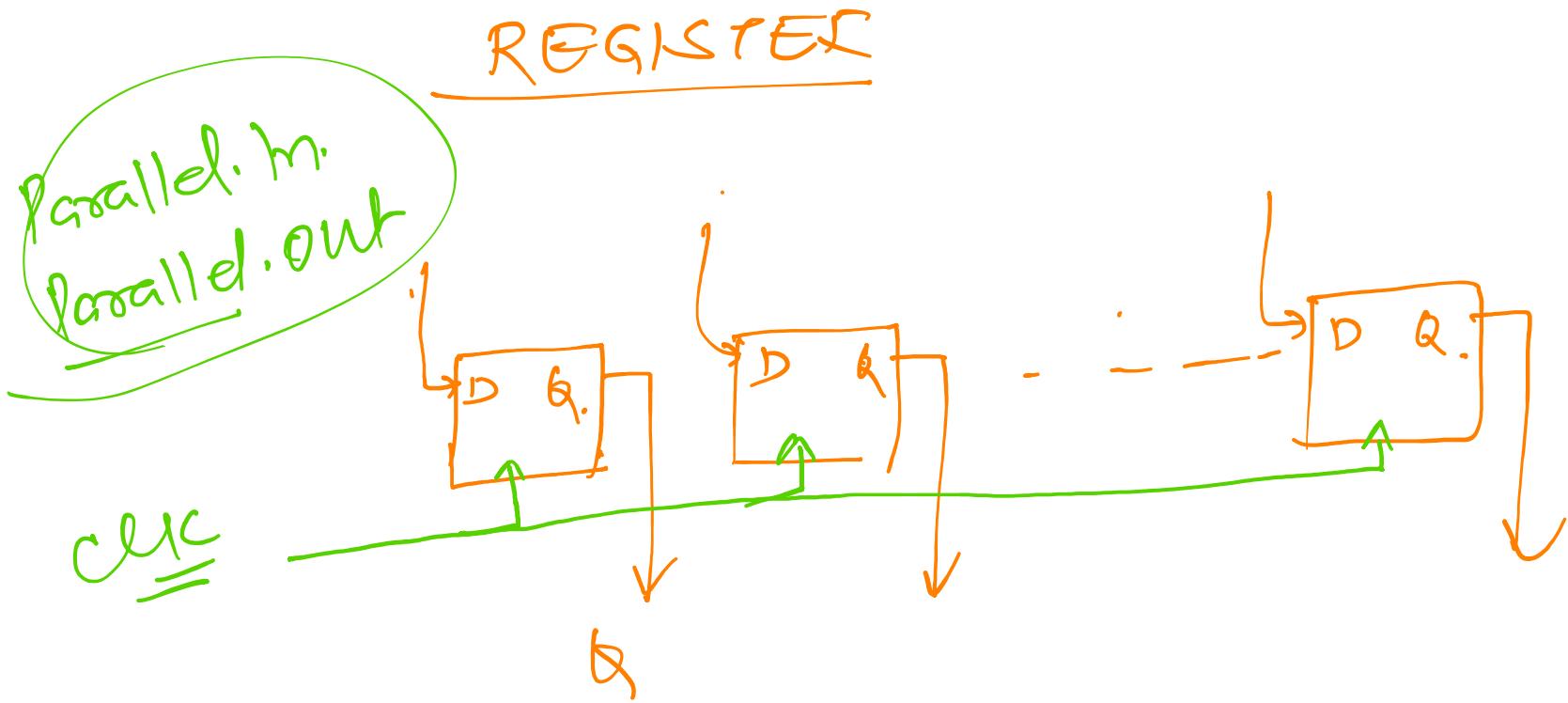
Master Slave Design

Finite State Machine

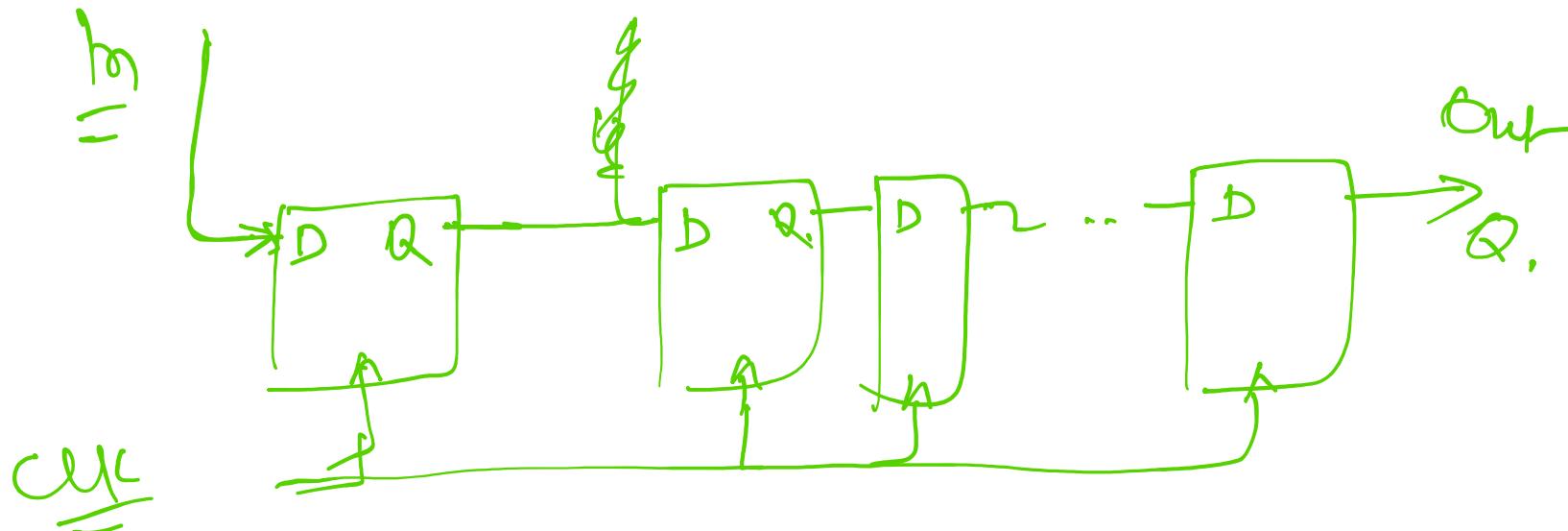
D - FF



Finite State Machine



Finite State Machine

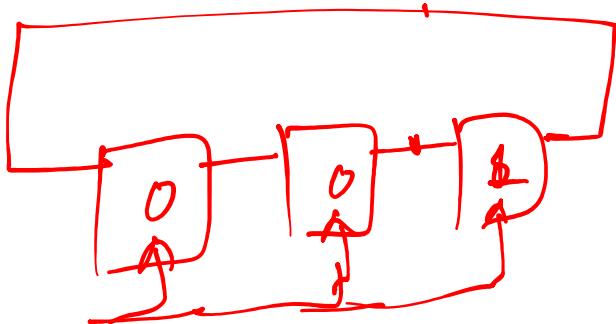


serial_in & serial_out =

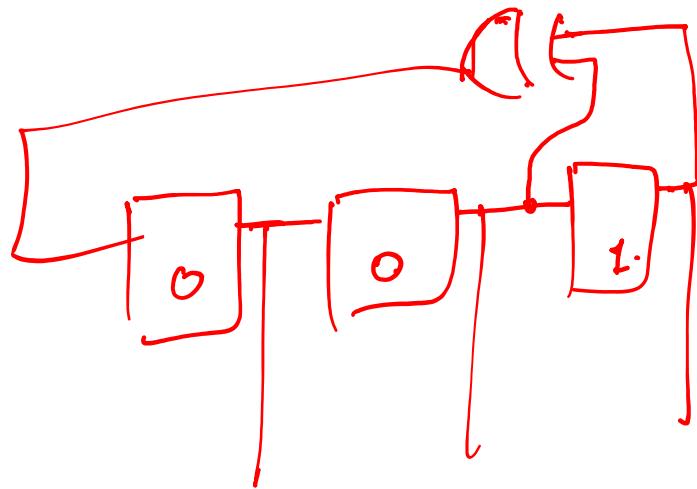
SHIFT

LFSR - Linear Feedback Shift Register





001
100
010
001



7

pseudo random sequence

My system went down. Please wait for 2-3 minutes

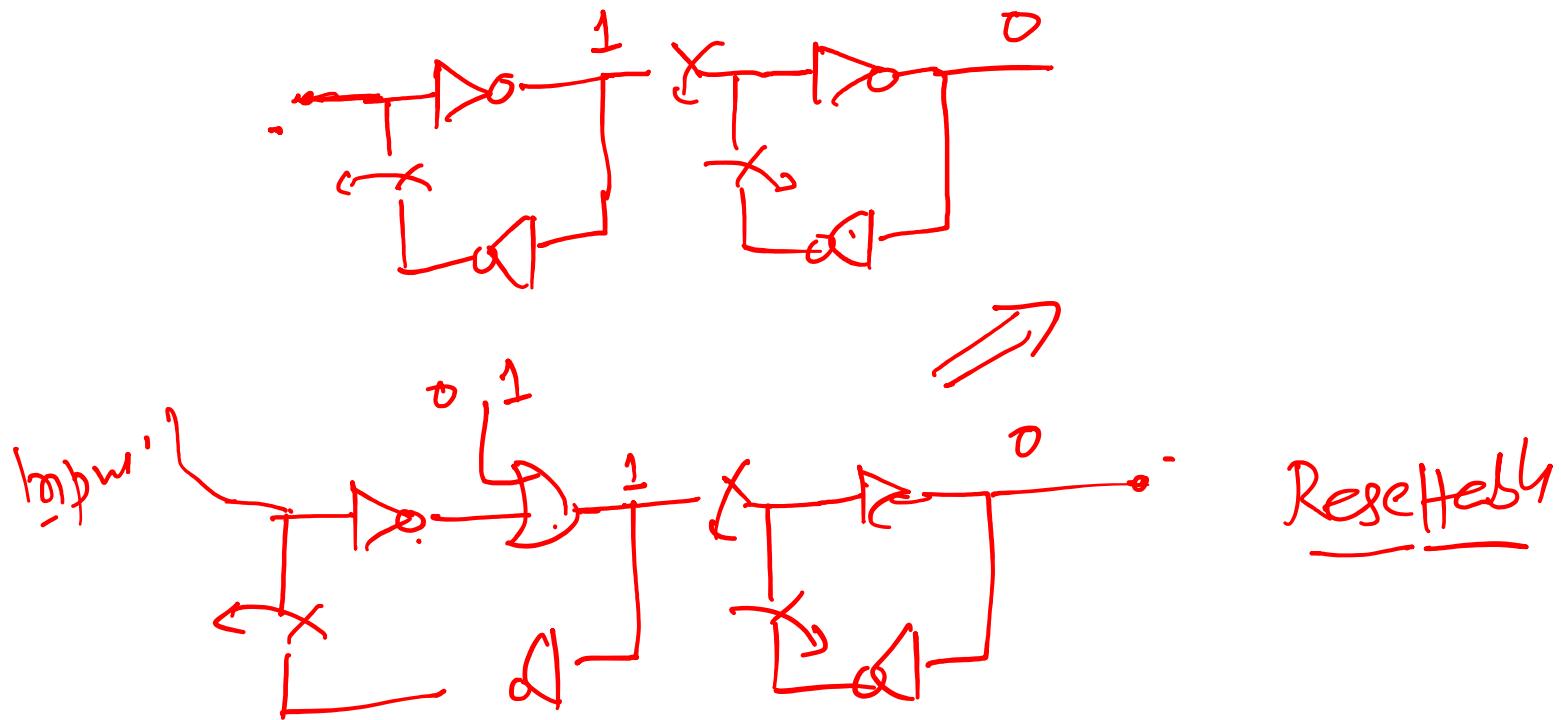
SORRY

10

CADSL



D-EF Standard

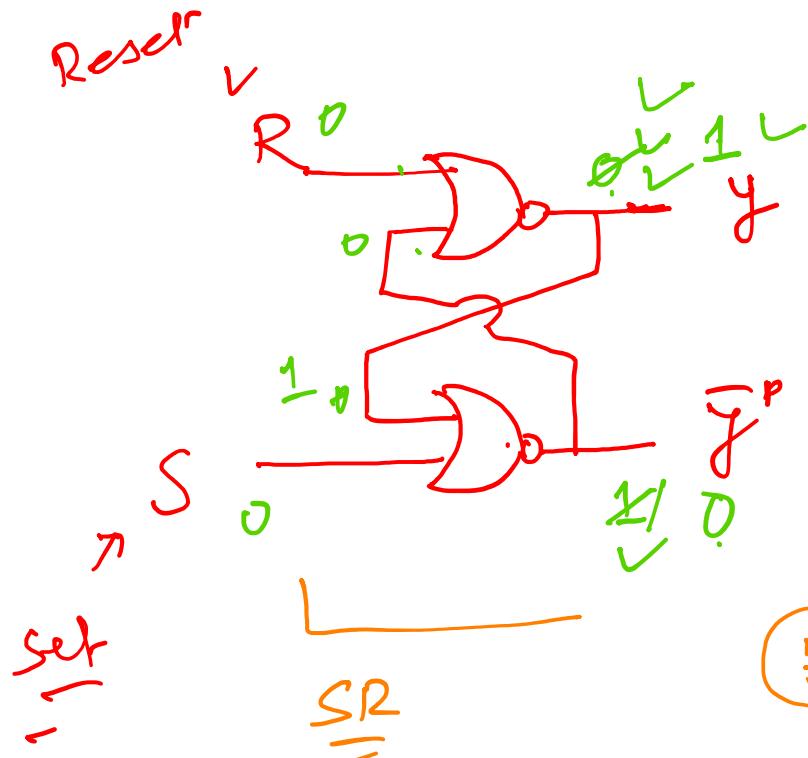


Storage

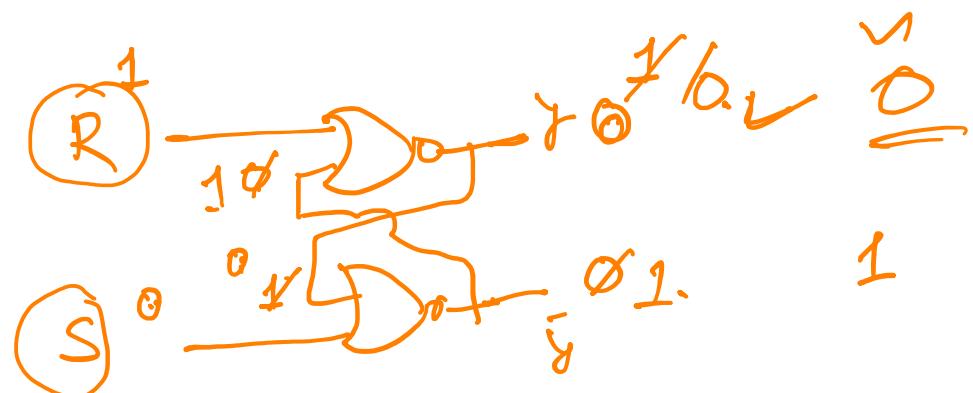
SR latch

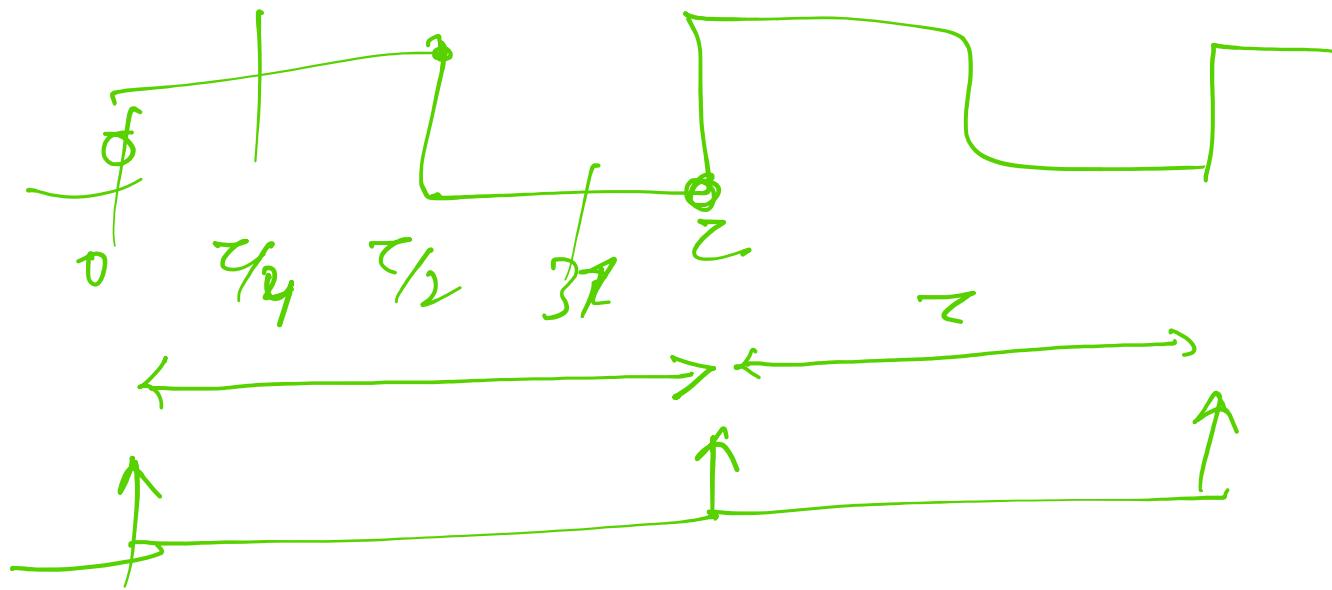
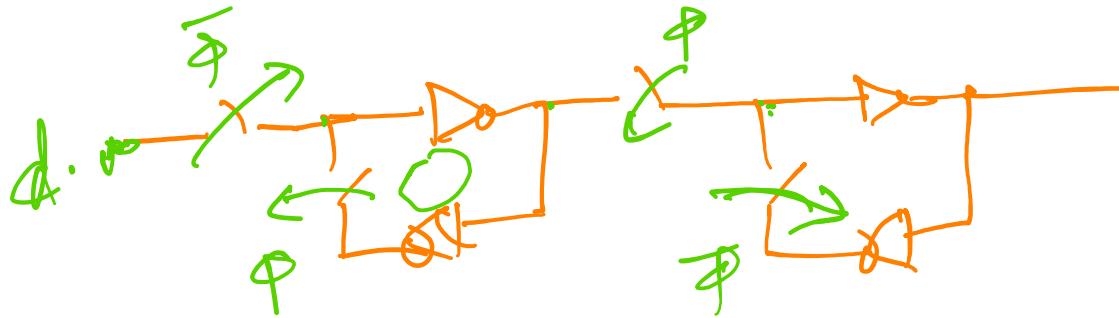
SR FF

JK FF / TFF



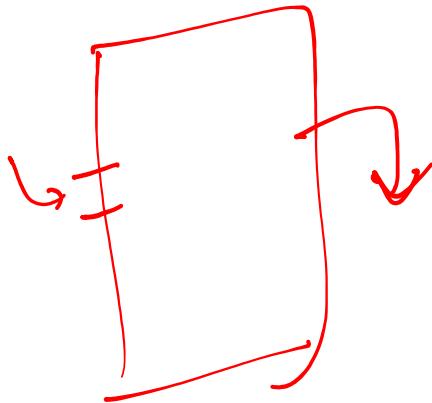
<u>R</u> <u>S</u>	→ Retain
1 0	→ 0
0 1	→ 1
1 1	→ Race





MEALY

₹ 15



MOORE

₹ 20

₹ 20

20 -
10 → Col.
Col.

₹ 5 / ₹ 10



Thank You

