

# Arithmetic Circuits

## Multiplier

---

Virendra Singh

Professor

Computer Architecture and Dependable Systems Lab

Department of Electrical Engineering

Indian Institute of Technology Bombay

<http://www.ee.iitb.ac.in/~viren/>

E-mail: [viren@ee.iitb.ac.in](mailto:viren@ee.iitb.ac.in)

*CS-226: Digital Logic Design*

---



*Lecture 19-A: 11 March 2021*

**CADSL**

# Binary Multiplication (Unsigned)

$1000_{\text{two}}$   
 $1001_{\text{two}}$

$= 8_{\text{ten}}$  ✓  
 $= 9_{\text{ten}}$  ✓

multiplicand ✓  
 multiplier ✓



$1000$   
 $0000$   
 $0000$   
 $1000$   


---

 $1001000_{\text{two}}$

$n \times n$   
 $2^n$

partial products

$= 72_{\text{ten}}$

*Basic algorithm: For  $n = 1, 32$ , only If  $n$ th bit of multiplier is 1, then add multiplicand  $\times 2^{n-1}$  to product*



# Adding Partial Products

				y3 x3	y2 x2	y1 x1	y0 x0	multiplicand multiplier
				x0y3	x0y2	x0y1	x0y0	four partial products to be summed
				x1y3	x1y2	x1y1		
				x2y3	x2y2	x2y1	x2y0	
				x3y3	x3y2	x3y1	x3y0	
p7	p6	p5	p4	p3	p2	p1	p0	

Requires three 4-bit additions. Slow.

$$p_2 = x_0y_2 + x_1y_1 + x_2y_0 + \text{Carry}$$

$$p_0 = x_0y_0$$

$$p_1 = x_0y_1 + x_1y_0 + \text{HA}$$



$$p_3 = \underbrace{x_0 y_3 + x_1 y_2 + x_2 y_1 + x_3 y_0}_{\text{FA}} + \text{Carry}$$

FA

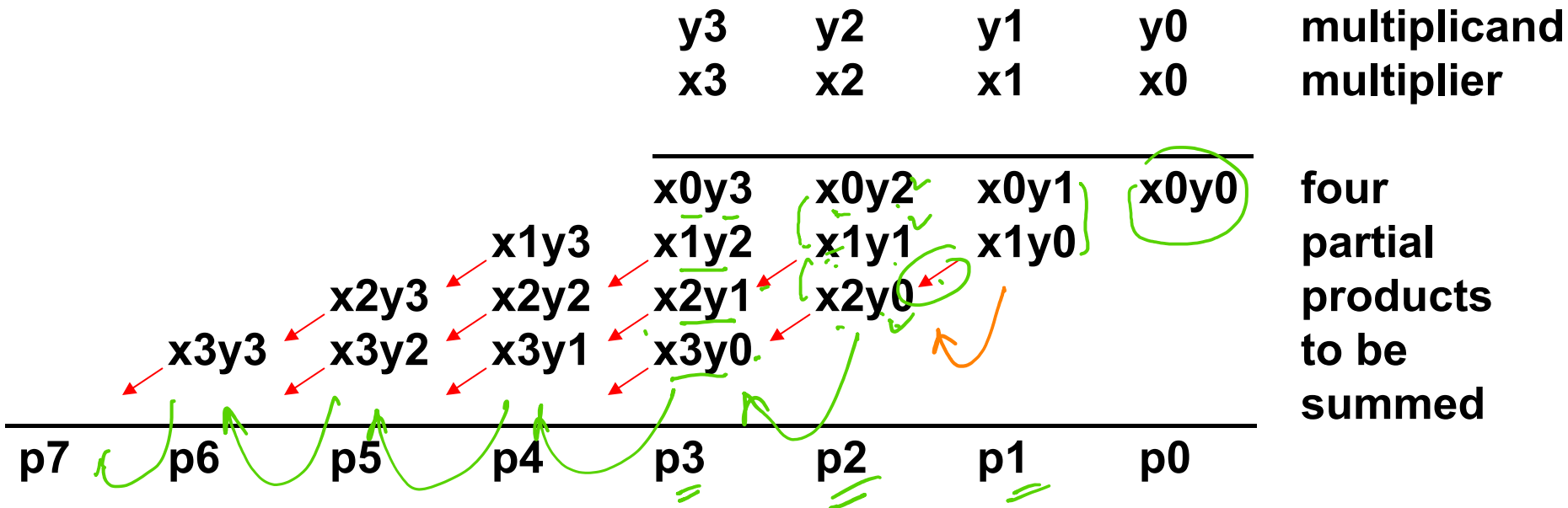
$$p_4 = \underbrace{x_1 y_3 + x_2 y_2 + x_3 y_1}_{\text{FA}} + \text{Carry}$$

FA

# gates



# Array Multiplier: Carry Forward



**Note:** Carry is added to the next partial product (carry-save addition). Adding the carry from the final stage needs an extra (ripple-carry stage). These additions are faster but we need four stages.

## Carry Save Adder

$$\begin{array}{r} 257 \\ 364 \\ \hline 511 \\ \text{Sum} \end{array}$$

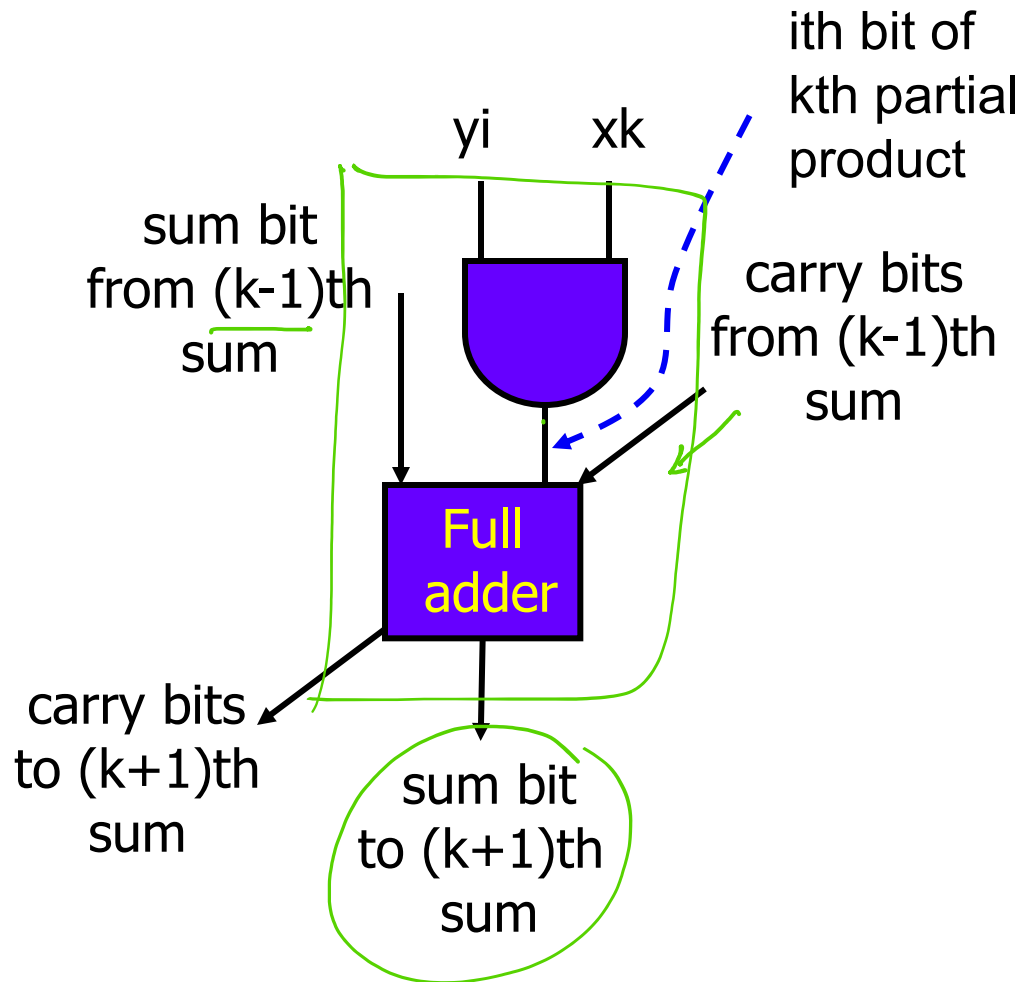
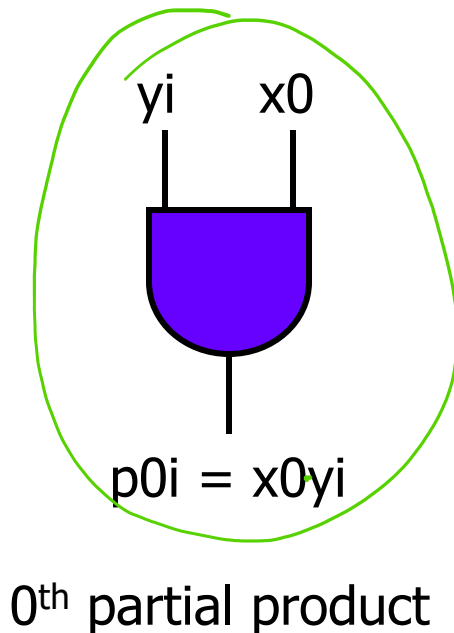
$$\begin{array}{r} 257 \\ 364 \\ \hline 11 \\ \hline \text{Carry} \end{array}$$

$$\begin{array}{r} 511 \\ 110 \\ \hline 621 \end{array}$$

Addition

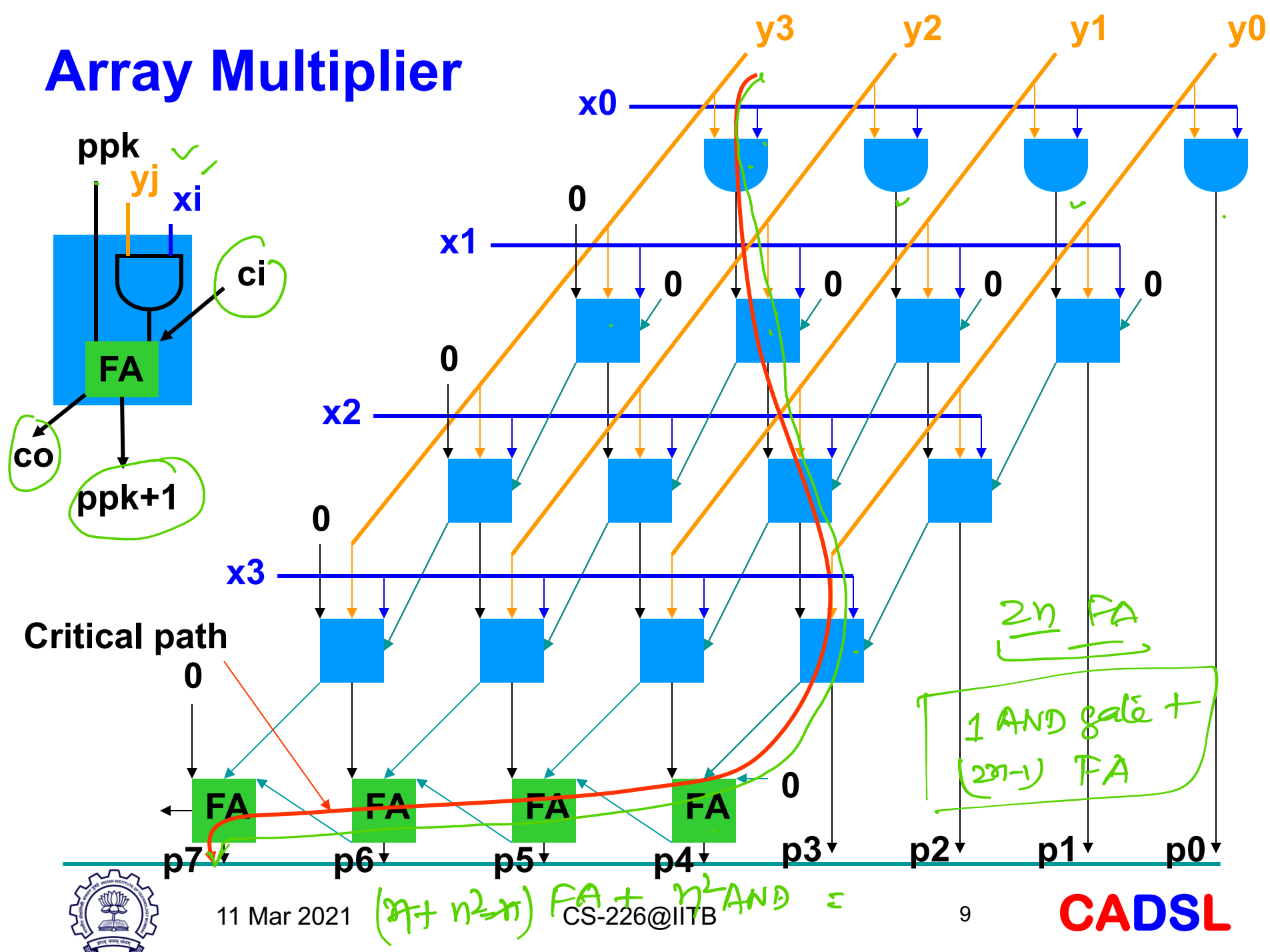
# Basic Building Blocks

- Two-input AND
- Full-adder





# Array Multiplier



# Thank You

