CS 254 - Assignment 4

Rules: ***1) For all questions, only structural VHDL code is permitted.***

2)All the entity statements given in the question must be used as it is.

3)Use the ieee.std_logic_1164 library data types. (Bit and bit vector are not permitted.)

1) Design a 4-bit ripple carry adder using only 1-bit full adders designed in question 4 of assignment 3

```
entity FourbitFullAdd is
        port ( a, b : in std_logic_vector (3 downto 0);
        cin: in std_logic;
        sum : out std_logic_vector (3 downto 0);
        carry: out std_logic);
end entity;
```

2) Design a 2-bit comparator using only 2x1 multiplexers. ‘a’ and ‘b’ are the input binary numbers of size two bits each. The output ‘l’ must be high only when ‘a’ is less than ‘b’. The output ‘g’ must be high only when ‘a’ is greater than ‘b’. The output ‘e’ must be high only when ‘a’ is equal to ‘b’. The comparator must be designed using minimized expressions for ‘l’, ‘g’, and ‘e’. The minimized expressions must be obtained using the Karnaugh map method taught in class. The minimized expressions must be implemented using only 2x1 multiplexers.

```
entity FourbitComp is
        port ( a, b  : in std_logic_vector (1 downto 0);
        l, g, e : out std_logic);
end entity;
```

Things required in Submission:

1. All VHDL files of top-level and sub-components. (.vhd or .vhdl files)
2. Screenshot of Waveform.
3. Truth table and Karnaugh map working for minimized expression (for all 3 variables) in question 2.

Note: Test bench is not required in submission but create a test bench and use it to test your design before submission. The waveforms generated during your test should be uploaded. No other project files are required. The vhdl files of each question should be kept in a separate folder.