

~~June 14, 2020~~

10/25/2024

A simple quick revision was done on 10/25/2024.

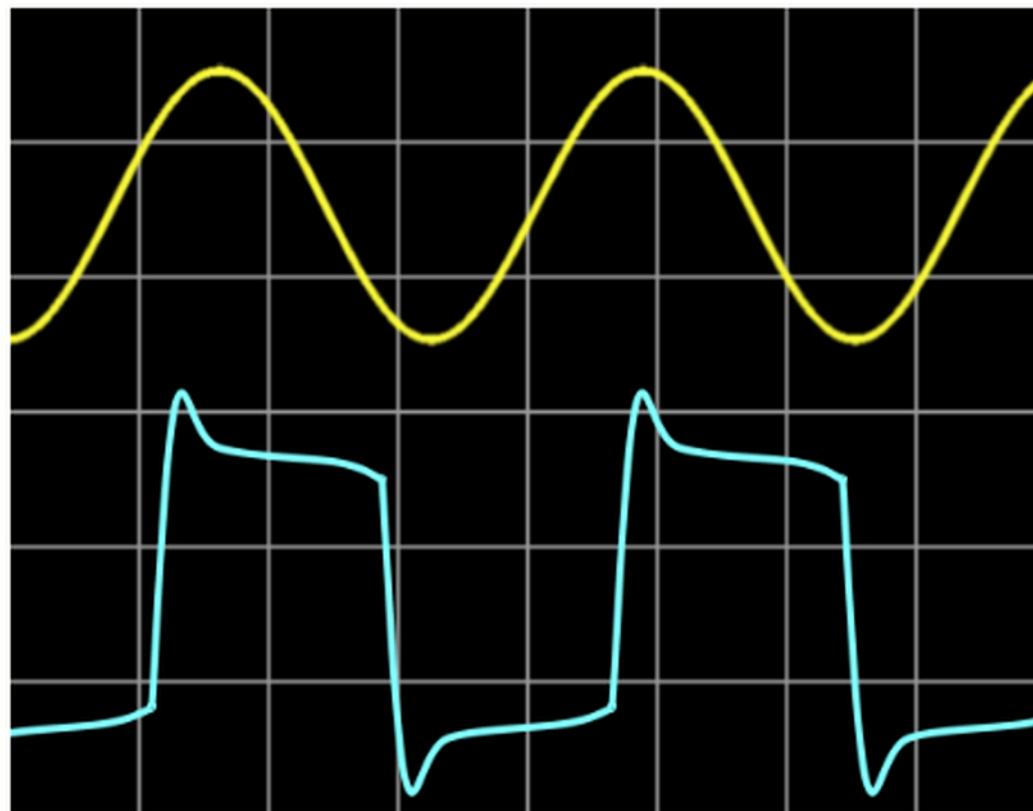
Chipscope_Intro_using_Vivado_ILA.pdf

ILA = Integrated Logic analyzer

Logic Analyzer and On-Chip Logic Analyzer

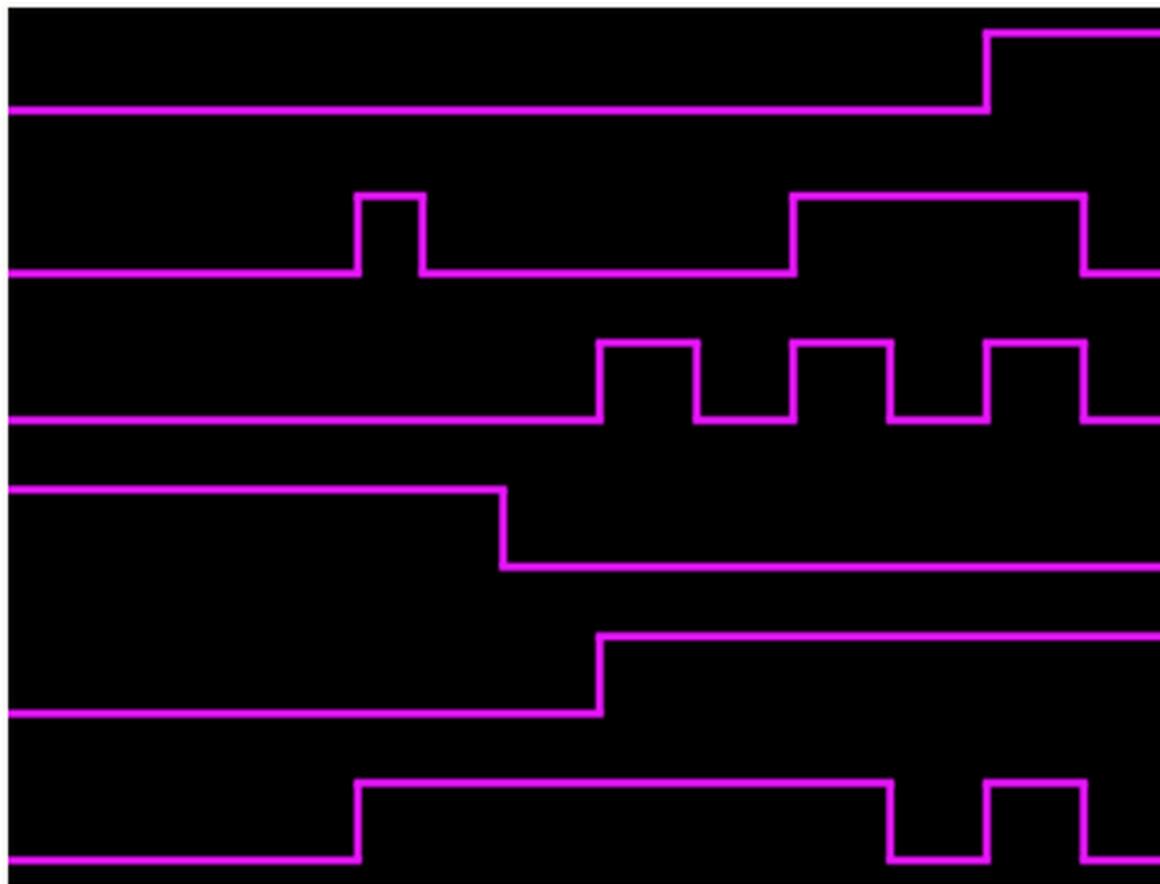
- **Logic Analyzer** **vs.** **Oscilloscope**
Digital **Analog**
32/64/128/256 channels **2 or 4 channels**
Trigger and Storage qualifications **Simple trigger**
- **SoC (System on Chip) and Embedded Processors in SoC**

<https://articles.saleae.com/logic-analyzers/logic-analyzer-vs.-oscilloscope>



Example of an oscilloscope displaying a sine wave and overshoot on two channels

<https://articles.saleae.com/logic-analyzers/logic-analyzer-vs.-oscilloscope>



Example of a logic analyzer displaying digital signals on six channels



References:

<https://docs.amd.com/r/en-US/ug908-vivado-programming-debugging/ILA>

<https://docs.amd.com/r/en-US/ug936-vivado-tutorial-programming-debugging/Target-Board-and-Server-Set-Up>

EE354L Detour lab

https://ece-classes.usc.edu/ee254/ee254l_lab_manual/detour_signal_schematic/ee354l_detour_rev7.pdf

EE201L Detour lab (original)

	GL	G1	G2	GR
Idle State	<○○	○○	○○	○○>
R1 State (G1 is ON)	<○○	●●	○○	○○>
R12 State (G1, G2 are ON)	<○○	●●	●●	○○>
R123 State (G1, G2, GR are ON)	<○○	●●	●●	●●>
Idle State	<○○	○○	○○	○○>
L1 State (G2 is ON)	<○○	○○	●●	○○>
L12 State (G2, G1 are ON)	<○○	●●	●●	○○>
L123 State (G2, G1, GL are ON)	<●●	●●	●●	○○>

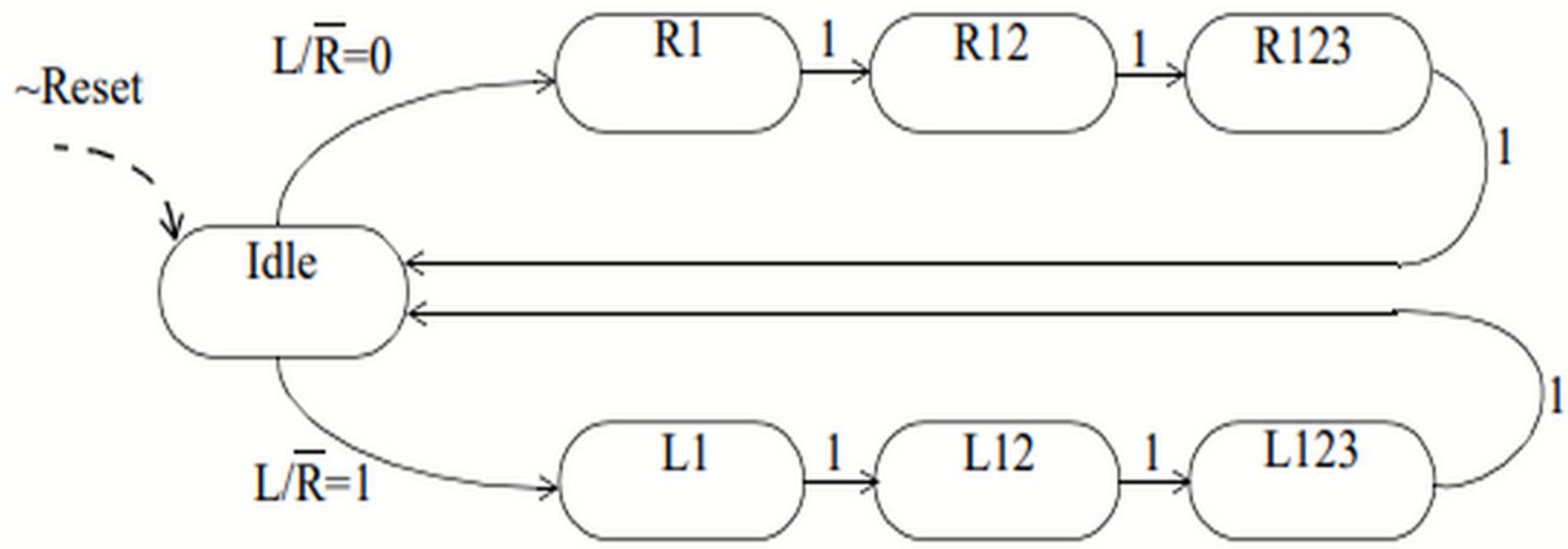
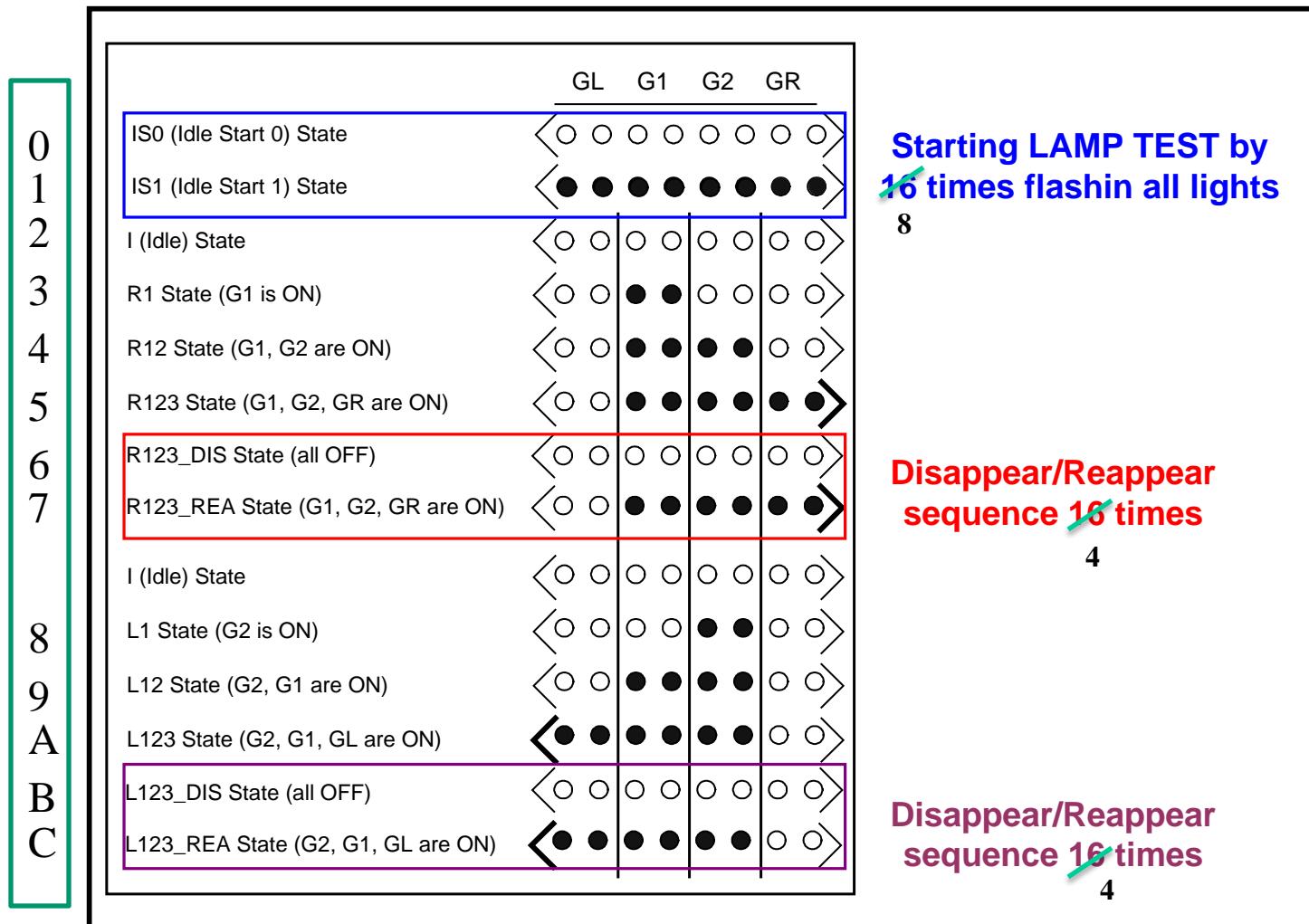
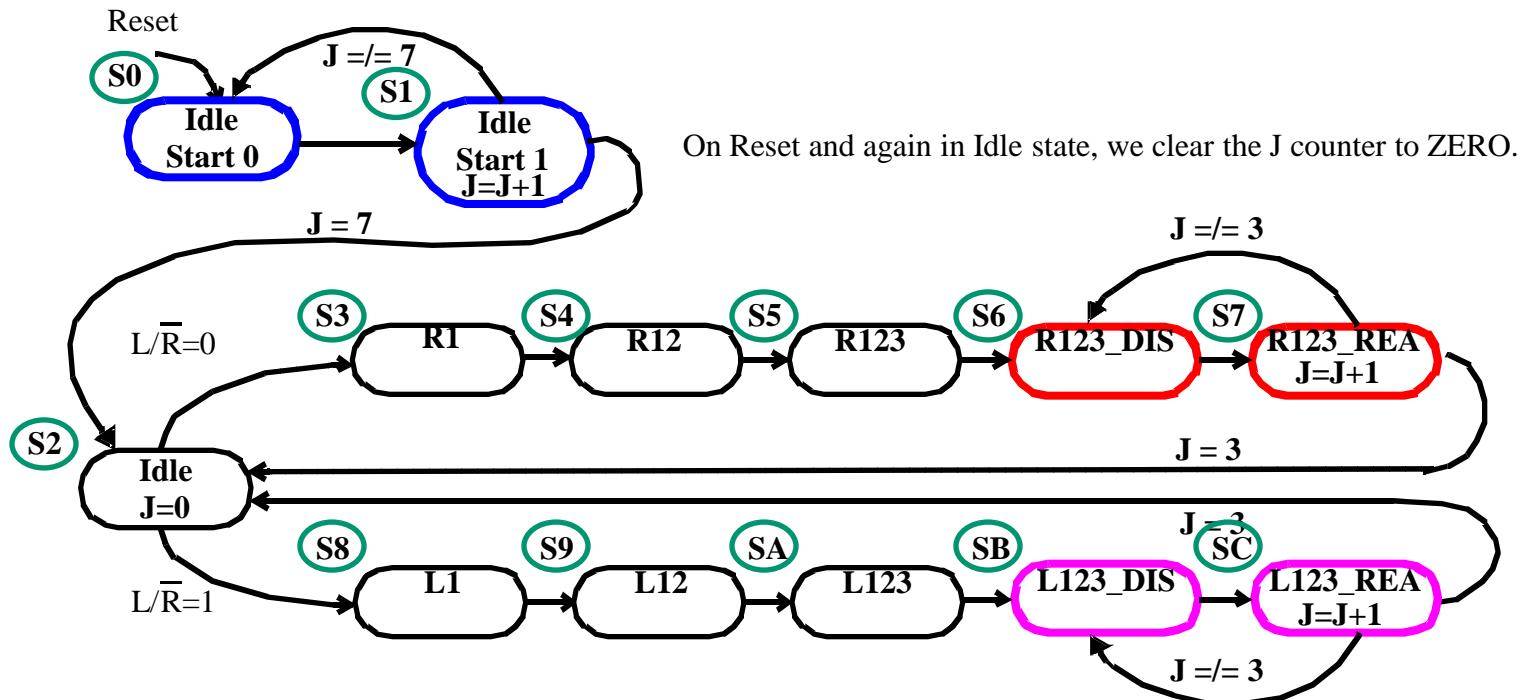


Fig 2: State diagram for the Detour Signal design

EE201L Detour lab (modified)



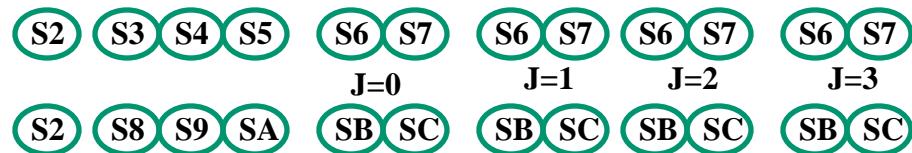
Modified Detour lab state diagram



During Reset it remains in **S0** state.

After Reset, it does **S0** **S1** eight times.

Then it does one of the two depending upon L/R.



ChipScope Pro Analyzer [detour_top]

File View JTAG Chain Device Trigger Setup Waveform Window Help

Trigger Run Mode: Single

Project: detour_top

JTAG Chain

- DEV:0 MyDevice0 (XC6SLX45)
 - UNIT:0 MyILA0 (ILA)
 - Trigger Setup
 - Waveform
 - Listing
 - Bus Plot

Signals: DEV: 0 UNIT: 0

- Data Port
 - /detour_1/detour_signals
 - /detour_1/J
 - /state_encoded
 - CH: 0 /divclk<25>
 - CH: 13 /sw1_IBUF
 - CH: 14 /sw2_IBUF
 - CH: 15 /sw3_IBUF
- Trigger Ports
 - TriggerPort0
 - TriggerPort1
 - TriggerPort2
 - TriggerPort3
 - TriggerPort4
 - TriggerPort5

Trigger Setup - DEV:0 MyDevice0 (XC6SLX45) UNIT:0 MyILA0 (ILA)

Match Unit	Function	Value	Radix	Counter
M0:TriggerPort0	==	XXXX	Bin	disabled
M1:TriggerPort1	==	1	Bin	disabled
/sw1_IBUF		1		
M2:TriggerPort2	==	1	Bin	disabled
/sw2_IBUF		1		
M3:TriggerPort3	==	1	Bin	disabled
/sw3_IBUF		1		
M4:TriggerPort4	==	1	Bin	disabled
/sw4_IBUF		1		
M5:TriggerPort5	==	XXX	Bin	disabled

Add Active Trigger Condition Name Trigger Condition Equation

TriggerCondition0 M1 --> !M1 --> M2 --> !M2 --> M3 --> !M3

Trig Type: Window Windows: 1 Depth: 64 Position: 39

Capture Storage Qualification: M4

Sample Buffer is full, slow or stopped clock IDLE

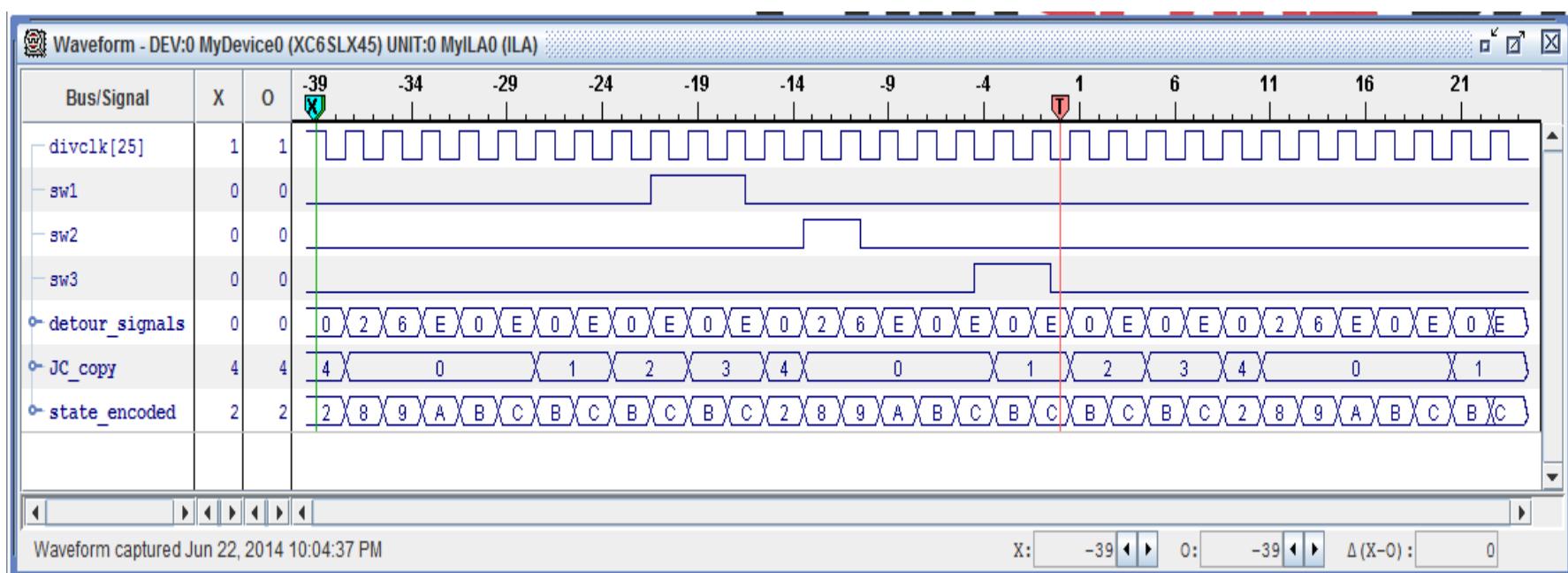
Waveform - DEV:0 MyDevice0 (XC6SLX45) UNIT:0 MyILA0 (ILA)

Bus/Signal	X	O	-39	-34	-29	-24	-19	-14	-9	-4	1	6	11	16	21
/divclk<25>	0	1	1	0	1	0	1	0	1	0	1	1	0	1	0
/sw1_IBUF	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0
/sw2_IBUF	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0
/sw3_IBUF	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0
/detour_1/d...	6	0	E	0	2	6	E	0	E	0	2	6	E	0	E
/detour_1/J	0	1	3	4	0	1	2	3	4	0	1	2	3	4	0
/state_encoded	9	B	C	2	8	9	A	B	C	B	C	B	C	B	C

Waveform captured Mar 25, 2013 12:09:53 AM X: -7 O: 0 Δ (X-O) : -7

Final Result!

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Some advanced topics

- Sampling on Rising or Falling edge
- Different Match Units
- Complex Trigger Conditions
- Virtual I/O

Can you see the clock?

- You can NOT see the **sampling clock!**
- To see **system clock** on the waveform, you need to use a trigger clock (sampling clock) with **higher frequency** (higher than the system clock, at least **double**).
- Most designers do not need to see the clock!

Sample on Rising or Falling edge?

- Ideally we should sample once per clock at the significant edge of the clock.
- Same edge sampling → The Sampling process should not introduce delay. You should capture data at *or just before the significant edge*, **not** just after the significant edge. *If it is just after the edge, you will be capturing data in transition (data in turmoil) !*

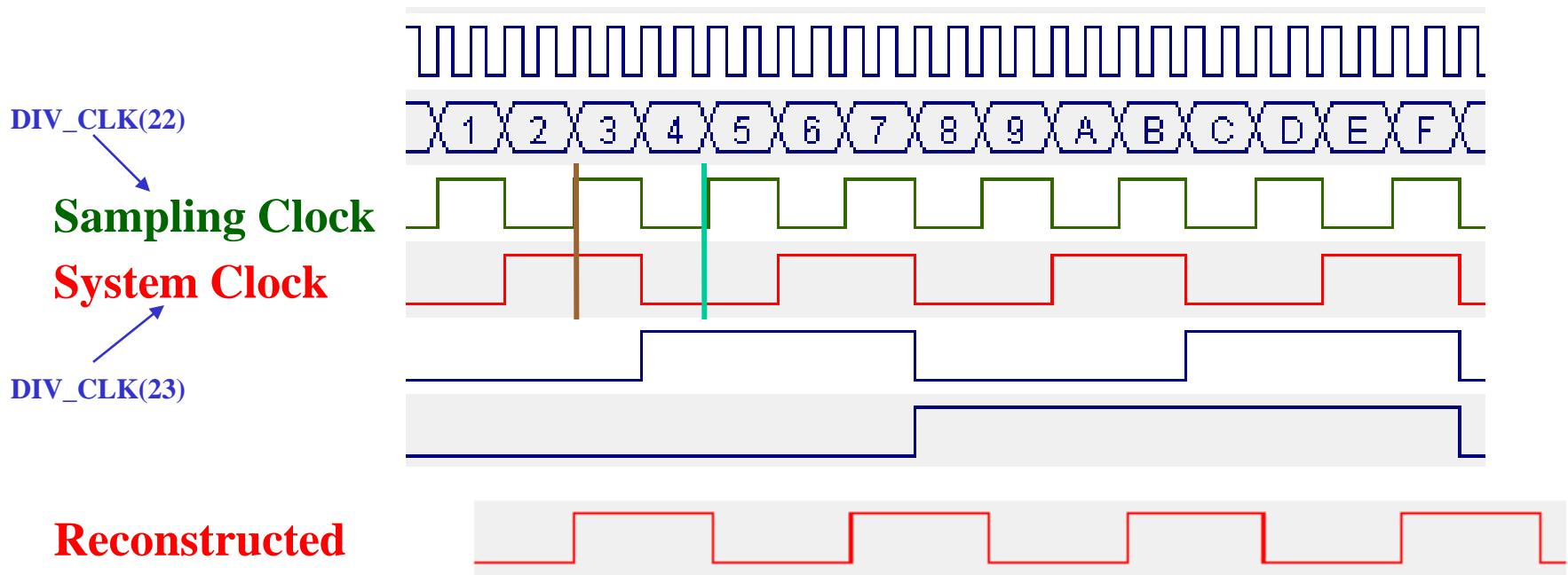
Sample on Rising or Falling edge?

in this detour demo for EE354L and EE560

- Here/we are sampling using high-speed clock (higher speed than the system clock). Actually double the clock rate.
- Here we are running at a low speed
- So it *safer* to sample somewhere in the middle of the clock.

Sample on Rising or Falling edge?

Two middles (one-fourth and three-fourth points) of the system clock coincide with the RISING edge of the high-speed clock.



Procedure to add an ILA IP to your project:

1. It is better to complete your design first without a chipscope (without and ILA debug probe)

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2. Then add an ILA core from the IP Catalog.
Search for ILA.



3. Configure the ILA to suit your needs.

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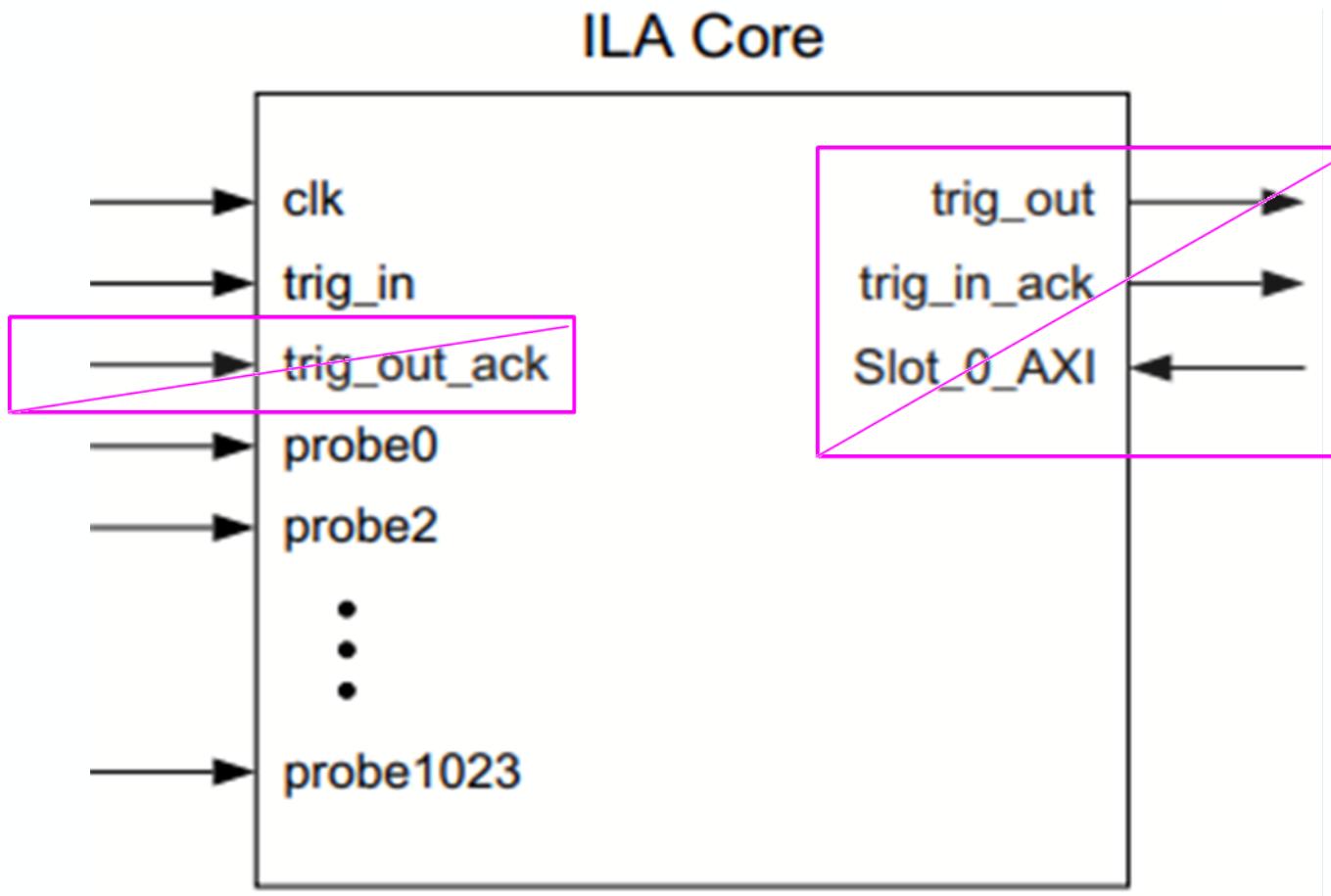


Figure 1-1: ILA Core Symbol

