~~June 14, 2020~~

10/25/2024

A simple quick revision was done on 10/25/2024.

Chipscope_Intro_using_Vivado_ILA.pdf

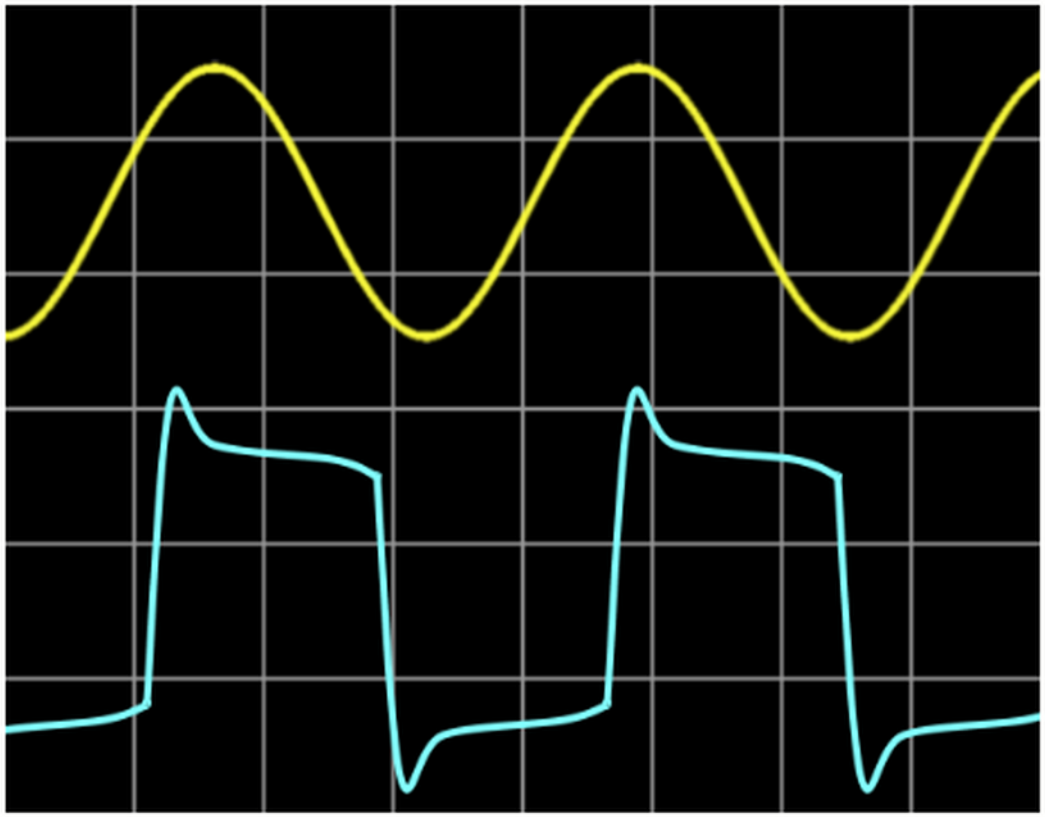
ILA = Integrated Logic analyzer

Logic Analyzer
and
On-Chip Logic Analyzer

- **Logic Analyzer** **vs.** **Oscilloscope**
  - **Digital** **Analog**
  - **32/64/128/256 channels** **2 or 4 channels**
  - **Trigger and Storage qualifications** **Simple trigger**

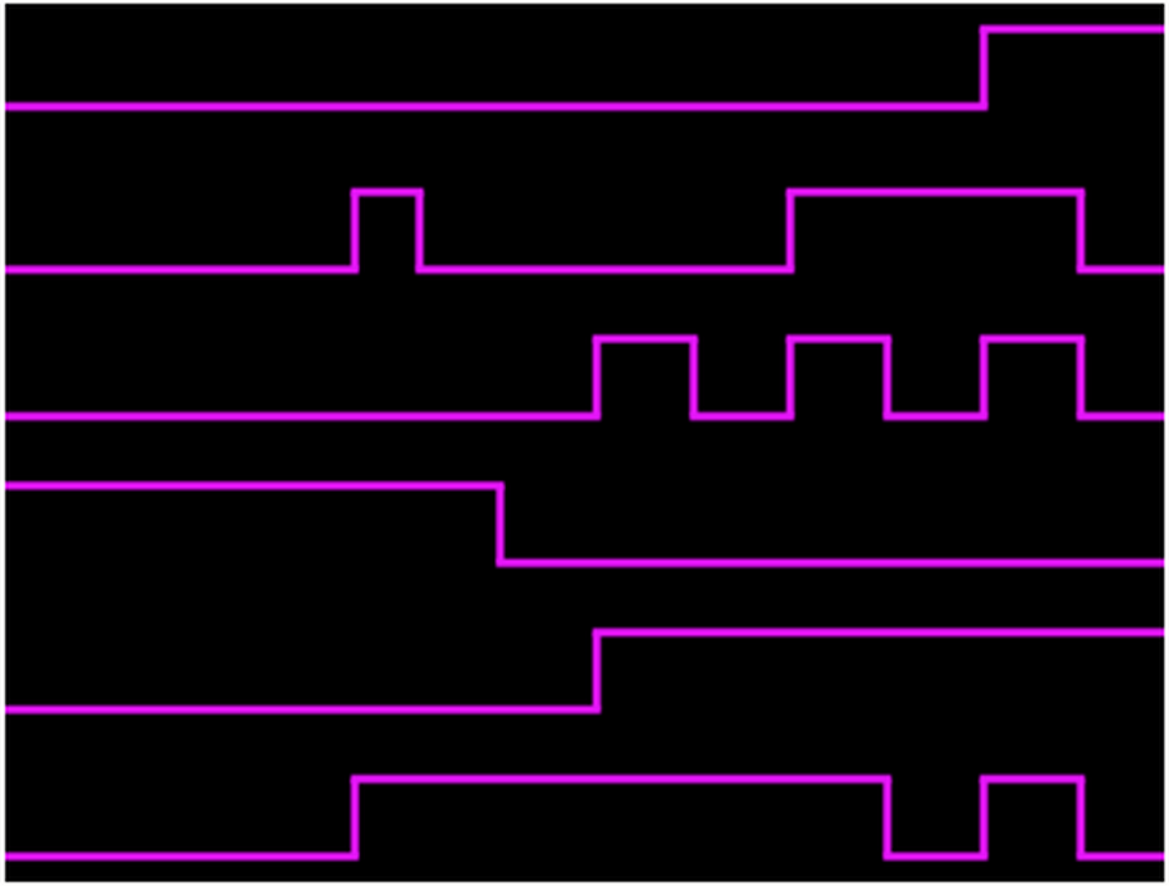
- **SoC (System on Chip) and Embedded Processors in SoC**

https://articles.saleae.com/logic-analyzers/logic-analyzer-vs.-oscilloscope



Example of an oscilloscope displaying a sine wave and overshoot on two channels

https://articles.saleae.com/logic-analyzers/logic-analyzer-vs.-oscilloscope



Example of a logic analyzer displaying digital signals on six channels

References:

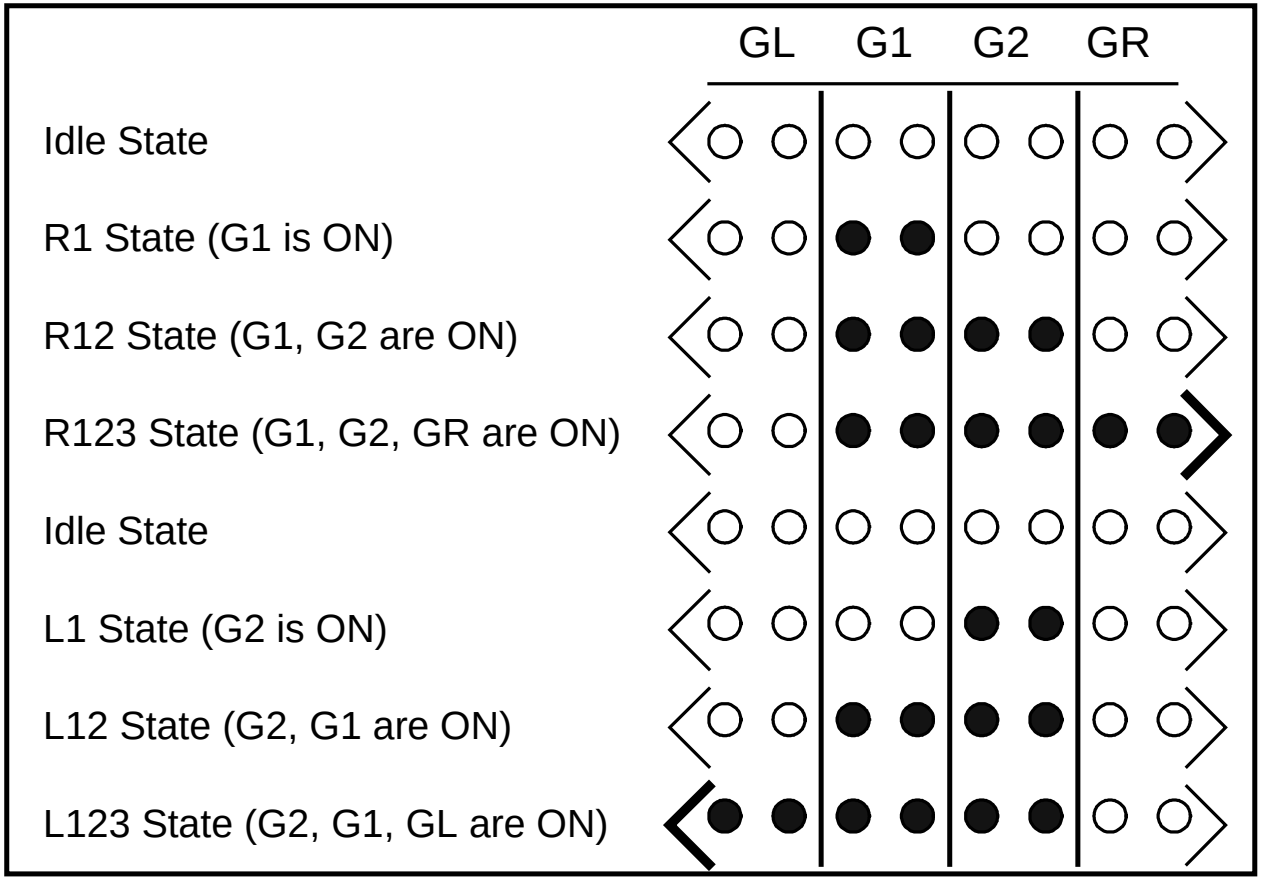
https://docs.amd.com/r/en-US/ug908-vivado-programming-debugging/ILA

https://docs.amd.com/r/en-US/ug936-vivado-tutorial-programming-debugging/Target-Board-and-Server-Set-Up

EE354L Detour lab

https://ece-classes.usc.edu/ee254/ee254l_lab_manual/detour_signal_schematic/ee354l_detour_rev7.pdf

EE201L Detour lab (original)



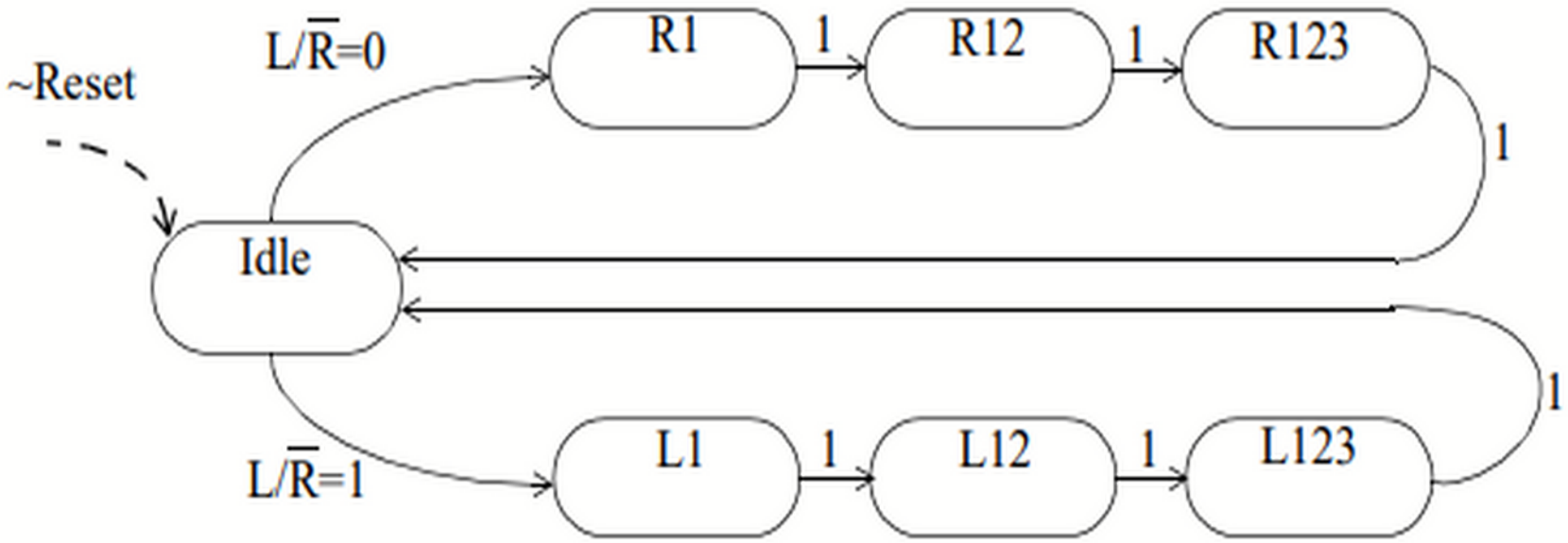
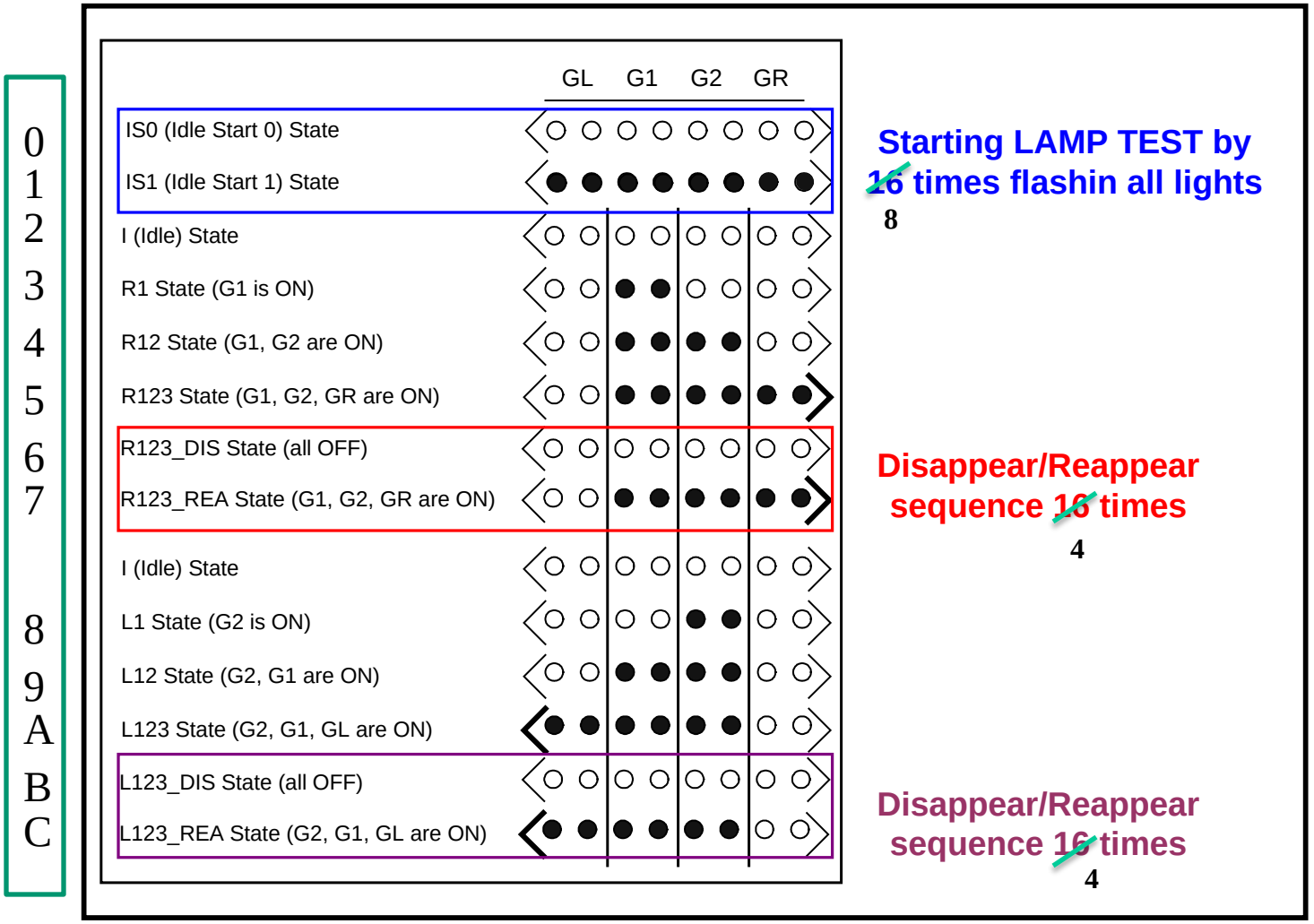
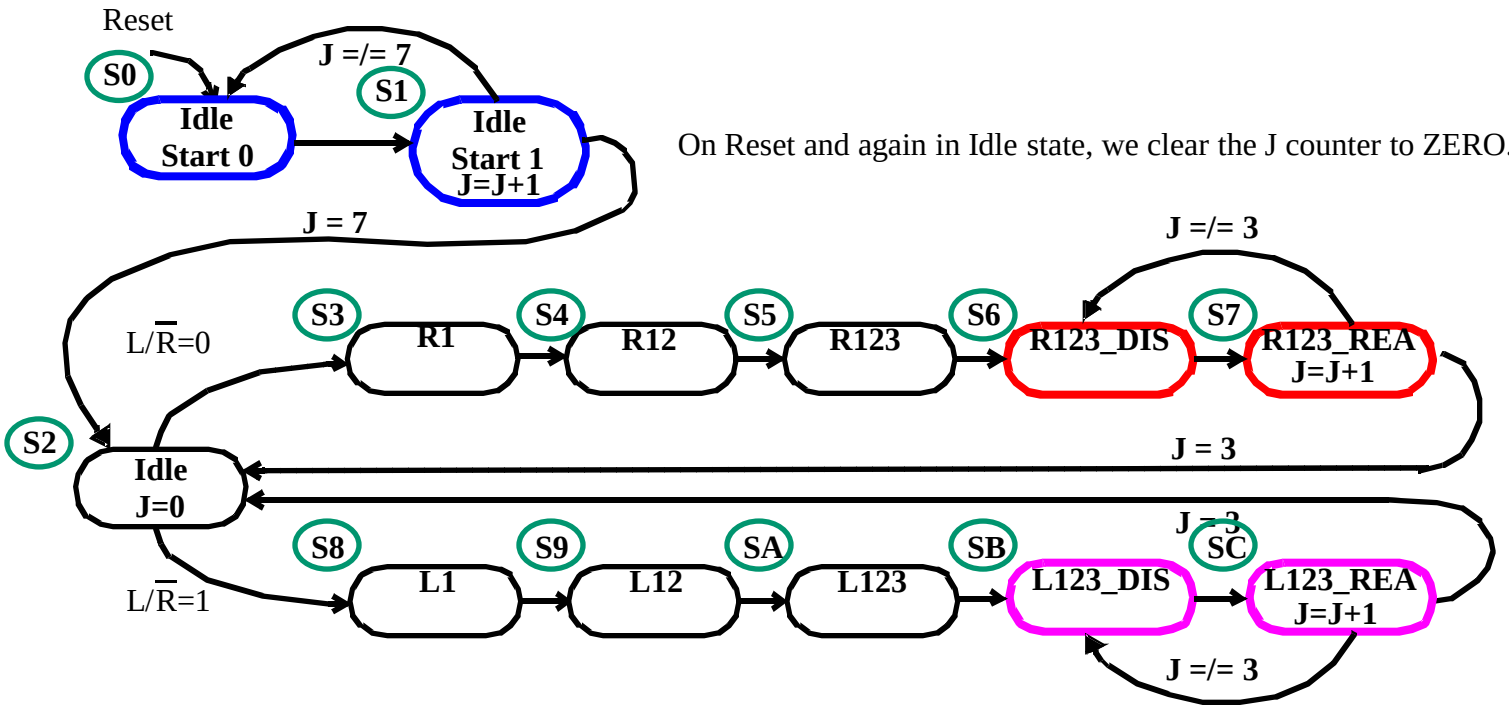


Fig 2: State diagram for the Detour Signal design

EE201L Detour lab (modified)



Modified Detour lab state diagram

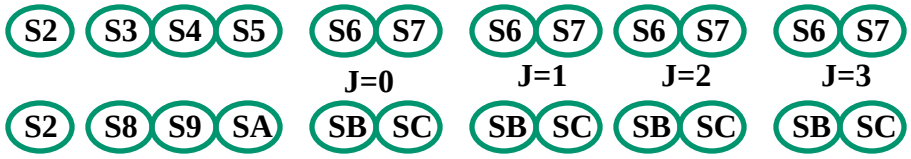


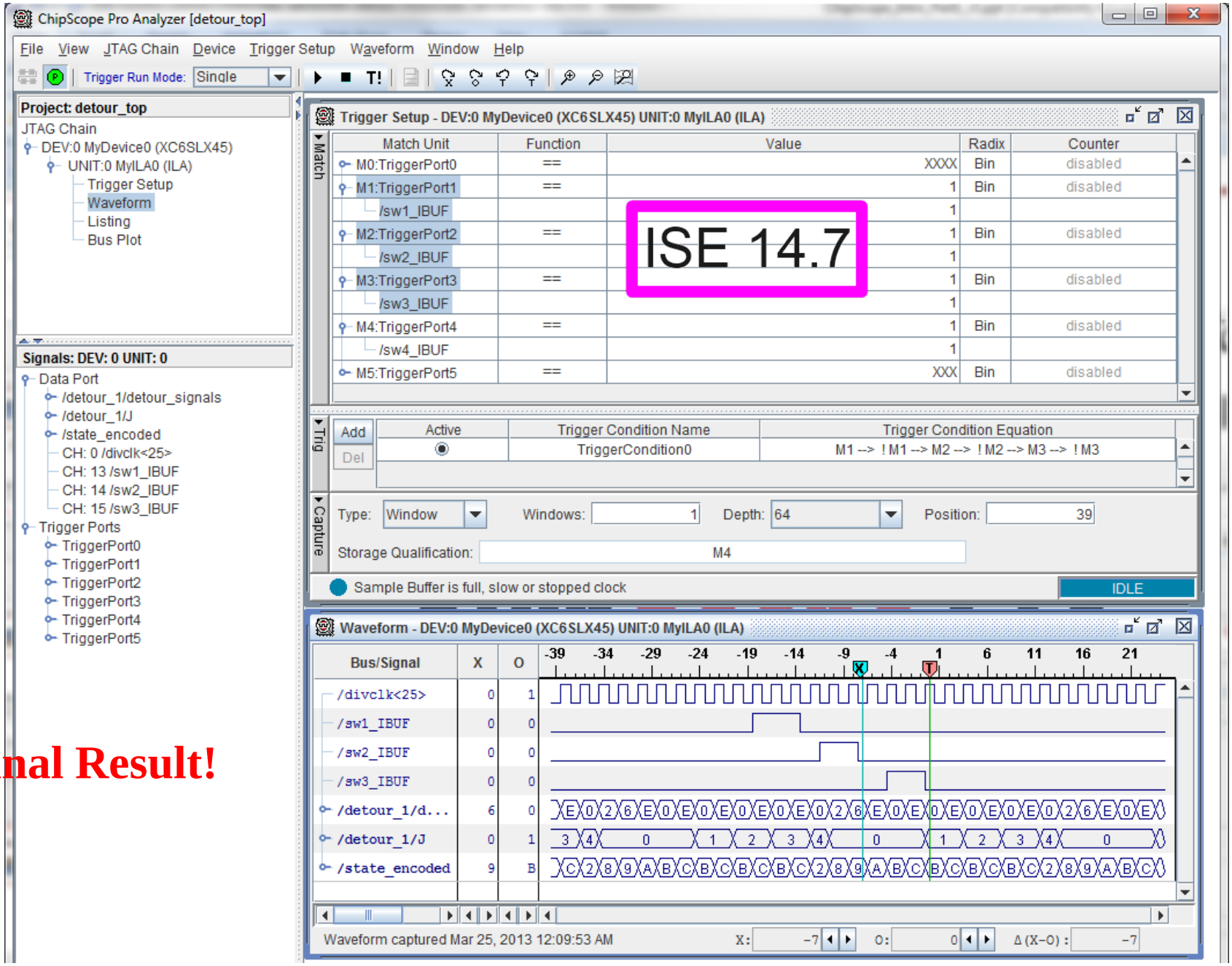
On Reset and again in Idle state, we clear the J counter to ZERO.

During Reset it remains in **S0** state.

After Reset, it does **S0** **S1** eight times.

Then it does one of the two depending upon $\overline{L/R}$.





Final Result!

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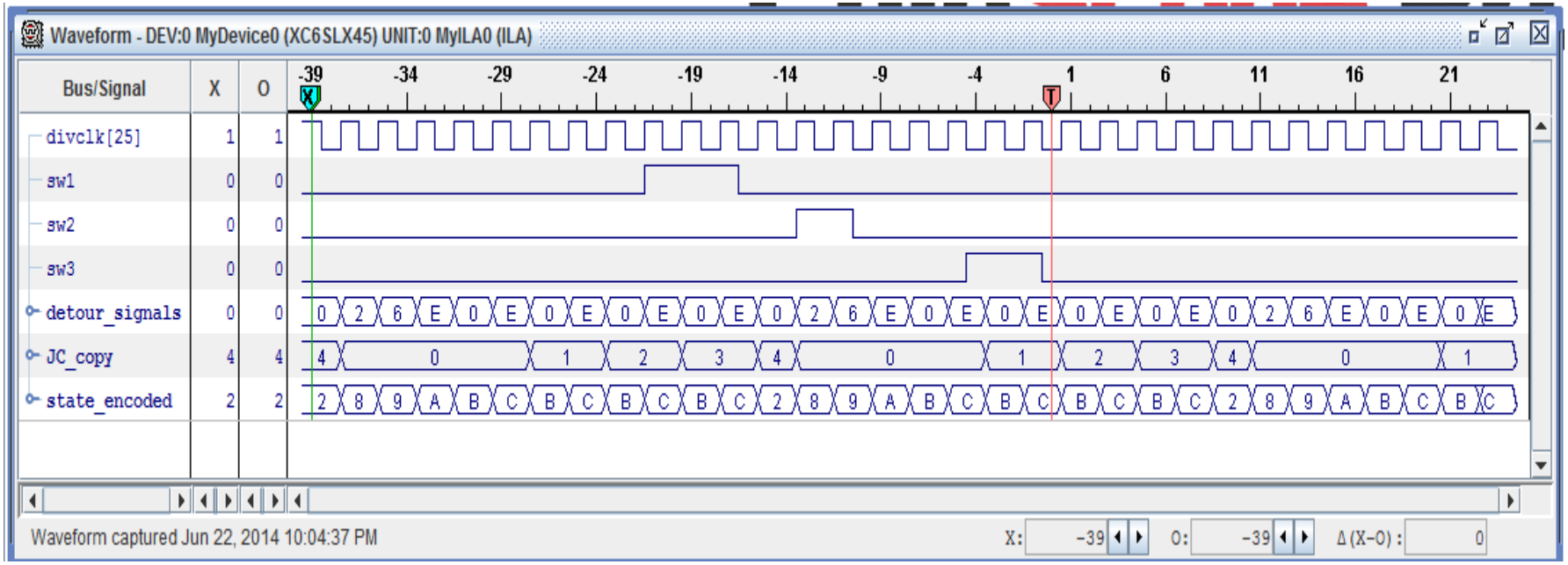

Waveform - DEV:0 MyDevice0 (XC6SLX45) UNIT:0 MyILA0 (ILA)
Bus/Signal
X
O
-39
-34
-29
-24
-19
-14
-9
-4
1
6
11
16
21
divclk[25]
sw1
sw2
sw3
detour_signals
JC_copy
state_encoded
Waveform captured Jun 22, 2014 10:04:37 PM
X: -39
O: -39
Δ(X-O): 0

Some advanced topics

- Sampling on Rising or Falling edge
- Different Match Units
- Complex Trigger Conditions
- Virtual I/O

Can you see the clock?

- You can NOT see the **sampling clock**!
- To see **system clock** on the waveform, you need to use a trigger clock (sampling clock) with **higher frequency** (higher than the system clock, at least **double**).
- Most designers do not need to see the clock!

Sample on Rising or Falling edge?

- Ideally we should sample once per clock at the significant edge of the clock.

- Same edge sampling ➔ The Sampling process should not introduce delay. You should capture data at *or just before the significant edge*, **not** just after the significant edge. *If it is just after the edge, you will be capturing data in transition (data in turmoil) !*

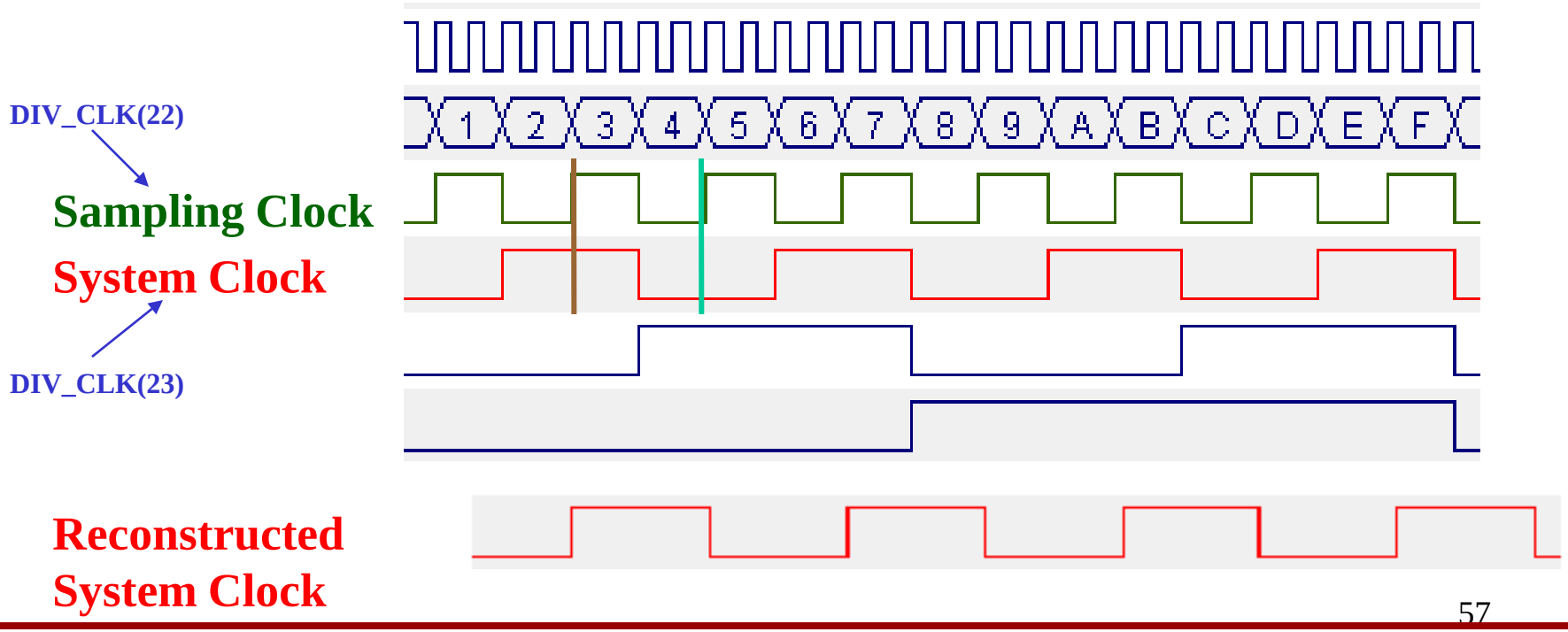
Sample on Rising or Falling edge?

in this detour demo for EE354L and EE560

- Here/we are sampling using high-speed clock (higher speed than the system clock). Actually double the clock rate.
- Here we are running at a low speed
- So it ***safer*** to sample somewhere in the middle of the clock.

Sample on Rising or Falling edge?

Two middles (one-fourth and three-fourth points) of the system clock coincide with the RISING edge of the high-speed clock.

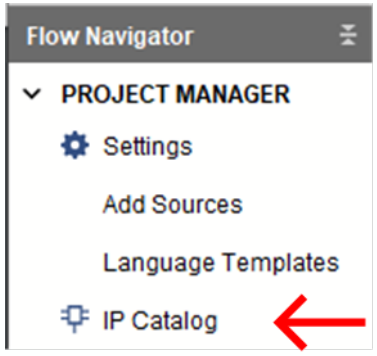


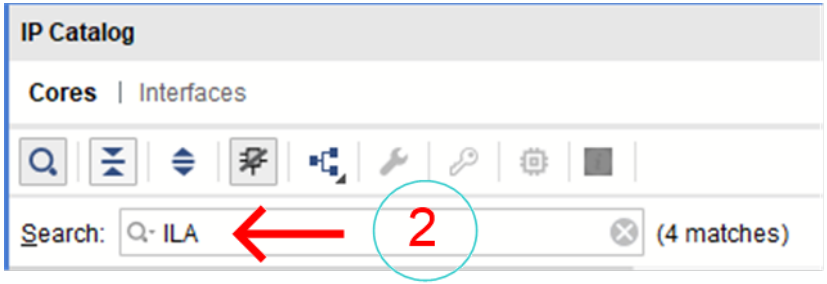
Procedure to add an ILA IP to your project:

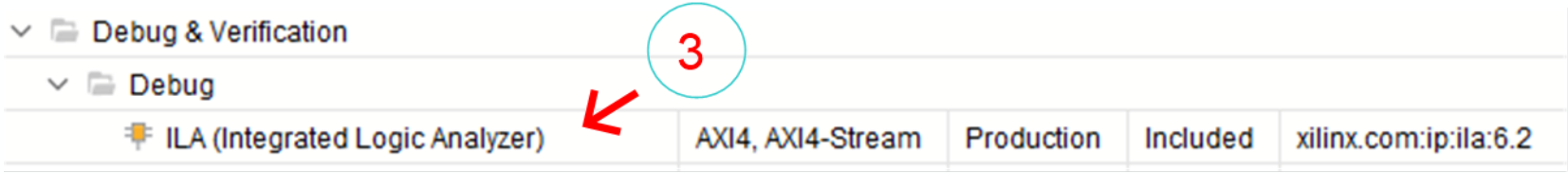
1. It is better to complete your design first without a chipscope (without and ILA debug probe)

ISE 14.7

2. Then add an ILA core from the IP Catalog. Search for ILA.







3. Configure the ILA to suit your needs.

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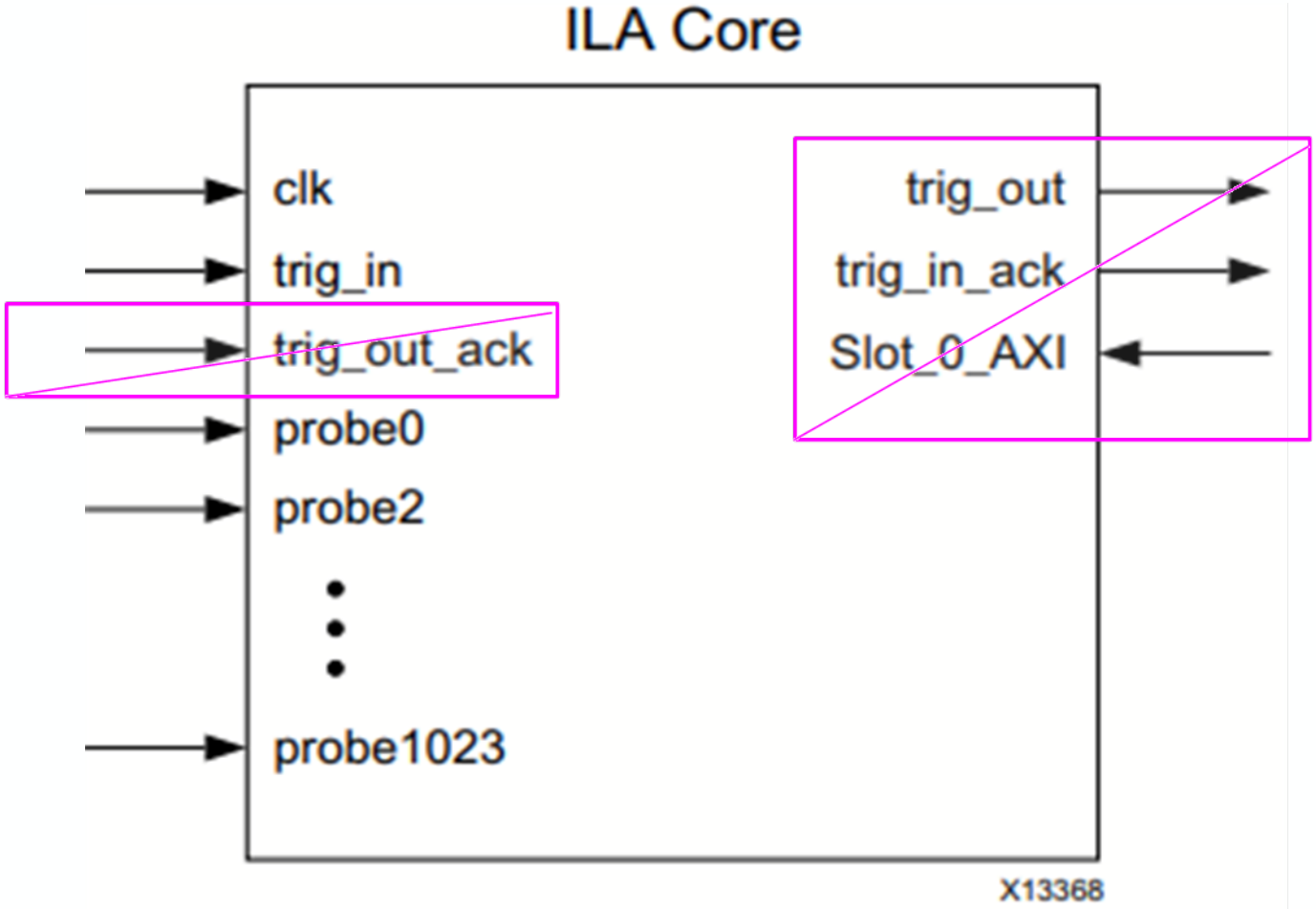

Figure 1-1: **ILA Core Symbol**