Computer Organization / Professor H. Roumani

Lab-L

The Question

1. Create a working directory for this exercise.
2. Store your `cpu.v` in that same directory.
3. Create a file in the working directory named **Engine.v**. Note that the name has to be **exactly** like this or else your submission will not be marked.
4. Copy and paste the code fragment at the bottom of this page to the newly created file.
5. Complete the development of the file such that:
   - You use only structural synthesis; i.e. you just instantiate circuits and connect wires (no blocks, no operators, nothing procedural).
   - You use one, **and only one**, instance of the 32-bit adder in your cpu.v file.
   - The output z is equal to the input times 3. For example, if a=5 then z should be 15, and if a=-5 then z should be -15.
6. Assume that the signals on the busses represent *signed* integers. If the product doesn't fit in 32 bits then it should wrap around the signed range as usual.

Hint: in order to multiply by 3 using only one adder you may be want to benefit from the fact that multiplying by 2 can be done without using any adder!

Testing

It is strongly recommended that you also write (but don't submit) a testing module (e.g. Prog.v) in which you instantiate `Engine`, supply some inputs to it, capture its output, and then determine if it behaves as expected. To compile all three files, use:

```
iverilog Prog.v Engine.v cpu.v
```

This is in fact how your submitted module will be marked.

Submitting Your Work

1. Issue the following command from the working directory:

   ```
   submit 2021 LabL_Tue Engine.v
   ```

2. Note that every submission you make **overwrites** the content and the timestamp of any previous one; i.e. we only keep the very last file you submit.

3. This test is **40 minute** long.

The Code Fragment

Copy and paste this fragment into the file to be submitted:

```
module Engine(z, a);
output [31:0] z;
input [31:0] a;

...

endmodule
```

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