Computer Organization / Professor H. Roumani

Lab-K

The Question

1. Create a working directory for this exercise.
2. Create a file in the working directory named **Engine.v**. Note that the name has to be **exactly** like this or else your submission will not be marked.
3. Copy and paste the code fragment at the bottom of this page to the newly created file.
4. Complete the development of the file such that it implements this circuit:

The engine circuit is combinational (no memory) and its 1-bit output z derives from its two 2-bit inputs a and b in accordance with this logic:

```
if (a == 3)
   z = b[0]; // i.e. the rightmost bit of b
else
   z = rm(a, b);
```

where rm is a ready-made circuit whose module has the following header:

```
module rm(out, in1, in2);
output out;
input[1:0] in1, in2;
```

The *rm* circuit computes the `or` of all 4 of its input wires (i.e. the 2 in `in1` and the 2 in `in2`). You don't need to implement *rm* since it has already been written and is part of iverilog's library. You can simply instantiate it and use it just like any of the basic gates.

5. Note also that your module should contain no initial or any other block within it. It should only involve instantiation of circuits and connections of wires.

Testing

It is strongly recommended that you also write (but don't submit) a testing module (e.g. Prog.v) in which you instantiate `Engine`, supply some inputs to it, capture its output, and then determine if it behaves as expected. This is in fact how your submitted module will be tested.

Submitting Your Work

1. Issue the following command from the working directory:

```
submit 2021 LabK_Tue Engine.v
```

2. Note that every submission you make **overwrites** the content and the timestamp of any previous one; i.e. we only keep the very last file you submit.

3. This test is **40 minute** long.

The Code Fragment

Copy and paste this fragment into the file to be submitted:

```
module Engine(z, a, b);
output z;
input[1:0] a, b;

...

endmodule
```

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