NCTU-EE IC LAB – Spring 2021

Lab05 Practice

Design: Queue and Stack

Data Preparation

1. Extract files from TA's directory:
   % tar xvf ~iclabta01/Lab05.tar
2. The extracted LAB directory contains:
   a. Practice/
   b. Exercise/

Design Description

In this practice, you need to simulate queue and stack. Inputs include random number(1~10) of data and action defining which data structure to use. Then you should output data which order depends on the data structure. This practice must be done by memory.

Inputs

Input	Bit Width	Definition and Description
clk	1	The clock signal will be in this signal path.
rst_n	1	Negative reset signal will be in this signal path.
in_valid	1	Validity of input signals.
in_data	8	Data to be stored.
action	1	The signal will be given at the first cycle of **in_valid**. The definition is as following: **0**: Queue. **1**: Stack.

Outputs

Output	Bit Width	Definition and Description
out_valid	1	Validity of out_data. 1'b0: out_data is not ready. 1'b1: out_data is ready.
out_data	8	Data pop from memory.

Specifications

1. Top module name: QS (design file name: QS.v)
2. **It is asynchronous reset and active-low architecture. If you use synchronous reset (considering reset after clock starting) in your design, you may fail to reset signals.**
3. **The reset signal (rst_n) would be given only once at the beginning of simulation. All output signals should be reset after the reset signal is asserted.**
4. The execution latency is limited in **5 cycles**. The latency is the clock cycles between the falling edge of the last **in_valid** and the rising edge of the first **out_valid**.
5. The clock period is **5 ns.**
6. The input delay is set to **0.5*(clock period)**.
7. The output delay is set to **0.5*(clock period)**, and the output loading is set to **0.05**.
8. The synthesis result of data type **cannot** include any **latches**.
9. The gate level simulation cannot include any timing violations without the *notimingcheck* command.
10. After synthesis, you can check QS.area and QS.timing. The area report is valid when the slack in the end of timing report should be **non-negative**.

Note

1. **Template folders and reference commands:**

   01_RTL/ (RTL simulation) **./01_run**

   02_SYN/ (Synthesis) **./01_run_dc**

   (Check if there is any **latch** in your design in **syn.log)**

   (Check the timing of design in /Report/QS**.timing**)

   (Check memory is used in /Report/QS**.area**)

   03_GATE / (Gate-level simulation) **./01_run**

   04_MEM/ (Memory location)

   (In practice, memory files are provided)

2. **Check memory is used in your design:**

   If you have use memory in your design, you can find "**Macro/Black Box area**" in area file after synthesis step.

```
Macro/Black Box area:          441686.250000
```

Example Waveform

Input and output signal: