

JIALE YAN

CURRENT STATUS

Digital IC Designer
Shanghai, 200120, P.R. China

CONTACT INFORMATION

yanjiale0317@gmail.com
(+86) 13671386517

EDUCATION

Tsinghua University (THU)
Beijing, P.R. China

Sep. 2016 - Jul. 2019

Rank 13/45 in the Institute of Microelectronics
Master in Integrated Circuit Engineering

Dissertation: Research on Key Technologies of Energy Efficient and Reconfigurable Accelerator for Generative Neural Networks, advised by Prof. Shouyi Yin

Harbin Institute of Technology (HIT)
Harbin, P.R. China

Sep. 2012 - Jun. 2016

Rank 3/93 in the School of Electronic Engineering
B.S. in Electronic Science and Technology

RESEARCH INTERESTS

Computer Architecture, Deep Learning, Approximate Computing, Reconfigurable Computing

PROJECT EXPERIENCE

Project: GNA

In THU

I have designed a reconfigurable and efficient accelerator for generative networks named GNA, which includes intra-PE processing, inter-PE processing and cross-layer scheduling techniques. I propose a dual convolution mapping method for CONV and DeCONV layers, and a cross-layer scheduling method for residual blocks. Owing to the proposed optimization, the GNA achieves high PE utilization and energy efficiency.

Work Experiences

After Graduation July. 2019 -

Project: Neural Network Quantization

I have some experiences about the quantization for the neural network. I propose an AutoML method for quantization by using the genetic algorithm to optimize the network's architecture parameters, for example the number of channel. Finally, the network's performance and accuracy improves in segmentation tasks.

Project: Ray Tracing in GPU (in work)

Now I focus on a new field about GPU in my daily work.

PUBLICATIONS

- [TCAD'18] **J. Yan**, S. Yin, F. Tu, L. Liu, S. Wei, "GNA: Reconfigurable and Efficient Architecture for Generative Network Acceleration," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2018.
- [SciChina'19] **Yan J L**, Zhang Y, Tu F B, et al. Research on low-power neural network computing accelerator (in Chinese). Sci SinInform, 2019, 49: 314–333.

HONORS AND AWARDS

Competition Awards

The 2nd Price in China Postgraduate Electronic Design Competition (Team Leader)	2017
The 3rd Price in National Post-Graduate Mathematical Contest in Modeling (Team Leader)	2017
The 3rd Price in National Competition of Transport Science and Technology	2015
The Honorable Mention in Mathematical Contest In Modeling Certificate of Achievement	2015
The 1st Price in Provincial Competition of National Mathematical Modeling Competition	2014

Honors

Provincial Excellent College Graduate	2016
HIT First Prize Scholarship (4 times)	2013, 2014, 2015, 2016
HIT Outstanding Student Cadre	2014
HIT Merit Student	2013

STUDENT WORK

2017-2018 Teacher Assistant in THU, two lessons "Industrial Frontiers" and "Computational Thinking"

<https://github.com/LouiValley/System-Design-in-Computational-Thinking-2018-Spring>

<https://github.com/LouiValley/Global-Industry-and-Technology-Strategy-2017>