Class D Full-Range Audio Power Amplifier

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Abstract

This audio amplifier is designed to amplify sounds across the entire audible frequency range. Its highly-efficient Class D architecture allows for significant reductions in size, weight, cost and power consumption.

What are Class D amplifiers and why are we making one?

Class D is a relatively new, highly power-efficient design for power amplifiers. This contrasts with conventional Class AB amplifiers which require more power and release more heat, for reasons which will be described below.

All amplifiers output a voltage which varies in time according to the input signal. The amount of power dissipated (wasted as heat) in an amplifier is determined by its output voltage as shown in Figure 1:

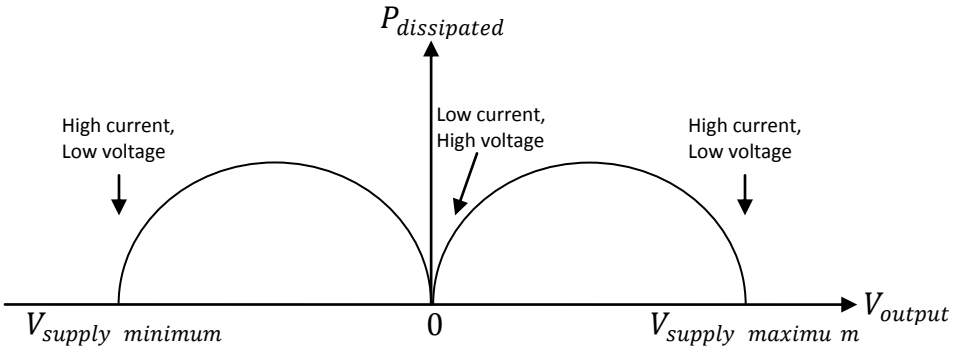

Figure 1: Relation of dissipated power to output voltage

This curve is caused by the push-pull transistor pair seen on the output stage of Class AB and Class D amplifiers. The dissipated power is the product of the voltage across each transistor and the current flowing through the transistor. When the output is zero, there is minimal current flowing through the transistors. When the output is at either maximum or minimum, there is lots of current flowing through one of the transistors but hardly any voltage across it. Hence the least power consumption is observed when the output voltage is either zero, maximum or minimum[1]. Class AB amplifiers deliver a continuous output voltage which frequently strays into the middle areas which cause the most wastage of power. This results in a power efficiency (defined as the ratio of audio power delivered to electrical power consumed) of up to 55%.

[1] James E. Solomon, "The Monolithic Operational Amplifier: A Tutorial Study", *IEEE Journal of Solid-State Circuits*, SC-9 (1974): 6, 4.

Class D amplifiers, however, do not output a continuous voltage. Instead they produce a rapid series of square voltage pulses which have either the maximum or minimum voltage. By controlling the width or frequency of these pulses, their average voltage can be controlled to resemble the intended output signal. This is analogous to quickly flickering a light bulb on and off so that it looks 50% dimmed. Since the amplifier outputs either the maximum or minimum voltage, the dissipated power is greatly reduced. The only times when significant power is consumed are during the rapid transitions between the maximum and minimum voltage. Finally, a low pass filter is employed to 'slow down' and average the voltage of the pulses, creating the desired continuous wave. It does this by storing energy when the pulse voltage is above the desired voltage and releasing energy when the pulse voltage is below the desired voltage[2].

Since less power is wasted, a much smaller power supply can be used. Power supplies generally contain the heaviest and costliest parts of any amplifier, particularly the large capacitors and transformer. This is what allows a Class D amplifier to be smaller, lighter, cheaper and less power-hungry than conventional designs of similar capability.

Being an audiophile, I was attracted to this project by the many clear advantages which Class D amplifiers have over other designs, particularly their extremely low output impedance which allows even very small Class D's to precisely control large subwoofers. Stereo Class D amplifiers also have very little cross-talk between channels due to the digitization of the amplified signal. Finally, I chose this project for the challenge of working with fairly high signal frequencies. This necessitates the design of very fast and compact circuitry.

[2] Conversations with Bill Walter of Linear Technologies.

The inner workings of the Class D amplifier

The first challenge to making a Class D amplifier is creating a series of pulses which average out to be the desired signal. I chose to make a Pulse-Width Modulated (PWM) amplifier where the voltage pulses have a width proportional to the voltage of the input signal. This is equivalent to saying that the width of each pulse should increase linearly with the magnitude of the input voltage. The simplest way to do this is to compare the voltage of the input signal with a very high speed triangle wave. The output is at maximum when the triangle wave's voltage is lower than the signal and at minimum when it is higher than the signal. This produces the required pulses, as shown below:

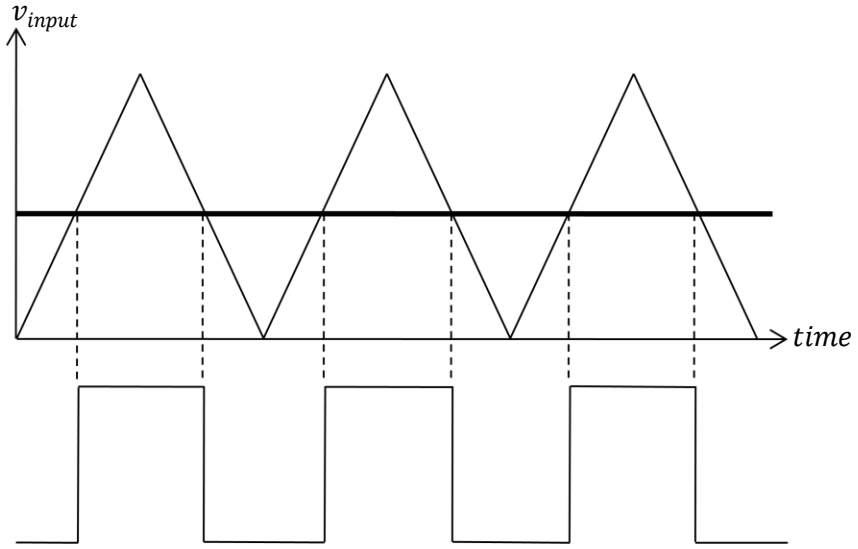

Figure 2:
55% input signal and corresponding 55% pulses

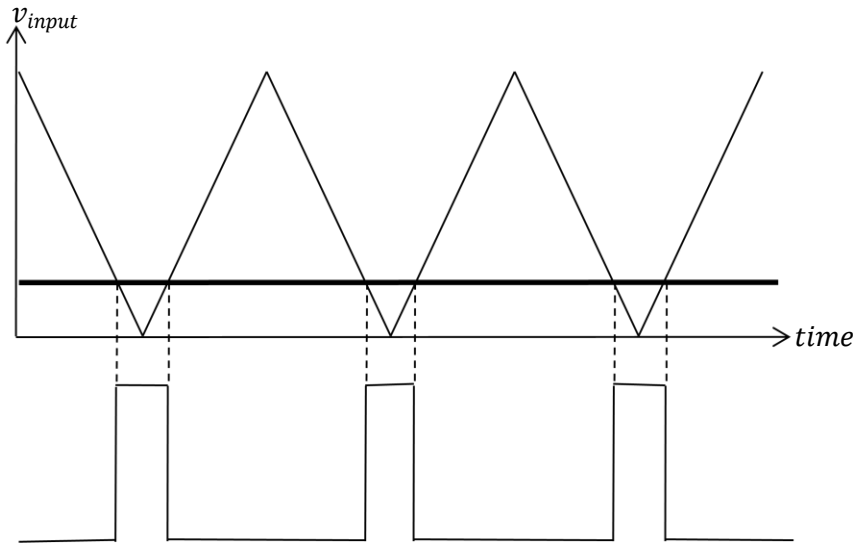

Figure 3:
15% input signal and corresponding 15% pulses

Once the pulses have been created, the next step is to produce duplicates of these pulses which have enough current to power the speaker. The best way to do this is using a MOSFET H-bridge, which consists of 4 MOSFETS used as switches in the configuration below:

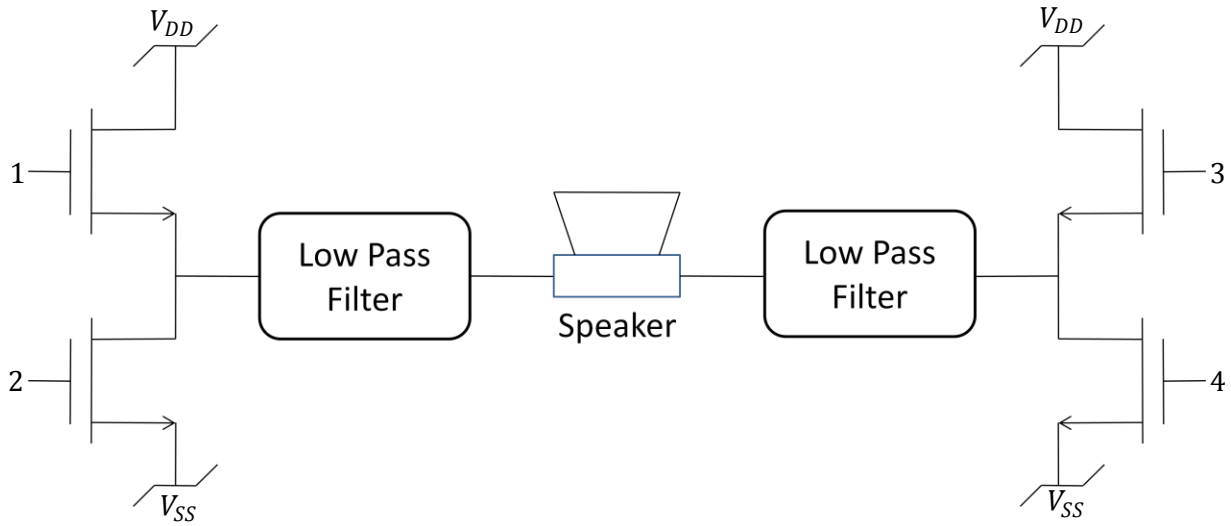

Figure 4: MOSFET H-Bridge

For high output voltage: Turn on 1 and 4, turn off 2 and 3.
For low output voltage: Turn on 2 and 3, turn off 1 and 4.

The problem with this configuration is during the moment when switching happens, MOSFETs 1 and 2 or MOSFETs 3 and 4 are both partially on for just a moment. This results in a phenomenon called 'shoot-through' where a dangerous pulse of current flows through the low-resistance path created by the two partially on MOSFETs, catastrophically damaging the circuit. My strategy to eliminate shoot-through is to turn off all the MOSFETs for just a moment between switching cycles. I create this delay by comparing two triangle waves to the input signal, where one triangle wave has a slightly higher voltage than the other[3]. This produces a pair of PWM signals. One is used to drive MOSFETs 1 and 4 whereas the other is used to drive MOSFETs 2 and 3. This mechanism is illustrated in Figure 5:

[3] Sergio Sánchez Moreno, *Class D Audio Amplifiers - Theory & Design* (ColdAmp Electronics, 2005)

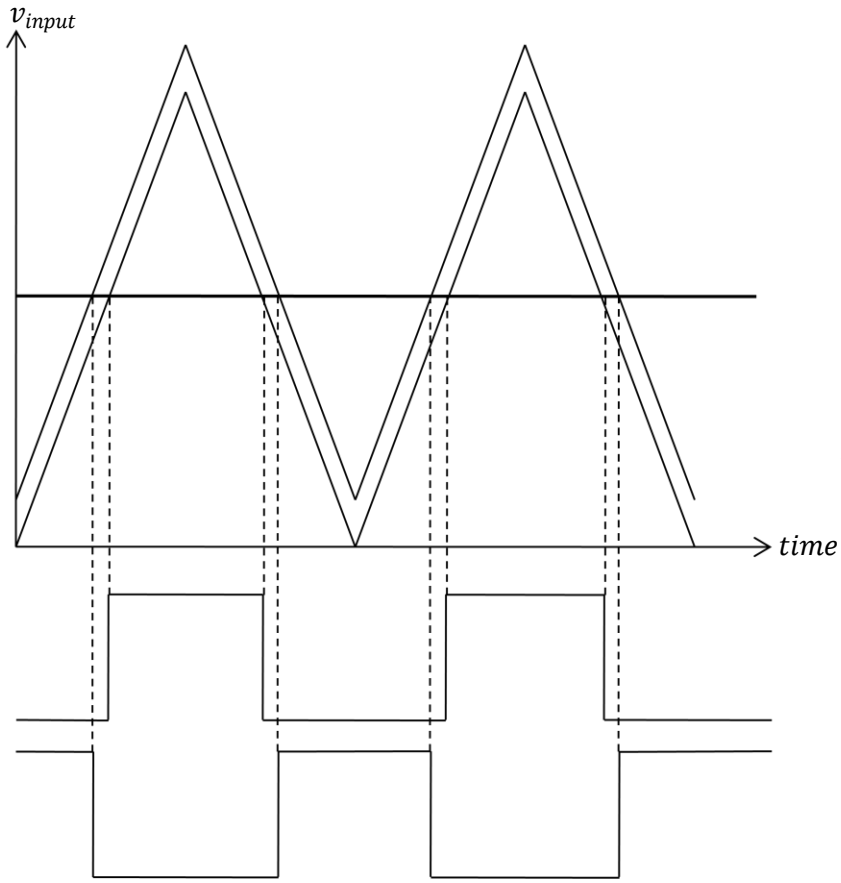

Figure 5:
Complementary MOSFET control waves with delay between waves.

Now that we have eliminated the shoot-through problem by introducing a delay, the width of the pulses is not exactly proportional to the input voltage. Even if we had not introduced the delay, imperfections in the circuitry would have ruined this proportionality. Hence we need to introduce an 'error-correcting' mechanism in the form of negative feedback to improve the accuracy of the amplifier's output. This is done by keeping a running sum of the 'total error' with an integrating circuit (where error is the proportional difference between the input and output signals of the amplifier) and minimizing this error by distorting the input signal being sent to the amplifier. This can be implemented as shown in Figure 6:

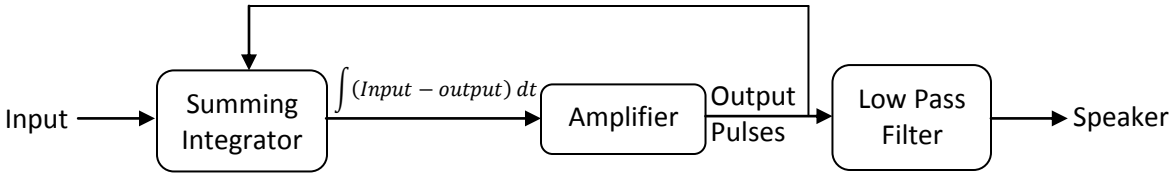

Figure 6: Block Diagram of Negative Feedback Path

Overview

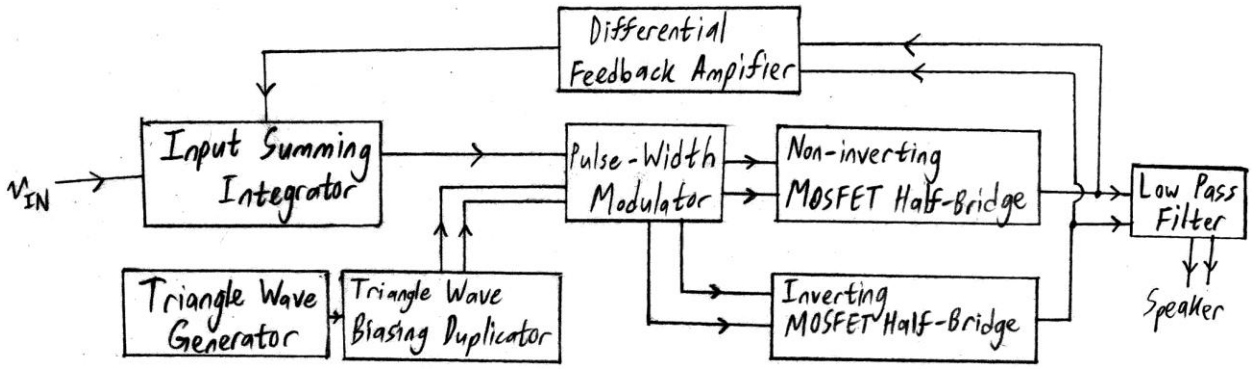

Figure 7: Block Diagram of Overall Circuit

Triangle Wave Generator **Page 9**

This circuit produces an accurate triangle wave at a fundamental frequency of 300 kHz.

Triangle Wave Biasing Duplicator **Page 11**

This circuit duplicates the triangle wave, adding a positive voltage offset to one and a negative voltage offset to the other.

Pulse Width Modulator (PWM) **Page 13**

This circuit compares the error-corrected input signal to the two triangle waves to produce two sets of pulses where one is slightly wider than the other.

MOSFET Half-Bridges **Page 14**

These identical circuits create a powerful, high-current duplicate of the PWM's weak pulses.

Low Pass Filter **Page 19**

The Low Pass Filter averages the output of the MOSFET half-bridges by slowing down the signal such that it resembles an audio signal. This audio signal is then sent directly to the driver.

Differential Feedback Amplifier **Page 21**

The differential feedback amplifier measures the voltage across the speaker's poles and sends this voltage back to the input summing integrator for comparison with the input signal.

Input Summing Integrator **Page 21**

This circuit compares the output of the amplifier to its input and stores a running total of the difference (the error) between the two. It then minimizes this difference by distorting the amplifier's input signal to compensate for the amplifier's non-linear amplification.

Individual Circuit Description & Analysis

NOTE: all op amps, comparators and logic ICs in the following diagrams have their power supplies bypassed with 150nF capacitors. The supply rails are at $\pm 14\text{V}$ unless stated otherwise.

Triangle Wave Generator

The triangle wave generator is the circuit which decides the speed at which all the other circuitry must run. As such, the frequency of the triangle wave must be chosen very carefully. The main considerations in this decision are the practical limits of filtering the switching noise from the output pulses. It is expensive to build a passive output filter which is higher than 2nd-order (which has a -40dB/decade cutoff), so the switching frequency should be at least an order of magnitude above the output filter cutoff frequency to be properly removed.

With these considerations in mind, I decided to place my output filter cutoff frequency at 30kHz (reasonably high above the 20kHz audio band). For the switching frequency to be attenuated by at least -40dB, I chose a triangle wave frequency of 300kHz, one order of magnitude above the 30kHz output filter cutoff.

My initial approach to designing the triangle wave generator was to build a square-wave integrator from one op amp and one comparator, as shown below:

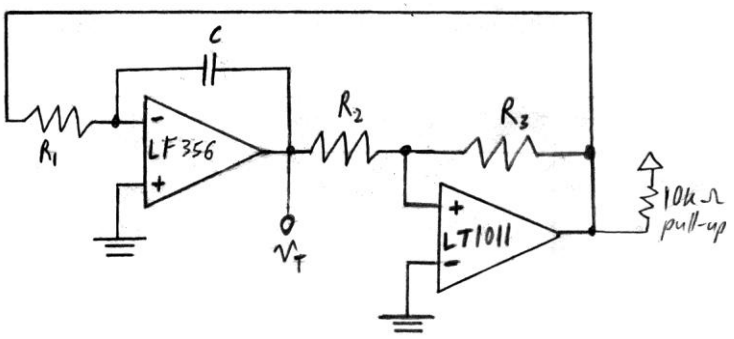

Figure 8: Triangle Wave generator built from discrete components

Unfortunately, due to the parasitic capacitances in the circuit and the fairly high frequency of the triangle wave, the resulting triangle wave had unsatisfactorily rounded peaks and very non-linear slopes. Even replacing the LF356 op amp with the more expensive and accurate LT1632 op amp did not solve this problem. On this note, I decided to abandon the design and Figure 8 and use the XR-2206 signal generator IC instead. Not only did this produce a more accurate triangle wave, it also reduced the cost of production. However, using the XR-2206 brought about its own share of issues: significant output impedance (about 600Ω), a significant DC offset and no control over the peak voltage of the triangle wave. These problems were fixed in the triangle wave biasing duplicator with a high pass filter and some gain. The triangle wave circuit taken from the XR-2206 datasheet is as follows:

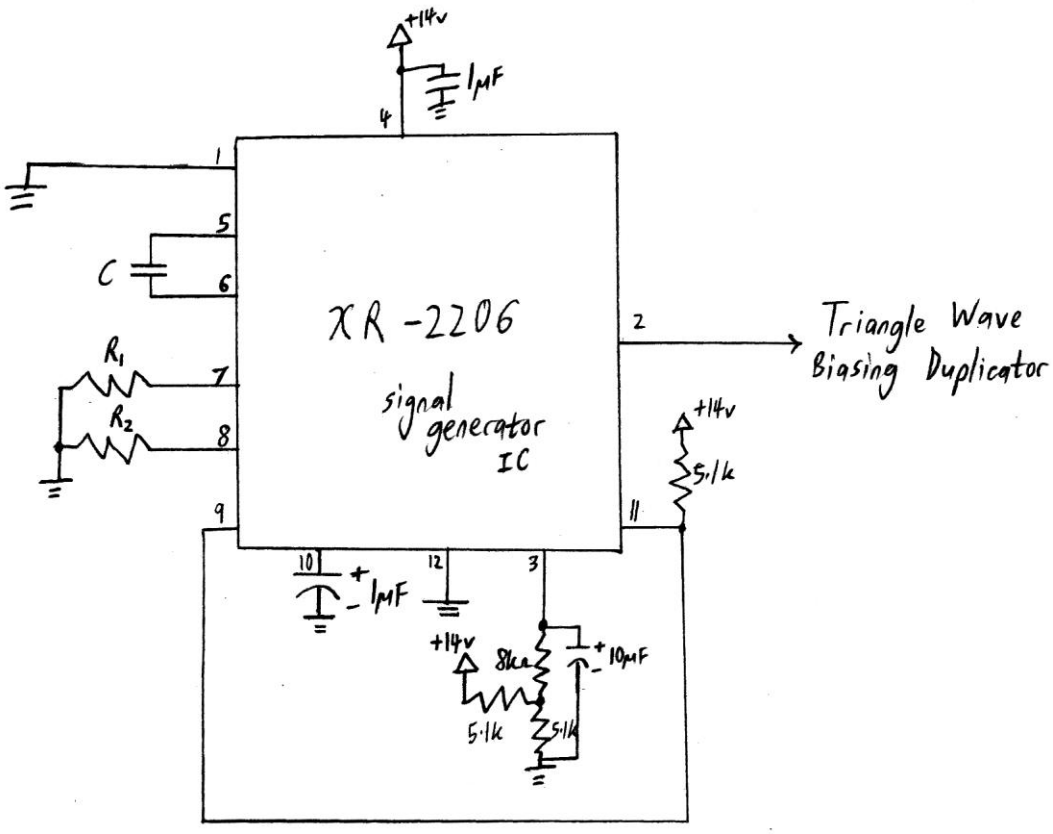

Figure 9: Triangle wave generator using the XR-2206 signal generator IC

The component values were calculated with these equations from the datasheet:

$$f = \frac{2}{C} \cdot \frac{1}{R_1 + R_2} = 300kHz$$

$$Duty\ cycle = \frac{R_1}{R_1 + R_2} = 50\% \text{ for a triangle wave}$$

Hence, $R_1 = R_2 = 2.2k\Omega$

$$C = 1.5nF$$

The result of this circuit is a fairly accurate triangle wave with very linear slopes and slightly rounded peaks at a fundamental frequency of 300kHz. Under the scope, its amplitude is $1.4V$. It is worth noting that the curved peaks of the triangle wave may actually cause the amplifier to compress any clipping peaks of the signal wave, resulting in tube-like clipping behavior.

Triangle Wave Biasing Duplicator

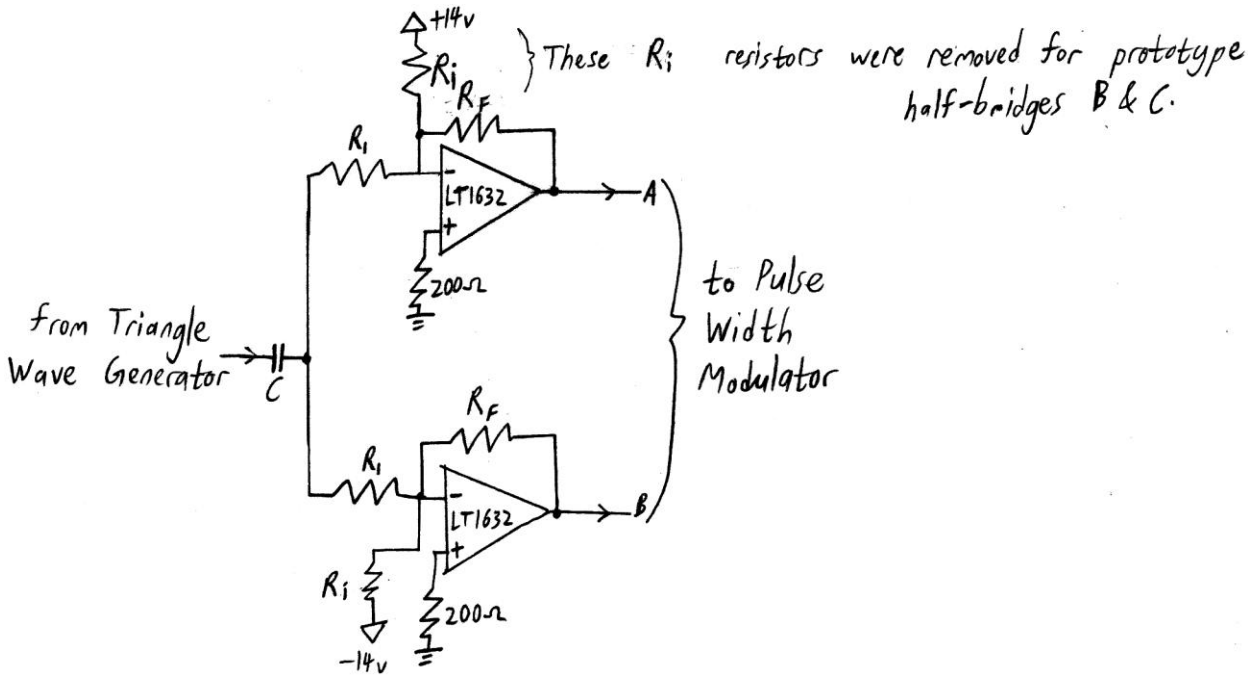

Figure 10: Triangle Wave Biasing Duplicator Circuit Diagram

This circuit does two things: remove the DC offset voltage from the triangle wave and produce two new triangle waves, one of which has a tiny voltage offset above the other. Despite its cost, the LT1632 op amp was used for this purpose because of its high bandwidth and convenient dual-op amp package. While the triangle wave's fundamental frequency is only 300kHz (not very high), this circuit has to preserve at least its 5th harmonic to retain the accuracy of the triangle wave. The op amp must provide a gain of >6dB while accurately outputting frequencies of 1.5MHz and above, so the use of the LT1632 (which has a gain-bandwidth product of 45MHz) is justified.

To maximize amplifier fidelity and efficiency, the input signal should have a peak voltage slightly below that of the triangle wave. Since the standard DAC (audio source) peak voltage is $2V_{rms} = 2.83V$ and the triangle wave from the triangle wave generator has an amplitude of $1.4V$, each duplicating circuit must have a triangle wave voltage gain of about 2. Taking into account the $R_{out} = 600\Omega$ of the triangle wave generator, we get the following transfer function:

$$\frac{v_A}{v_{tri\ gen}} = \frac{v_B}{v_{tri\ gen}} = \frac{R_F}{2R_1} \cdot \frac{sR_1C}{1 + s(R_{out} + R_1)C}$$

To obtain a gain of 2 at frequencies of 300kHz and above, I chose the following values:

$$R_1 = 220\Omega$$

$$R_F = 2.7k\Omega$$

$$C = 150nF$$

The next step is to calculate the value of R_i to determine the voltage offset between the duplicated triangle waves and hence the dead-time between the switching of the MOSFETs. I decided on a dead-time of 30ns as an acceptable compromise between introducing too much crossover distortion and increasing the risk of shoot-through. But how much voltage offset would be required to create the 30ns dead-time? First we had to find the slope of the triangle wave:

$$Slope = \frac{dv}{dt} = \frac{V_{peak\,-to-peak}}{t_{rise}} = \frac{2V_{peak}}{1/2f} = 4V_{peak}\,f = 3.39\,{}^{MV}/_{S}$$

$$V_{offset} = 30ns \cdot Slope = 0.1V$$

I implemented this as a $-0.05V$ offset in the upper biasing op amp and a $+0.05V$ offset in the lower biasing op amp to preserve symmetry. Using the standard inverting op amp formula:

$$\frac{V_{offset}}{2} = 0.05V = 14V \cdot \frac{R_F}{R_i}$$

Since we have already chosen $R_F = 2.7k\Omega$,

$$R_i = 750k\Omega$$

In testing, this circuit successfully generated a pair of triangle waves with voltage offsets of +0.05v and -0.05v around the ground voltage. Both triangle waves have an amplitude of $2.83V$, matching the standard DAC output voltage.

Pulse Width Modulator

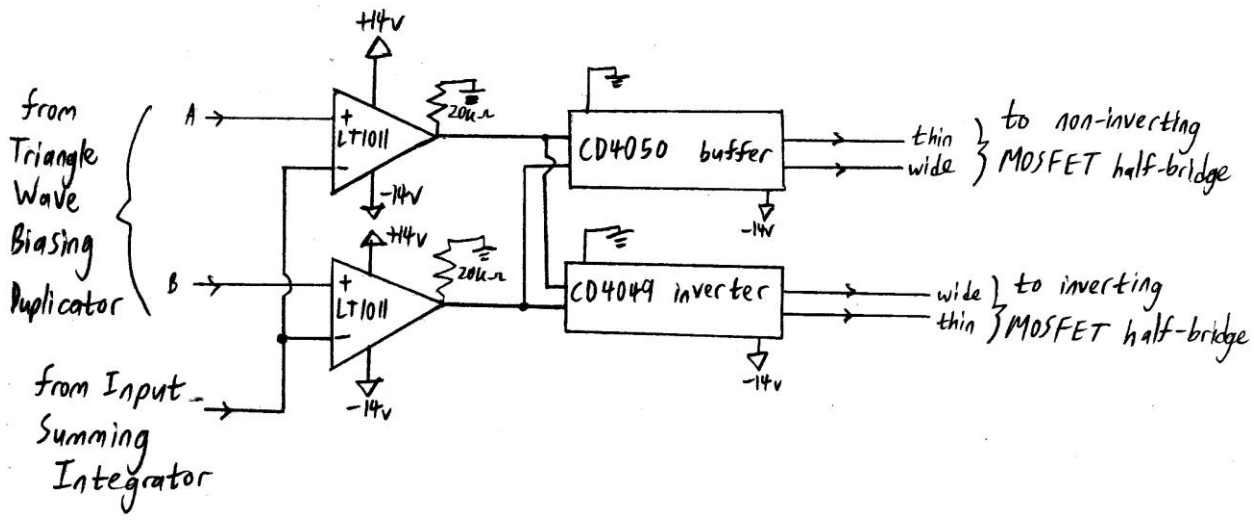

Figure 11: Pulse Width Modulator Circuit Diagram

This circuit compares the two voltage-offset triangle waves to the error-corrected input signal from the input summing integrator. I chose to use the LT1011 comparator for this purpose because of its fast response time (<250ns) and excellent output current sourcing/sinking (50mA). Of these two criteria, the high output current is more important as the comparators have to supply enough current to very rapidly change the input voltage of the CD4050 and CD4049 CMOS logic ICs.

My choice of the CD4050 buffer and CD4049 inverter ICs was due to their relatively large supply voltages. These two components act as buffers to drive the MOSFET control logic in the subsequent MOSFET half-bridge stage. The CD4049 also inverts the PWM signal to provide the complementary pulses required by the inverting MOSFET half-bridge. The use of the 'wide/thin' to describe the outputs of this circuit refers to the slightly wider PWMs produced by the comparator receiving a triangle wave with a positive offset. This distinction is important in ensuring that the 'dead-time' is spent with both MOSFETs in each half bridge turned off rather than on.

Upon testing, it was found that the actual dead-time in the PWM pulses averaged around 40ns but varied between 13ns and 70ns depending on the rate of change of the input signal voltage. This makes sense as the amount of time-delay introduced by the $0.1V$ triangle wave voltage offset is a factor of the relative slopes of the triangle wave and input signal voltages, and the previous calculations were made with the assumption that the input signal was a constant voltage.

MOSFET Half-Bridge

The MOSFET half-bridge is the most difficult part of this project due to the following issues:

1. It is the circuit most likely to be damaged by the dreaded 'shoot-through' problem, where both MOSFETs in the half-bridge are momentarily on during switching. This causes a large current pulse to travel through the two MOSFETs, usually destroying these components, their drivers and any nearby logic circuitry.
2. The top MOSFET in the half-bridge 'rides' on the output voltage. To turn on this MOSFET when the output voltage is high, the circuit has to deliver a turn-on voltage to the upper MOSFET which is even higher than the positive supply voltage of the circuit.
3. The top MOSFET's control signals must also be level-shifted to be 'low' at the output voltage and 'high' at many volts (14V in this case) above the output voltage. Furthermore, this level-shifting has to work at breakneck speeds (with a propagation delay on the order of nanoseconds) to not overly distort the output signal.

Relying on my dead-time mechanism to fix issue 1, I built a level-shifter with a single bipolar junction transistor to fix issue 3, hoping that the minimal components would allow it to run fast. The remaining issue was to deliver a voltage to the upper MOSFET and its logic circuitry which was a constant value above the output voltage, even if this meant exceeding the positive supply voltage. I solved this problem with a 'bootstrapped' capacitor[4] acting as a portable power supply referenced to the output voltage. A diode connected the capacitor to ground, such that whenever the output was low the capacitor would recharge to 14V. The circuit is as follows:

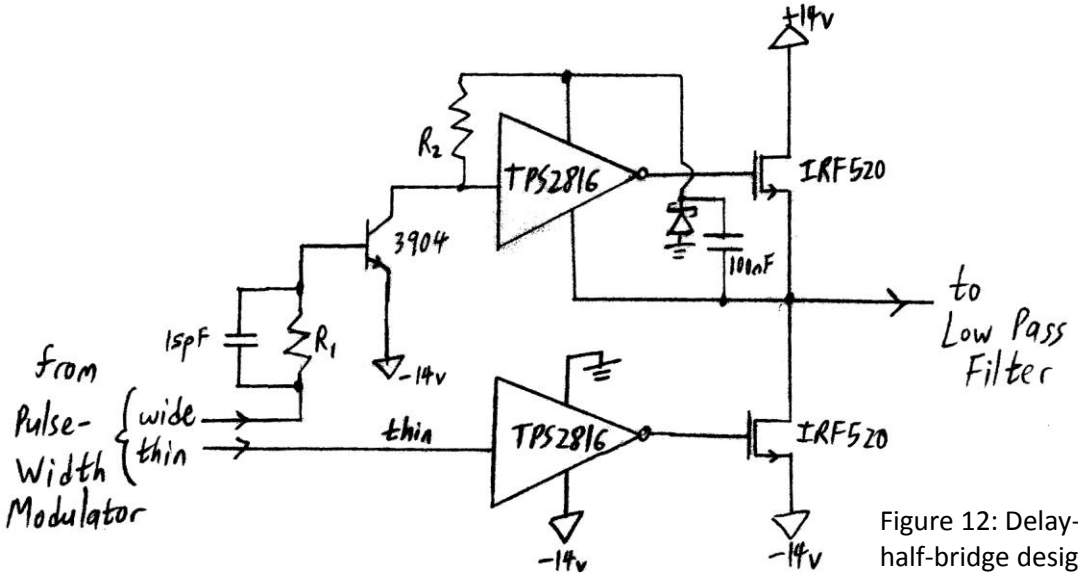

Figure 12: Delay-based MOSFET half-bridge design

[4] Sergio Sánchez Moreno, *Class D Audio Amplifiers - Theory & Design* (ColdAmp Electronics, 2005)

The level shifter constructed from the 2N3904 transistor, R_1 and R_2 also acts as an inverter for the 'wide' control signal, so that the top MOSFET is turned on antiphase with the lower MOSFET. When the 'wide' control signal goes high at 0V, (14-0.6)V can be seen across resistor R_1.

Choosing $R_1 = 100k\Omega$:

$$i_{B,2N3904} = \frac{(14 - 0.6)V}{10k\Omega} = 0.13mA$$

Assuming $i_E = 100i_B = 13mA$,

$v_{R_2} = i_E \cdot R_2 = 14V$ to send a low signal to the top MOSFET driver.

Hence, $R_2 = \frac{v_{R_2}}{i_E} = \frac{14V}{13mA} = 1.1k\Omega$

When the 'wide' control signal goes low at -14V, no current flows into the base of the 2N3904, so the emitter current also drops to zero. There is no voltage across R_2, so the top MOSFET driver sees a high signal.

The 15pF capacitor serves to further speed up the level shifter by compensating the parasitic base-to-emitter capacitance of the 2N3904 transistor. I chose to use the TPS2816 inverting MOSFET driver ICs to provide large pulses of current (>2A) to quickly change the input voltage of the IRF520 MOSFETs. I chose the IRF520 in turn because of its high output current (9.2A) and low gate charge (<30nC).

Unfortunately, this circuit did not work because the level shifter did not respond at a sufficiently high speed when the output voltage was -14V. It is plausible that a more sophisticated level shifter would have allowed this circuit to perform as intended, but I decided to abandon the delay-based shoot-through protection and use CMOS logic[5] instead.

[5] As suggested by Bill Walter of Linear Technologies.

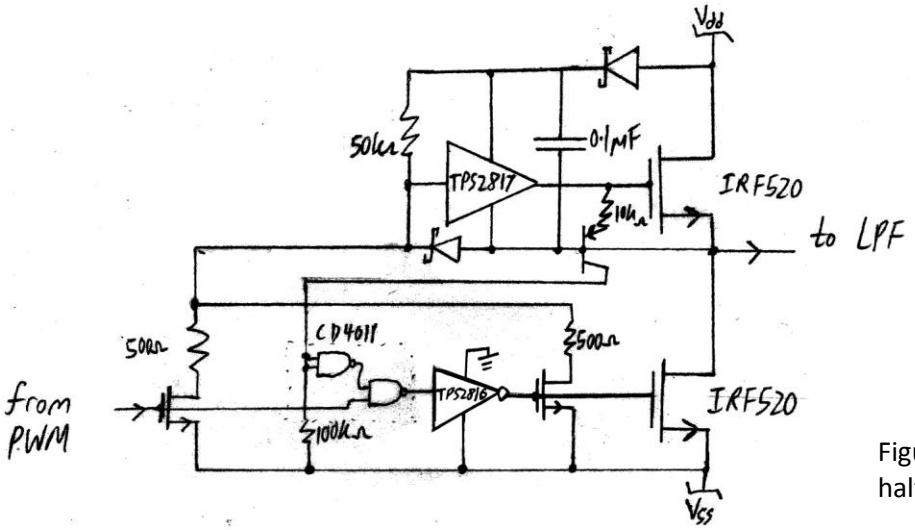

Figure 13: CMOS logic MOSFET half-bridge design

When the input signal is low, no current flows through the 50kΩ resistor so the TPS2817's input voltage is high. The top MOSFET turns on, and as current flows down from V_{dd} to the base of the bipolar junction transistor, the NAND gate leading to the TPS2816 sees a low signal from the inverter and a low signal from the input. It sends a high signal to the TPS2816, which being inverting, turns off the lower MOSFET.

When the input signal transitions from low to high, the NAND gate leading to the TPS2816 now sees a low signal from the inverter (as the top MOSFET is still on) and a high signal from the input, causing the lower MOSFET to remain off. However, the top MOSFET soon turns off as current flowing through the 50kΩ resistor sets the TPS2817's input voltage to low. As the top MOSFET switches off, no more base current flows to the bipolar junction transistor and hence there is no more voltage across the 100kΩ resistor, so the NAND gate leading to the TPS2816 sees a high signal from the inverter and a high signal from the input, causing the lower MOSFET to turn on. This illustrates how the circuit prevents the lower MOSFET from turning on until the upper MOSFET is fully turned off.

When the input signal transitions from high to low, the lower MOSFET is still on. By extension, the small signal MOSFET directly in front of the TPS2816 is also on, and the current sourced by this MOSFET maintains the voltage drop across the 50kΩ resistor. This keeps the upper MOSFET off until the lower MOSFET is no longer receiving a 'high' signal, at which point there is no longer any voltage drop across the 50kΩ resistor and the upper MOSFET is allowed to turn on. This illustrates how the circuit prevents the upper MOSFET from turning on until the lower MOSFET is fully turned off.

Unfortunately, this circuit still did not work. The main issue was the turn-on transients; since the circuit had no means of permanently setting the logic to 'turn off' for both MOSFETs and there was no 'soft start' mechanism to ensure that the circuit started up with the appropriate

logic values to reliably operate, the circuit simply shorted the rails and locked up the entire project. This led me to a third approach with the initial start-up conditions taken into consideration, using transistor logic[6].

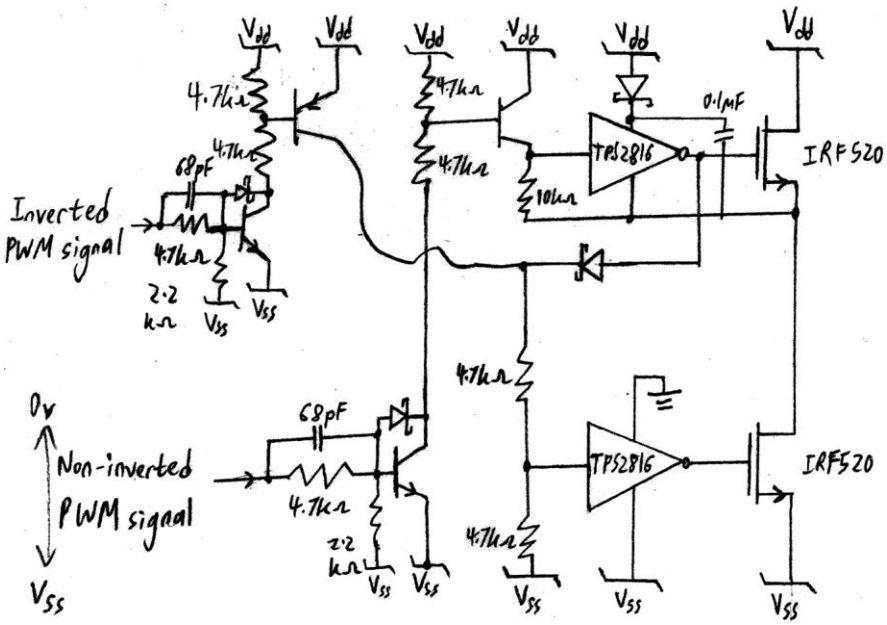

Figure 13: Transistor logic MOSFET half-bridge design

This circuit requires both an inverted and non-inverted PWM signal. Its shoot-through prevention logic is based on one simple premise: when the upper MOSFET is on, current flows through the Schottky diode at its gate, through the pair of 4.7kΩ resistors below it. This forces the input of the lower MOSFET driver high, turning off the lower MOSFET. In other words, the circuit gives the upper MOSFET top priority, only allowing the lower MOSFET to turn on when the upper MOSFET is already off. Despite its simplicity, this circuit still did not perform as intended due to the parasitic capacitances in the breadboard on which the circuit was built. Even with the use of 68pF 'speed caps', high-frequency RF transistors and Schottky diodes on the 1st transistor stage to prevent the transistors from entering deep saturation, the circuit showed over a microsecond of dead time between output pulses; about two orders of magnitude more dead-time than had been initially intended. Even if the dead-time could have been reduced by air-wiring the logic circuitry, it is unclear if the circuit would have worked.

My fourth approach to the shoot-through and level shifting problem (which was never attempted as due to lack of time) was to return to the delay-based system to prevent shoot-through and implement the level-shifting with a very high-speed single-pole, double-throw analog switch. A separate boost converter would provide a permanent third voltage supply rail of +24V for the use of the analog switch. This switch would be controlled by the PWM signal to send either -14V or +24V to the input of the upper MOSFET driver. However, even this idea is

[6] As suggested by John Memishian of Analog Devices

not without its flaws. It is unclear how reliable the MOSFET drivers would be if they were repeatedly given an input voltage which was far outside the bounds of their supply voltages; while it would probably work in the short term, it directly flouts the recommended input voltages specified in the datasheet. Furthermore, the absolute best chip I could find for the job was the ADG436, an SPDT switch which accepts large supply voltages. Even then, the ADG436 has a turn-off and turn-on time of over 100ns, giving the circuit a dead-time of about 3% of the total pulse width. This would introduce significant non-linearities and greatly reduce the power efficiency of the amplifier.

The best solution, in my opinion, would be to implement the original delay-based circuit with a more sophisticated level shifter and build the entire circuit on a surface-mount printed circuit board to reduce the effect of parasitic resistances and capacitances. Every successful Class D design I have yet uncovered has relied on either on-chip circuitry or surface-mounted discrete components.

Low Pass Filter

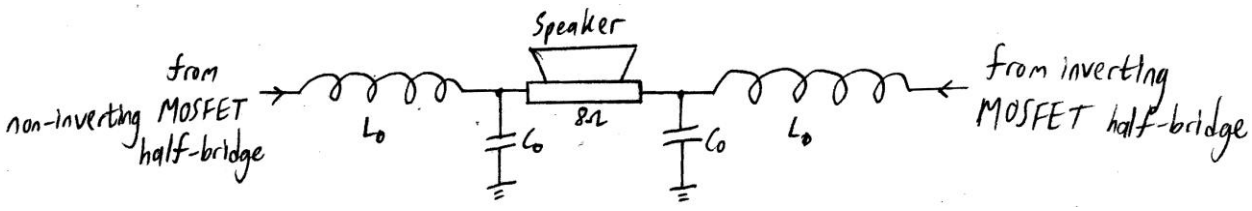

Figure 14: Low pass filter circuit diagram

The low pass filter is designed to remove frequencies 300kHz (the switching frequency) and above. However, it should neither attenuate nor phase-shift frequencies in the 20Hz-20kHz audio band. As mentioned in my description of the triangle wave generator, I chose to build a 2nd order low-pass filter with a cutoff frequency of 30kHz so that the 300kHz switching frequency would be attenuated by about 40dB. The 10kHz headroom between the cutoff frequency and the top of the audio band also keeps most of the phase shifting out of the audio band. To find the transfer function of this filter, I grounded one of the two inputs and calculated the effect of the other input's voltage on the speaker. This resulted in the following transfer function:

$$\frac{v_{input}}{v_{speaker}} = \frac{1}{1 + \frac{1}{4}sL_0 + s^2L_0C_0}$$

If we set $L_0 = 64C_0$, this equation reduces to:

$$\frac{v_{input}}{v_{speaker}} = \frac{1}{(1 + s \cdot 8C_0)^2}$$

This results in the following two constraints:

$$f_{-6dB} = \frac{1}{2\pi} \cdot \frac{1}{8C_0} = 30kHz$$

$$L_0 = 64C_0$$

Chosen component values:

$$C_0 = 680nF$$

$$L_0 = 43.5\mu H$$

The inductors were hand-wound using toroidal ferrite cores from one of the 6.101 magnetic core kits. The appropriate number of turns was calculated with the following formula:

$$N = \sqrt{\frac{\mu_0 \mu_r LD}{r^2}} = \sqrt{L \cdot \frac{\mu_0 \mu_r D}{r^2}}$$

According to the kit manual, my choice of ferrite core had a value of $\frac{\mu_0 \mu_r D}{r^2} = 55mH^{-1}$ so I needed to make 49 turns. I chose to use 16-Gauge wire because it is rated for 5.9A of current, almost twice the maximum current ($I_{max} = \frac{28V}{8\Omega} = 3.5A$) I expected in this circuit.

In testing, I measured the following gain-frequency curve:

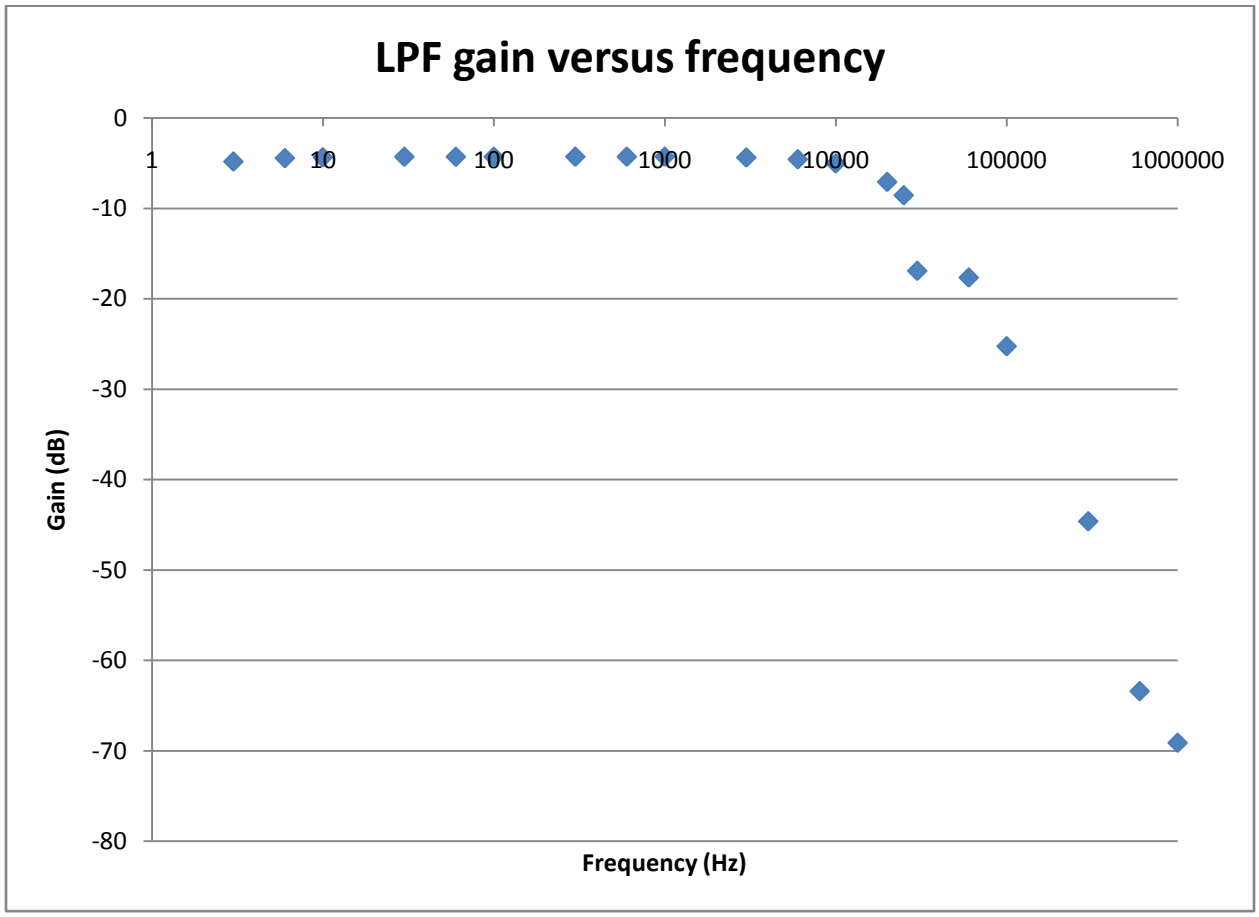

Figure 15: Graph of low pass filter gain versus frequency

According to the data above, the filter has a -4.3dB insertion loss and attenuates to -3dB at 23.4kHz, a safe interval above the audio band. As expected, it attenuates 300kHz frequencies by 44.6dB which is about 40dB more attenuation than in the audio band. The -6dB point is at 27kHz rather than 30kHz; this inconsistency is likely due to my use of an 8.2Ω test load rather than an exact 8Ω load.

Input Summing Integrator & Differential Feedback Amplifier

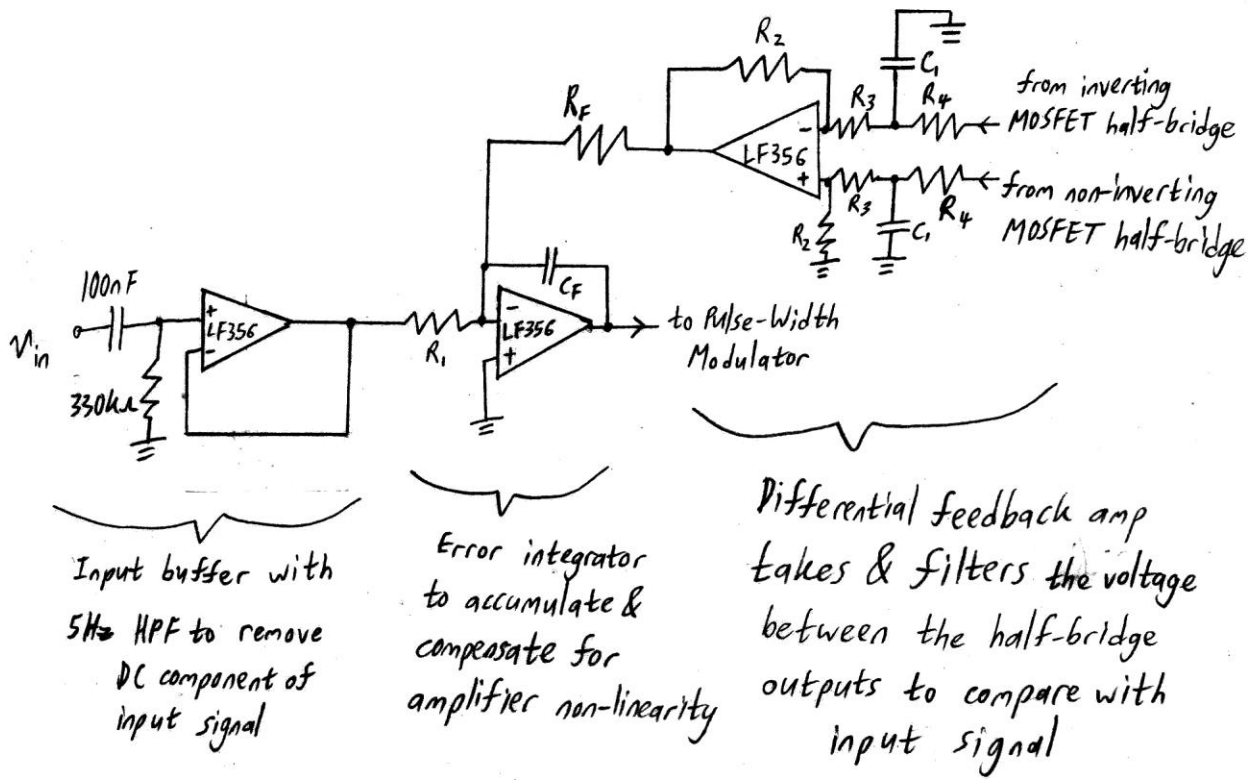

Figure 16: Input Summing Integrator & Differential Feedback Amplifier Circuit Diagram

These two components make up the error-correcting (negative feedback) portion of the circuit, performing the calculation described in Figure 6. It is worth noting that the MOSFET H-bridge (Figure 4) used to produce the amplifier's powerful output pulses has been split into two separate, identical half-bridges. The voltage of the pulses which are sent to the low pass filter and speaker is hence the voltage of the non-inverting MOSFET half-bridge's output minus that of the inverting half-bridge. The differential feedback amplifier's purpose is to perform this subtraction and send the result to the input summing integrator. There is also an input buffer (composed of a voltage follower) which removes the constant DC voltage from the input signal. This DC voltage does not affect the sound in any way and will damage the speaker and circuitry if it is amplified. It has a cutoff frequency of 5Hz (the lowest frequency reproducible by an audio CD) as shown in the following calculation:

$$f_{-3dB} = \frac{1}{2\pi \cdot RC} = \frac{1}{2\pi(330k\Omega)(100nF)} = 4.8Hz$$

One major issue with this circuit is stability. The negative feedback mechanism is prone to oscillation whenever the output pulse switches between high and low values, and special care must be taken to ensure that the oscillation decays quickly.

Resistors R_3 and R_4 and capacitors labeled C_1 form a first-order low pass filter to reduce the sharpness of the output switching. The voltage of this 'blunted' output waveform is flipped (it is antiphase with the input signal) so the summing action of the input summing integrator effectively subtracts the output waveform from the input signal to obtain the error. The integrator circuit formed by the LF356 op amp, resistors $R_1$and R_F and capacitor C_F keeps a running sum of past deviations from the 'correct' output by continuously integrating the error. This total error is the signal which is actually sent to the amplifier[7].

The transfer function of the differential feedback amplifier:

$$\frac{v_{out}}{v_{noninv\ \ hbridge} - v_{inv\ hbridge}} = \frac{R_2}{R_3 + R_4}\left(\frac{1}{1 + {}^{s}/_{w_1}}\right)$$

$$\text{where } w_1 = 2\pi f_1 = \frac{1}{C_1(R_3||R_4)}$$

The overall transfer function of the amplifier:

$$\frac{v_{noninv\ \ hbridge} - v_{inv\ hbridge}}{v_{in}} = -\frac{R_F}{R_1}\cdot\frac{R_3 + R_4}{R_2}\cdot\frac{1 + {}^{s}/_{w_1}}{{}^{s^2}/_{w_1 w_2} + {}^{s}/_{w_2} + 1}$$

$$= -\frac{R_F}{R_1}\cdot\frac{R_3 + R_4}{R_2}\cdot\frac{1 + {}^{s}/_{w_1}}{\left({}^{s}/_{w_0}\right)^2 + \sqrt{\frac{w_1}{w_2}}\left({}^{s}/_{w_0}\right) + 1}$$

$$\text{where } w_2 = 2\pi f_2 = \frac{R_2}{R_3 + R_4}\cdot\frac{Gain_{\,amp}}{R_F C_F}$$

$$\text{and } w_0 = 2\pi f_0 = \sqrt{w_1 w_2}$$

$$\text{Hence, } Q_0 = \frac{f_0}{BW_{amp}} = \frac{\frac{1}{2\pi}\sqrt{w_1 w_2}}{\frac{1}{2\pi}w_1} = \sqrt{\frac{w_2}{w_1}}$$

$Q_0$is a decent approximation of the number of cycles of ringing which follow every output voltage switch. Since we want as little ringing as possible, let $Q_0 = 0.5$.

[7] W. Marshall Leach, Jr., *Introduction to Electroacoustics and Audio Amplifier Design,* 2nd Edition (Kendall/Hunt, 2001)

This results in:

$$Q_0 = 0.5 = \sqrt{\frac{w_2}{w_1}}$$

$$w_1 = 4w_2$$

$$f_1 = 4f_2$$

Since our switching frequency is 300kHz and the differential feedback amplifier should dampen frequencies above the switching frequency, let

$$f_1 = 300kHz = \frac{1}{2\pi} \cdot \frac{1}{C_1(R_3||R_4)}$$

$$f_2 = \frac{1}{4} f_1 = 75kHz = \frac{1}{2\pi} \cdot \frac{R_2}{R_3 + R_4} \cdot \frac{Gain_{amp}}{R_F C_F}$$

The last consideration is the gain of the amplifier. The gain of a Class D amplifier is:

$$Gain_{amp} = \frac{v_{peak\ ,output}}{v_{peak\ ,triangle\ \ wave}} = \frac{14V}{2V_{rms}\sqrt{2}} = 4.95$$

This results in the following component values:

$$R_2 = 30k\Omega$$

$$R_3 = R_4 = 1.6k\Omega$$

$$R_F = 16k\Omega$$

$$C_1 = 680pF$$

$$C_F = 6.8nF$$

R_1 determines the ratio of input signal to negative feedback which is used in the error-correcting mechanism and was to be chosen empirically by listening to the amplifier's output and adjusting the resistance until the amplifier sounded 'right'. Unfortunately, due to issues with the MOSFET half-bridge circuits which have been described above, the project never reached this stage of testing.

My choice of the LF356 op amps for this circuit was due to their low cost, high input impedance and moderate high frequency performance. Considering that the feedback stage involves a low pass filter to ignore high frequencies from the output pulses, I had no reason to use a device with more bandwidth.

Conclusion

In reviewing past 6.101 attempts to design a Class D amplifier, I have come to the conclusion that mine is unique for including a negative feedback mechanism and implementing the level shifting, MOSFET logic, MOSFET driving and shoot-through protection with discrete components. Previous 6.101 Class D amplifiers have simply generated a PWM signal and fed it into a full-bridge driver/control IC such as the HIP4080, leaving the IC to perform the level shifting, shoot-through protection and MOSFET logic and driving. Although my design was also not as successful as past attempts (the malfunctioning half-bridges prevented it from producing sound), by doing all these functions with separate components, I feel that I have studied the major issues hampering the design of Class D amplifiers in greater detail. These issues include:

1. Parasitic capacitances and resistances in the breadboard cause tremendous slowdown to the MOSFET control logic. It is essential that the control logic be done either on-chip, with air-wiring or on a surface mount PCB with a ground plane.
2. The level-shifting of control signals to the upper MOSFET drivers is one of the biggest challenges of any Class D design. The level-shifter must equally delay the control signals arriving to the upper and lower MOSFET drivers. Furthermore, It must run fast enough (<10ns t_{PD}) to not excessively damage the linearity of the amplifier's gain. Furthermore, it must maintain this speed regardless of whether the output voltage is high or low.
3. Turn-on conditions are a major problem. A soft-start circuit should be used to gradually increase the supply voltage and any system using logic to prevent shoot-through should also include a mechanism which sets up the circuit's initial conditions for correct continuous operation.

My advice to future 6.101 students attempting this project is to air-wire the level-shifter circuitry to reduce the impact of breadboard parasitics, as the other option using discrete components (building a surface-mount PCB) requires earlier planning and more circuit simulation than the final project schedule generally permits. Also, use non-inverting MOSFET drivers rather than inverting MOSFET drivers is greatly advised. With inverting MOSFET drivers, it is more difficult to toggle the top MOSFET driver's input signal during the moment of switching. This is because the driver needs a signal higher than the positive supply rail to move the output from high to low. It also needs a signal at the circuit's negative supply rail to move the output from low to high. In contrast, a non-inverting driver would need a signal at ground to begin switching in either direction. This is easier to implement because you do not need to initialize switching by delivering voltages at either extreme. Careful selection of the other components is also essential. H-bridge MOSFETs with minimal gate capacitance are essential for high-speed switching. All other active devices should also be as high-speed as possible to minimize crossover distortion and control signal delay.

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