

Basic working of MIPS Lite simulator:

The simulator must start executing from the first line in the memory image trace. The memory image trace contains the code segment as well as the data segment. The lines at the top of the trace file represents instructions and the lines at the bottom of the trace represent the data segment. As the simulator executes each line from the memory image, the total number of clock cycles increments by 1. The simulator must execute all the instructions until it encounters a HALT instruction. Below shown is the pipeline diagram for the first 8 instructions in the sample memory image trace. The total number of cycles required to execute the first eight instructions is 12 cycles. Since all the eight instructions are add instructions, the total number of arithmetic instructions is 8.

Clock Cycle	1	2	3	4	5	6	7	8	9	10	11	12
				ME								
ADDI R1,R0,1000	IF	ID	EX	M	WB							
				ME								
ADDI R2,R0,1200		IF	ID	EX	M	WB						
					ME							
ADD R7,R0,R0			IF	ID	EX	M	WB					
						ME						
ADD R8,R0,R0				IF	ID	EX	M	WB				
							ME					
ADD R9,R0,R0					IF	ID	EX	M	WB			
								ME				
ADD R10,R0,R0						IF	ID	EX	M	WB		
									ME			
ADDI R11, R0,50							IF	ID	EX	M	WB	
											ME	
ADD R12, R0,32								IF	ID	EX	M	WB
												B

Total clock cycles = 12

Total Arithmetic instructions = 8