

Final Project Report

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1 Prelab

Given the transistor datasheets for the 2N3904 and 2N3906 BJTs, we determine the values of the parameters C_π , C_μ and other necessary parameters by reading the corresponding graphs. Let us consider the results for both below:

According to the datasheet, we have the following values for the small-signal characteristic $C_{\mu 0} = 3.6\text{pF}$ and $C_{je0} = 4.5\text{pF}$. Then, in order to determine $C_\pi = C_{je} + g_m \tau_f$, we consider the equations $C_{je} = 1.8C_{je0} = 8.1\text{pF}$ and $C_\pi = C_{je} + \tau_F \cdot g_m$, for some corresponding g_m . On the other hand, we have $C_\mu = \frac{1}{\sqrt{1 + \frac{V_B}{0.7V}}}$, for some corresponding V_B .

2 Design

In order to derive the values corresponding to each of the resistors in such a way that they satisfy the constraints requested, we start from the biasing. We wanted our biasing to mainly satisfy two constraints: **1.** the power dissipation had to be lower than 100mW, which implies that the total current going through all the branches could not be larger than 6.67mA; and **2.** the voltage gain for the second stage, corresponding to $A_v = -g_{m2}R_C$ must be greater than at least 100.

First, we know that the current going through transistor Q2 is dependent on the fixed voltage V_{E2} and the resistor R_{E2} ; thus, we can choose the resistor and the voltage in such a way that we get our desired current. In our case, we chose a current $I_{C2} \approx 4.4\text{mA}$. Following this, we want to set the voltage $V_{E2} = 1.7\text{V}$, which in turn would result in $V_{E1} = 2.4\text{V}$ and $V_{B1} = 3.1\text{V}$. The resistor chosen is $R_{E2} = 390\Omega$.

Once this is given, we set the resistors $R_1 = 5.6\text{k}\Omega$ and $R_2 = 15\text{k}\Omega$ and $R_{E1} = 2.6\text{k}\Omega$ such that $V_{B1} = (15V) \frac{R_2}{R_2 + R_1} = 3.1\text{V}$ and to have a small current $I_{C1} = 0.92\text{mA}$. Then, we choose the rest of the biasing as follows:

$$V_{C2} = 2.9V$$

$$V_{C3} = 8.6V$$

$$V_{B3} = 3.6V$$

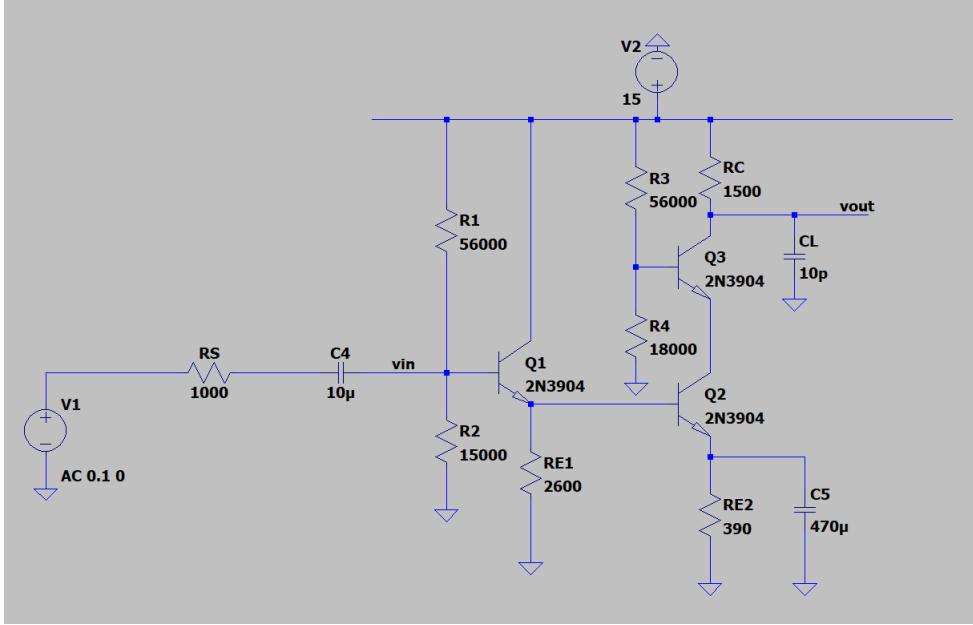


Figure 1: Current topology chosen for the project.

Note that the voltage $V_{C3} = 8.6V$ is such that $15V - V_{C3} > 2V$ and $V_{C2} - V_{C3} > 2V$, thus allowing for a voltage swing peak-to-peak larger than 2V. In order to satisfy the constrain of $V_{B3} = (15V) \frac{R_4}{R_3+R_4} = 3.6V$, we chose the resistors $R_3 = 56k\Omega$ and $R_4 = 18k\Omega$. The restriction in V_{C3} also requires that $R_C = 1.5k\Omega$.

Following this, we have that the gain of this amplifier will be given by:

$$A_v = A_{v1} \cdot A_{v2}$$

where A_{v1} and A_{v2} are the first and second stages of amplification, respectively. We can assume that the first stage of amplification will work as an ideal buffer due to its common-collector configuration, thus having that $A_{v1} \approx 1$. Then, for the second stage we will have a gain of $A_{v2} = -g_{m2}R_C$. Given that $g_{m2} = \frac{4.4mA}{26mV} \approx 0.17mS$, we will end up with a small-signal gain of:

$$A_v = 1 \cdot A_{v2} = (0.17mS)(1500\Omega) = 253.85$$

which is well beyond the requirements of this project. In addition to this, we have that the currents $I_{C2} + I_{C1} < 6.67mA$, also satisfying the power consumption constraints.

Finally, we consider the bandwidth of the amplifier. In order to do this, we calculate the zero time-value constants for the combined capacitors $C_1 = C_{\pi 2} + 2C_{\mu 2}$, $C_2 = C_{\pi 3}$, and $C_3 = C_L + C_{\mu 3}$. We neglect the values for C_{cs} due

to lack of parameters provided in the datasheets. Looking at the diagram, we obtain:

- $\tau_{C_1} = C_1(R_{E1}||r_{\pi2}||\frac{1}{g_{m1}})$
- $\tau_{C_2} = C_2(\frac{1}{g_{m3}})$, assuming that $r_{o2} \gg \frac{1}{g_{m3}}$
- $\tau_{C_3} = C_3(R_C)$, assuming that $r_{o3} \gg R_C$

Plugging in the corresponding values and using $f_h = \frac{\omega_h}{2\pi}$, we obtain:

$$f_h = \frac{1}{2\pi(\tau_{C_1} + \tau_{C_2} + \tau_{C_3})} = 5.68\text{MHz}$$

Then, to calculate the lower bandwidth limit, we calculate the infinite time-value constants for the coupling and bypass capacitors sitting at R_{E2} and R_1 respectively. We assign them large values (such as $470\mu\text{F}$) in order to minimize the value of f_l as much as possible:

- $\tau_{C_4} = C_4(R_{E2}||\frac{1}{g_{m1}})$
- $\tau_{C_5} = C_5(R_S||r_\pi + \beta R_{E1}||R_1||R_2)$

Plugging the corresponding values and using $f_l = \frac{\omega_l}{2\pi}$, we obtain:

$$f_l = \frac{1}{2\pi(\tau_{C_4} + \tau_{C_5})} = 13.34\text{Hz}$$

3 Results

The values provided were tested on the lab using a breadboard and the oscilloscopes, with an input waveform of 0.1V peak-to-peak, various frequencies and no DC offset. The results can be seen below for the measured values for the DC biasing voltages:

Quantity	Expected Value	Measured Value
V_{B1}	3.1V	3.11V
V_{E1}	2.4V	2.44V
V_{E2}	1.7V	1.72V
V_{C2}	2.9V	2.93V
V_{B3}	3.6V	3.64V
V_{C3}	8.6V	8.58V

This results in the following current values at DC bias using $I = \frac{V}{R}$ and/or the multimeter:

Quantity	Expected Value	Measured Value
I_{C2}, I_{C3}	4.4mA	4.41mA
I_{R3}	0.204mA	0.203mA
I_{R4}	0.200mA	0.202mA
I_{B2}	25.9 μ A	25.9 μ A
I_{E1}	92.3 μ A	93.8 μ A
I_{B1}	0.543 μ A	0.552 μ A
I_{R1}	0.213mA	0.212mA
I_{R2}	0.207mA	0.207mA

Then, the small-signal gain was measured using a $v_{in} = 100mV$ peak-to-peak sine signal at a frequency of 200kHz. With the 100:1 attenuator and the 253.85 gain of the two-stage amplifier, we can expect a resulting signal $v_{out} = (100mV) \frac{1}{100} (253.85) = 253mV$. The observed peak-to-peak voltage measured at v_{out} has a value even higher, of 303mV (as shown below), satisfying our expectations.

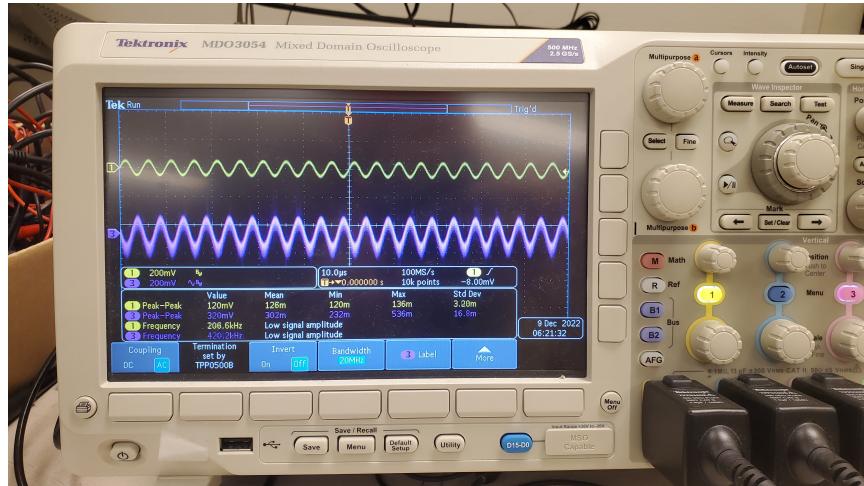


Figure 2: Oscilloscope measurement. The input waveform is of 100mVpp; thus having that the 100:1 attenuator in addition with the gain should return a signal of around 250mVpp

Finally, we measure the frequency response by observing the measured output voltage at frequencies from 100kHz to 20MHz:

Frequency	Output peak-to-peak voltage
100kHz	307mV
200kHz	302mV
300kHz	306mV
400kHz	309mV
500kHz	305mV
600kHz	302mV
700kHz	302mV
800kHz	300mV
900kHz	304mV
1MHz	306mV
2MHz	299mV
3MHz	284mV
4MHz	273mV
5MHz	261mV
6MHz	246mV
7MHz	232mV
8MHz	215mV
9MHz	198mV
10MHz	180mV
11MHz	164mV
12MHz	152mV
13MHz	149mV
14MHz	141mV
15MHz	137mV
16MHz	134mV
17MHz	135mV
18MHz	138mV
19MHz	143mV
20MHz	140mV

As observed, we do not observe a large drop on the measurements for the gain until we break the 4Mhz line; as expected from our calculations in the lab.