Aichip

學號：N26091542

姓名：張奕翔
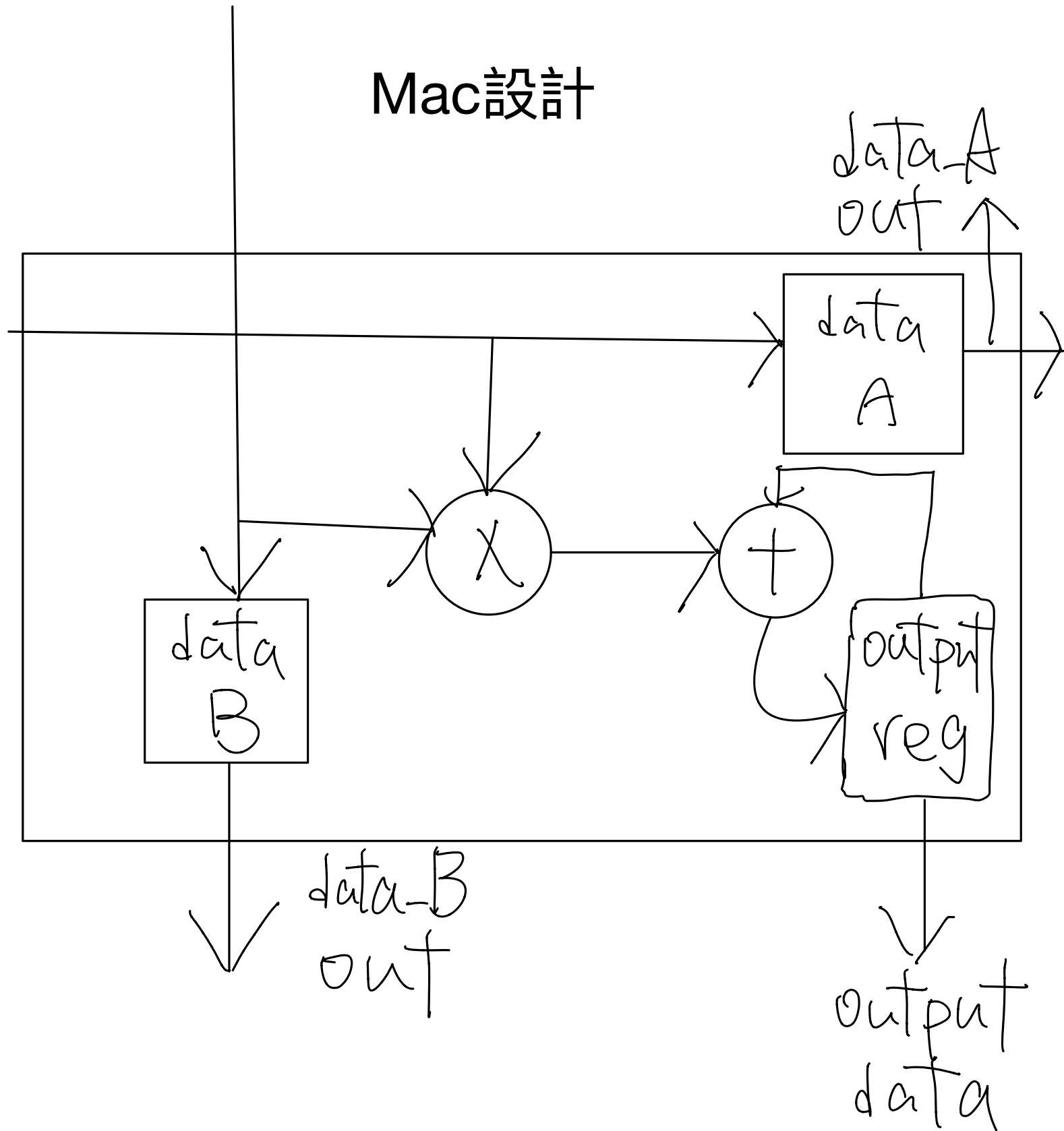
Mac設計

data_A
out

data
A

data
B

X

+

output
reg

data_B
out
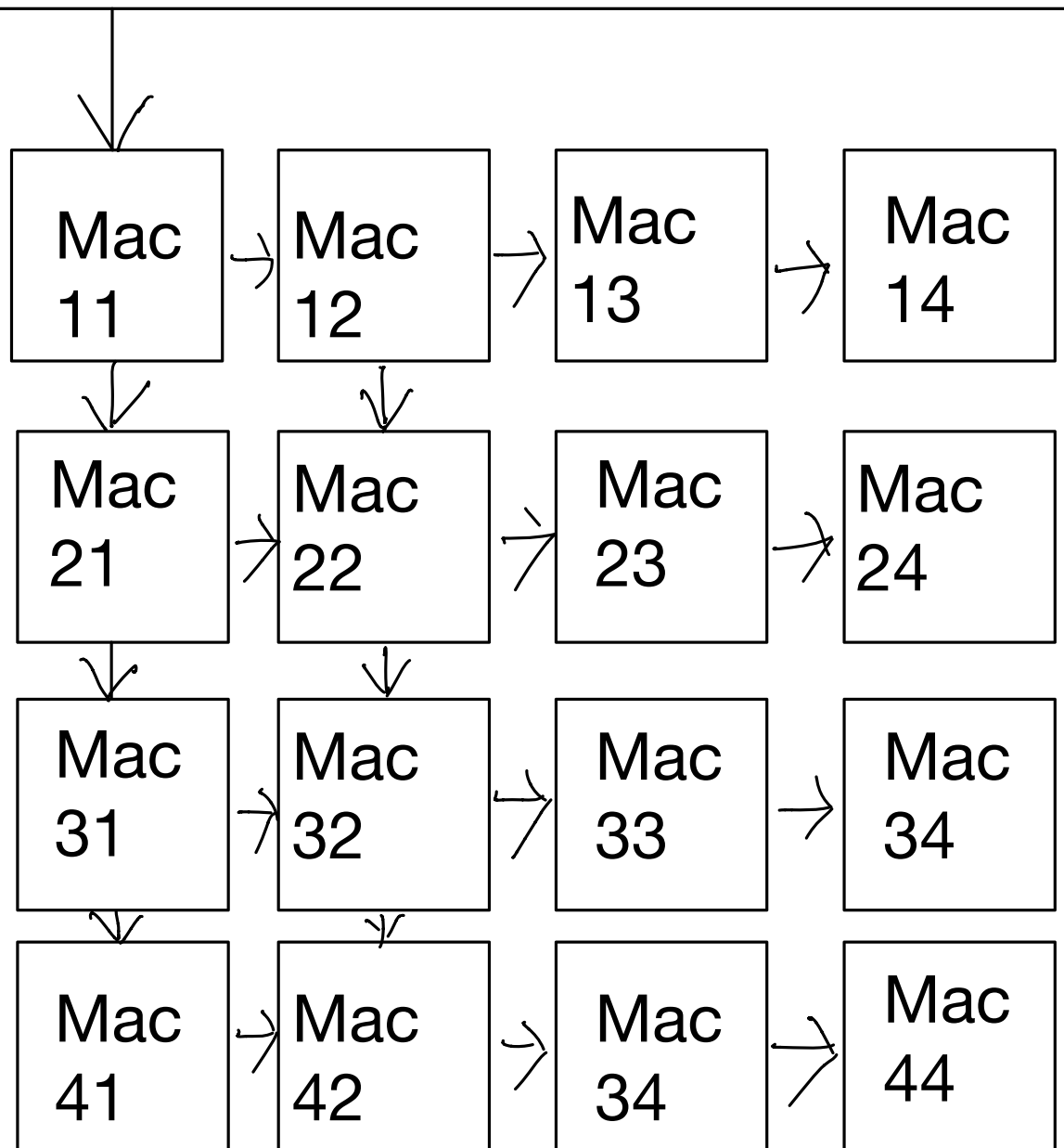
output
data

使用output stationary
Partial sum is accumulated
with the macs

CLOCK 1

a11 b11	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0
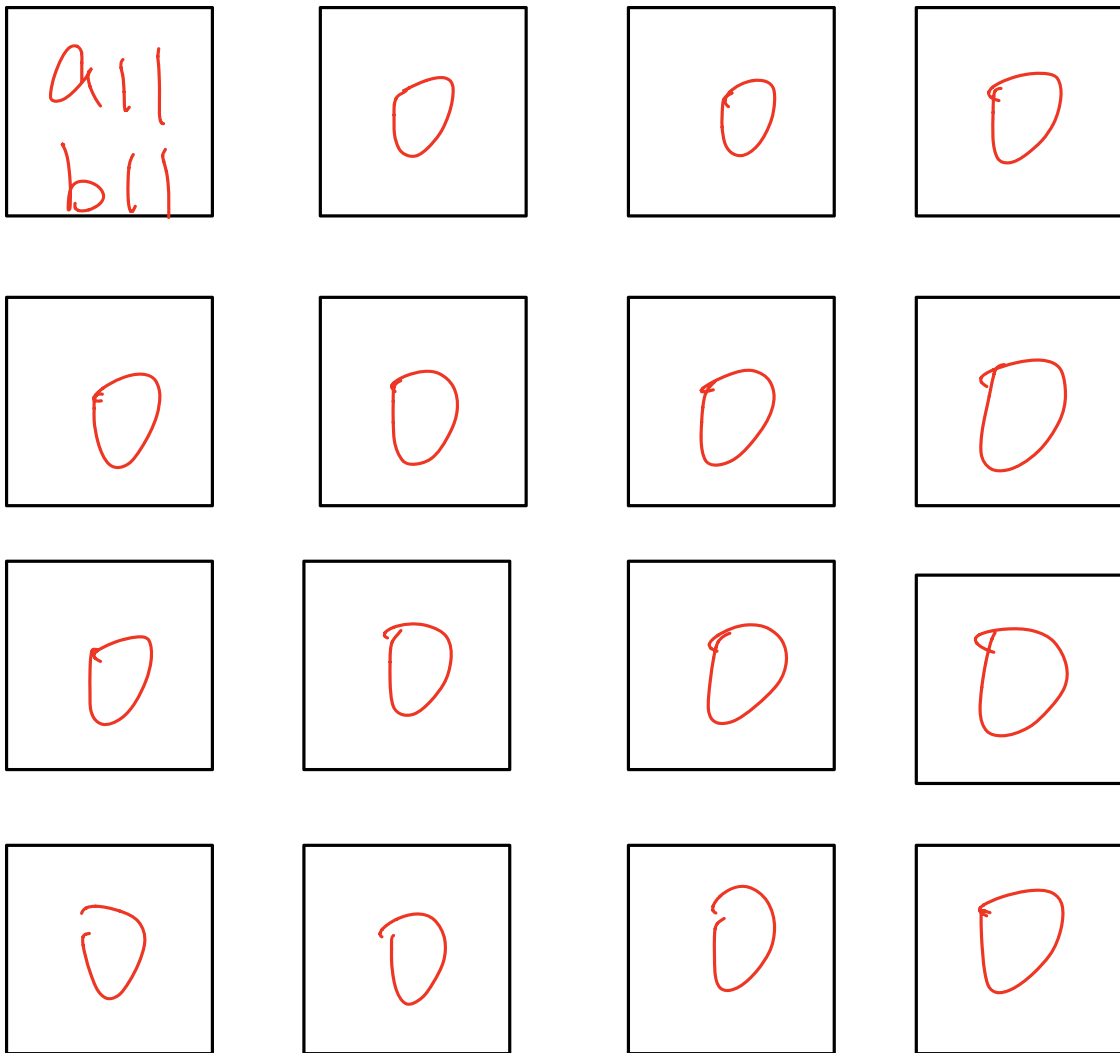
CLOCK 2

$a12$ $b21$	$a11$ $b12$	0	0
$a21$ $b11$	0	0	0
0	0	0	0
0	0	0	0

CLOCK 3

$a13$ $b31$	$a12$ $b22$	$a11$ $b13$	0
$a22$ $b21$	$a21$ $b12$	0	0

a31 b11	0	0	0
0	0	0	0

CLOCK 4

a14 b41	a13 b32	a12 b23	a11 b14
a23 b31	a22 b22	a21 b13	0
a32 b21	a31 b12	0	0
a41 b11	0	0	0

以上為 data flow and TPU Architecture