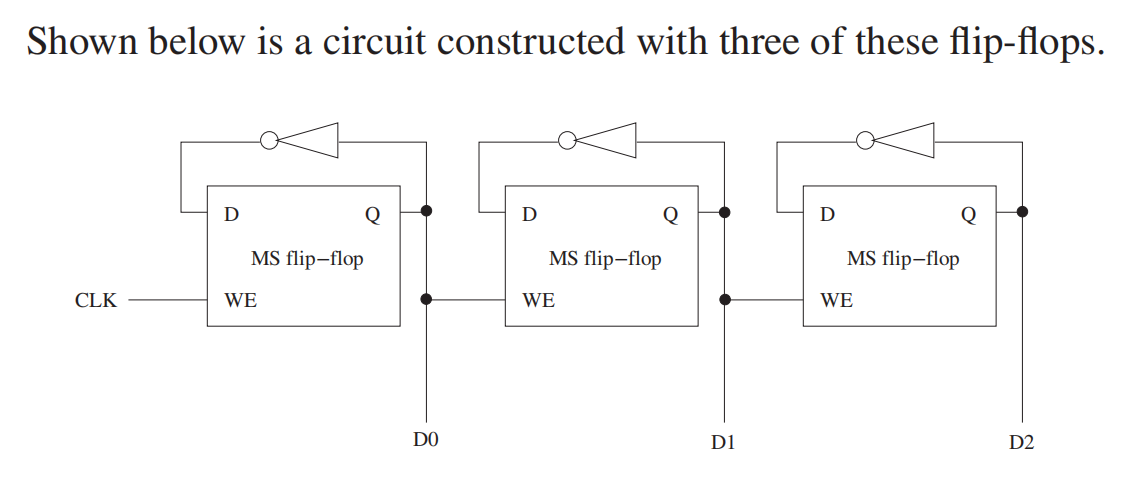
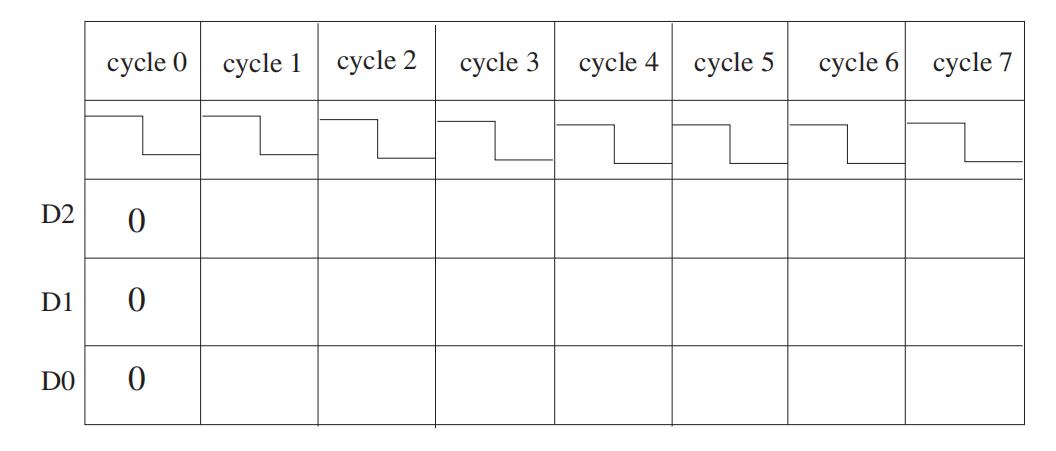
3.53

*Answer*:



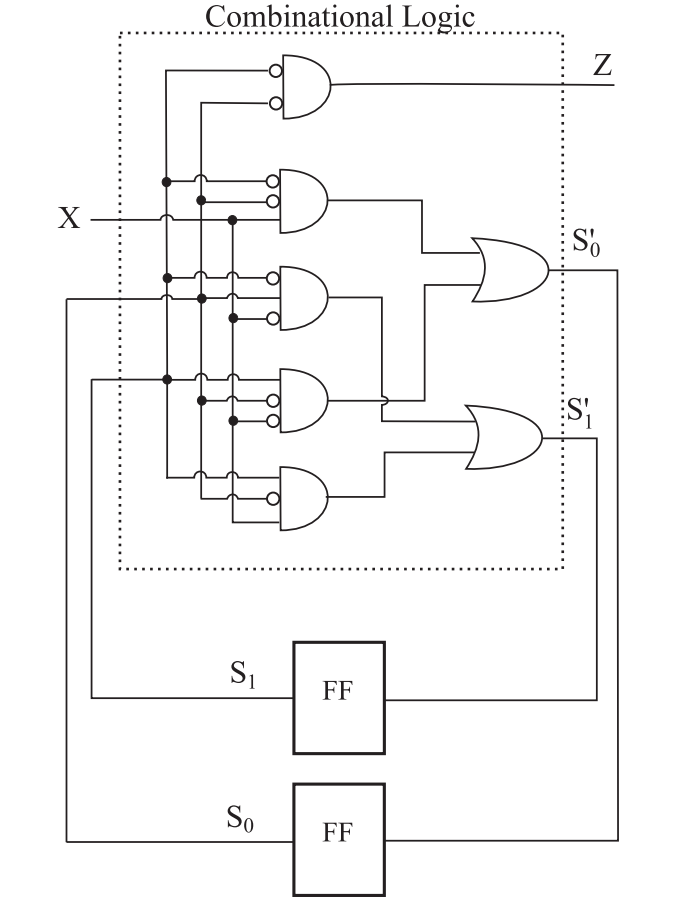
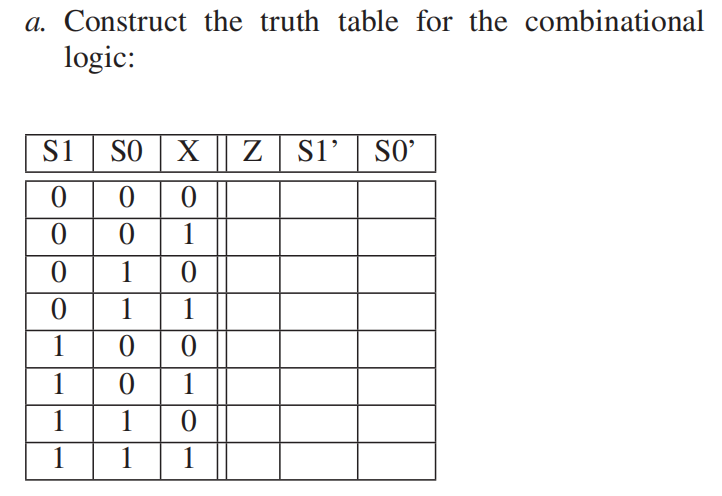
1 1 1 1 0 0 0

1 1 0 0 1 1 0

1 0 1 0 1 0 1

The circuit is doing a counting function.

3.61 The logic diagram shown below is a finite state machine.



1 0 0

1 0 1

0 1 0

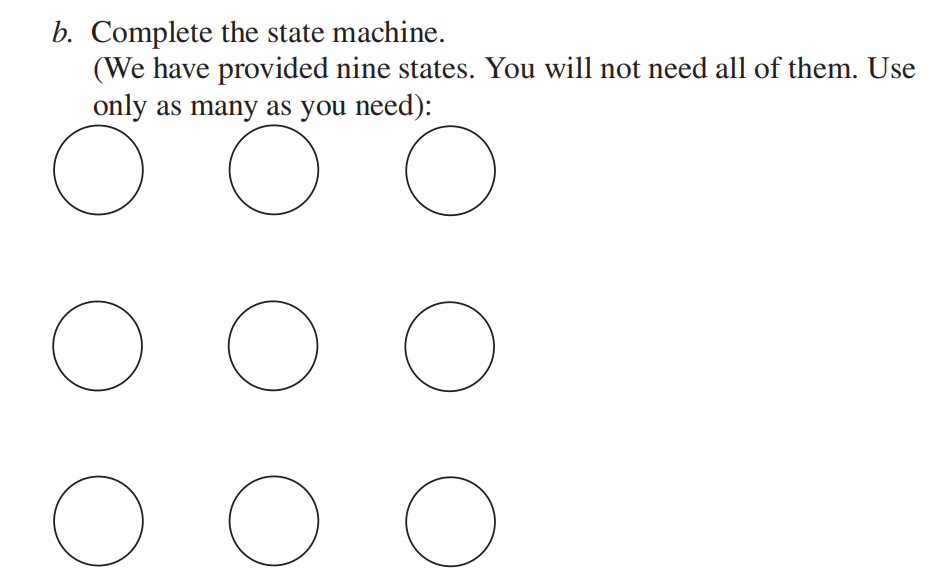
0 0 0

0 0 1

0 1 0

0 0 0

0 0 0

**

X=1

X=0

X=0

X=1

10/0

01/0

00/1

X=0

X=1

11/0

X=0/1

4.1 Name the five components of the von Neumann model. For each

component, state its purpose.

*Answer*:

The von Neumann model consists of five parts: memory, a processing unit, input, output, and a control unit.

Memory: Storage the data and the program

Processing unit: Process and compute the information

Input: Get information into the computer (keyboard)

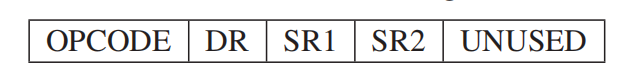
Output: Get information out of the computer (monitor)

Control unit: Keeps track of both where we are within the process of executing the program, thus making sure all parts perform correctly.

4.3 What is misleading about the name program counter? Why is the name instruction pointer more insightful?

*Answer：*

The program counter doesn’t contain counts. The contents of this register is “pointing” to the next instruction to be processed. Therefore, the name "instruction pointer" is more suitable for it.

4.8 Suppose a 32-bit instruction takes the following format:

If there are 225 opcodes and 120 registers,

a.What’s the minimum number of bits required to represent the OPCODE

b.What is the minimum number of bits required to represent the destination register (DR)?

c.What is the maximum number of UNUSED bits in the instruction encoding?

*Answer:*

1. 8bits. (225<256=2^8)
2. 7bits. (120<128=2^7)
3. 3bits. (32-8-7-7-7)

4.10 Examples 4.1, 4.2, and 4.5 illustrate the processing of the ADD, LDR,

and JMP instructions. The PC, IR, MAR, and MDR are written in various phases of the instruction cycle, depending on the opcode of the particular instruction. In each location in the following table, enter the opcodes that write to the corresponding register (row) during the corresponding phase (column) of the instruction cycle.

Answer:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Fetch Ins | Decode | Eva addr | Fetch data | Exe | Store |
| PC | 0001,0110,1100 |  |  |  | 1100 |  |
| IR | 0001,0110,1100 |  |  |  |  |  |
| MAR | 0001,0110,1100 |  |  | 0110 |  |  |
| MDR | 0001,0110,1100 |  |  | 0110 |  |  |