5.2 A memory’s addressability is 64 bits. What does that tell you about the size of the MAR and MDR?

*Answer:*

The data is stored in MDR, and the addressability is 64 bits, so the size of the MDR is 64 bits. But the size of the MAR is not known.

5.4 We have a memory consisting of 256 locations,and each location contains 16 bits.

a. How many bits are required for the address?

b. If we use the PC-relative addressing mode, and want to allow control transfer between instructions 20 locations away, how many bits of a branch instruction are needed to specify the PC-relative offset?

c. If a control instruction is in location 3, what is the PC-relative offset of address 10? Assume that the control transfer instructions work the same way as in the LC-3.

*Answer:*

1. 8 bits. Since 256=2^8, 256 addresses require 8 bits.
2. 8 bits. [Becuase ±20 gives a range of 40, the branch instructions need 6 bits.](https://bing.com/search?q=PC-relative+addressing+mode+branch+instruction+bits" \t "https://www.bing.com/_blank)
3. The offset is 6. The control instruction is in location 3, so the PC is pointing to position 4, and 10-4=6.

5.9 We would like to have an instruction that does nothing. Many ISAs actually have an opcode devoted to doing nothing. It is usually called NOP, for NO OPERATION. The instruction is fetched, decoded, and executed. The execution phase is to do nothing! Which of the following three instructions could be used for NOP and have the program still work correctly?

a. 0001 001 001 1 00000

b. 0000 111 000000001

c. 0000 000 000000000

What does the ADD instruction do that the others do not do?

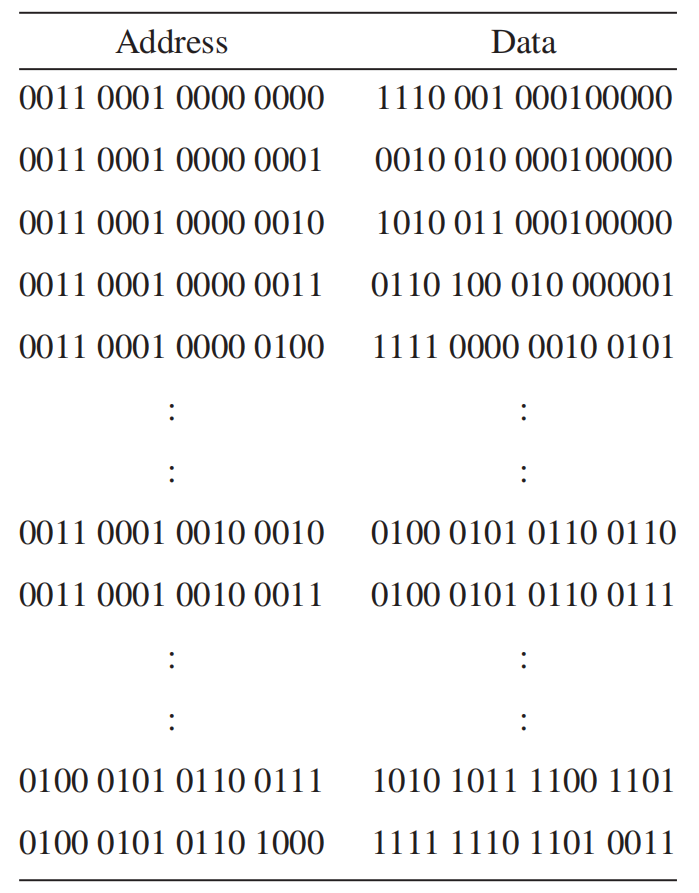
*Answer:*

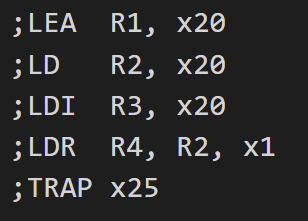
*Choose c*

a is ADD R1,R1, #0. b and c are both BR instructions. If BR’s conditional codes nzp is 111, the program must jump. And if BR’s conditional codes nzp is 000, the program won’t jump and will have no effect on the value of the conditional codes. So c is the same as NOP.

ADD instruction has no effect on the value of the register, but will have effect on the value of the control codes(n,z,p).

5.15 State the contents of R1, R2, R3, and R4 after the program starting at location x3100 halts.





PC = x3101 => R1 = PC +x20 = x3121

PC = x3102 => R2 = MEM[PC +x20] = x4566

PC = x3103 => R3 = MEM[MEM[PC +x20]] = xABCD

PC = x3104 => R4 = MEM[R2+1] = xABCD

5.16 Which LC-3 addressing mode makes the most sense to use under the following conditions? (There may be more than one correct answer to each of these; therefore, justify your answers with some explanation.)

a. You want to load one value from an address that is less than±2^8 locations away.

b. You want to load one value from an address that is more than 2^8 locations away.

c. You want to load an array of sequential addresses.

Answer:

1. PC-relative mode. Because the address is less than ±2^8 , 9 bits is enough.
2. Indirect mode. The address is more than ±2^8 , 9 bits is not enough. But indirect mode can include all addresses.
3. Base-offset mode. The base addressing method is mainly used to solve the dynamic positioning problem of the program.