9.2 Why is a ready bit not needed if synchronous I/O is used?

*Answer:*

Because the processor will know exactly when the data arrived and when it was taken away (input and output) by the time clock. It will input or output at certain intervals, and ensure that the input data is received and the output data goes to the device.

9.6 What problem could occur if a program does not check the ready bit of the KBSR before reading the KBDR?

*Answer:*

If KBSR[15] is 0, the data in KBDR has been read but the program reads the same character again and again.

9.10 What problem could occur if the CPU does not check the DSR before writing to the DDR?

*Answer*:

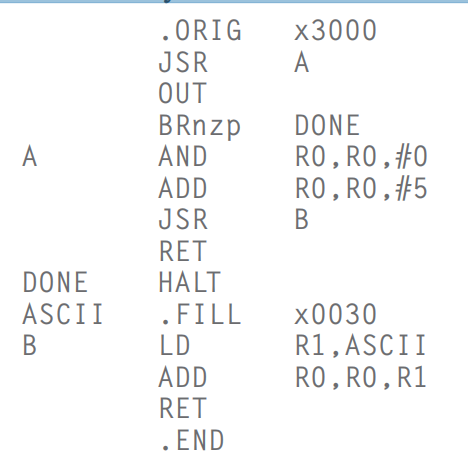
If the CPU does not check the DSR before writing to the DDR, the previous value in DDR could be lost and therefore cannot be written to the DDR.

9.14 An LC-3 Load instruction specifies the address xFE02. How do we know whether to load from the KBDR or from memory location xFE02?

*Answer:*

Address Control Logic would help. Because the memory address ends in xFDFF. If the address is xFEO2, it will access KBDR. But to the user, accessing to KBDR looks like a normal memory load instruction.

9.26 The following program is supposed to print the number 5 on the screen. It does not work. Why? Answer in no more than ten words, please.

*Answer:*

Unable to go back (first jump A) because R7 was overwritten.