

FEATURES

- Four 4.5 V rms (typical) differential inputs**
- On-chip phase-locked loop (PLL) for master clock**
- Low electromagnetic interference (EMI) design**
- 109 dB (typical) analog-to-digital converter (ADC) dynamic range**
- Total harmonic distortion + noise (THD + N): -95 dB (typical)**
- Selectable digital high-pass filter**
- 24-bit stereo ADC with 8 kHz to 192 kHz sample rates**
- Digital volume control with autoramp function**
- I²C/SPI controllable for flexibility**
- Software-controllable clickless mute**
- Software power-down**
- Right justified, left justified, I²S, and TDM modes**
- Master and slave operation modes**
- 40-lead LFCSP**
- Qualified for automotive applications**

APPLICATIONS

- Automotive audio systems**
- Active noise cancellation systems**

GENERAL DESCRIPTION

The ADAU1979 incorporates four high performance, analog-to-digital converters (ADCs) with 4.5 V rms capable ac-coupled inputs. The ADCs use a multibit sigma-delta ($\Sigma-\Delta$) architecture with continuous time front end for low EMI. An I²C/serial peripheral interface (SPI) control port is included that allows a microcontroller to adjust volume and many other parameters. The ADAU1979 uses only a single 3.3 V supply. The device internally generates the required digital DVDD supply. The low power architecture reduces the power consumption. The on-chip PLL can derive the master clock from an external clock input or frame clock (sample rate clock). When fed with the frame clock, it eliminates the need for a separate high frequency master clock in the system. The ADAU1979 is available in a **40-lead LFCSP**.

Note that throughout this data sheet, multifunction pins, such as SCL/CCLK, are referred to either by the entire pin name or by a single function of the pin, for example, CCLK, when only that function is relevant.

PRELIMINARY

FUNCTIONAL BLOCK DIAGRAM

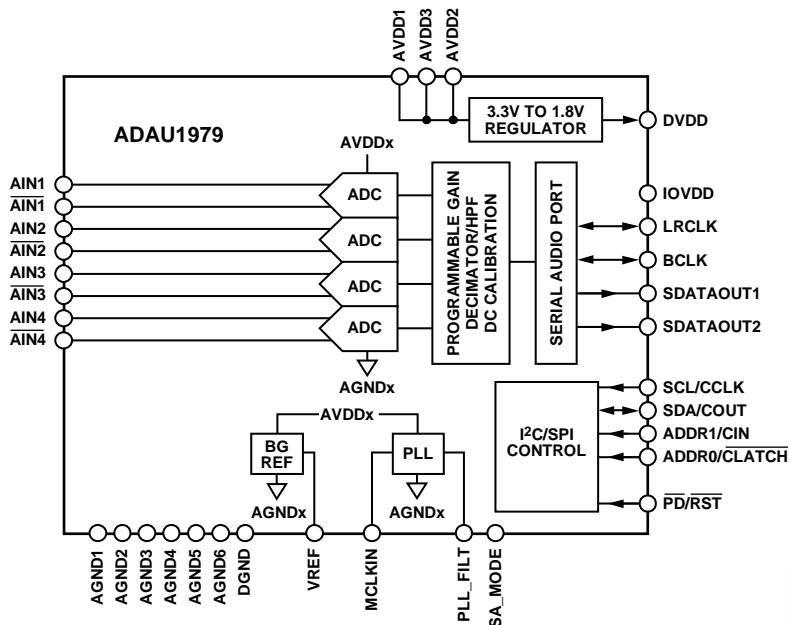

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Figure 1.

Rev. B

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REVISION HISTORY

8/2024—Rev. A to Rev. B

Changes to Table 5	5
Changes to Power-On Reset Sequence.....	12

4/2021—Rev. 0 to Rev. A

Changes to Table 6	7
Updated Outline Dimensions	42

11/2013—Revision 0: Initial Version

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SPECIFICATIONS

Performance of all channels is identical, exclusive of the interchannel gain mismatch and interchannel phase deviation specifications. AVDDx/IOVDD = 3.3 V; DVDD (internally generated) = 1.8 V; TA = -40°C to +105°C, unless otherwise noted. Master clock = 12.288 MHz (48 kHz fs, 256 × fs mode); input sample rate = 48 kHz; measurement bandwidth = 20 Hz to 20 kHz; word width = 24 bits; load capacitance (digital output) = 20 pF; load current (digital output) = ±1 mA; digital input voltage high = 2.0 V; and digital input voltage low = 0.8 V.

ANALOG PERFORMANCE SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LINE INPUT					
Full Scale AC Differential Input Voltage		4.18	4.5	4.82	V rms
Full Scale Single-Ended Input Voltage		2.09	2.25	2.41	V rms
Input Common-Mode Voltage	VIN,cm at AINx/ $\overline{\text{AINx}}$ pins		1.5		V dc
ANALOG-TO-DIGITAL CONVERTERS					
Differential Input Resistance	Between AINx and $\overline{\text{AINx}}$		64.34		kΩ
Single-Ended Input Resistance	Between AINx and $\overline{\text{AINx}}$		32.17		kΩ
ADC Resolution			24		Bits
Dynamic Range (A-Weighted) Line Input ¹	Input = 1 kHz, -60 dBFS (0 dBFS = 4.5 V rms input)	103	109		dB
Total Harmonic Distortion + Noise (THD + N)	Input = 1 kHz, -1 dBFS (0 dBFS = 4.5 V rms input)		-95	-87	dB
Digital Gain Post ADC		0	60		dB
Gain Error		-10		+10	%
Interchannel Gain Mismatch		-0.25		+0.25	dB
Gain Drift			100		ppm/°C
Common-Mode Rejection Ratio (CMRR)	400 mV rms, 1 kHz	50	65		dB
	400 mV rms, 20 kHz		56		dB
Power Supply Rejection Ratio (PSRR)	100 mV rms, 1 kHz on AVDD = 3.3 V		70		dB
Interchannel Isolation			100		dB
Interchannel Phase Deviation			0		Degrees
REFERENCE					
Internal Reference Voltage	VREF pin	1.47	1.50	1.54	V
Output Impedance		20			kΩ
ADC SERIAL PORT					
Output Sample Rate		8	192		kHz

¹ This is for a sampling frequency, fs, ranging from 44.1 kHz to 192 kHz.

DIGITAL INPUT/OUTPUT SPECIFICATIONS

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT					
High Level Input Voltage (V _{IH})		0.7 × IOVDD			V
Low Level Input Voltage (V _{IL})			0.3 × IOVDD		V
Input Leakage Current		-10	+10		µA
Input Capacitance			5		pF
OUTPUT					
High Level Output Voltage (V _{OH})	I _{OH} = 1 mA	IOVDD - 0.60			V
Low Level Output Voltage (V _{OL})	I _{OL} = 1 mA		0.4		V

POWER SUPPLY SPECIFICATIONS

AVDD = 3.3 V, DVDD = 1.8 V, IOVDD = 3.3 V, and f_s = 48 kHz (master mode), unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY					
DVDD	On-chip low dropout (LDO) regulator	1.62	1.8	1.98	V
AVDDx		3.0	3.3	3.6	V
IOVDD		1.62	3.3	3.6	V
IOVDD CURRENT	Master clock = $256 \times f_s$				
Normal Operation	f_s = 48 kHz	450			μA
	f_s = 96 kHz	880			μA
	f_s = 192 kHz	1.75			mA
Power-Down	f_s = 48 kHz to 192 kHz	20			μA
AVDDx CURRENT	4-channel ADC, DVDD internal	14			mA
Normal Operation	4-channel ADC, DVDD external	9.5			mA
Power-Down		270			μA
DVDD CURRENT					
Normal Operation	DVDD external	5			mA
Power-Down		65			μA
POWER DISSIPATION					
Normal Operation	Master clock = $256 \times f_s$, 48 kHz				
Analog Supply	DVDD internal	46.2			mW
	DVDD external	31			mW
Digital Supply	DVDD external	8.1			mW
Digital I/O Supply	IOVDD = 3.3 V	1.49			mW
Power-Down, All Supplies		960			μW

DIGITAL FILTER SPECIFICATIONS**Table 4.**

Parameter	Mode	Factor	Min	Typ	Max	Unit
ADC DECIMATION FILTER	All modes, typical at f_s = 48 kHz					
Pass Band		0.4375 $\times f_s$	21			kHz
Pass-Band Ripple			± 0.015			dB
Transition Band		0.5 $\times f_s$	24			kHz
Stop Band		0.5625 $\times f_s$	27			kHz
Stop-Band Attenuation			79			dB
Group Delay	f_s = 8 kHz to 96 kHz	22.9844/ f_s	479			μs
	f_s = 192 kHz		35			μs
HIGH-PASS FILTER	All modes, typical at 48 kHz					
Cutoff Frequency	At -3 dB point		0.9375			Hz
Phase Deviation	At 20 Hz		10			Degrees
Settling Time			1			sec
ADC DIGITAL GAIN	All modes		0	60		dB
Gain Step Size			0.375			dB

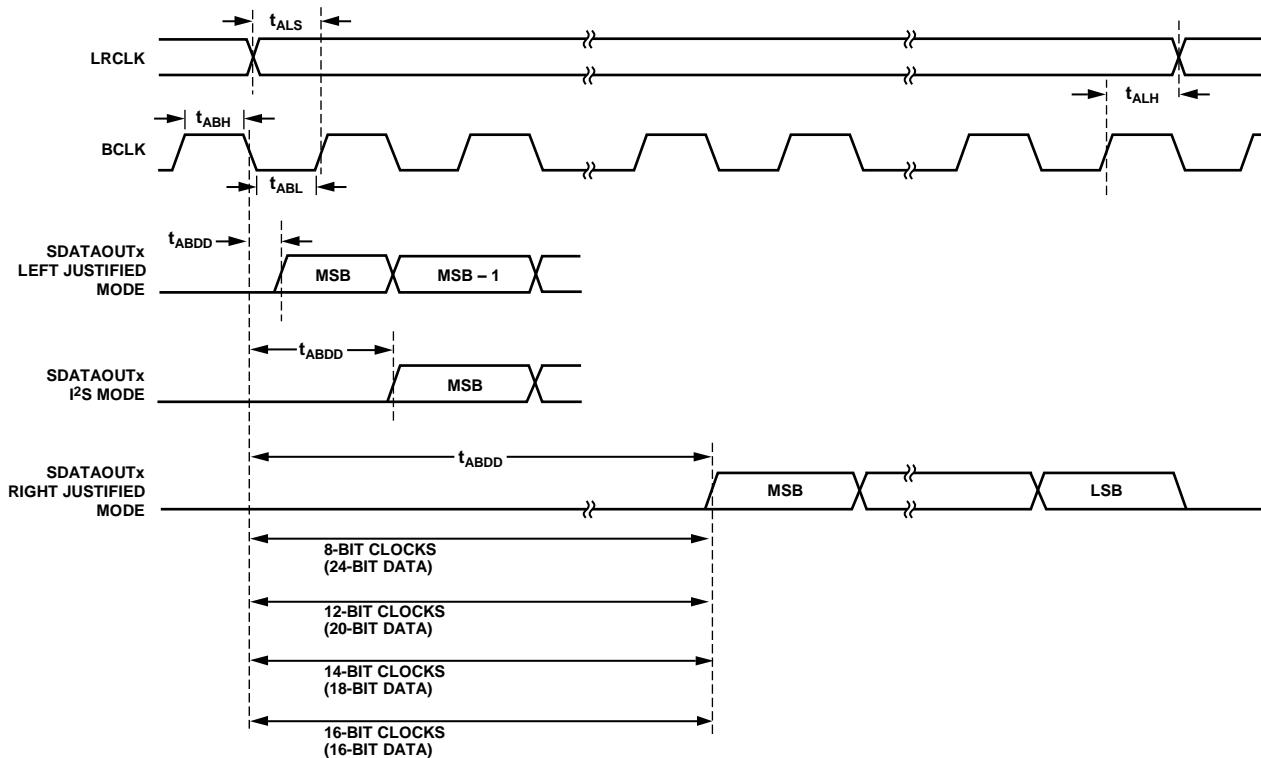
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TIMING SPECIFICATIONS**Table 5.**

Parameter	Limit at t_{MIN} t_{MAX}	Unit	Description
INPUT MASTER CLOCK (MCLK)			
Duty Cycle f _{MCLKIN}	40 60 See Table 9	% MHz	MCLKIN duty cycle; MCLKIN at $256 \times f_s$, $384 \times f_s$, $512 \times f_s$, and $768 \times f_s$ MCLKIN frequency, PLL in MCLK mode
RESET			
Reset Pulse, t _{RESET}	15	ns	RST low
PLL			
Lock Time	10	ms	MCLK mode
ADC SERIAL OUTPUT PORT			
t _{ABH}	10	ns	See Figure 2 BCLK high, slave mode
t _{ABL}	10	ns	BCLK low, slave mode
t _{ALS}	10	ns	LRCLK setup to BCLK rising, slave mode
t _{ALH}	5	ns	LRCLK hold from BCLK rising, slave mode
t _{ABDD}	18	ns	SDATAOUTx delay from BCLK falling
SPI PORT			
f _{CCLK}	10	MHz	See Figure 3 CCLK frequency
t _{CCPH}	35	ns	CCLK high
t _{CCPL}	35	ns	CCLK low
t _{CDS}	10	ns	CIN setup to CCLK rising
t _{CDH}	10	ns	CIN hold from CCLK rising
t _{CLS}	10	ns	CLATCH setup to CCLK rising
t _{CLH}	40	ns	CLATCH hold from CCLK rising
t _{CLPH}	10	ns	CLATCH high
t _{COE}	30	ns	COUT enable from CLATCH falling
t _{COD}	30	ns	COUT delay from CCLK falling
t _{COTS}	30	ns	COUT tristate from CLATCH rising
I ² C PORT			
f _{SCL}	400	kHz	See Figure 4 SCL frequency
t _{SCLH}	0.6	μs	SCL high
t _{SCLL}	1.3	μs	SCL low
t _{SCS}	0.6	μs	Setup time; relevant for repeated start condition
t _{SCH}	0.6	μs	Hold time; after this period of time, the first clock pulse is generated
t _{DS}	100	ns	Data setup time
t _{DH}	0	ns	Data hold time
t _{SCR}	300	ns	SCL rise time
t _{SCF}	300	ns	SCL fall time
t _{SDR}	300	ns	SDA rise time
t _{SDF}	300	ns	SDA fall time
t _{BFT}	1.3	μs	Bus-free time; time between stop and start
t _{SUSTO}	0.6	μs	Setup time for stop condition

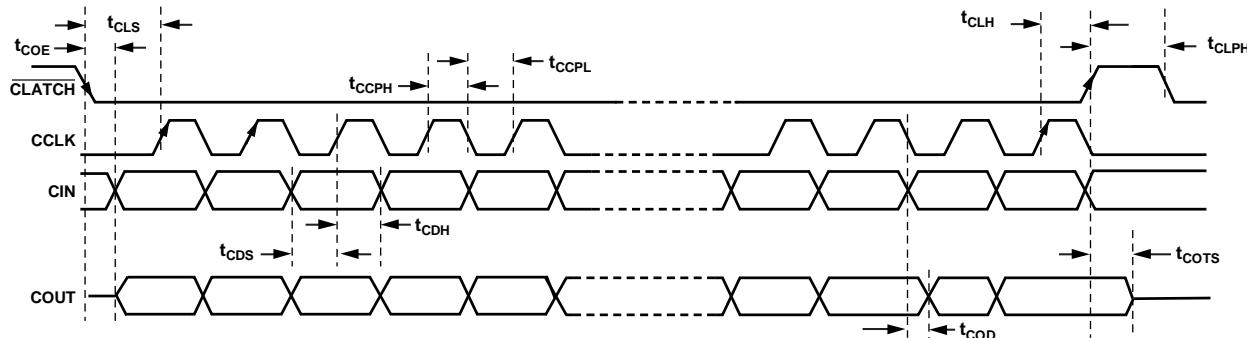
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Timing Diagrams

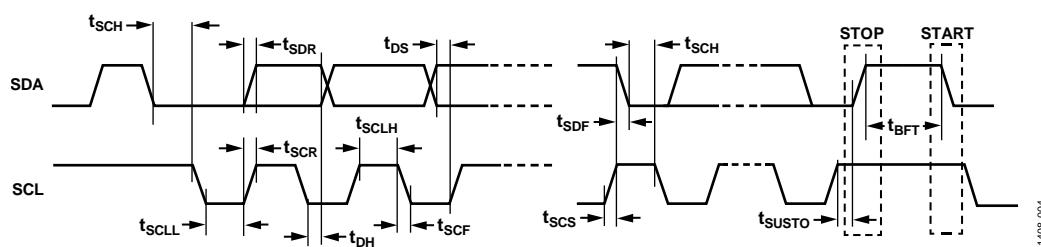
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Figure 2. ADC Serial Output Port Timing



11408-003

Figure 3. SPI Port Timing



11408-004

Figure 4. I²C Port Timing

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Analog (AVDDx) Supply	-0.3 V to +3.6 V
Digital Supply	
DVDD	-0.3 V to +1.98 V
IOVDD	-0.3 V to +3.63 V
Input Current (Except Supply Pins)	± 20 mA
Analog Input Voltage (Signal Pins)	-2.2 V to +5.2 V
Digital Input Voltage (Signal Pins)	-0.3 V to +3.6 V
Temperature	
Operating Range (Ambient)	-40°C to +105°C
Junction Range	-40°C to +125°C
Storage Range	-65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} represents junction to ambient thermal resistance, and θ_{JC} represents the junction to case thermal resistance. All characteristics are for a standard JEDEC board per JESD-51.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-40-14	32.8	1.93	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PRELIMINARY

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

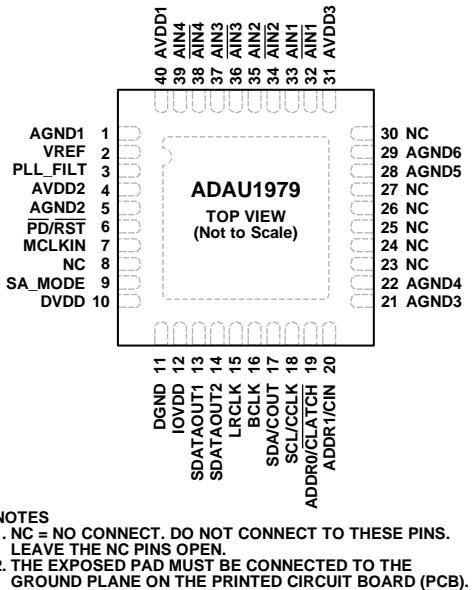


Figure 5. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type ¹	Description
1	AGND1	P	Analog Ground.
2	VREF	O	Voltage Reference. Decouple VREF to AGND with a 10 μ F capacitor in parallel with a 100 nF capacitor.
3	PLL_FILT	O	Phase-Locked Loop Filter. Return PLL_FILT to AVDD using recommended loop filter components.
4	AVDD2	P	Analog Power Supply. Connect AVDD2 to an analog 3.3 V supply.
5	AGND2	P	Analog Ground.
6	PD/RST	I	Power-Down/Reset (Active Low).
7	MCLKIN	I	Master Clock Input.
8, 23 to 27, 30	NC		No Connect. Do not connect to these pins. Leave the NC pins open.
9	SA_MODE	I	Standalone Mode. Connect SA_MODE to IOVDD using a 10 k Ω pull-up resistor for standalone mode.
10	DVDD	O	1.8 V Digital Power Supply Output. Decouple DVDD to DGND with 100 nF and 10 μ F capacitors.
11	DGND	P	Digital Ground.
12	IOVDD	P	Digital I/O Power Supply. Connect IOVDD to a supply from 1.8 V to 3.3 V.
13	SDATAOUT1	O	ADC Serial Data Output Pair 1 (ADC L1 and ADC R1).
14	SDATAOUT2	O	ADC Serial Data Output Pair 2 (ADC L2 and ADC R2).
15	LRCLK	I/O	Frame Clock for ADC Serial Port.
16	BCLK	I/O	Bit Clock for ADC Serial Port.
17	SDA/COUT	I/O	Serial Data Input/Output (I ² C)/Control Data Output (SPI).
18	SCL/CCLK	I	Serial Clock Input (I ² C)/Control Clock Input (SPI).
19	ADDR0/	I	Chip Address Bit 0 Setting (I ² C)/Chip Select Input for Control Data (SPI).

Pin No.	Mnemonic	Type ¹	Description
	CLATCH		
20	ADDR1/CIN	I	Chip Address Bit 1 Setting (I ² C)/Control Data Input (SPI).
21	AGND3	P	Analog Ground.
22	AGND4	P	Analog Ground.
28	AGND5	P	Analog Ground.
29	AGND6	P	Analog Ground.
31	AVDD3	P	Analog Power Supply. Connect AVDD3 to an analog 3.3 V supply.
32	<u>AIN1</u>	I	Analog Input Channel 1 Inverting Input.
33	<u>AIN1</u>	I	Analog Input Channel 1 Noninverting Input.
34	<u>AIN2</u>	I	Analog Input Channel 2 Inverting Input.
35	<u>AIN2</u>	I	Analog Input Channel 2 Noninverting Input.
36	<u>AIN3</u>	I	Analog Input Channel 3 Inverting Input.
37	<u>AIN3</u>	I	Analog Input Channel 3 Noninverting Input.
38	<u>AIN4</u>	I	Analog Input Channel 4 Inverting Input.
39	<u>AIN4</u>	I	Analog Input Channel 4 Noninverting Input.
40	AVDD1	P	Analog Power Supply. Connect AVDD1 to an analog 3.3 V supply.
	EP		Exposed Pad. The exposed pad must be connected to the ground plane on the printed circuit board (PCB).

¹ P = power, O = output, I = input, I/O = input/output.

PRELIMINARY

TYPICAL PERFORMANCE CHARACTERISTICS

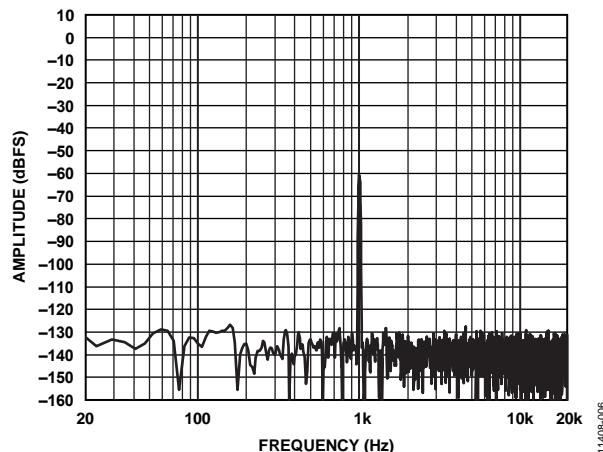


Figure 6. Fast Fourier Transform, 4.5 mV Differential Input at $f_s = 48$ kHz

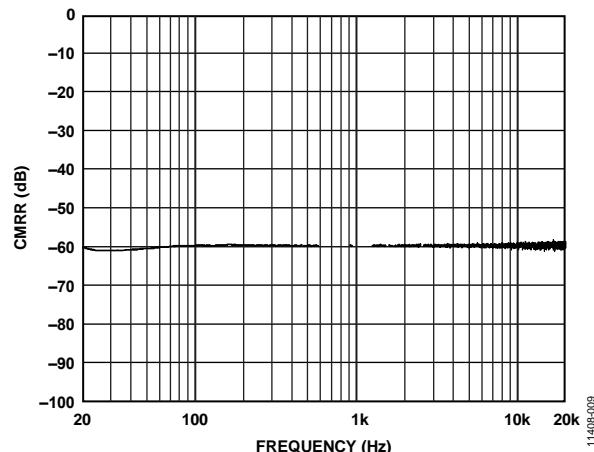


Figure 9. CMRR Differential Input, Referenced to 450 mV Differential Input

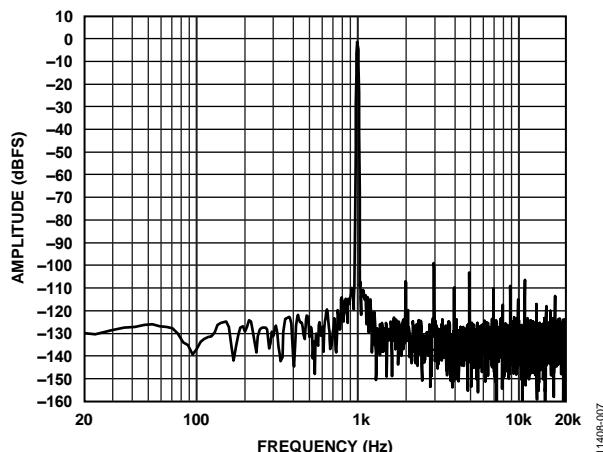


Figure 7. Fast Fourier Transform, -1 dBFS Differential Input

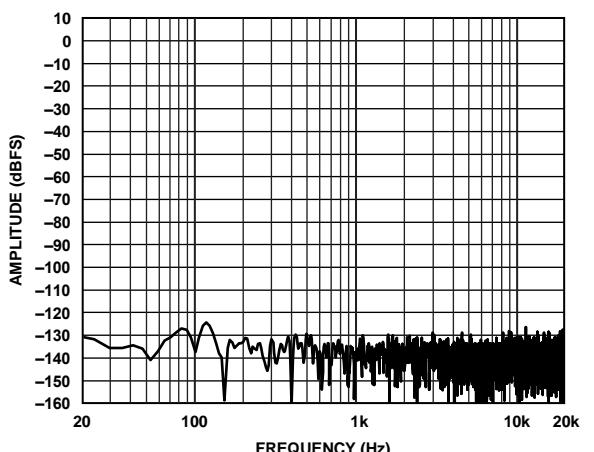


Figure 10. Fast Fourier Transform, No Input

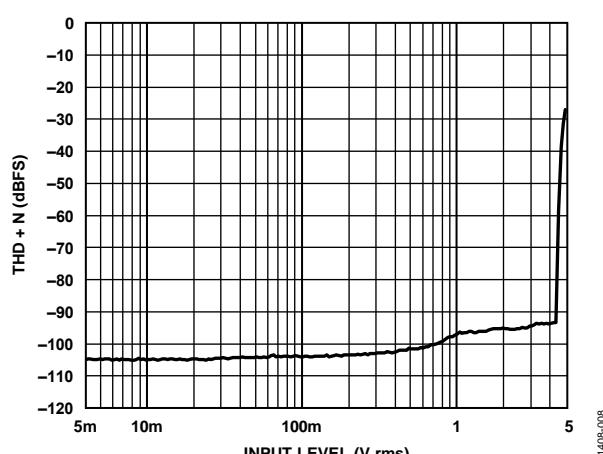


Figure 8. THD + N vs. Input Amplitude

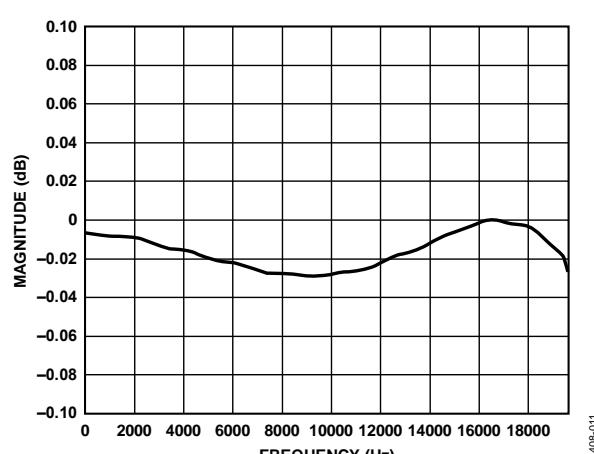


Figure 11. ADC Pass-Band Ripple at $f_s = 48$ kHz

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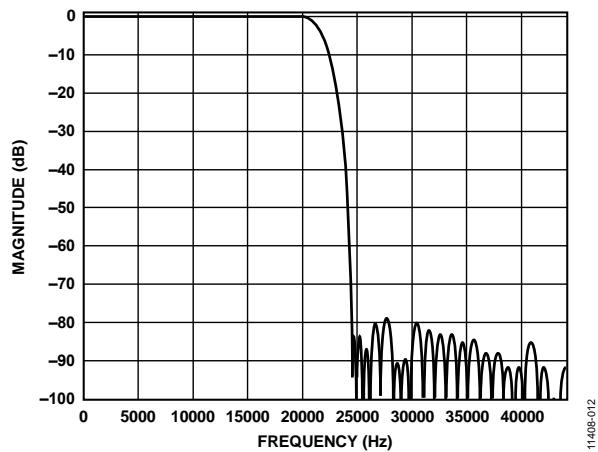


Figure 12. ADC Filter Stop-Band Response at $f_s = 48 \text{ kHz}$

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PRELIMINARY

THEORY OF OPERATION

OVERVIEW

The ADAU1979 incorporates four high performance ADCs and a phase-locked loop (PLL) circuit for generating the necessary on-chip clock signals.

POWER SUPPLY AND VOLTAGE REFERENCE

The ADAU1979 requires a single 3.3 V power supply. Decouple all AVDDx pins to the nearest AGNDx pin with 100 nF ceramic chip capacitors placed as near the AVDDx pins as possible to minimize noise pickup. A bulk aluminum electrolytic capacitor of at least 10 μ F must be provided on the same PCB as the ADC. It is important that the analog supply be as clean as possible for best performance.

The supply voltage for the digital core (DVDD) is generated using an internal low dropout regulator. The typical DVDD output is 1.8 V and must be decoupled using a 100 nF ceramic capacitor and a 10 μ F capacitor. Place the 100 nF ceramic capacitor as near the DVDD pin as possible.

The voltage reference for the analog blocks is generated internally and output at the VREF pin (Pin 2). The typical voltage at the VREF pin is 1.5 V with an AVDDx of 3.3 V.

All digital inputs are compatible with TTL and CMOS levels. All outputs are driven from the IOVDD supply. The IOVDD can be in the 1.8 V to 3.3 V range. The IOVDD pin must be decoupled with a 100 nF capacitor placed as near the IOVDD pin as possible.

The ADC internal voltage reference is output from the VREF pin and must be decoupled using a 100 nF ceramic capacitor in parallel with a 10 μ F capacitor. The VREF pin has limited current capability. The voltage reference is used as a reference to the ADC; therefore, it is recommended not to draw current from this pin for external circuits. When using this reference, use a noninverting amplifier buffer to provide a reference to other circuits in the application.

In reset mode, the VREF pin is disabled to save power and is enabled only when the PD/RST pin is pulled high.

POWER-ON RESET SEQUENCE

The ADAU1979 requires that a single 3.3 V power supply be provided externally at the AVDDx pin. The device internally generates DVDD (1.8 V), which is used for the digital core of the ADC. The DVDD supply output pin (Pin 10) is provided to connect the decoupling capacitors to DGND. The typical recommended values for the decoupling capacitors are 100 nF in parallel with 10 μ F. During a reset, the DVDD regulator is disabled to reduce power consumption. After the PD/RST pin (Pin 6) is pulled high, the device enables the DVDD regulator. However, the internal ADC and digital core reset are controlled by the internal power-on reset (POR) signal circuit, which monitors the DVDD level. Therefore, the device does not exit a reset until DVDD reaches 1.2 V and the POR signal is released. The DVDD settling time depends on the charge-up time for the external capacitors and on the AVDDx ramp-up time.

The PLL is enabled a fixed amount of time after the POR is released. Once the PLL is provided stable clocks it has a maximum lock time of 10mS in MCLK mode as mentioned in Table 5. Once the PLL is locked, its output (the internal master clock) is divided and used to provide input clocks to the state machine.

The state machine is also enabled for a fixed amount of time after the POR is released. Once the state machine has initialized, the ADC and other blocks become operational. The state machine initialization is not gated by PLL lock, only the state machine enable. PLL lock can occur after state machine enable with incorrect initialization configuration. In such cases, there's a risk of indeterminate ADC behavior for the ADAU1978. One such instance where this could occur is if the input clocks to the PLL take a long time to stabilize.

For proper initialization of the state machine, the software configuration needs to ensure that the ADAU1978 is not software-powered up until the PLL lock stabilizes. Thus, in MCLK mode the PWUP bit (Bit [0] of Register Address 0x00) can only be asserted at least 10 mS after DVDD > 1.2 V and the input clocks are stable.

POR HYSTERESIS

The internal POR circuit is provided with hysteresis to ensure that a reset of the device is not initiated by an instantaneous glitch on DVDD. The typical trip points are 1.2 V with PD/RST high and 0.6 V ($\pm 20\%$) with PD/RST low. This ensures that the core is not reset until the DVDD level falls below the 0.6 V trip point.

As soon as the PD/RST pin is pulled high, the internal regulator starts charging up C_{EXT} on the DVDD pin. The DVDD charge-up time is based on the output resistance of the regulator and the external decoupling capacitor. The time constant can be calculated as

$$t_c = R_{OUT} \times C_{EXT}$$

where $R_{OUT} = 20 \Omega$ typical.

For example, if C_{EXT} is 10 μ F, t_c is 200 μ s, and is the time that it takes to reach the DVDD voltage, within 63.6%.

The power-on reset circuit releases an internal reset of the core when DVDD reaches 1.2 V (see Figure 13). Therefore, it is recommended to wait for at least the t_c period to elapse before sending I²C or SPI control signals.

PRELIMINARY

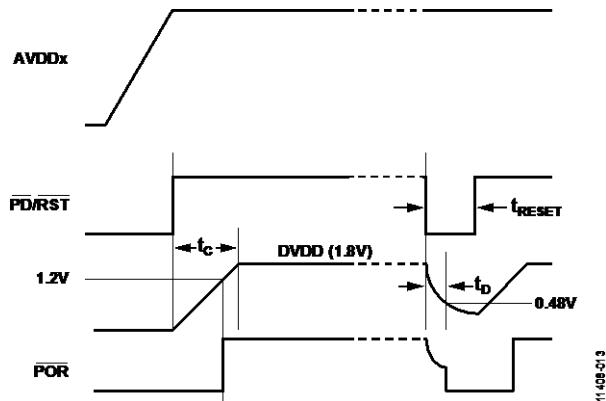


Figure 13. Power-On Reset Timing

When applying a hardware reset to the device by pulling the PD/RST pin (Pin 6) low and then high, there are certain time restrictions. During the PD/RST low pulse period, the DVDD starts discharging. The discharge time constant is determined by the internal resistance of the regulator and C_{EXT}. Use the following equation to estimate the time required for DVDD to fall from 1.8 V to 0.48 V (0.6 V – 20%):

$$t_D = 1.32 \times R_{INT} \times C_{EXT}$$

where $R_{INT} = 64 \text{ k}\Omega$ typical. (R_{INT} can vary due to process by $\pm 20\%$.)

For example, if C_{EXT} is $10 \mu\text{F}$, t_D is 0.845 sec.

Depending on C_{EXT} , t_D may vary and, in turn, affect the minimum hold period for the PD/RST pulse. The PD/RST pulse must be held low for the entire t_D time period to initialize the core properly.

Reduce the required PD/RST low pulse period by adding a resistor across C_{EXT} . Calculate the new t_D value as

$$t_D = 1.32 \times R_{EQ} \times C_{EXT}$$

where $R_{EQ} = 64 \text{ k}\Omega \parallel R_{EXT}$.

The resistor ensures that DVDD not only discharges quickly during a reset or an AVDDx power loss but also resets the internal blocks correctly. Note that some power loss in this resistor is to be expected because the resistor constantly draws current from DVDD. The typical value for C_{EXT} is $10 \mu\text{F}$ and $3 \text{ k}\Omega$ for R_{EXT} . This results in a time constant of

$$t_D = 1.32 \times R_{EQ} \times C_{EXT} = 37.8 \text{ ms}$$

where $R_{EQ} = 2.866 \text{ k}\Omega$ ($64 \text{ k}\Omega \parallel 3 \text{ k}\Omega$).

Using this equation at a set C_{EXT} value, the R_{EXT} can be calculated for a desired PD/RST pulse period.

There is also a software reset bit (S_RST, Bit 7 of Register 0x00) available that can be used to reset the part, but note that during an AVDDx power loss, the software reset may not ensure proper initialization because DVDD may not be stable.

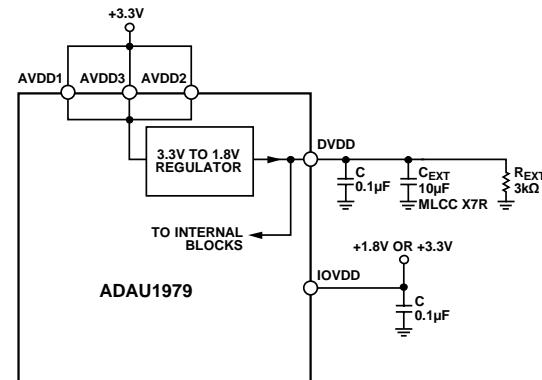


Figure 14. DVDD Regulator Output Connections

PLL AND CLOCK

The ADAU1979 has a built-in analog PLL to provide a jitter-free master clock to the internal ADC. The PLL must be programmed for the appropriate input clock frequency. The PLL_CONTROL Register 0x01 sets the PLL.

The CLK_S bit (Bit 4) of Register 0x01 sets the clock source for the PLL. The clock source can be either the MCLKIN pin or the LRCLK pin (slave mode). In LRCLK mode, the PLL supports sample rates between 32 kHz and 192 kHz.

In MCLK input mode, the MCS bits (Bits[2:0] of Register 0x01) must be set to the desired input clock frequency for the MCLKIN pin. Table 9 shows the master clock input frequency required for the most common sample rates and the MCS bit settings.

The PLL_LOCK bit (Bit 7) of Register 0x01 indicates the lock status of the PLL. It is recommended that the PLL lock status be read after initial power-up to ensure that the PLL outputs the correct frequency before unmuting the audio outputs.

Table 9. Required Master Clock Input Frequency for Common Sample Rates

MCS (Bits[2:0])	f _s (kHz)	Frequency Multiplication Ratio	MCLKIN Frequency (MHz)
000	32	$128 \times f_s$	4.096
001	32	$256 \times f_s$	8.192
010	32	$384 \times f_s$	12.288
011	32	$512 \times f_s$	16.384
100	32	$768 \times f_s$	24.576
000	44.1	$128 \times f_s$	5.6448
001	44.1	$256 \times f_s$	11.2896
010	44.1	$384 \times f_s$	16.9344
011	44.1	$512 \times f_s$	22.5792
100	44.1	$768 \times f_s$	33.8688
000	48	$128 \times f_s$	6.144
001	48	$256 \times f_s$	12.288
010	48	$384 \times f_s$	18.432
011	48	$512 \times f_s$	24.576

100	48	$768 \times f_s$	36.864
000	96	$64 \times f_s$	6.144
001	96	$128 \times f_s$	12.288
010	96	$192 \times f_s$	18.432
011	96	$256 \times f_s$	24.576
100	96	$384 \times f_s$	36.864
000	192	$32 \times f_s$	6.144
001	192	$64 \times f_s$	12.288
010	192	$96 \times f_s$	18.432
011	192	$128 \times f_s$	24.576
100	192	$192 \times f_s$	36.864

The PLL can accept the audio frame clock (sample rate clock) as the input, but the serial port must be configured as a slave, and the frame clock must be fed to the device from the master. It is strongly recommended that the PLL be disabled, reprogrammed with the new setting, and then reenabled. A lock bit is provided that is polled via I²C to check whether the PLL has acquired lock.

The PLL requires an external filter, which is connected at the PLL_FILT pin (Pin 3). The recommended PLL filter circuit for MCLK or LRCLK mode is shown in Figure 15. Using NPO capacitors is recommended for temperature stability. Place the filter components near the device for best performance.

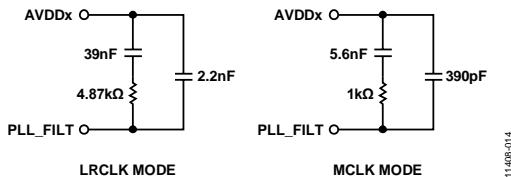


Figure 15. PLL Filter

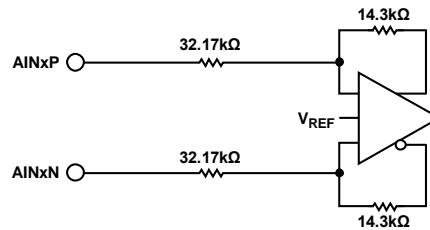
ANALOG INPUTS

The ADAU1979 has four differential analog inputs. The ADCs can accommodate both dc- and ac-coupled input signals.

The block diagram shown in Figure 16 represents the typical input circuit.

In most audio applications, the dc content of the signal is removed by using a coupling capacitor. However, the ADAU1979 consists of a unique input structure that allows ac coupling of the input signals. The typical input resistance is approximately 32 kΩ from each input to AGNDx.

The high-pass filter has a 1.4 Hz, 6 dB per octave cutoff at a 48 kHz sample rate. The cutoff frequency scales directly with the sample frequency. However, care is required in dc-coupled applications to ensure that the common-mode dc voltage does not exceed the specified limit. The input required for the full-scale ADC output (0 dBFS) is typically 4.5 V rms differential.



$V_{ID} = V$ INPUT DIFFERENTIAL
 V_{CM} AT AINxP/AINxN = 1.5V

Figure 16. Analog Input Block

11408-014

Line Inputs

This section describes some of the possible methods to connect the line level inputs of the ADAU1979.

Line Input Balanced or Differential Input DC-Coupled Case

For an input signal of 4.5 V rms differential with approximately 1.5 V common-mode dc, the signal at each input pin has a 2.25 V rms or 6.36 V p-p signal swing. At a common-mode dc of 1.5 V, the signal can swing between $(1.5 + 3.18) = 4.68$ V and $(1.5 - 3.18) = -1.68$ V at each input. Therefore, this is approximately 12.72 V p-p differential across AINx and AINx and measures near 0 dBFS (ac only with a dc high-pass filter) at the ADC output (see Figure 17).

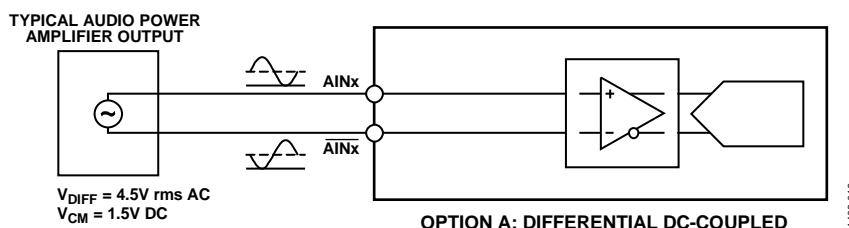
Line Input Balanced or Differential Input AC-Coupled Case

For connecting the ADAU1979 to a head unit amplifier output, ac coupling is recommended. In this case, the AINx/AINx pins are at a common-mode level of 1.5 V. Use the attenuator to reduce the input level if it is more than 4.5 V rms.

Use the following equation to identify the C1 and C2 values for the required low frequency cutoff:

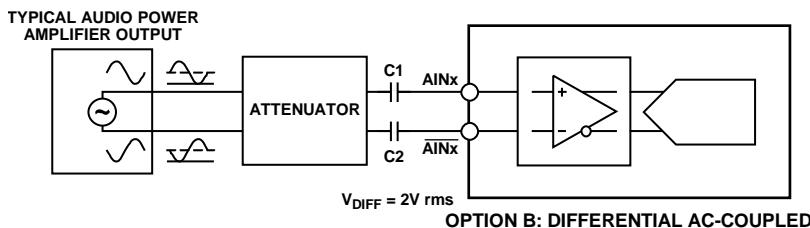
$$C1 \text{ or } C2 = 1/(2 \times \pi \times f_c \times \text{Input Resistance})$$

where the *Input Resistance* of the ADAU1979 is 32.17 kΩ typical.



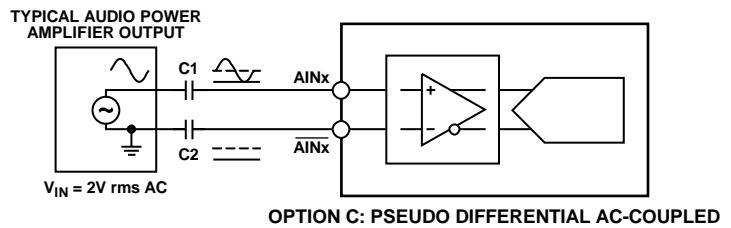
11408-016

Figure 17. Connecting the Line Level Inputs—Differential DC-Coupled Case



11408-017

Figure 18. Connecting the Line Level Inputs—Differential AC-Coupled Case



11408-018

Figure 19. Connecting the Line Level Inputs—Pseudo Differential AC-Coupled Case

Refer to Figure 18 for information about connecting the line level inputs to the ADAU1979.

Line Input Unbalanced or Single-Ended, Pseudo Differential AC-Coupled Case

For a single-ended application, reduce the signal swing by half because only one input is used for the signal and the other is connected to 0 V. Doing this reduces the input signal capability to 2.25 V rms in the single-ended application and measures approximately -6.16 dBFS (ac only with a dc high-pass filter) at the ADC output.

See Figure 19 for additional information. The value of C1/C2 is similar to the balanced ac-coupled case previously mentioned in the Line Input Balanced or Differential Input AC-Coupled Case section.

ADC

The ADAU1979 contains four Σ-Δ ADC channels configured as two stereo pairs with configurable differential/single-ended inputs. The ADC can operate at a nominal sample rate of 32 kHz up to 192 kHz. The ADCs include on-board digital antialiasing filters with 79 dB stop-band attenuation and linear phase response. Digital outputs are supplied through two serial data output pins (one for each stereo pair) and a common frame clock (LRCLK) and bit clock (BCLK). Alternatively, one of the TDM modes can be used to support up to 16 channels on a single TDM data line.

With smaller amplitude input signals, a 10-bit programmable digital gain compensation for an individual channel is provided to scale up the output word to full scale. Take care to avoid overcompensation (large gain compensation), which leads to clipping and THD degradation in the ADC.

The ADCs also have a dc offset calibration algorithm to null the systematic dc offset of the ADC. This feature is useful for dc measurement applications.

ADC SUMMING MODES

The four ADCs can be grouped into either a single stereo ADC or a single mono ADC to increase the SNR for the application. Two options are available: one option for summing two channels of the ADC and another option for summing all four channels of the ADC. Summing is performed in the digital block.

2-Channel Summing Mode

When the SUM_MODE bits (Bits[7:6] of Register 0x0E) are set to 01, the Channel 1 and Channel 2 ADC data are combined and output from the SDATAOUT1 pin. Similarly, the Channel 3 and Channel 4 ADC data are combined and output from the SDATAOUT2 pin. As a result, the SNR improves by 3 dB. For this mode, both Channel 1 and Channel 2 must be connected to the same input signal source. Similarly, Channel 3 and Channel 4 must be connected to the same input signal source.

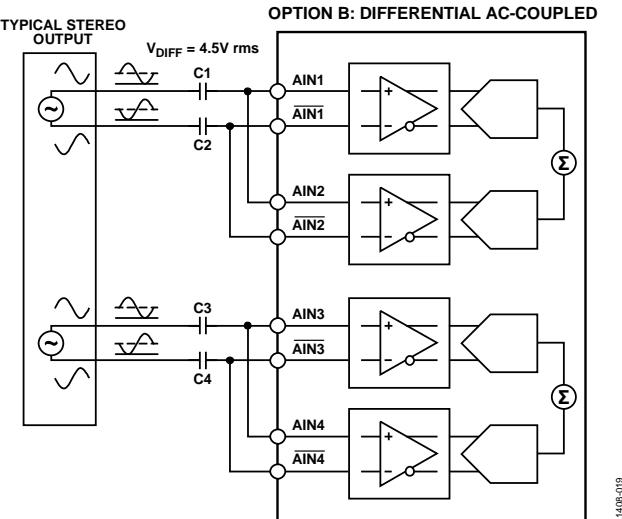


Figure 20. 2-Channel Summing Mode Connection Diagram

1-Channel Summing Mode

When the SUM_MODE Bits (Bits[7:6] of Register 0x0E) are set to 10, the Channel 1 through Channel 4 ADC data are combined and output from the SDATAOUT1 pin. As a result, the SNR improves by 6 dB. For this mode, all four channels must be connected to the same input signal source.

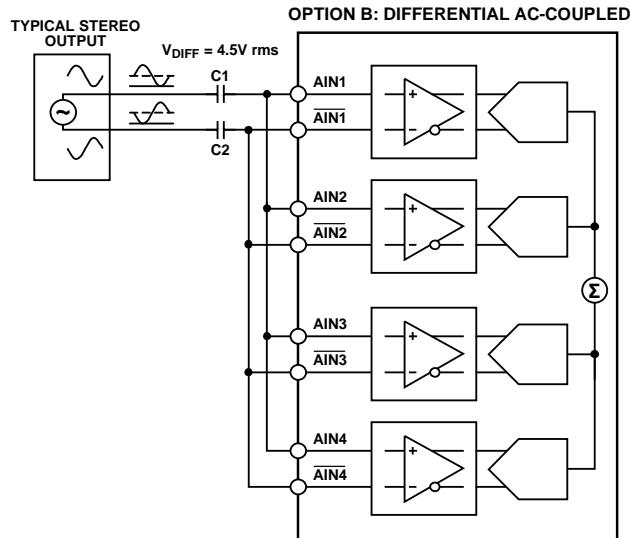


Figure 21. 1-Channel Summing Mode Connection Diagram

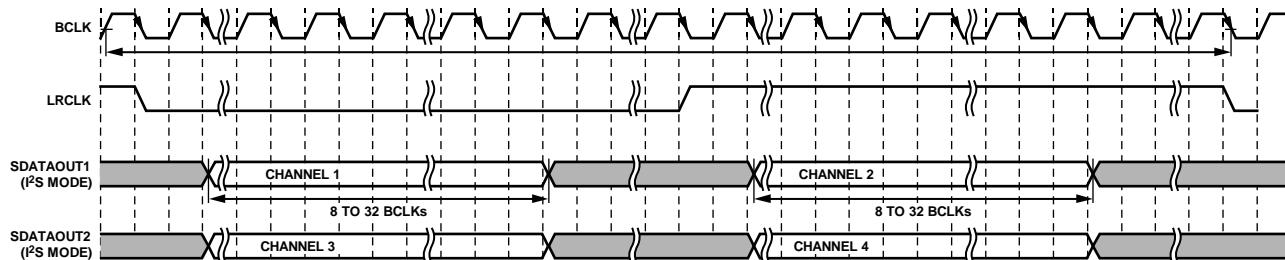
PRELIMINARY

SERIAL AUDIO DATA OUTPUT PORTS, DATA FORMAT

The serial audio port comprises four pins: BCLK, LRCLK, SDATAOUT1, and SDATAOUT2. The ADAU1979 ADC outputs are available on the SDATAOUT1 and SDATAOUT2 pins in serial format. The BCLK and LRCLK pins serve as the bit clock and frame clock, respectively. The port can be operated as a master or slave and can be set either in stereo mode (2-channel mode) or in TDM multichannel mode. The supported popular audio formats are I²S, left justified (LJ), and right justified (RJ).

Stereo Mode

In 2-channel or stereo mode, the SDATAOUT1 outputs ADC data for Channel 1 and Channel 2, and the SDATAOUT2 outputs ADC data for Channel 3 and Channel 4. Figure 22 through Figure 24 show the supported audio formats.

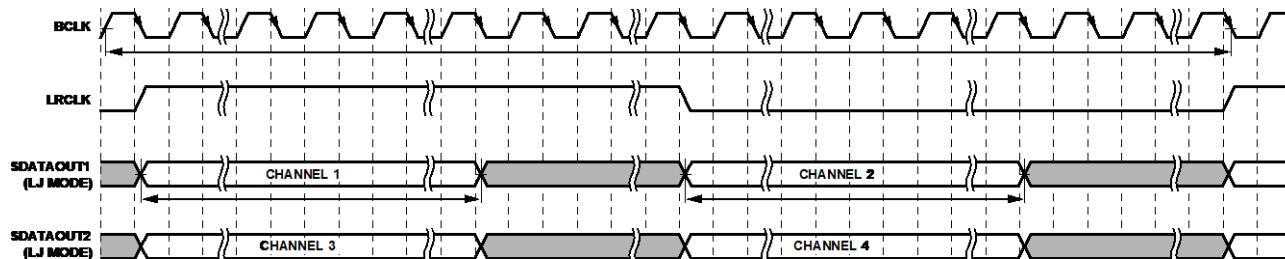


NOTES

1. SAI = 0.
2. SDATA_FMT = 0 (I²S).

Figure 22. I²S Audio Format

11408-024

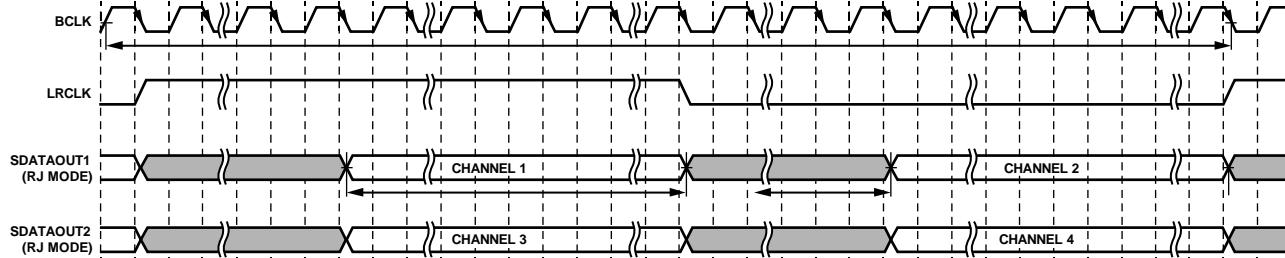


NOTES

1. SDATA_FMT = 1 (LJ).

Figure 23. Left Justified Audio Format

11408-025



NOTES

1. SDATA_FMT = 2 (RJ, 24-BIT).

Figure 24. Right Justified Audio Format

11408-026

TDM Mode

Register 0x05 through Register 0x08 provide programmability for the TDM mode. The TDM slot width, data width, and channel assignment, as well as the pin used to output the data, are programmable.

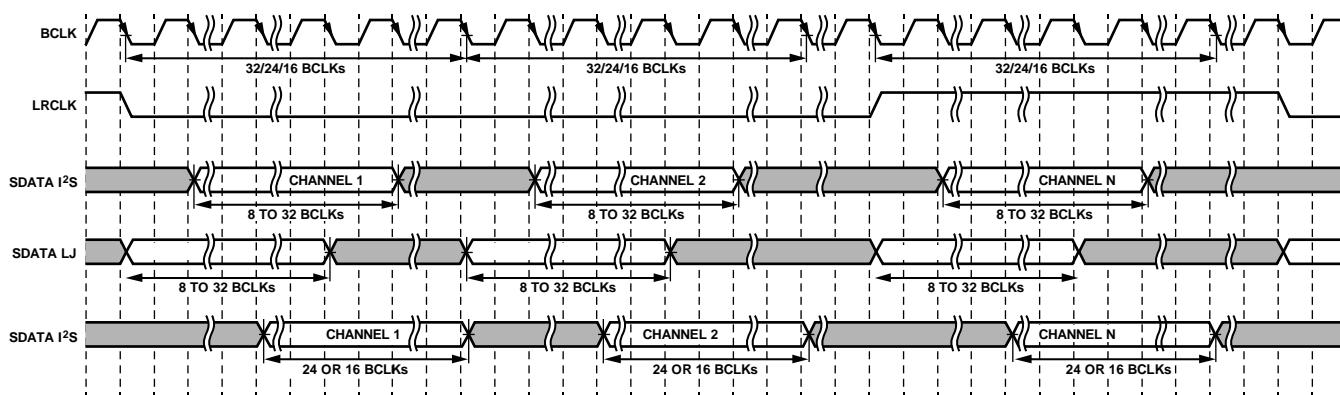
By default, serial data is output on the SDATAOUT1 pin; however, the SDATA_SEL bit (Bit 7 of Register 0x06) can be used to change the setting so that serial data is output from the SDATAOUT2 pin.

The TDM mode supports two, four, eight, or 16 channels. The ADAU1979 outputs four channels of data in the assigned slots (Figure 27 shows the TDM mode slot assignments).

During the unused slots, the output pin becomes high-Z so that the same data line can be shared with other devices on the TDM bus.

The TDM port can be operated as either a master or a slave. In master mode, the BCLK and LRCLK pins are output from the ADAU1979, whereas in slave mode, the BCLK and LRCLK pins are set to receive the clock from the master in the system.

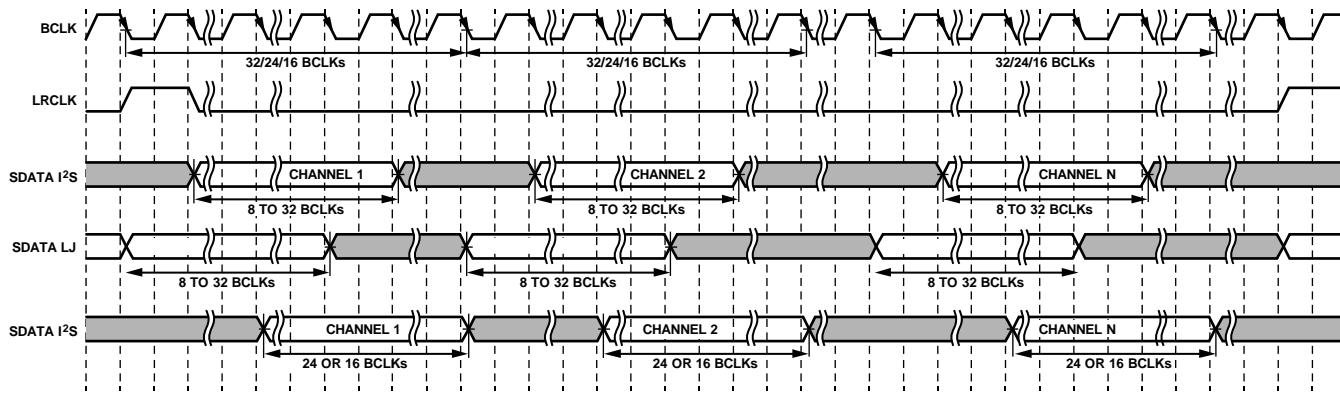
Both the nonpulse and pulse modes are supported. In nonpulse mode, the LRCLK signal is typically 50% of the duty cycle, whereas in pulse mode, the LRCLK signal must be at least one BCLK wide (see Figure 25 and Figure 26).



- NOTES**
1. SAI = 001 (2 CHANNELS), 010 (4 CHANNELS), 011 (8 CHANNELS), 100 (16 CHANNELS).
 2. SDATA_FMT = 00 (I²S), 01 (LJ), 10 (RJ, 24-BIT), 11 (RJ, 16-BIT).
 3. BCLK_EDGE = 0.
 4. LR_MODE = 0.
 5. SLOT_WIDTH = 00 (32 BCLKs), 01 (24 BCLKs), 10 (16 BCLKs).

11408-027

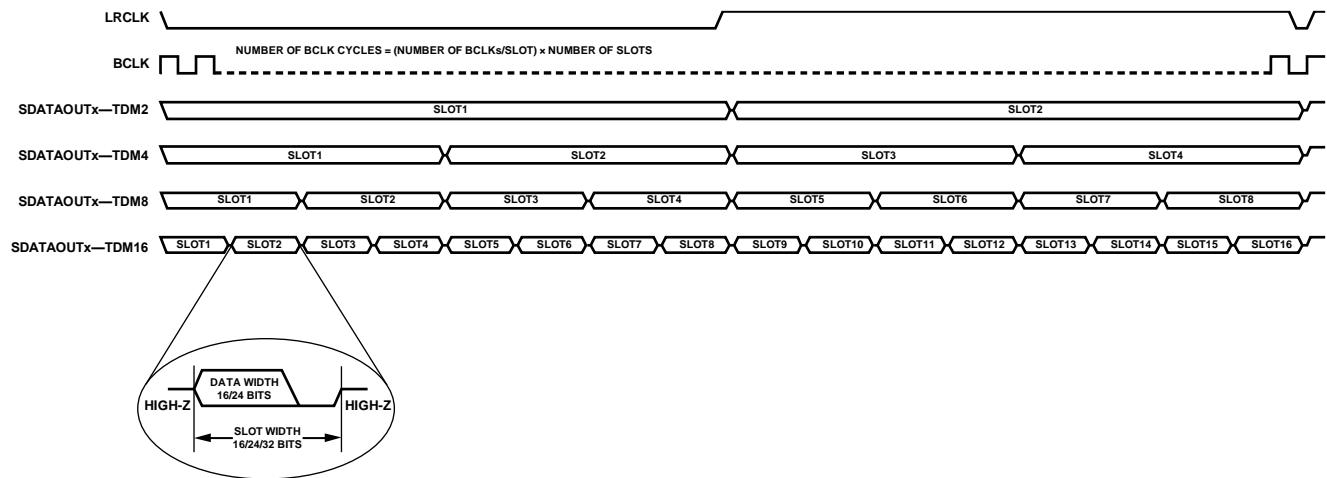
Figure 25. TDM Nonpulse Mode Audio Format



- NOTES**
1. SAI = 001 (2 CHANNELS), 010 (4 CHANNELS), 011 (8 CHANNELS), 100 (16 CHANNELS).
 2. SDATA_FMT = 00 (I²S), 01 (LJ), 10 (RJ, 24-BIT), 11 (RJ, 16-BIT).
 3. BCLK_EDGE = 0.
 4. LR_MODE = 1.
 5. SLOT_WIDTH = 00 (32 BCLKs), 01 (24 BCLKs), 10 (16 BCLKs).

11408-028

Figure 26. TDM Pulse Mode Audio Format



11408-029

Figure 27. TDM Mode Slot Assignment

Table 10. Bit Clock Frequency TDM Mode

Mode	BCLK Frequency		
	16 Bit Clocks Per Slot	24 Bit Clocks Per Slot	32 Bit Clocks Per Slot
TDM2	$32 \times f_s$	$48 \times f_s$	$64 \times f_s$
TDM4	$64 \times f_s$	$96 \times f_s$	$128 \times f_s$
TDM8	$128 \times f_s$	$192 \times f_s$	$256 \times f_s$
TDM16	$256 \times f_s$	$384 \times f_s$	$512 \times f_s$

The bit clock frequency depends on the sample rate, the slot width, and the number of bit clocks per slot. Use Table 10 to calculate the BCLK frequency.

The sample rate (f_s) can range from 8 kHz up to 192 kHz. However, in master mode, the maximum bit clock frequency (BCLK) is 24.576 MHz. For example, for a sample rate of 192 kHz, $128 \times f_s$ is the maximum possible BCLK frequency. Therefore, only 128-bit clock cycles are available per TDM

frame. There are two options in this case: either operate with a 32-bit data width in TDM4 or operate with a 16-bit data width in TDM8. In slave mode, this limitation does not exist because the bit clock and frame clock are fed to the ADAU1979. Various combinations of BCLK frequencies and modes are available, but take care to choose the combination that is most suitable for the application.

PRELIMINARY

Connection Options

Figure 28 through Figure 32 show the available options for connecting the serial audio port in I²S or TDM mode. In TDM mode, it is recommended to include a pull-down resistor on the data signal to prevent the line from floating when the SDATAOUTx pin of the ADAU1979 becomes high-Z during an inactive period. Select a resistor value such that no more than 2 mA is drawn from the SDATAOUTx pin. Although the resistor value is typically in the 10 kΩ to 47 kΩ range, the appropriate resistor value depends on the devices on the data bus.

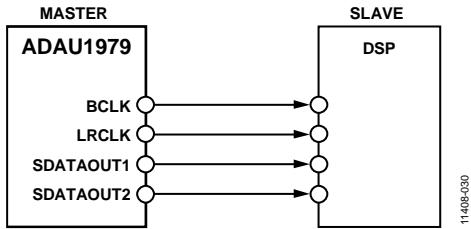


Figure 28. Serial Port Connection Option 1—I²S/Left Justified/Right Justified Modes, ADAU1979 Master

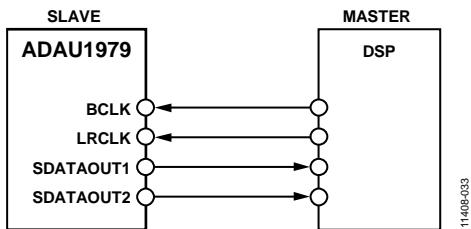


Figure 29. Serial Port Connection Option 2—I²S/Left Justified/Right Justified Modes, ADAU1979 Slave

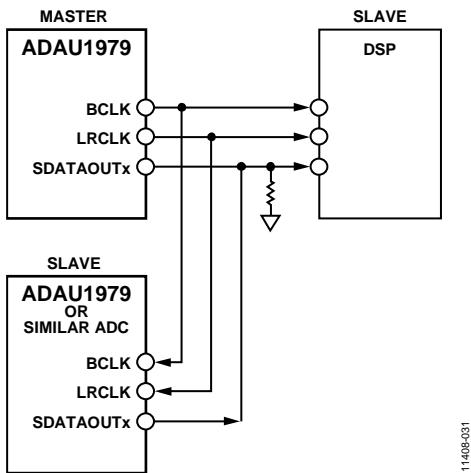


Figure 30. Serial Port Connection Option 3—TDM Mode, ADAU1979

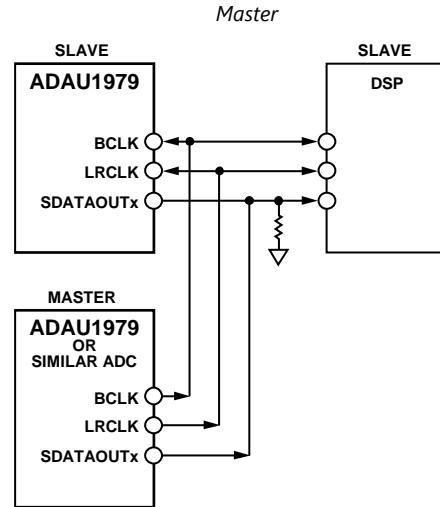


Figure 31. Serial Port Connection Option 4—TDM Mode, Second ADC Master

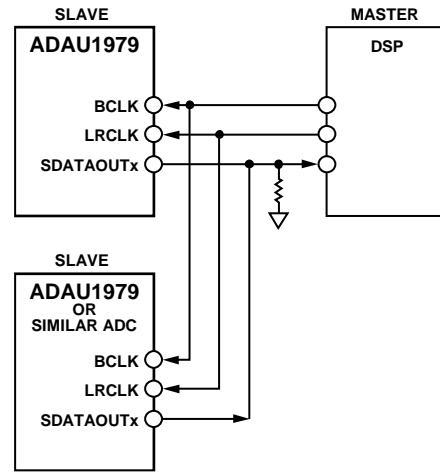


Figure 32. Serial Port Connection Option 5—TDM Mode, DSP Master

CONTROL PORTS

The ADAU1979 control port allows two modes of operation, either 2-wire I²C mode or 4-wire SPI mode, for setting the internal registers of the device. Both the I²C and SPI modes allow read and write capability of the registers. All the registers are eight bits wide. The registers start at Address 0x00 and end at Address 0x1A.

The control port in both I²C and SPI modes is slave only and, therefore, requires the master in the system to operate. The registers can be accessed with or without the master clock to the device. However, to operate the PLL, serial audio ports, and boost converter, the master clock is necessary.

By default, the ADAU1979 operates in I²C mode, but the device can be put into SPI mode by pulling the CLATCH pin low three times.

The control port pins are multifunctional, depending on the mode in which the device is operating. Table 12 describes the control port pin functions in both modes.

I²C MODE

The ADAU1979 supports a 2-wire serial (I²C-compatible) bus protocol. Two pins, serial data (SDA) and serial clock (SCL), are used to communicate with the system I²C master controller. In I²C mode, the ADAU1979 is always a slave on the bus, meaning that it cannot initiate a data transfer. Each slave device on the I²C bus is recognized by a unique device address. The device address and R/W byte for the ADAU1979 are shown in Table 11. The address resides in the first seven bits of the I²C write. Bit 7 and Bit 6 of the I²C address for the ADAU1979 are set by the levels on the ADDR1 and ADDR0 pins. The LSB of the first I²C byte (the R/W bit) from the master identifies whether it is a read or write operation. Logic Level 1 in the LSB (Bit 0) corresponds to a read operation, and Logic Level 0 corresponds to a write operation.

Table 11. I²C First Byte Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDR1	ADDR0	1	0	0	0	1	R/ \overline{W}

The first seven bits of the I²C chip address for the ADAU1979 are xx10001. Set Bit 7 and Bit 6 of the address byte using the ADDR1 and ADDR0 pins, which set the chip address to the desired value.

The 7-bit I²C device address can be set to one of four of the following possible options using the ADDR1 and ADDR0 pins:

- I²C Device Address 0010001 (0x11)
- I²C Device Address 0110001 (0x31)
- I²C Device Address 1010001 (0x51)
- I²C Device Address 1110001 (0x71)

In I²C mode, both the SDA and SCL pins require that an appropriate pull-up resistor be connected to IOVDD. Ensure that the voltage on these signal lines does not exceed the voltage on the IOVDD pin. Figure 44 shows a typical connection diagram for the I²C mode.

Calculate the value of the pull-up resistor for the SDA or SCL pin as follows.

$$\text{Minimum } R_{\text{PULL UP}} = (\text{IOVDD} - V_{IL}) / I_{\text{SINK}}$$

where:

IOVDD is the I/O supply voltage, typically ranging from 1.8 V up to 3.3 V.

V_{IL} is the maximum voltage at Logic Level 0 (that is, 0.4 V, as per the I²C specifications).

I_{SINK} is the current sink capability of the I/O pin.

The SDA pin can sink 2 mA of current; therefore, the minimum value of $R_{\text{PULL UP}}$ for an IOVDD of 3.3 V is 1.5 k Ω .

Depending on the capacitance of the printed circuit board, the speed of the bus can be restricted to meet the rise time and fall time specifications.

For fast mode with a bit rate of around 1 Mbps, the rise time must be less than 550 ns. Use the following equation to determine whether the rise time specification can be met:

$$t = 0.8473 \times R_{\text{PULL UP}} \times C_{\text{BOARD}}$$

where C_{BOARD} must be less than 236 pF to meet the 300 ns rise time requirement.

For the SCL pin, the calculations depend on the current sink capability of the I²C master used in the system.

Table 12. Control Port Pin Functions

Pin No.	Mnemonic	I ² C Mode		SPI Mode	
		Pin Function	Pin Type	Pin Function	Pin Type
17	SDA/COUT	SDA data	I/O	COUT data	O
18	SCL/CCLK	SCL clock	I	CCLK clock	I
19	ADDR0/CLATCH	I ² C Device Address Bit 0	I	CLATCH chip select	I
20	ADDR1/CIN	I ² C Device Address Bit 1	I	CIN data	I

Addressing

Initially, each device on the I²C bus is in an idle state and monitors the SDA and SCL lines for a start condition and the proper address. The I²C master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address/data stream follows. All devices on the bus respond to the start condition and acquire the next eight bits from the master (the 7-bit address plus the R/W bit) MSB first. The master sends the 7-bit device address with the R/W bit to all the slaves on the bus. The device with the matching address responds by pulling the data line (SDA) low during the ninth clock pulse. This ninth bit is known as an acknowledge bit. All other devices withdraw from the bus at this point and return to the idle condition.

The R/W bit determines the direction of the data. A Logic 0 on the LSB of the first byte means that the master is to write information to the slave, whereas a Logic 1 means that the master is to read information from the slave after writing the address and repeating the start address. A data transfer takes place until a master initiates a stop condition. A stop condition occurs when SDA transitions from low to high while SCL is held high.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence during normal read and write operations, the ADAU1979 immediately jumps to the idle condition.

Figure 33 and Figure 34 use the following abbreviations:
ACK = acknowledge
No ACK = no acknowledge

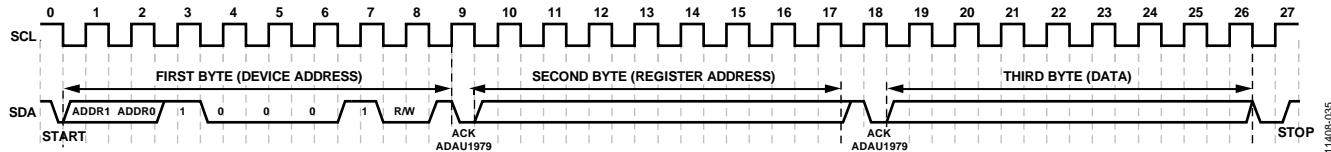


Figure 33. I²C Write to ADAU1979 Single Byte

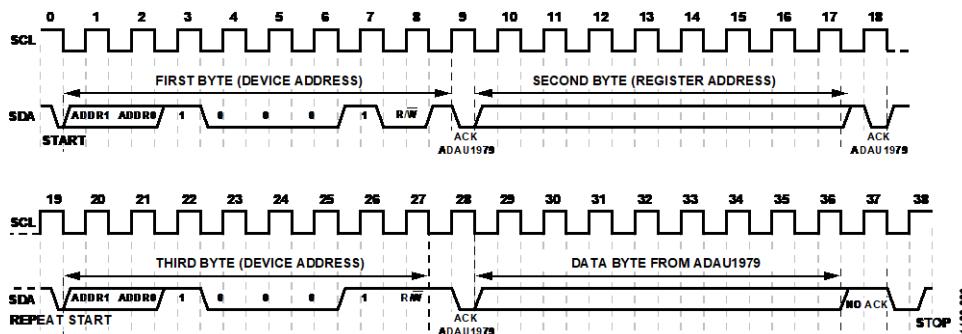


Figure 34. I²C Read from ADAU1979 Single Byte

I²C Read and Write Operations

Figure 35 shows the format of a single-word I²C write operation. Every ninth clock pulse, the ADAU1979 issues an acknowledge by pulling SDA low.

Figure 36 shows the format of a burst mode I²C write sequence. This figure shows an example of a write to sequential single-byte registers. The ADAU1979 increments its address register after every byte because the requested address corresponds to a register or memory area with a 1-byte word length.

Figure 37 shows the format of a single-word I²C read operation. Note that the first R/W bit is 0, indicating a write operation. This is because the address still needs to be written to set up the internal address. After the ADAU1979 acknowledges the receipt of the address, the master must

issue a repeated start command followed by the chip address byte with the R/W bit set to 1 (read). This causes the ADAU1979 SDA to reverse and begin driving data back to the master. The master then responds every ninth pulse with an acknowledge pulse to the ADAU1979.

Figure 38 shows the format of a burst mode I²C read sequence. This figure shows an example of a read from sequential single-byte registers. The ADAU1979 increments its address registers after every byte because the ADAU1979 uses an 8-bit register address.

Figure 35 to Figure 38 use the following abbreviations:

S = start bit

P = stop bit

AM = acknowledge by master

AS = acknowledge by slave

S	CHIP ADDRESS, R/W = 0	AS	REGISTER ADDRESS 8 BITS	AS	DATA BYTE		P
---	--------------------------	----	----------------------------	----	-----------	--	---

11408-037

Figure 35. Single-Word I²C Write Format

S	CHIP ADDRESS, R/W = 0	AS	REGISTER ADDRESS 8 BITS	CHIP ADDRESS, R/W = 0	AS	DATA BYTE 1	AS	DATA BYTE 2	AS	DATA BYTE 3	AS	DATA BYTE 4	AS	...	P
---	-----------------------------	----	-------------------------------	-----------------------------	----	----------------	----	----------------	----	----------------	----	----------------	----	-----	---

11408-038

Figure 36. Burst Mode I²C Write Format

S	CHIP ADDRESS, R/W = 0	AS	REGISTER ADDRESS 8 BITS	AS	S	CHIP ADDRESS, R/W = 1	AS	DATA BYTE 1	P
---	-----------------------------	----	-------------------------------	----	---	-----------------------------	----	----------------	---

11408-039

Figure 37. Single-Word I²C Read Format

S	CHIP ADDRESS, R/W = 0	AS	REGISTER ADDRESS 8 BITS	AS	S	CHIP ADDRESS, R/W = 1	AS	DATA BYTE 1	AM	DATA BYTE 2	AM	...	P
---	-----------------------------	----	-------------------------------	----	---	-----------------------------	----	----------------	----	----------------	----	-----	---

11408-040

Figure 38. Burst Mode I²C Read Format

SPI MODE

By default, the ADAU1979 is in I²C mode. To invoke SPI control mode, pull CLATCH low three times. This is achieved by performing three dummy writes to the SPI port (the ADAU1979 does not acknowledge these three writes, see Figure 39). Beginning with the fourth SPI write, data can be written to or read from the device. The ADAU1979 can be taken out of SPI mode only by a full reset initiated by power cycling the device.

The SPI port uses a 4-wire interface, consisting of the CLATCH, CCLK, CIN, and COUT signals, and it is always a slave port. The CLATCH signal goes low at the beginning of a transaction and high at the end of a transaction. The CCLK signal latches COUT on a low-to-high transition. COUT data is shifted out of the ADAU1979 on the falling edge of CCLK and is clocked into a receiving device, such as a microcontroller, on the CCLK rising edge. The CIN signal carries the serial input data, and the COUT signal carries the serial output data. The COUT signal remains tristated until a read operation is requested. This allows direct connection to other SPI-compatible peripheral COUT ports for sharing the same system controller port. All SPI transactions have the same basic generic control word format, as shown in Table 15. A timing diagram is shown in Figure 3. Write all data MSB first.

Chip Address R/W

The LSB of the first byte of an SPI transaction is a R/W bit. This bit determines whether the communication is a read (Logic Level 1) or a write (Logic Level 0). This format is shown in Table 13.

Table 13. SPI Address and R/W Byte Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	R/W

Register Address

The 8-bit address word is decoded to a location in one of the registers. This address is the location of the appropriate register.

Data Bytes

The number of data bytes varies according to the register being accessed. During a burst mode SPI write, an initial register address is written followed by a continuous sequence of data for consecutive register locations.

A sample timing diagram for a single-word SPI write operation to a register is shown in Figure 40. A sample timing diagram of a single-word SPI read operation is shown in Figure 41. The COUT pin transitions being high-Z to being driven at the beginning of Byte 3. In this example, Byte 0 to Byte 1 contain the device address, the R/W bit, and the register address to be read. Subsequent bytes carry the data from the device.

Standalone Mode

The ADAU1979 can also operate in standalone mode. However, in standalone mode, the boost converter, microphone bias, and diagnostics blocks are powered down. To set the device in standalone mode, pull the SA_MODE pin to IOVDD. In this mode, some pins change functionality to provide more flexibility (see Table 14 for more information).

Table 14. Pin Functionality in Standalone Mode

Pin Function ¹	Setting	Description
ADDR0	0	I ² S SAI format
	1	TDM modes, determined by the SDATAOUT2 pin
ADDR1	0	Master mode SAI
	1	Slave mode SAI
SDA	0	MCLK = 256 × f _s , PLL on
	1	MCLK = 384 × f _s , PLL on
SCL	0	48 kHz sample rate
	1	96 kHz sample rate
SDATAOUT2	0	TDM4—LRCLK pulse
	1	TDM8—LRCLK pulse

¹ Pin functionality, not full pin names, is listed. See Table 12 for additional information.

Table 15. Generic Control Word Format

Byte 0	Byte 1	Byte 2	Byte 3 ¹
Device Address[6:0], R/W	Register Address[7:0]	Data[7:0]	Data[7:0]

¹ Continues to end of data.

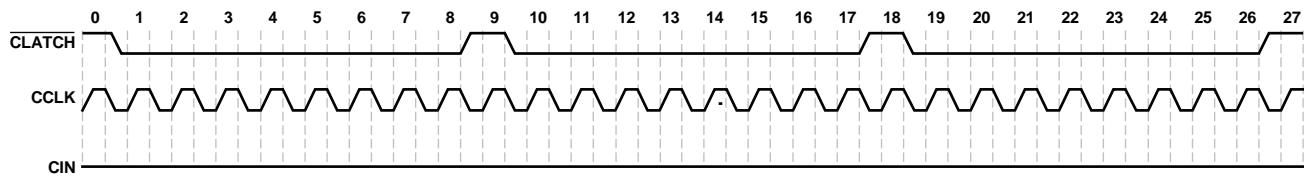


Figure 39. SPI Mode Initial Sequence

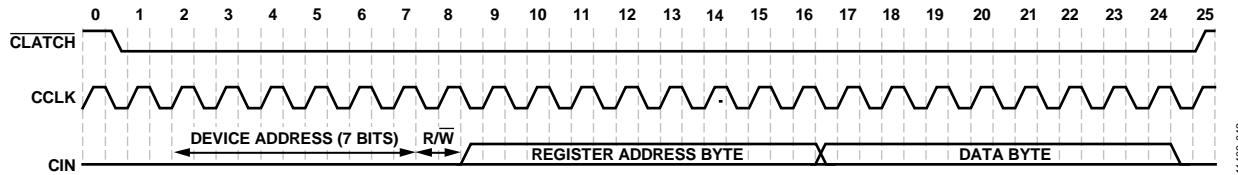


Figure 40. SPI Write to ADAU1979 Clocking (Single-Word Write Mode)

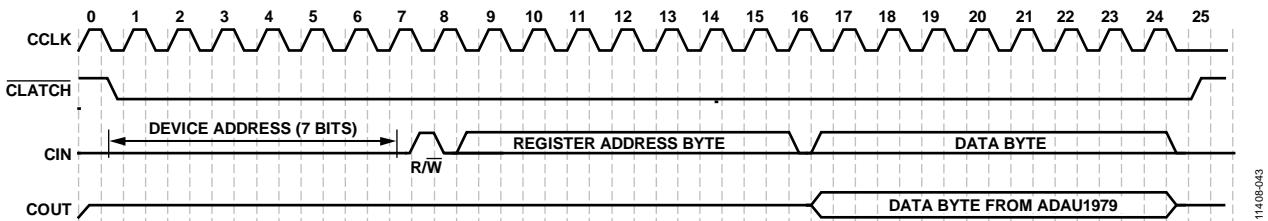


Figure 41. SPI Read from ADAU1979 Clocking (Single-Word Read Mode)

PRELIMINARY

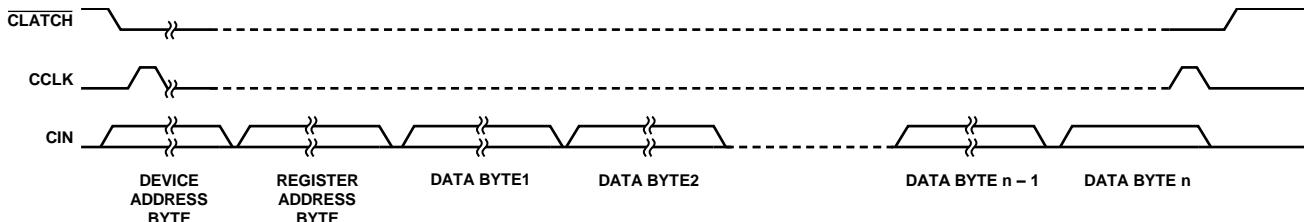


Figure 42. SPI Write to ADAU1979 (Multiple Bytes)

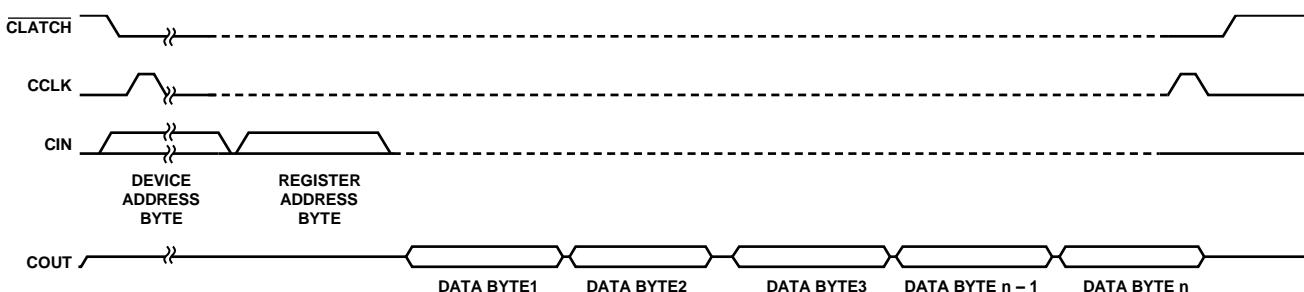


Figure 43. SPI Read from ADAU1979 (Multiple Bytes)

REGISTER SUMMARY

Table 16. REGMAP ADAU1979 Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW			
0x00	M_POWER	[7:0]	S_RST	RESERVED				PWUP			0x00	RW			
0x01	PLL_CONTROL	[7:0]	PLL_LOCK	PLL_MUTE	RESERVED	CLK_S	RESERVED	MCS			0x41	RW			
0x02	RESERVED	[7:0]	RESERVED				Reserved				Reserved	Reserved			
0x03	RESERVED	[7:0]	RESERVED				Reserved				Reserved	Reserved			
0x04	BLOCK_POWER_SAI	[7:0]	LR_POL	BCLKEDGE	LDO_EN	VREF_EN	ADC_EN4	ADC_EN3	ADC_EN2	ADC_EN1	0x3F	RW			
0x05	SAI_CTRL0	[7:0]	SDATA_FMT			SAI		FS			0x02	RW			
0x06	SAI_CTRL1	[7:0]	SDATA_SEL	SLOT_WIDTH		DATA_WIDTH	LR_MODE	SAI_MSB	BCLKRATE	SAI_MS	0x00	RW			
0x07	SAI_CMAP12	[7:0]	CMAP_C2				CMAP_C1				0x10	RW			
0x08	SAI_CMAP34	[7:0]	CMAP_C4				CMAP_C3				0x32	RW			
0x09	SAI_OVERTEMP	[7:0]	SAI_DRV_C4	SAI_DRV_C3	SAI_DRV_C2	SAI_DRV_C1	DRV_HIZ	RESERVED	RESERVED	OT	0xF0	RW			
0x0A	POSTADC_GAIN1	[7:0]	PADC_GAIN1				PADC_GAIN1				0xA0	RW			
0x0B	POSTADC_GAIN2	[7:0]	PADC_GAIN2				PADC_GAIN2				0xA0	RW			
0x0C	POSTADC_GAIN3	[7:0]	PADC_GAIN3				PADC_GAIN3				0xA0	RW			
0x0D	POSTADC_GAIN4	[7:0]	PADC_GAIN4				PADC_GAIN4				0xA0	RW			
0x0E	MISC_CONTROL	[7:0]	SUM_MODE		RESERVED	MMUTE	RESERVED			DC_CAL	0x02	RW			
0x0F	RESERVED	[7:0]	RESERVED		RESERVED		RESERVED		RESERVED		0xFF	RW			
0x10	RESERVED	[7:0]	RESERVED				RESERVED	RESERVED	RESERVED	RESERVED	0x0F	RW			
0x11	RESERVED	[7:0]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	0x00	RW			
0x12	RESERVED	[7:0]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	0x00	RW			
0x13	RESERVED	[7:0]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	0x00	RW			
0x14	RESERVED	[7:0]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	0x00	RW			
0x15	RESERVED	[7:0]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	0x20	RW			
0x16	RESERVED	[7:0]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	0x00	RW			
0x17	RESERVED	[7:0]	RESERVED		RESERVED		RESERVED		RESERVED		Reserved	Reserved			
0x18	RESERVED	[7:0]	RESERVED		RESERVED		RESERVED	RESERVED	RESERVED	RESERVED	Reserved	Reserved			
0x19	ASDC_CLIP	[7:0]	RESERVED				ADC_CLIP4	ADC_CLIP3	ADC_CLIP2	ADC_CLIP1	0x00	RW			
0x1A	DC_HPF_CAL	[7:0]	DC_SUB_C4	DC_SUB_C3	DC_SUB_C2	DC_SUB_C1	DC_HPF_C4	DC_HPF_C3	DC_HPF_C2	DC_HPF_C1	0x00	RW			

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REGISTER DETAILS

MASTER POWER AND SOFT RESET REGISTER

Address: 0x00, **Reset:** 0x00, **Name:** M_POWER

The power management control register enables the boost regulator, microphone bias, PLL, band gap reference, ADC, and LDO regulator.

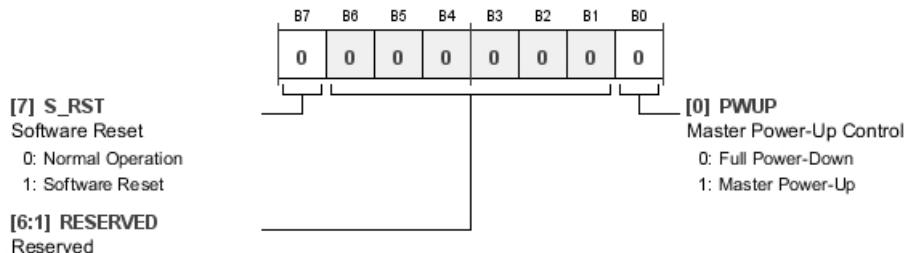


Table 17. Bit Descriptions for M_POWER

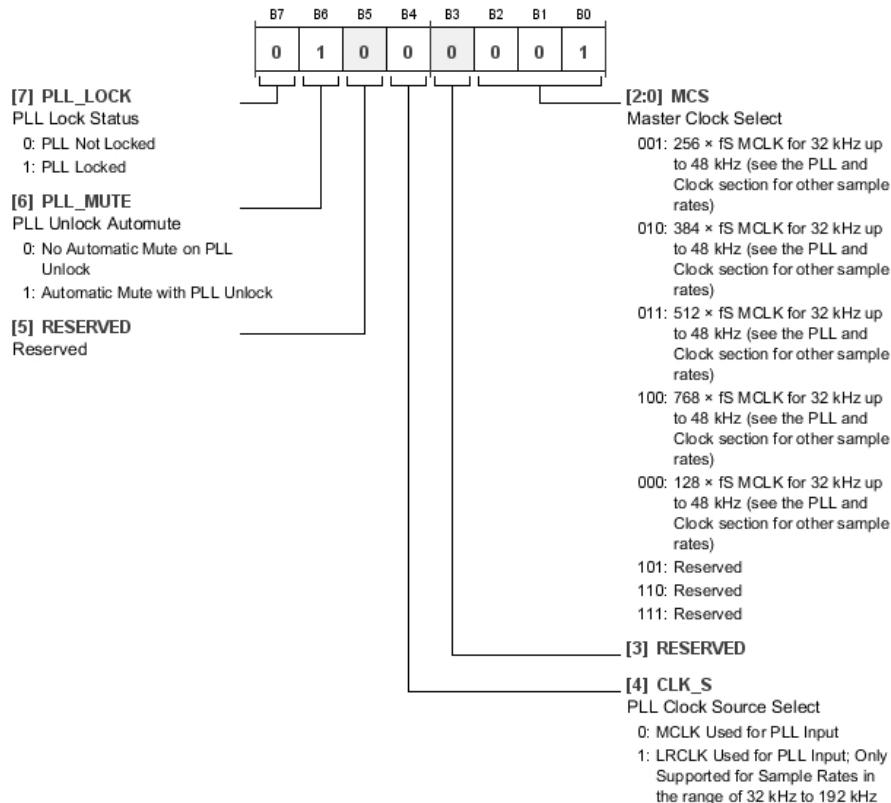
Bits	Bit Name	Settings	Description	Reset	Access
7	S_RST		Software Reset. The software reset resets all internal circuitry and all control registers to their respective default states. It is not necessary to reset the ADAU1979 during a power-up or power-down cycle. 0: Normal Operation. 1: Software Reset.	0x0	RW
[6:1]	RESERVED		Reserved.	0x00	RW
0	PWUP		Master Power-Up Control. The master power-up control fully powers up or powers down the ADAU1979. This must be set to 1 to power up the ADAU1979. Individual blocks can be powered down via their respective power control registers. 0: Full Power-Down. 1: Master Power-Up.	0x0	RW

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PRELIMINARY

PLL CONTROL REGISTER

Address: 0x01, Reset: 0x41, Name: PLL_CONTROL

**Table 18. Bit Descriptions for PLL_CONTROL**

Bits	Bit Name	Settings	Description	Reset	Access
7	PLL_LOCK	0 1	PLL Lock Status. PLL lock status bit. When set to 1, the PLL is locked. PLL Not Locked. PLL Locked.	0x0	R
6	PLL_MUTE	0 1	PLL Unlock Automute. When set to 1, it mutes the ADC output if PLL becomes unlocked. No Automatic Mute on PLL Unlock. Automatic Mute with PLL Unlock.	0x1	RW
5	RESERVED	-	Reserved.	0x0	RW
4	CLK_S	0 1	PLL Clock Source Select. Selecting input clock source for PLL. MCLK Used for PLL Input. LRCLK Used for PLL Input; Only Supported for Sample Rates in the Range of 32 kHz to 192 kHz.	0x0	RW
3	RESERVED	-	Reserved.	0x0	RW
[2:0]	MCS	001 010 011	Master Clock Select. MCS bits determine the frequency multiplication ratio of the PLL. It must be set based on the input MCLK frequency and sample rate. 256 × f _s MCLK for 32 kHz up to 48 kHz (see the PLL and Clock section for other sample rates). 384 × f _s MCLK for 32 kHz up to 48 kHz (see the PLL and Clock section for other sample rates). 512 × f _s MCLK for 32 kHz up to 48 kHz (see the PLL and Clock section for other sample rates).	0x1	RW

Bits	Bit Name	Settings	Description	Reset	Access
		100	768 × f_s MCLK for 32 kHz up to 48 kHz (see the PLL and Clock section for other sample rates).		
		000	128 × f_s MCLK for 32 kHz up to 48 kHz (see the PLL and Clock section for other sample rates).		
		101	Reserved.		
		110	Reserved.		
		111	Reserved.		

BLOCK POWER CONTROL AND SERIAL PORT CONTROL REGISTER

Address: 0x04, Reset: 0x3F, Name: BLOCK_POWER_SAI

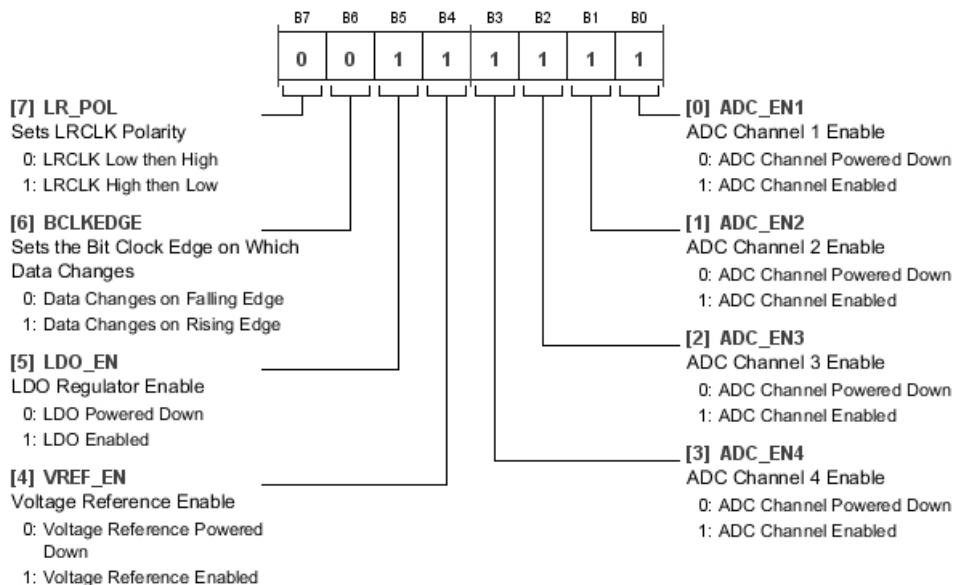


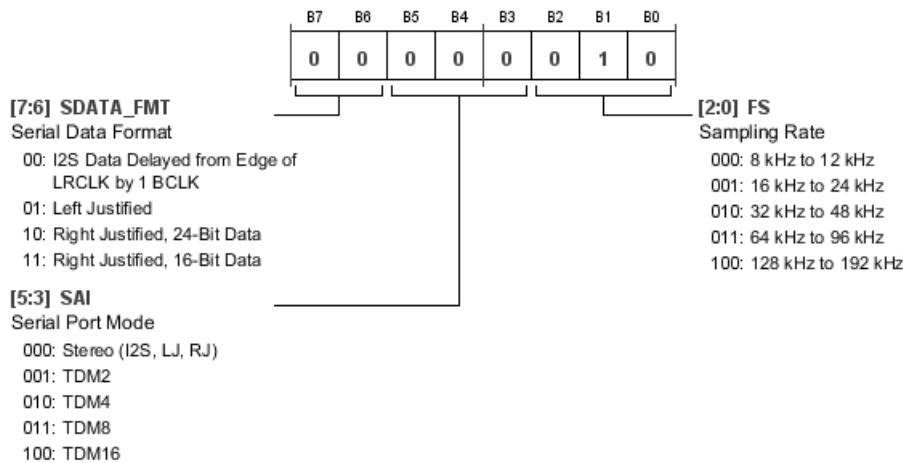
Table 19. Bit Descriptions for BLOCK_POWER_SAI

Bits	Bit Name	Settings	Description	Reset	Access
7	LR_POL	0 1	Sets LRCLK Polarity LRCLK Low then High LRCLK High then Low	0x0	RW
6	BCLKEDGE	0 1	Sets the Bit Clock Edge on Which Data Changes Data Changes on Falling Edge Data Changes on Rising Edge	0x0	RW
5	LDO_EN	0 1	LDO Regulator Enable LDO Powered Down LDO Enabled	0x1	RW
4	VREF_EN	0 1	Voltage Reference Enable Voltage Reference Powered Down Voltage Reference Enabled	0x1	RW
3	ADC_EN4	0 1	ADC Channel 4 Enable ADC Channel Powered Down ADC Channel Enabled	0x1	RW
2	ADC_EN3	0	ADC Channel 3 Enable ADC Channel Powered Down	0x1	RW

Bits	Bit Name	Settings	Description	Reset	Access
		1	ADC Channel Enabled		
1	ADC_EN2	0	ADC Channel 2 Enable	0x1	RW
		1	ADC Channel Powered Down		
0	ADC_EN1	0	ADC Channel 1 Enable	0x1	RW
		1	ADC Channel Powered Down		
		1	ADC Channel Enabled		

SERIAL PORT CONTROL REGISTER 1

Address: 0x05, Reset: 0x02, Name: SAI_CTRL0

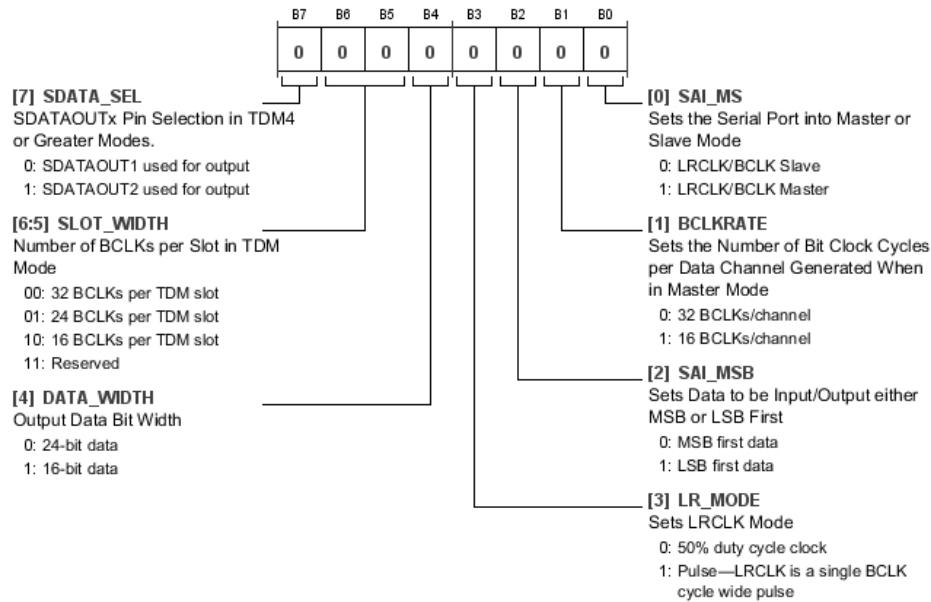
**Table 20. Bit Descriptions for SAI_CTRL0**

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	SDATA_FMT	00 01 10 11	Serial Data Format I ² S Data Delayed from Edge of LRCLK by 1 BCLK Left Justified Right Justified, 24-Bit Data Right Justified, 16-Bit Data	0x0	RW
[5:3]	SAI	000 001 010 011 100	Serial Port Mode Stereo (I ² S, LJ, RJ) TDM2 TDM4 TDM8 TDM16	0x0	RW
[2:0]	FS	000 001 010 011 100	Sampling Rate 8 kHz to 12 kHz 16 kHz to 24 kHz 32 kHz to 48 kHz 64 kHz to 96 kHz 128 kHz to 192 kHz	0x2	RW

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SERIAL PORT CONTROL REGISTER 2

Address: 0x06, Reset: 0x00, Name: SAI_CTRL1

**Table 21. Bit Descriptions for SAI_CTRL1**

Bits	Bit Name	Settings	Description	Reset	Access
7	SDATA_SEL	0	SDATAOUTx Pin Selection in TDM4 or Greater Modes	0x0	RW
		1	SDATAOUT1 used for output		
		1	SDATAOUT2 used for output		
[6:5]	SLOT_WIDTH	00	Number of BCLKs per Slot in TDM Mode	0x0	RW
		01	32 BCLKs per TDM slot		
		10	24 BCLKs per TDM slot		
		11	16 BCLKs per TDM slot		
		Reserved			
4	DATA_WIDTH	0	Output Data Bit Width	0x0	RW
		1	24-bit data		
		1	16-bit data		
3	LR_MODE	0	Sets LRCLK Mode	0x0	RW
		1	50% duty cycle clock		
		1	Pulse—LRCLK is a single BCLK cycle wide pulse		
2	SAI_MSB	0	Sets Data to be Input/Output Either MSB or LSB First	0x0	RW
		1	MSB first data		
		1	LSB first data		
1	BCLKRATE	0	Sets the Number of Bit Clock Cycles per Data Channel Generated When in Master Mode	0x0	RW
		0	32 BCLKs/channel		
		1	16 BCLKs/channel		
0	SAI_MS	0	Sets the Serial Port into Master or Slave Mode	0x0	RW
		1	LRCLK/BCLK slave		
		1	LRCLK/BCLK master		

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CHANNEL 1 AND CHANNEL 2 MAPPING FOR OUTPUT SERIAL PORTS REGISTER

Address: 0x07, Reset: 0x10, Name: SAI_CMAP12

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	1	0	0	0	0
[7:4] CMAP_C2				[3:0] CMAP_C1			
ADC Channel 2 Output Mapping						ADC Channel 1 Output Mapping	
0000: Slot 1 for Channel				0000: Slot 1 for Channel			
0001: Slot 2 for Channel				0001: Slot 2 for Channel			
0010: Slot 3 for Channel (on SDATAOUT2 in stereo modes)				0010: Slot 3 for Channel (on SDATAOUT2 in stereo modes)			
0011: Slot 4 for Channel (on SDATAOUT2 in stereo modes)				0011: Slot 4 for Channel (on SDATAOUT2 in stereo modes)			
0100: Slot 5 for Channel (TDM8+ only)				0100: Slot 5 for Channel (TDM8+ only)			
0101: Slot 6 for Channel (TDM8+ only)				0101: Slot 6 for Channel (TDM8+ only)			
0110: Slot 7 for Channel (TDM8+ only)				0110: Slot 7 for Channel (TDM8+ only)			
0111: Slot 8 for Channel (TDM8+ only)				0111: Slot 8 for Channel (TDM8+ only)			
1000: Slot 9 for Channel (TDM16 only)				1000: Slot 9 for Channel (TDM16 only)			
1001: Slot 10 for Channel (TDM16 only)				1001: Slot 10 for Channel (TDM16 only)			
1010: Slot 11 for Channel (TDM16 only)				1010: Slot 11 for Channel (TDM16 only)			
1011: Slot 12 for Channel (TDM16 only)				1011: Slot 12 for Channel (TDM16 only)			
1100: Slot 13 for Channel (TDM16 only)				1100: Slot 13 for Channel (TDM16 only)			
1101: Slot 14 for Channel (TDM16 only)				1101: Slot 14 for Channel (TDM16 only)			
1110: Slot 15 for Channel (TDM16 only)				1110: Slot 15 for Channel (TDM16 only)			
1111: Slot 16 for Channel (TDM16 only)				1111: Slot 16 for Channel (TDM16 only)			

Table 22. Bit Descriptions for SAI_CMAP12

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	CMAP_C2	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110	ADC Channel 2 Output Mapping. Slot 1 for Channel Slot 2 for Channel Slot 3 for Channel (on SDATAOUT2 in stereo modes) Slot 4 for Channel (on SDATAOUT2 in stereo modes) Slot 5 for Channel (TDM8+ only) Slot 6 for Channel (TDM8+ only) Slot 7 for Channel (TDM8+ only) Slot 8 for Channel (TDM8+ only) Slot 9 for Channel (TDM16 only) Slot 10 for Channel (TDM16 only) Slot 11 for Channel (TDM16 only) Slot 12 for Channel (TDM16 only) Slot 13 for Channel (TDM16 only) Slot 14 for Channel (TDM16 only) Slot 15 for Channel (TDM16 only)	0x1	RW

Bits	Bit Name	Settings	Description	Reset	Access
		1111	Slot 16 for Channel (TDM16 only)		
[3:0]	CMAP_C1	0000	Slot 1 for Channel	0x0	RW
		0001	Slot 2 for Channel		
		0010	Slot 3 for Channel (on SDATAOUT2 in stereo modes)		
		0011	Slot 4 for Channel (on SDATAOUT2 in stereo modes)		
		0100	Slot 5 for Channel (TDM8+ only)		
		0101	Slot 6 for Channel (TDM8+ only)		
		0110	Slot 7 for Channel (TDM8+ only)		
		0111	Slot 8 for Channel (TDM8+ only)		
		1000	Slot 9 for Channel (TDM16 only)		
		1001	Slot 10 for Channel (TDM16 only)		
		1010	Slot 11 for Channel (TDM16 only)		
		1011	Slot 12 for Channel (TDM16 only)		
		1100	Slot 13 for Channel (TDM16 only)		
		1101	Slot 14 for Channel (TDM16 only)		
		1110	Slot 15 for Channel (TDM16 only)		
		1111	Slot 16 for Channel (TDM16 only)		

PRELIMINARY

CHANNEL 3 AND CHANNEL 4 MAPPING FOR OUTPUT SERIAL PORTS REGISTER

Address: 0x08, Reset: 0x32, Name: SAI_CMAP34

B7	B6	B5	B4	B3	B2	B1	B0
[7:4] CMAP_C4				[3:0] CMAP_C3			
ADC Channel 4 Output Mapping				ADC Channel 3 Output Mapping			
0000: Slot 1 for Channel	0001: Slot 2 for Channel	0010: Slot 3 for Channel (on SDATAOUT2 in stereo modes)	0011: Slot 4 for Channel (on SDATAOUT2 in stereo modes)	0000: Slot 1 for Channel	0001: Slot 2 for Channel	0010: Slot 3 for Channel (on SDATAOUT2 in stereo modes)	0011: Slot 4 for Channel (on SDATAOUT2 in stereo modes)
0100: Slot 5 for Channel (TDM8+ only)	0101: Slot 6 for Channel (TDM8+ only)	0110: Slot 7 for Channel (TDM8+ only)	0111: Slot 8 for Channel (TDM8+ only)	0100: Slot 5 for Channel (TDM8+ only)	0101: Slot 6 for Channel (TDM8+ only)	0110: Slot 7 for Channel (TDM8+ only)	0111: Slot 8 for Channel (TDM8+ only)
1000: Slot 9 for Channel (TDM16 only)	1001: Slot 10 for Channel (TDM16 only)	1010: Slot 11 for Channel (TDM16 only)	1011: Slot 12 for Channel (TDM16 only)	1000: Slot 9 for Channel (TDM16 only)	1001: Slot 10 for Channel (TDM16 only)	1010: Slot 11 for Channel (TDM16 only)	1011: Slot 12 for Channel (TDM16 only)
1100: Slot 13 for Channel (TDM16 only)	1101: Slot 14 for Channel (TDM16 only)	1110: Slot 15 for Channel (TDM16 only)	1111: Slot 16 for Channel (TDM16 only)	1100: Slot 13 for Channel (TDM16 only)	1101: Slot 14 for Channel (TDM16 only)	1110: Slot 15 for Channel (TDM16 only)	1111: Slot 16 for Channel (TDM16 only)

Table 23. Bit Descriptions for SAI_CMAP34

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	CMAP_C4		ADC Channel 4 Output Mapping 0000: Slot 1 for Channel 0001: Slot 2 for Channel 0010: Slot 3 for Channel (on SDATAOUT2 in stereo modes) 0011: Slot 4 for Channel (on SDATAOUT2 in stereo modes) 0100: Slot 5 for Channel (TDM8+ only) 0101: Slot 6 for Channel (TDM8+ only) 0110: Slot 7 for Channel (TDM8+ only) 0111: Slot 8 for Channel (TDM8+ only) 1000: Slot 9 for Channel (TDM16 only) 1001: Slot 10 for Channel (TDM16 only) 1010: Slot 11 for Channel (TDM16 only) 1011: Slot 12 for Channel (TDM16 only) 1100: Slot 13 for Channel (TDM16 only) 1101: Slot 14 for Channel (TDM16 only)	0x3	RW

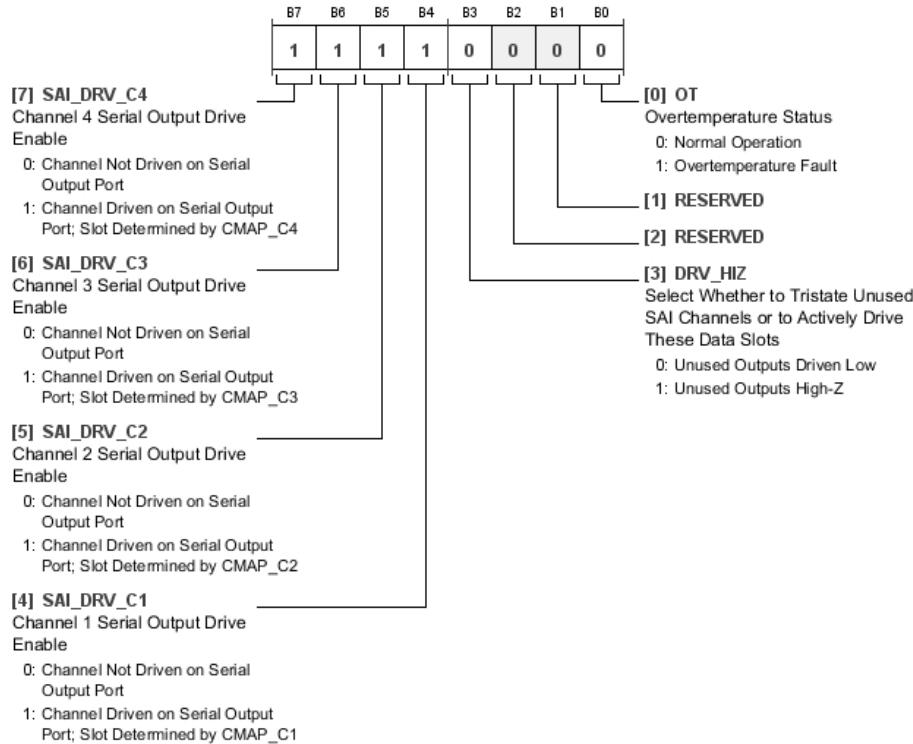
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Bits	Bit Name	Settings	Description	Reset	Access
		1110 1111	Slot 15 for Channel (TDM16 only) Slot 16 for Channel (TDM16 only)		
[3:0]	CMAP_C3	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	ADC Channel 3 Output Mapping Slot 1 for Channel Slot 2 for Channel Slot 3 for Channel (on SDATAOUT2 in stereo modes) Slot 4 for Channel (on SDATAOUT2 in stereo modes) Slot 5 for Channel (TDM8+ only) Slot 6 for Channel (TDM8+ only) Slot 7 for Channel (TDM8+ only) Slot 8 for Channel (TDM8+ only) Slot 9 for Channel (TDM16 only) Slot 10 for Channel (TDM16 only) Slot 11 for Channel (TDM16 only) Slot 12 for Channel (TDM16 only) Slot 13 for Channel (TDM16 only) Slot 14 for Channel (TDM16 only) Slot 15 for Channel (TDM16 only) Slot 16 for Channel (TDM16 only)	0x2	RW

PRELIMINARY

SERIAL OUTPUT DRIVE CONTROL AND OVERTEMPERATURE PROTECTION STATUS REGISTER

Address: 0x09, Reset: 0xF0, Name: SAI_OVERTEMP

**Table 24. Bit Descriptions for SAI_OVERTEMP**

Bits	Bit Name	Settings	Description	Reset	Access
7	SAI_DRV_C4	0 1	Channel 4 Serial Output Drive Enable. Channel Not Driven on Serial Output Port. Channel Driven on Serial Output Port. Slot determined by CMAP_C4.	0x1	RW
6	SAI_DRV_C3	0 1	Channel 3 Serial Output Drive Enable. Channel Not Driven on Serial Output Port. Channel Driven on Serial Output Port. Slot determined by CMAP_C3.	0x1	RW
5	SAI_DRV_C2	0 1	Channel 2 Serial Output Drive Enable. Channel Not Driven on Serial Output Port. Channel Driven on Serial Output Port. Slot determined by CMAP_C2.	0x1	RW
4	SAI_DRV_C1	0 1	Channel 1 Serial Output Drive Enable. Channel Not Driven on Serial Output Port. Channel Driven on Serial Output Port. Slot determined by CMAP_C1.	0x1	RW
3	DRV_HIZ	0 1	Select Whether to Tristate Unused SAI Channels or Actively Drive These Data Slots. Unused outputs driven low. Unused outputs high-Z.	0x0	RW
[2:1]	RESERVED		Reserved	0x0	R
0	OT	0 1	Overtemperature Status Normal Operation. Overtemperature Fault.	0x0	R

PRELIMINARY

POST ADC GAIN CHANNEL 1 CONTROL REGISTER

Address: 0x0A, Reset: 0xA0, Name: POSTADC_GAIN1

B7	B6	B5	B4	B3	B2	B1	B0
1	0	1	0	0	0	0	0

[7:0] PADC_GAIN1
 Channel 1 Post ADC Gain
 00000000: +60 dB Gain
 00000001: +59.625 dB Gain
 00000010: +59.25 dB Gain
 ...
 10011111: +0.375 dB Gain
 10100000: 0 dB Gain
 10100001: -0.375 dB Gain
 ...
 11111110: -35.625 dB Gain
 11111111: Mute

Table 25. Bit Descriptions for POSTADC_GAIN1

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PADC_GAIN1	00000000 00000001 00000010 ... 10011111 10100000 10100001 ... 11111110 11111111	Channel 1 Post ADC Gain +60 dB Gain +59.625 dB Gain +59.25 dB Gain ... +0.375 dB Gain 0 dB Gain -0.375 dB Gain ... -35.625 dB Gain Mute	0xA0	RW

PRELIMINARY

POST ADC GAIN CHANNEL 2 CONTROL REGISTER

Address: 0x0B, Reset: 0xA0, Name: POSTADC_GAIN2

B7	B6	B5	B4	B3	B2	B1	B0
1	0	1	0	0	0	0	0

[7:0] PADC_GAIN2
 Channel 2 Post ADC Gain
 00000000: +60 dB Gain
 00000001: +59.625 dB Gain
 00000010: +59.25 dB Gain
 ...
 10011111: +0.375 dB Gain
 10100000: 0 dB Gain
 10100001: -0.375 dB Gain
 ...
 11111110: -35.625 dB Gain
 11111111: Mute

Table 26. Bit Descriptions for POSTADC_GAIN2

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PADC_GAIN2	00000000 00000001 00000010 ... 10011111 10100000 10100001 ... 11111110 11111111	Channel 2 Post ADC Gain +60 dB Gain +59.625 dB Gain +59.25 dB Gain ... +0.375 dB Gain 0 dB Gain -0.375 dB Gain ... -35.625 dB Gain Mute	0xA0	RW

POST ADC GAIN CHANNEL 3 CONTROL REGISTER

Address: 0x0C, Reset: 0xA0, Name: POSTADC_GAIN3

B7	B6	B5	B4	B3	B2	B1	B0
1	0	1	0	0	0	0	0

[7:0] PADC_GAIN3
 Channel 3 Post ADC Gain
 00000000: +60 dB Gain
 00000001: +59.625 dB Gain
 00000010: +59.25 dB Gain
 ...
 10011111: +0.375 dB Gain
 10100000: 0 dB Gain
 10100001: -0.375 dB Gain
 ...
 11111110: -35.625 dB Gain
 11111111: Mute

Table 27. Bit Descriptions for POSTADC_GAIN3

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PADC_GAIN3	00000000 00000001 00000010 ... 10011111 10100000 10100001 ... 11111110 11111111	Channel 3 Post ADC Gain +60 dB Gain +59.625 dB Gain +59.25 dB Gain ... +0.375 dB Gain 0 dB Gain -0.375 dB Gain ... -35.625 dB Gain Mute	0xA0	RW

PRELIMINARY

POST ADC GAIN CHANNEL 4 CONTROL REGISTER

Address: 0x0D, Reset: 0xA0, Name: POSTADC_GAIN4

B7	B6	B5	B4	B3	B2	B1	B0
1	0	1	0	0	0	0	0

[7:0] PADC_GAIN4
 Channel 4 Post ADC Gain
 00000000: +60 dB Gain
 00000001: +59.625 dB Gain
 00000010: +59.25 dB Gain
 ...
 10011111: +0.375 dB Gain
 10100000: 0 dB Gain
 10100001: -0.375 dB Gain
 ...
 11111110: -35.625 dB Gain
 11111111: Mute

Table 28. Bit Descriptions for POSTADC_GAIN4

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PADC_GAIN4	00000000 00000001 00000010 ... 10011111 10100000 10100001 ... 11111110 11111111	Channel 4 Post ADC Gain. +60 dB Gain +59.625 dB Gain +59.25 dB Gain ... +0.375 dB Gain 0 dB Gain -0.375 dB Gain ... -35.625 dB Gain Mute	0xA0	RW

HIGH-PASS FILTER AND DC OFFSET CONTROL REGISTER AND MASTER MUTE REGISTER

Address: 0x0E, Reset: 0x02, Name: MISC_CONTROL

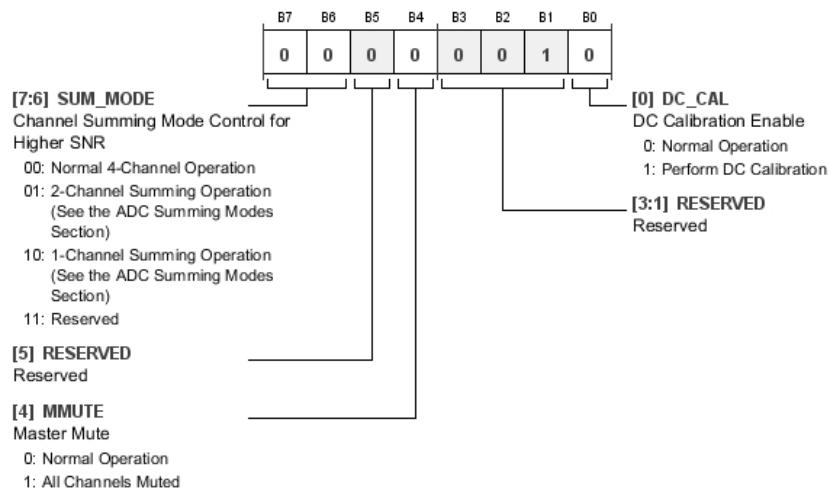
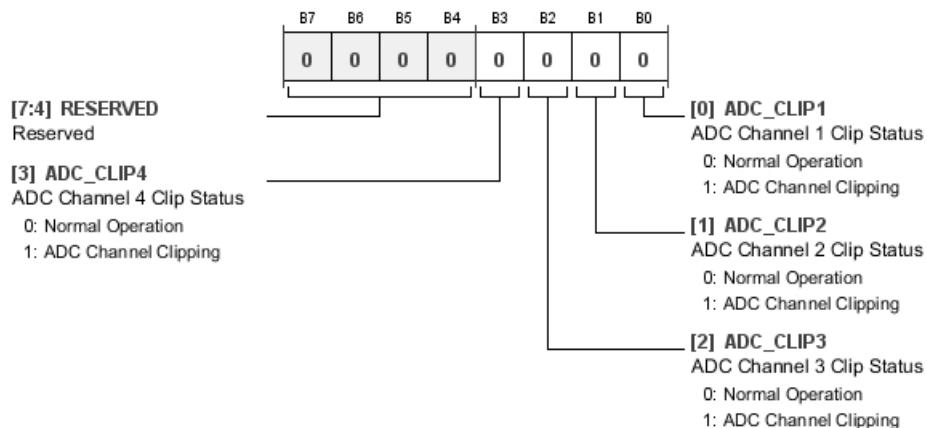


Table 29. Bit Descriptions for MISC_CONTROL

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	SUM_MODE	00 01 10 11	Channel Summing Mode Control for Higher SNR Normal 4-Channel Operation 2-Channel Summing Operation (See the ADC Summing Modes Section) 1-Channel Summing Operation (See the ADC Summing Modes Section) Reserved	0x0	RW
5	RESERVED		Reserved	0x0	RW
4	MMUTE	0 1	Master Mute Normal Operation All Channels Muted	0x0	RW
[3:1]	RESERVED		Reserved	0x0	RW
0	DC_CAL	0 1	DC Calibration Enable Normal Operation Perform DC Calibration	0x0	RW

ADC CLIPPING STATUS REGISTER

Address: 0x19, Reset: 0x00, Name: ASDC_CLIP

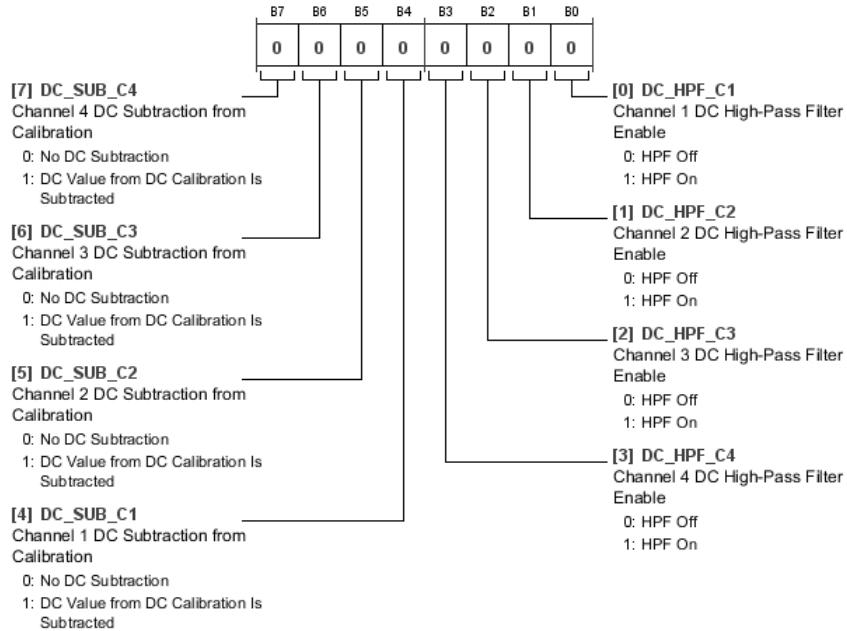
**Table 30. Bit Descriptions for ASDC_CLIP**

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved	0x0	RW
3	ADC_CLIP4	0 1	ADC Channel 4 Clip Status Normal Operation ADC Channel Clipping	0x0	R
2	ADC_CLIP3	0 1	ADC Channel 3 Clip Status Normal Operation ADC Channel Clipping	0x0	R
1	ADC_CLIP2	0 1	ADC Channel 2 Clip Status Normal Operation ADC Channel Clipping	0x0	R
0	ADC_CLIP1	0 1	ADC Channel 1 Clip Status Normal Operation ADC Channel Clipping	0x0	R

PRELIMINARY

DIGITAL DC HIGH-PASS FILTER AND CALIBRATION REGISTER

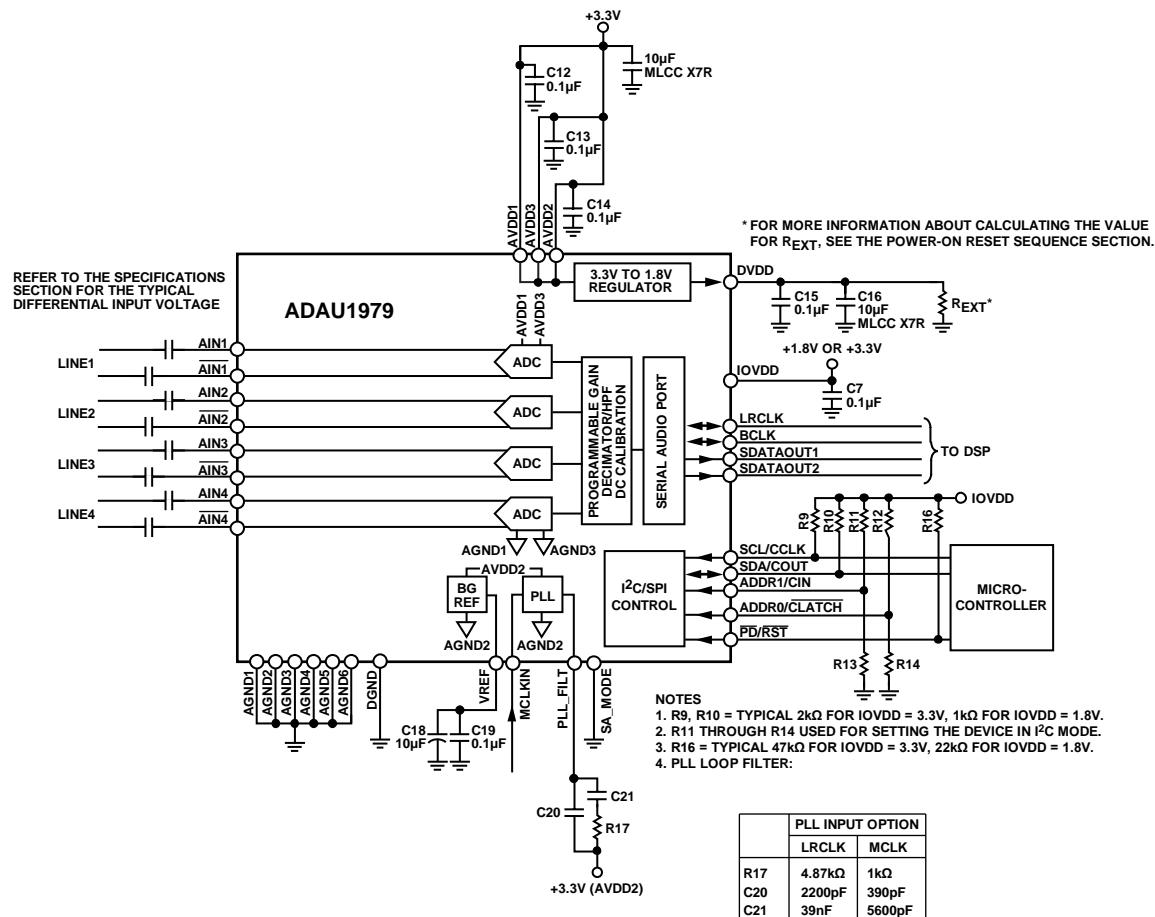
Address: 0x1A, Reset: 0x00, Name: DC_HPF_CAL

**Table 31. Bit Descriptions for DC_HPF_CAL**

Bits	Bit Name	Settings	Description	Reset	Access
7	DC_SUB_C4	0 1	Channel 4 DC Subtraction from Calibration No DC Subtraction DC Value from DC Calibration Is Subtracted	0x0	RW
6	DC_SUB_C3	0 1	Channel 3 DC Subtraction from Calibration No DC Subtraction DC Value from DC Calibration Is Subtracted	0x0	RW
5	DC_SUB_C2	0 1	Channel 2 DC Subtraction from Calibration No DC Subtraction DC Value from DC Calibration Is Subtracted	0x0	RW
4	DC_SUB_C1	0 1	Channel 1 DC Subtraction from Calibration No DC Subtraction DC Value from DC Calibration Is Subtracted	0x0	RW
3	DC_HPF_C4	0 1	Channel 4 DC High-Pass Filter Enable HPF Off HPF On	0x0	RW
2	DC_HPF_C3	0 1	Channel 3 DC High-Pass Filter Enable HPF Off HPF On	0x0	RW
1	DC_HPF_C2	0 1	Channel 2 DC High-Pass Filter Enable HPF Off HPF On	0x0	RW
0	DC_HPF_C1	0 1	Channel 1 DC High-Pass Filter Enable HPF Off HPF On	0x0	RW

PRELIMINARY

TYPICAL APPLICATION CIRCUIT

Figure 44. Typical Application Circuit, Four Inputs, I^2C and I^2S Mode

PRELIMINARY

OUTLINE DIMENSIONS

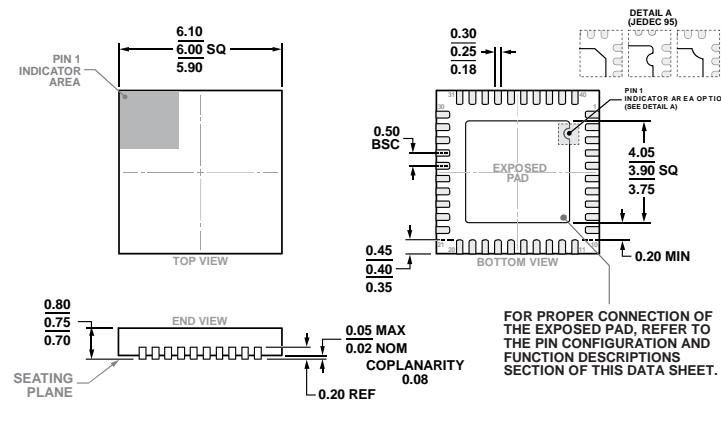


Figure 45. 40-Lead Lead Frame Chip Scale Package [LFCSP]

6 mm x 6 mm Body and 0.75 mm Package Height

(CP-40-14)

(CP-40-14) Dimensions shown in millimeters

ORDERING GUIDE

Model^{1, 2}	Temperature Range	Package Description	Package Option
ADAU1979WBCPZ	–40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-14
ADAU1979WBCPZ-RL	–40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP], 13" Tape and Reel	CP-40-14
EVAL-ADAU1979Z		Evaluation Board	

¹ Z = RoHS Compliant Part.

² W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADAU1979WBCPZ models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).