Lab 4 Final Report

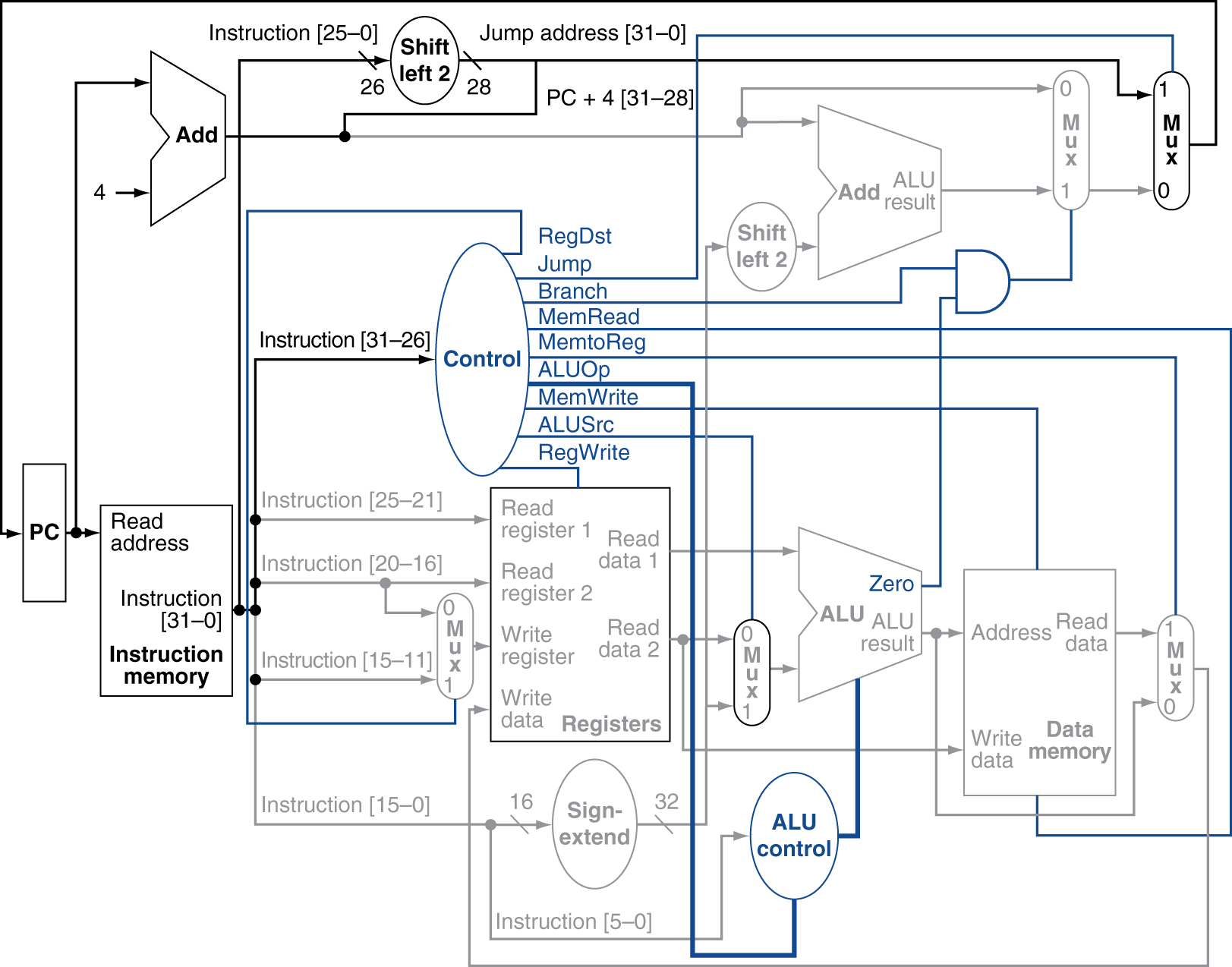
# Team Members

Team member: Name

Team member: Name

# Implementation Diagram

(Draw your design similar to the one shown below)



# Datapath

Describe the main datapath components and how they are connected.

# ALU Control

Describe ALU operations and the associated control in details.

# Control Unit

Describe the control unit and its inputs and outputs in details.

# Simulation Results Memory and Register File at clock cycle 0

You need to print out the data and instructions in your memory and register file throughout the simulation as follows.

## Memory and register file contents at clock cycle 0

Memory (data + instruction):

|  |  |  |
| --- | --- | --- |
| Address | Hex Value | Binary Value |
| 0x000 | 0x0000 | 0000 0000 0000 0000 |
| 0x002 | 0xFFFB | 1111 1111 1111 1011 |
| … | … | … |

Register file (data):

|  |  |  |
| --- | --- | --- |
| Register # | Hex Value | Binary Value |
| 1 | 0x0000 | 0000 0000 0000 0000 |
| 2 | 0x0027 | 0000 0000 0010 0111 |
| … | … | … |

## Memory and register file contents for each loop:

You need to print out the data (not instructions) in your memory and register file after each loop. L, M, N should be the clock cycle numbers after each loop (e.g., L = 55 cycles after the first loop, N = 110 cycles after the second loop, etc). Your program should count the number of clock cycles after executing instructions.

**After the first loop, clock cycle: L**

Memory (data + instruction):

|  |  |  |
| --- | --- | --- |
| Address | Hex Value | Binary Value |
| 0x000 | 0x0000 | 0000 0000 0000 0000 |
| 0x002 | 0xFFFB | 1111 1111 1111 1011 |
| … | … | … |

Register file (data):

|  |  |  |
| --- | --- | --- |
| Register # | Hex Value | Binary Value |
| 1 | 0x0000 | 0000 0000 0000 0000 |
| 2 | 0x0027 | 0000 0000 0010 0111 |
| … | … | … |

**After the second loop, clock cycle: M**

Memory Table: …

Register File: **…**

**After the nth loop, clock cycle: N**

Memory Table: …

Register File: **…**

# Integrated output data from the simulation results

Summarize the output **data (not instructions)** for the memory and register file for n loops of the test program.

Memory (data):

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Address | Hex value after each loop | | | | | |
| Initial | 1st | 2nd | 3rd | …. | nth |
| 0x00 | FFFB | FFFB | …. | …. | …. | …. |
| 0x002 | 0005 | 0005 | …. | …. | …. | …. |
| …. | …. | …. | …. | …. | …. | …. |

Register file (data):

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Address | Hex value after each loop | | | | | |
| Initial | 1st | 2nd | 3rd | …. | nth |
| 1 | 0000 | 0001 | …. | …. | …. | …. |
| 2 | 0000 | 0001 | …. | …. | …. | …. |
| …. | …. | …. | …. | …. | …. | …. |

# Bonus Materials (if any)

Describe the modification to the design you made to implement the bonus parts of lab4

# Discussion

Explain how your team optimized the simulation program, if any.

Explain which part does not work correctly in your design, if any.

Explain any other discussions regarding the project if applicable and relevant.

# Final Version of Simulator Code (Attached)