EGRE 365

Digital Systems

In Class Assignment 2

Lab Section: Wednesday 10 AM

Lab Date:October 23, 2024

Report Date: October 23, 2024

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Pledge: On my honor, We have neither given nor received unauthorized aid on this assignment.

Signed: Brandon Frazier

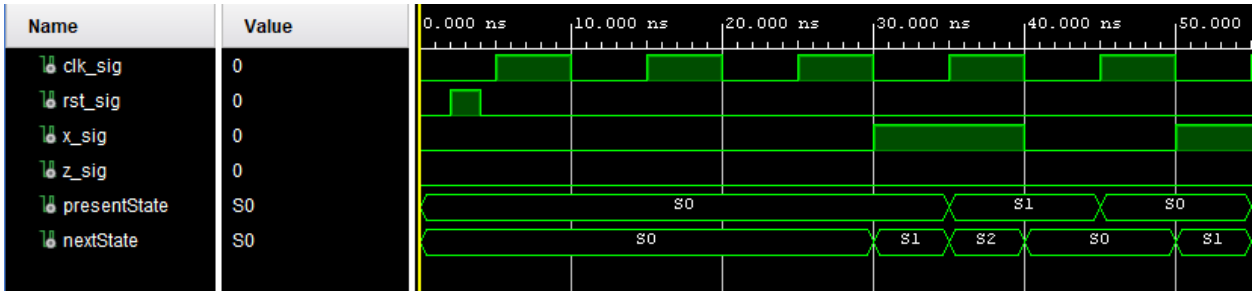
State Machine Design:

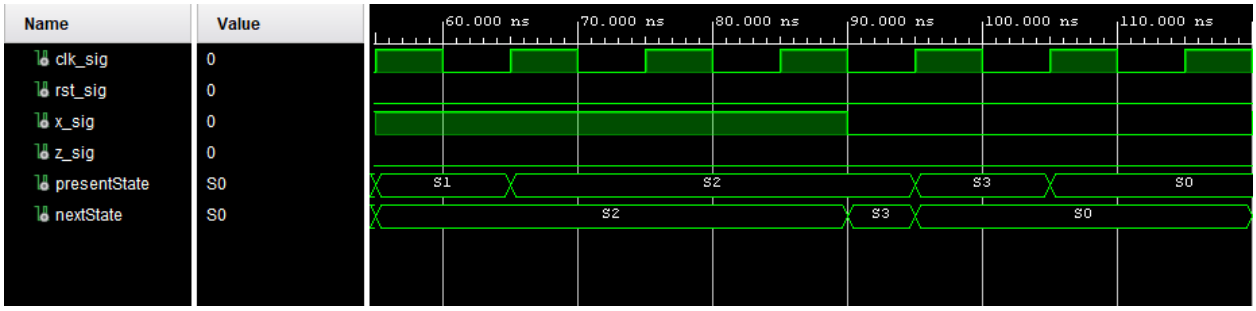
```
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24
25  entity ica1SM is
26    Port (x, clk, rst: in std_logic;
27          z: out std_logic);
28  end ica1SM;
29
30  architecture Behavioral of ica1SM is
31      type stateType is (S0, S1, S2, S3, S4);
32      signal presentState, nextState : stateType;
33  begin
34
35  clockProc : process(clk, rst)
36  begin
37      if(rst = '1') then
38          presentState <= S0;
39          --nextState <= S0;
40      elsif(rising_edge(clk)) then
41          presentState <= nextState;
42      end if;
43  end process clockProc;
44
45  nextStateProc : process(presentState, x)
46  begin
47      case presentState is
48          when S0 =>
49              if(x = '0') then
50                  nextState <= S0;
51              else
52                  nextState <= S1;
53              end if;
54          when S1 =>
55              if(x = '0') then
56                  nextState <= S0;
57              else
58                  nextState <= S2;
59              end if;
60          when S2 =>
61              if(x = '0') then
62                  nextState <= S3;
63              else
64                  nextState <= S2;
65              end if;
66          when S3 =>
67              if(x = '0') then
68                  nextState <= S0;
69              else
70                  nextState <= S4;
71              end if;
72          when S4 =>
73              if(x = '0') then
74                  nextState <= S0;
75              else
76                  nextState <= S2;
77              end if;
78          end case;
79  end process nextStateProc;
80
81  outputProc: process(presentState)
82  begin
83      if(presentState = S4) then
84          Z <= '1';
85      else
86          Z <= '0';
87      end if;
88  end process outputProc;
89
90  end Behavioral;
91
```

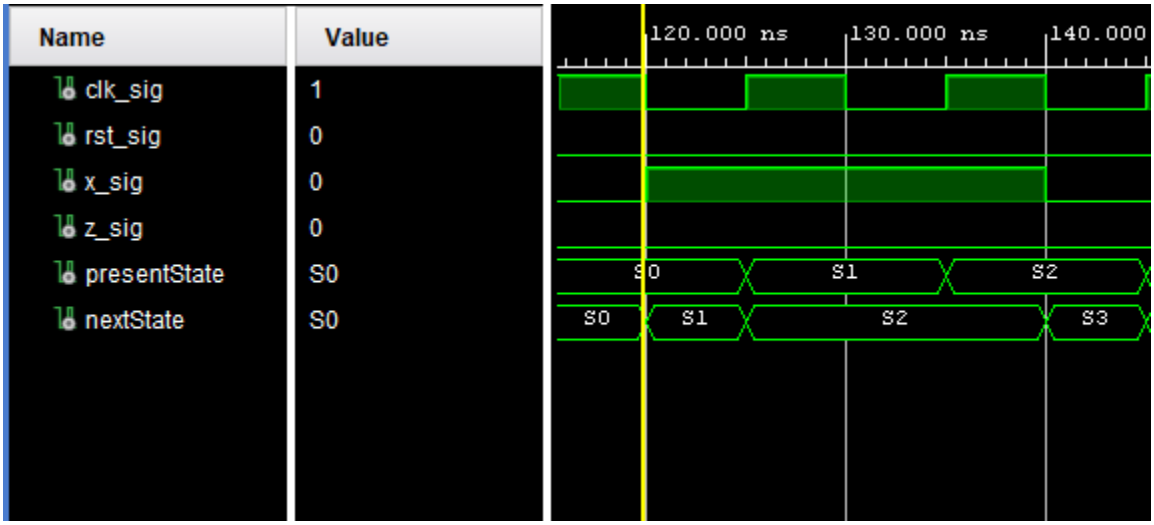
State Machine Test Bench

```
library ieee;
use ieee.std_logic_1164.all;

entity ica1TB is
end ica1TB;

architecture behavior of ica1TB is

  signal clk_sig : std_logic := '0';
  signal rst_sig : std_logic := '0';
  signal x_sig,z_sig : std_logic;
  constant Tperiod : time := 10 ns;

  begin

    process(clk_sig)
      begin
        clk_sig <= not clk_sig after Tperiod/2;
    end process;

  rst_sig <= '0', '1' after 2 ns, '0' after 4 ns;

  x_sig <= '0', '1' after 30 ns, '0' after 40 ns, '1' after 50 ns,
  '0' after 90 ns, '0' after 110 ns, '1' after 120 ns,
  '0' after 140 ns, '1' after 150 ns, '0' after 170 ns,
  '1' after 180 ns, '0' after 190 ns;



    -- this is the component instantiation for the
    -- DUT - the device we are testing
    DUT : entity work.ica1SM(Behavioral)
      port map(clk => clk_sig, rst => rst_sig,
               x => x_sig, z => z_sig);


end behavior;
```

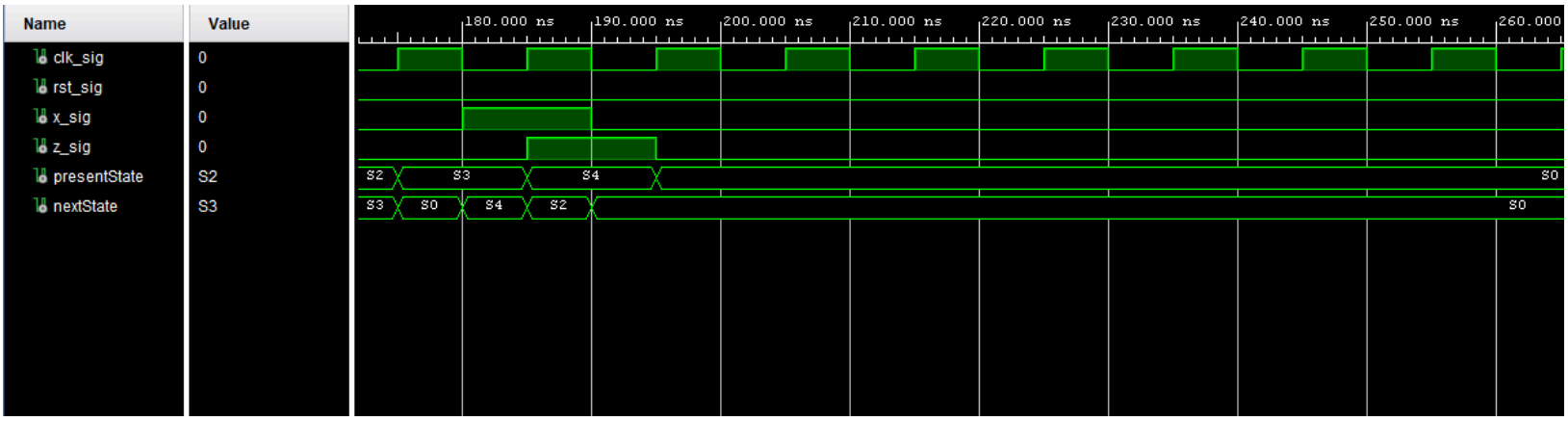
Test Bench Run




Name
Value
clk_sig
rst_sig
x_sig
z_sig
presentState
nextState
0
0
0
0
S0
S0
60.000 ns
70.000 ns
80.000 ns
90.000 ns
100.000 ns
110.000 ns
S1
S2
S3
S0
S2
S3
S0


Name
Value
clk_sig
rst_sig
x_sig
z_sig
presentState
nextState
1
0
0
0
S0
S0
120.000 ns
130.000 ns
140.000
S0
S1
S2
S0
S1
S2
S3


Name
Value
clk_sig
rst_sig
x_sig
z_sig
presentState
nextState
0
0
0
0
S2
S3
140.000 ns
150.000 ns
160.000 ns
170.000
S2
S3
S4
S2
S2
S3
S0
S4
S2
S3


Name
Value
clk_sig
rst_sig
x_sig
z_sig
presentState
nextState
0
0
0
0
S2
S3
180.000 ns
190.000 ns
200.000 ns
210.000 ns
220.000 ns
230.000 ns
240.000 ns
250.000 ns
260.000
S2
S3
S4
S0
S3
S0
S4
S2
S0