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2  -- Company:
3  -- Engineer: Brandon Frazier
4  --
5  -- Create Date: 10/23/2024 10:05:29 AM
6  -- Design Name:
7  -- Module Name: icalSM - Behavioral
8  -- Project Name:
9  -- Target Devices:
10 -- Tool Versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19 -----
20
21
22 library IEEE;
23 use IEEE.STD_LOGIC_1164.ALL;
24
25 entity icalSM is
26     Port (x, clk, rst: in std_logic;
27           z: out std_logic);
28 end icalSM;
29
30 architecture Behavioral of icalSM is
31     type stateType is (S0, S1, S2, S3, S4);
32     signal presentState, nextState : stateType;
33 begin
34
35     clockProc : process(clk, rst)
36     begin
37         if(rst = '1') then
38             presentState <= S0;
39             --nextState <= S0;
40         elsif(rising_edge(clk)) then
41             presentState <= nextState;
42         end if;
43     end process clockProc;
44
45     nextStateProc : process(presentState, x)
46     begin
47         case presentState is
48             when S0 =>
49                 if(x = '0') then
50                     nextState <= S0;
51                 else
52                     nextState <= S1;
53                 end if;
54             when S1 =>
55                 if(x = '0') then
56                     nextState <= S0;
57                 else
58                     nextState <= S2;
59                 end if;
60             when S2 =>
61                 if(x = '0') then
62                     nextState <= S3;
63                 else
64                     nextState <= S2;
65                 end if;
66             when S3 =>
67                 if(x = '0') then
68                     nextState <= S0;
69                 else

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70         nextState <= S4;
71     end if;
72     when S4 =>
73         if(x = '0') then
74             nextState <= S0;
75         else
76             nextState <= S2;
77         end if;
78     end case;
79 end process nextStateProc;
80
81 outputProc: process(presentState)
82 begin
83     if(presentState = S4) then
84         Z <= '1';
85     else
86         Z <= '0';
87     end if;
88 end process outputProc;
89
90 end Behavioral;
91

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