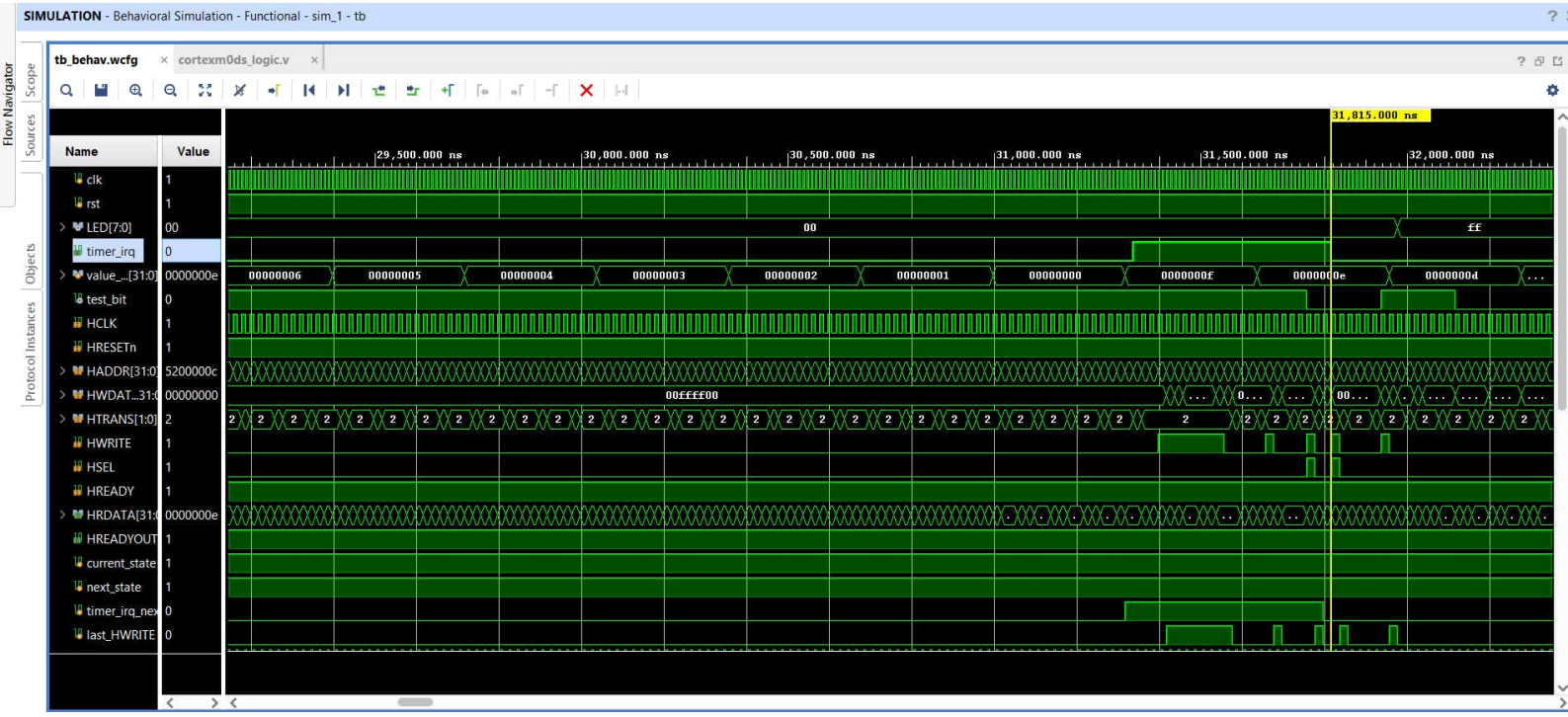
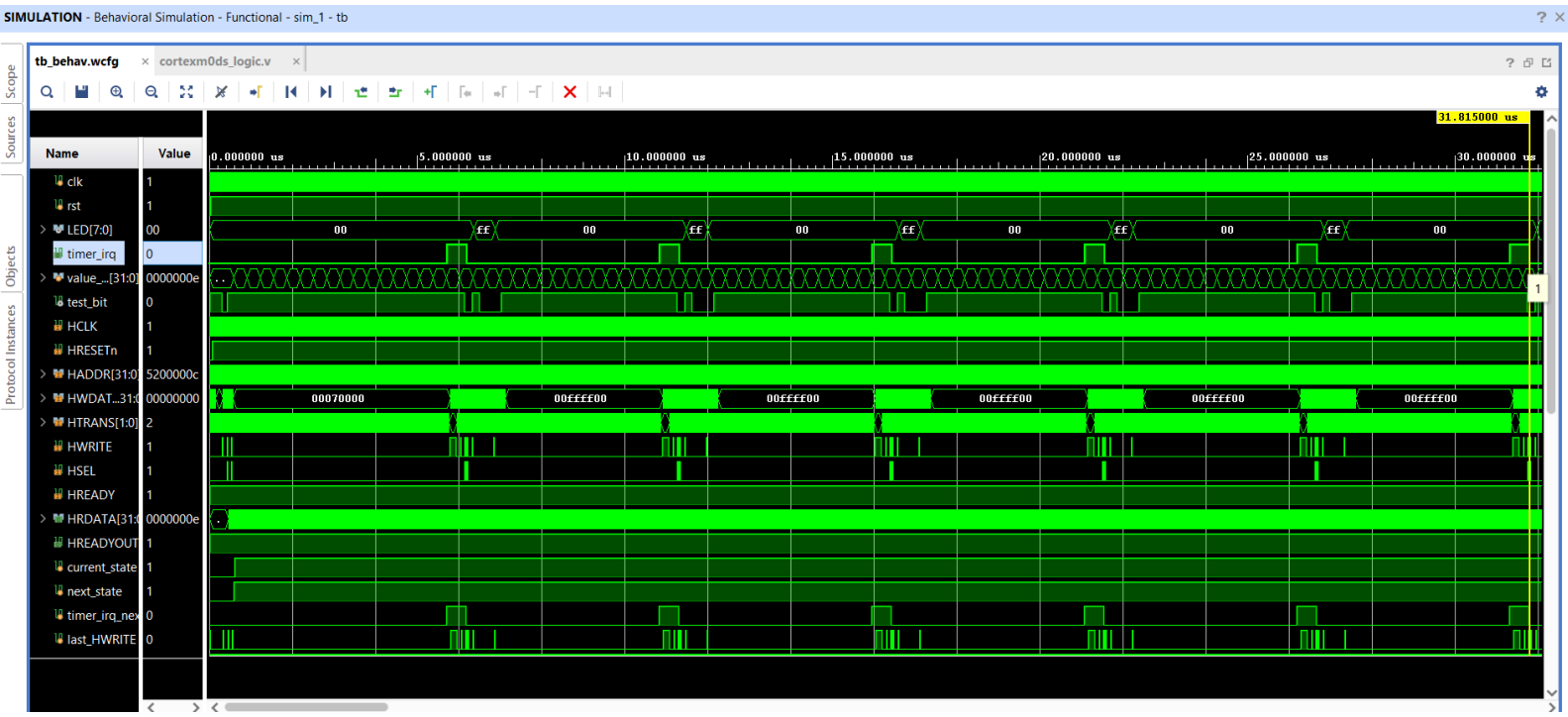
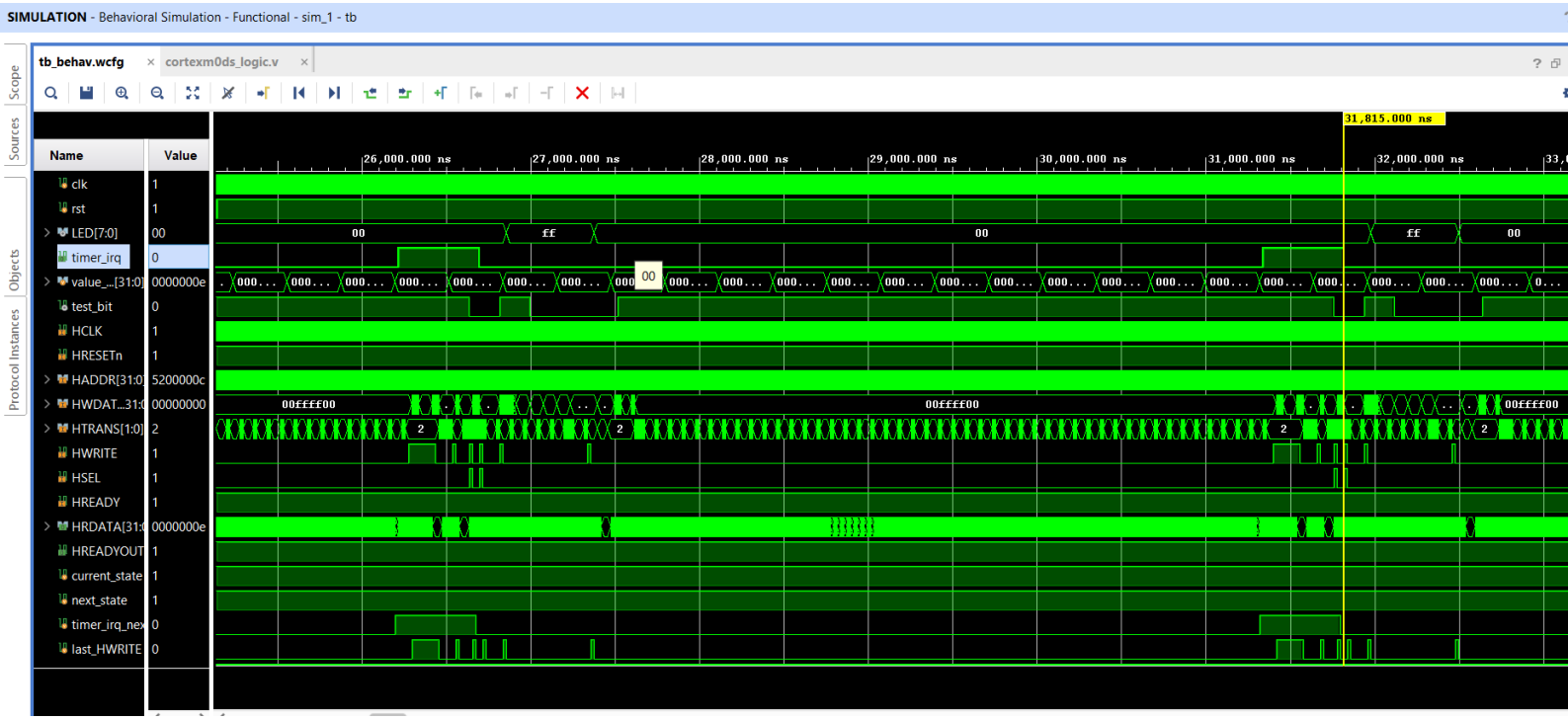
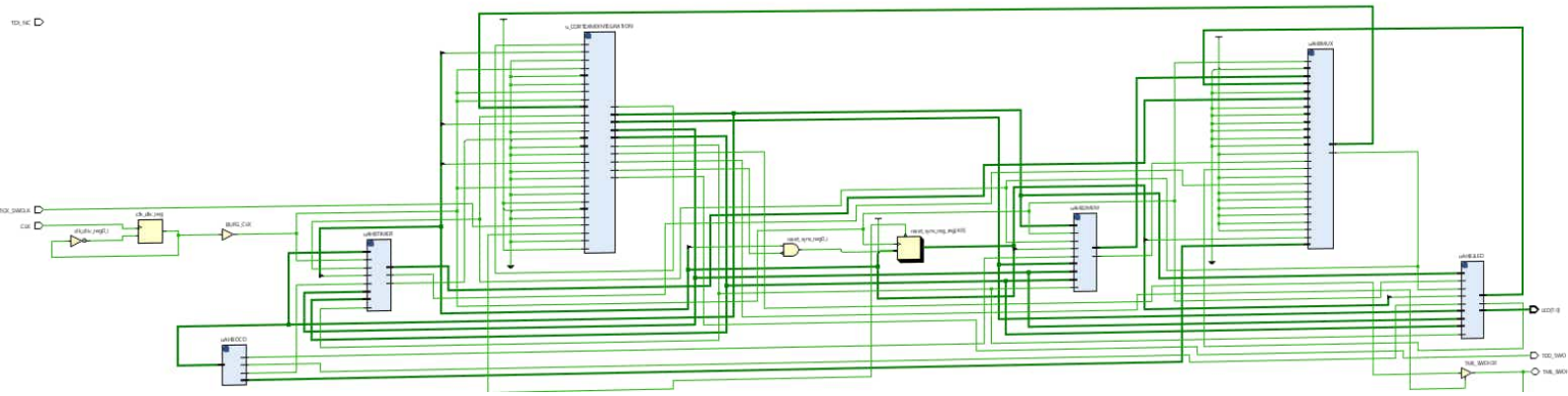

SIMULATION - Behavioral Simulation - Functional - sim_1 - tb
tb_behav.wcfg
cortexm0ds_logic.v
Flow Navigator
Scope
Sources
Objects
Protocol Instances
Name
Value
clk
rst
LED[7:0]
timer_irq
value_...[31:0]
test_bit
HCLK
HRESETn
HADDR[31:0]
HWDAT...31:0
HTRANS[1:0]
HWRITE
HSEL
HREADY
HRDATA[31:0]
HREADYOUT
current_state
next_state
timer_irq_nex
last_HWRITE
29,500.000 ns
30,000.000 ns
30,500.000 ns
31,000.000 ns
31,500.000 ns
31,815.000 ns
32,000.000 ns
00
ff
00000006
00000005
00000004
00000003
00000002
00000001
00000000
0000000f
0000000e
0000000d
00ffff00


SIMULATION - Behavioral Simulation - Functional - sim_1 - tb
tb_behav.wcfg
cortexm0ds_logic.v
Scope
Sources
Objects
Protocol Instances
Name
Value
clk
rst
LED[7:0]
timer_irq
value_...[31:0]
test_bit
HCLK
HRESETn
HADDR[31:0]
HWDAT...31:0]
HTRANS[1:0]
HWRITE
HSEL
HREADY
HRDATA[31:0]
HREADYOUT
current_state
next_state
timer_irq_nex
last_HWRITE
0.000000 us
5.000000 us
10.000000 us
15.000000 us
20.000000 us
25.000000 us
30.000000 us
31.815000 us


SIMULATION - Behavioral Simulation - Functional - sim_1 - tb
tb_behav.wcfg
cortexm0ds_logic.v
Scope
Sources
Objects
Protocol Instances
Name
Value
clk
rst
LED[7:0]
timer_irq
value_...[31:0]
test_bit
HCLK
HRESETn
HADDR[31:0]
HWDAT...31:0]
HTRANS[1:0]
HWRITE
HSEL
HREADY
HRDATA[31:0]
HREADYOUT
current_state
next_state
timer_irq_nex
last_HWRITE
26,000.000 ns
27,000.000 ns
28,000.000 ns
29,000.000 ns
30,000.000 ns
31,000.000 ns
31,815.000 ns
32,000.000 ns

Package | Device | cortexm0ds_logic.v | Schematic

16 Cells 14 I/O Ports 238 Nets

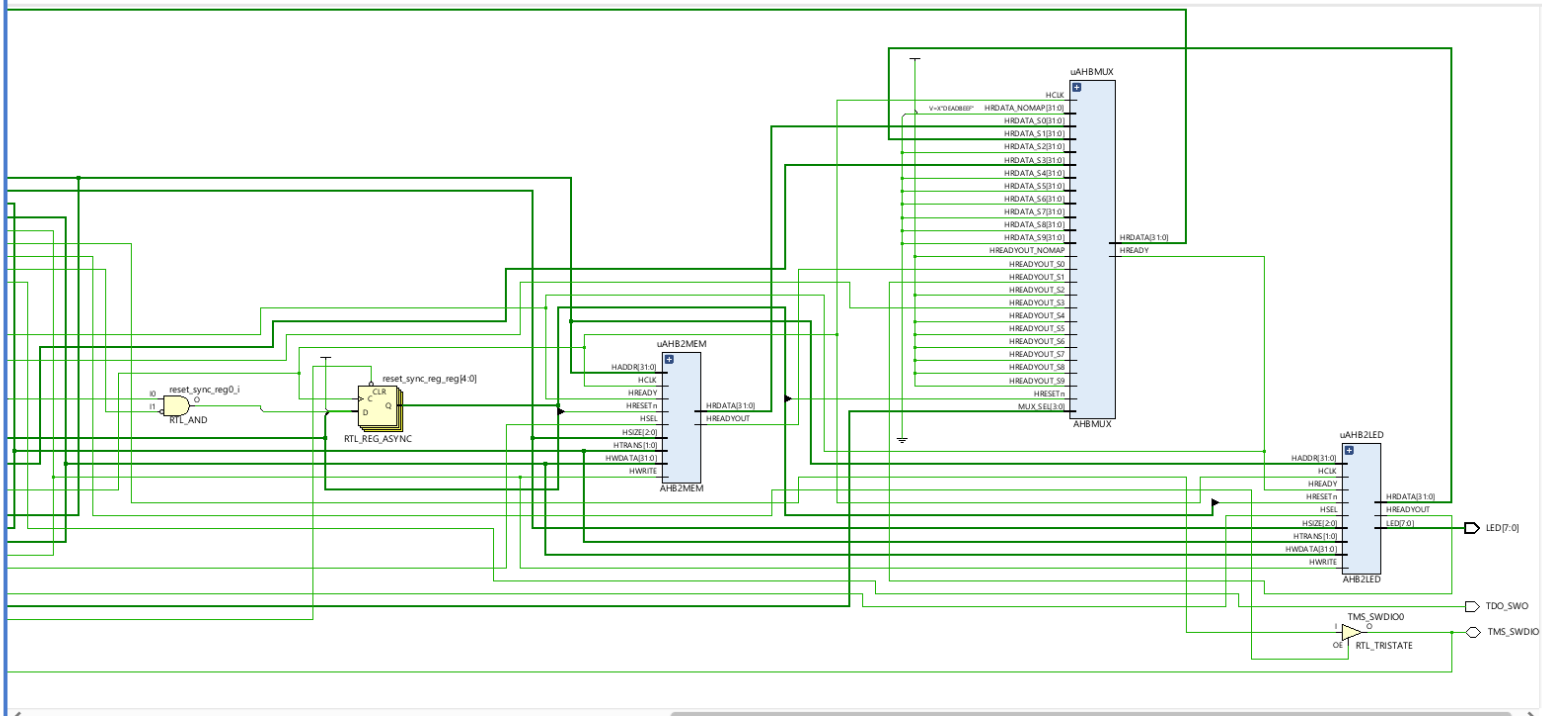


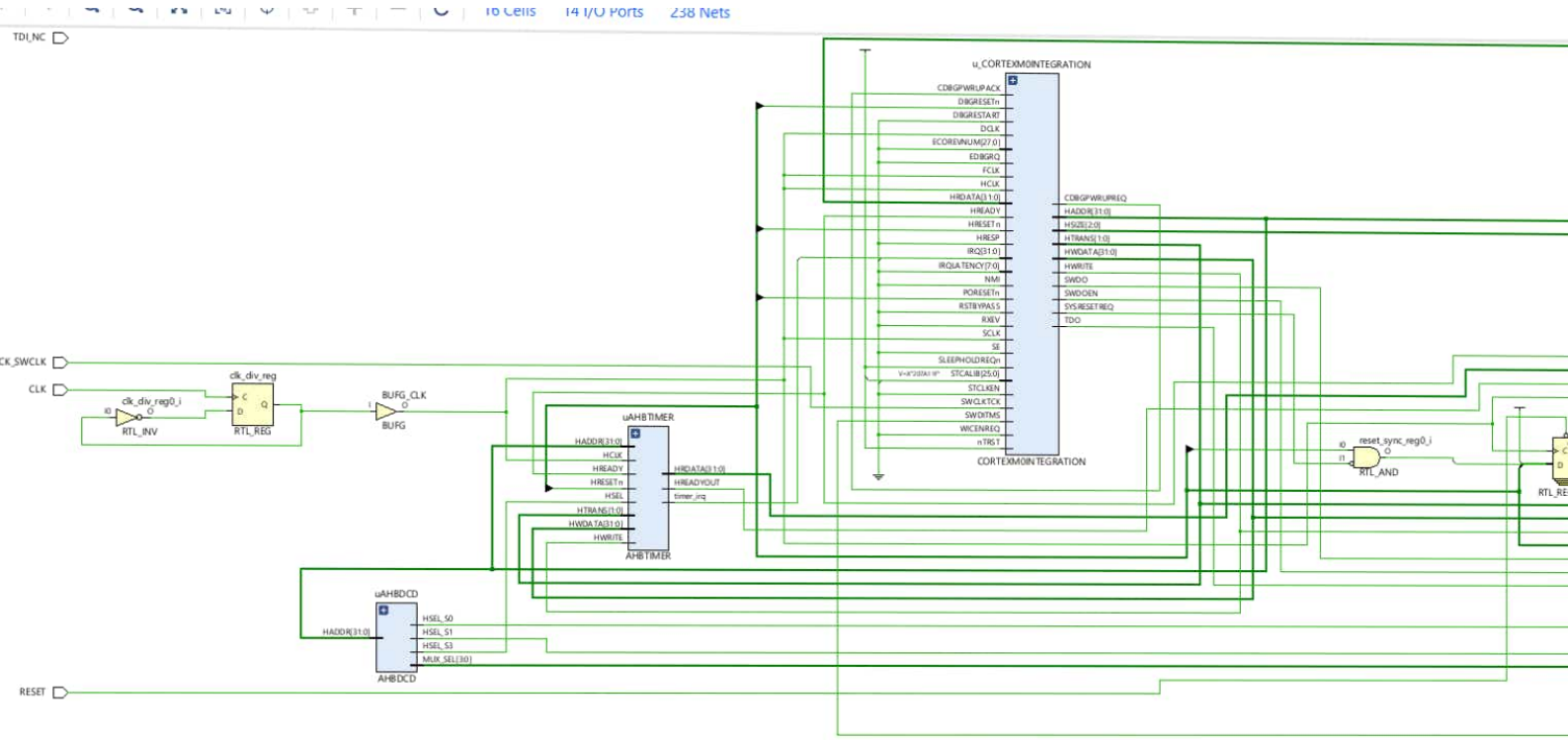
ELABORATED DESIGN - xc7a100tcsg324-1

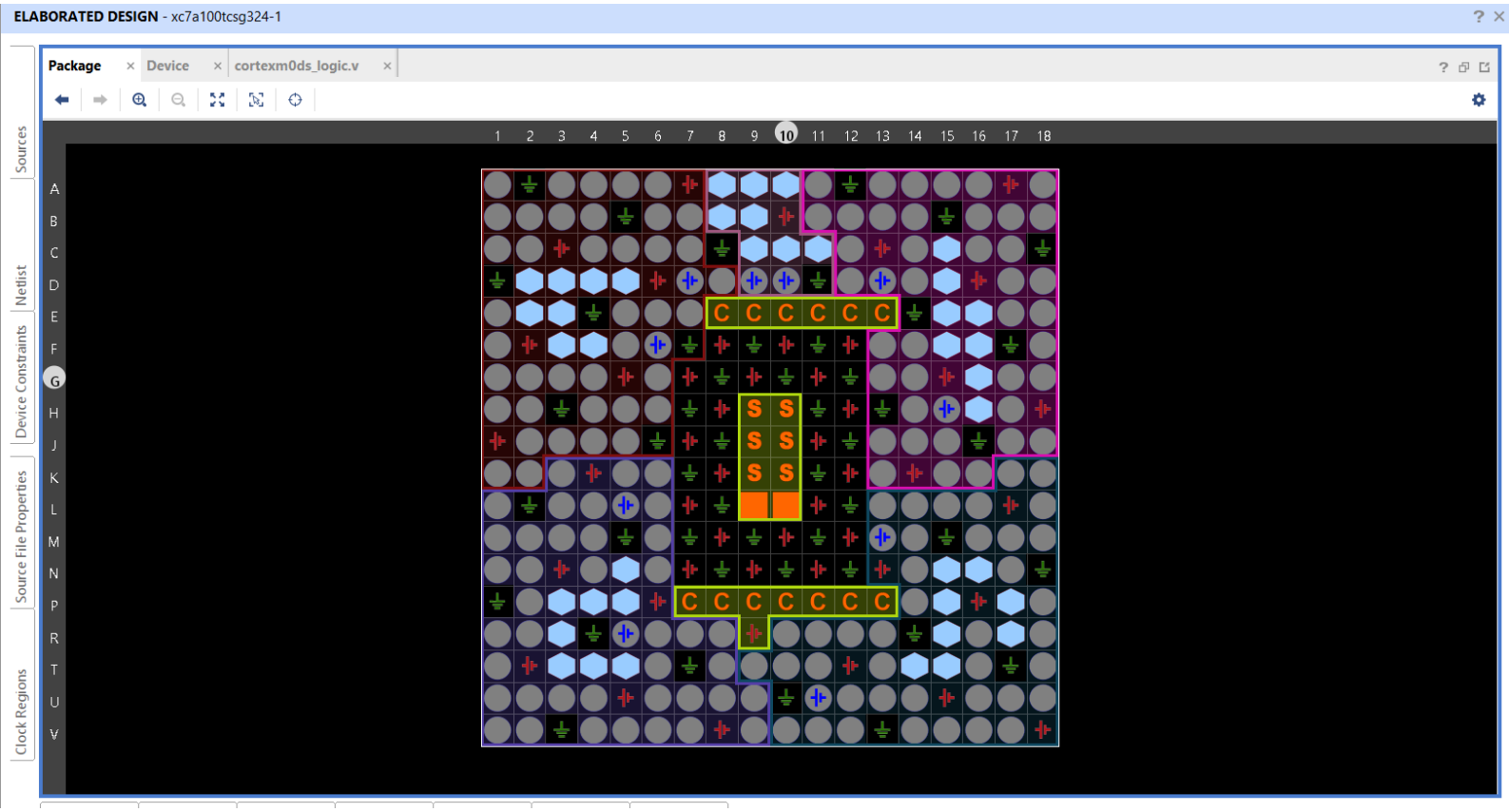
Package | Device | cortexm0ds_logic.v | Schematic

16 Cells | 14 I/O Ports | 238 Nets

Sources | Netlist | Device Constraints | Bus Net Properties | Clock Regions




16 Cells
14 I/O Ports
238 Nets
TDI_NC
u_CORTEXM0INTEGRATION
CDBGPWRUPACK
DBGRESETn
DBGRESTART
DCLK
ECOREVNUM[27:0]
EDBGRQ
FCLK
HCLK
HRDATA[31:0]
HREADY
HRESETn
HRESP
IRQ[31:0]
IRQLATENCY[7:0]
NMI
PORESETn
RSTBYPASS
RXEV
SCLK
SE
SLEEPHOLDREQn
STCALIB[25:0]
STCLKEN
SWCLKTCK
SWDITMS
WICENREQ
nTRST
CDBGPWRUPREQ
HADDR[31:0]
HSIZE[2:0]
HTRANS[1:0]
HWDATA[31:0]
HWRITE
SWDO
SWDOEN
SYSRESETREQ
TDO
CORTEXM0INTEGRATION
CK_SWCLK
CLK
clk_div_reg
clk_div_reg0_i
RTL_INV
RTL_REG
BUFG_CLK
BUFG
uAHBTIMER
HADDR[31:0]
HCLK
HREADY
HRESETn
HSEL
HTRANS[1:0]
HWDATA[31:0]
HWRITE
HRDATA[31:0]
HREADYOUT
timer_irq
AHBTIMER
reset_sync_reg0_i
RTL_AND
uAHBDCD
HADDR[31:0]
HSEL_S0
HSEL_S1
HSEL_S3
MUX_SEL[3:0]
AHBDCD
RESET


ELABORATED DESIGN - xc7a100tcsg324-1
Package
Device
cortexm0ds_logic.v
Sources
Netlist
Device Constraints
Source File Properties
Clock Regions
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
A B C D E F G H J K L M N P R T U V
C C C C C C
S S
S S
S S
C C C C C C C