Digital Systems Design
ECSE 323

Lab Report 2
Keyboard Encoder

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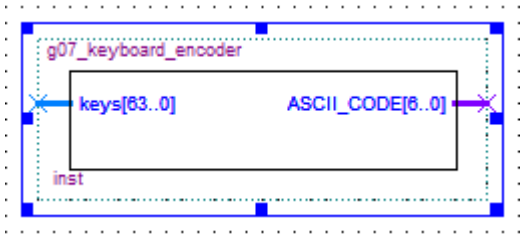
1 Circuit Description

The keyboard encoder circuit takes a 64 bit input, and returns a 7 bit output. The 7 bit output represents the ascii code of the selected key, with each input line representing a single key. The codes are mapped from " " (space character, ascii 32) on the 0th input, to "_" (underscore, ascii 95) on the 63rd input.
This ordering was chosen as the simplest conversion from key index to an appropriate ascii code.



1.1 Circuit Internal

To actually create the circuit, a simple 64 to 6 bit encoder was used (which was in turn made of four 16 to 4 encoders from lab 1). The output of that circuit then had 32 added to it, to shift the result to an appropriate ascii code.

2 Circuit Testing

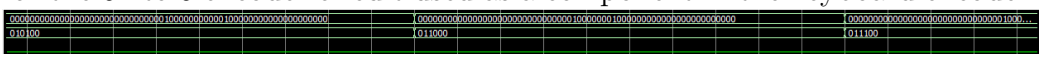
The keyboard encoder was tested twice. Once using a vhdl testbench that walked through cases, and once using the Altera FPGA board. Both rounds of testing were successful.

2.1 VHDL Testbench

The VHDL testbench ran through all 64 of the simple cases.

The multiple key cases were not tested, as those had been covered in tests

for the 64 to 6 encoder circuit used as a component in the keyboard encoder.



2.2 Altera FPGA Board

The circuit was also tested on the Altera De1-SOC board. To do so, the output of the encoder was put through an ascii code to 7 segment display decoder. This converted a subset of characters to the necessary codes for displaying characters. Switches on the FPGA board were linked to single key inputs, and a 7 segment display on the board was used to verify that the correct codes were being displayed.

Grade Sheet for Lab #2

Fall 2016.

Group Number: 7.

Group Member Name: Jaeho Lee. Student Number: 260633759.

Group Member Name: Andrew Lowther. Student Number: 260655337.

Marks			TA Signatures
2	1.	VHDL code for the *64:6 encoder* circuit	Andrew
2	2.	Simulation of the *64:6 encoder* circuit	Andrew
2	3.	VHDL code for the *keyboard encoder* circuit	Arash
2	4.	Simulation of the *keyboard encoder* circuit	Arash
2	5.	VHDL code for the *7_segment_decoder* circuit	Andrew
2	6.	Simulation of the *7_segment_decoder* circuit	Andrew
2	7.	Testing of the *7_segment_decoder* circuit on the DE1 board	Andrew

Each part should be demonstrated to one of the TAs who will then give a grade and sign the grade sheet. Grades for each part will be either 0, 1, or 2. A mark of 2 will be given if everything is done correctly. A grade of 1 will be given if there are significant problems, but an attempt was made. A grade of 0 will be given for parts that were not done at all, or for which there is no TA signature.