Digital Systems Design
ECSE 323
Lab Report 1 16-4 Encoder

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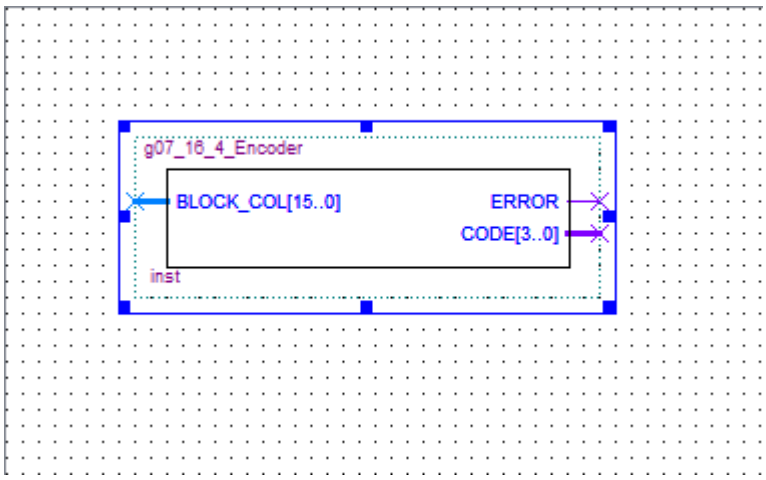
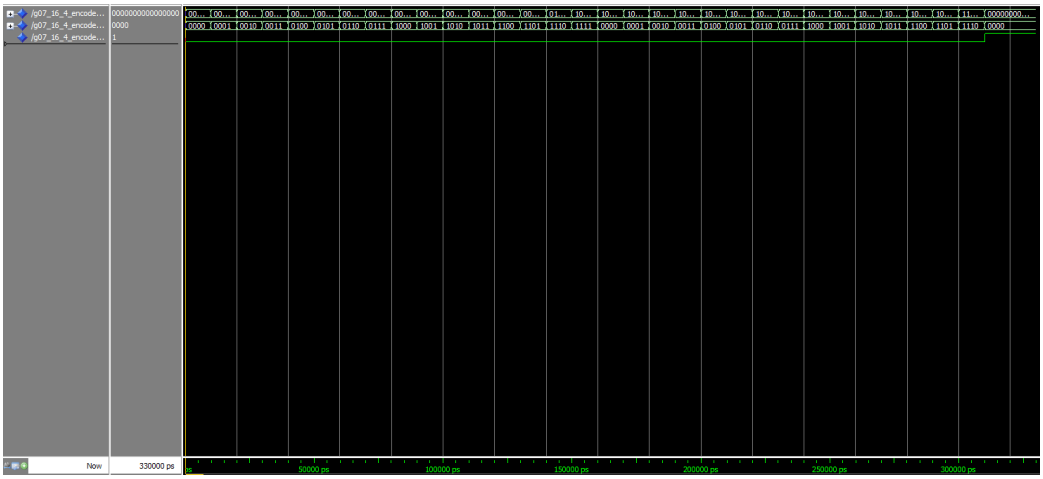


1 Circuit Explanation

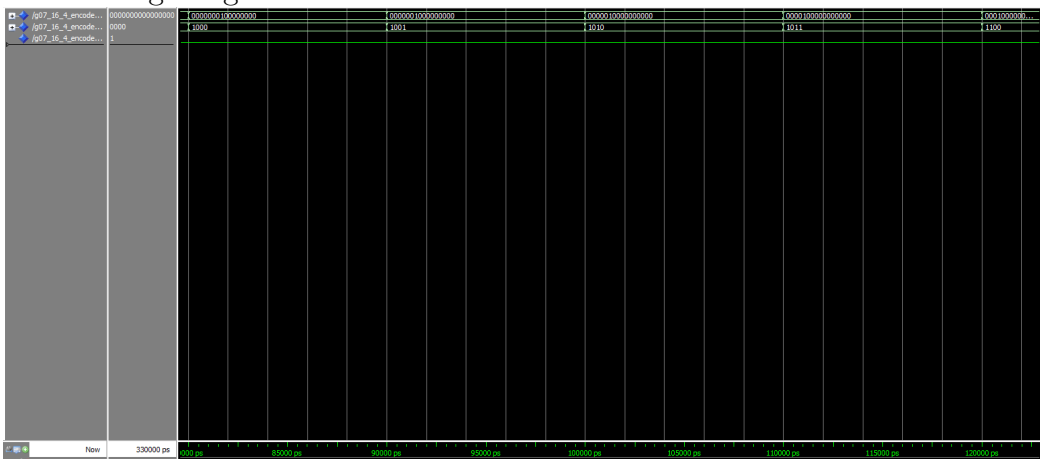
A 16:4 Encoder circuit has been created for this lab. The encoder circuit has a 16-bit input bus, a 4-bit output bus, and a single bit error output port. The purpose of the encoder is to get the number of low input bits from 16-bit input until the first high bit appears (i.e. the index of the lowest high input). The 4-bit output represents the number of low inputs until the first high input named, and is named CODE. The one single bit output is ERROR which is high when none of the input bit is high. Since we have 16-bit inputs, there are $2^{16} = 65534$ possible combinations and CODE is in range of 0 to 15.

2 Circuit Validation

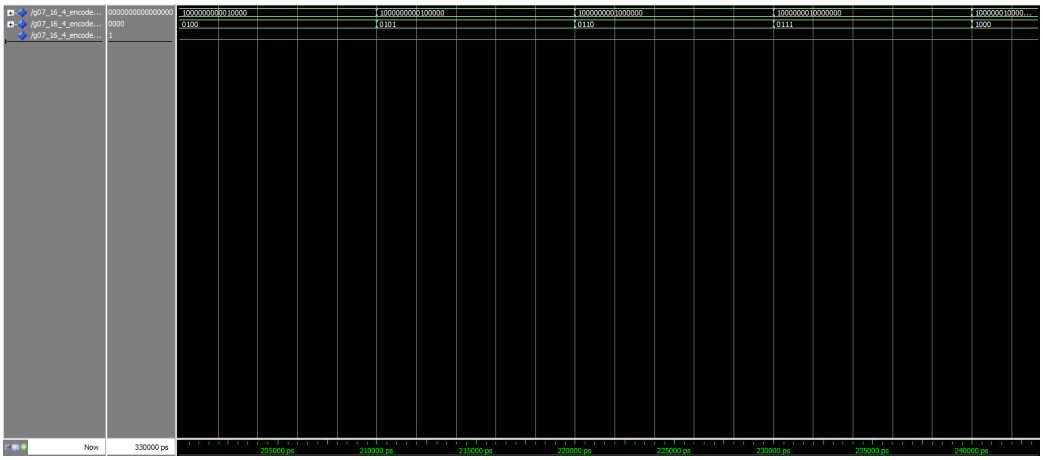
Two scripts were written to test the circuit. The first covered each of the simple cases:



With a single high bit:



The error case, where all bits were low, and then a set of more complex cases, where there were two high bits:



Because the code for the circuit should function regardless of the number of extra high bits, testing with one extra was assumed to cover all such cases. To double check, an exhaustive case was written, which generated all possible outputs. This was also run, and various points were inspected. Those were the cases from the limited test (to ensure matching results), other points, such as having all 1's except the 16th bit, and all 0's but the 16th bit, were checked to verify that the circuit was correctly handling the multiple-high cases.

Grade Sheet for Lab #1

Fall 2016.

Group Number: 07

Group Member Name: JAEHO LEE Student Number: 260633759

Group Member Name: ANDREW LOWTHER Student Number: 260558337

Marks			TA Signatures
2	1.	Schematic diagram for the 6-bit comparator	
2	2.	VHDL file for the 6-bit comparator	
2	3.	Initial partial simulation results for the 6-bit comparator	
2	4.	Complete simulation results for the 6-bit comparator	
2	5.	VHDL description for the 16:4 encoder circuit	
2	6.	Simulation Testbench VHDL for the 16:4 encoder circuit	
2	7.	Simulation results for the 16:4 encoder circuit	

Each part should be demonstrated to one of the TAs who will then give a grade and sign the grade sheet. Grades for each part will be either 0, 1, or 2. A mark of 2 will be given if everything is done correctly. A grade of 1 will be given if there are significant problems, but an attempt was made. A grade of 0 will be given for parts that were not done at all, or for which there is no TA signature.