PMW3360DM-T2QU: Optical Gaming Navigation Chip

General Description:

PMW3360DM-T2QU is PixArt Imaging's high end gaming integrated chip which comprises of navigation chip and IR LED integrated in a 16pin molded lead-frame DIP package. It provides best in class gaming experience with the enhanced features of high speed, high resolution, high accuracy and selectable lift detection height to fulfill professional gamers' need. The chip comes with self-adjusting variable frame rate algorithm to enable wireless gaming application. It is designed to be used with LM19-LSI lens to achieve optimum performance.

Key Features:

- Integrated 16 pin molded lead-frame DIP package with IR LED
- Operating Voltage: 1.8V - 2.1V
- Lift detection options
  - Manual lift cut off calibration
  - 2mm
  - 3mm
- High speed motion detection 250ips (typical) and acceleration 50g (max).
- Selectable resolutions up to 12000cpi with 100cpi step size
- Resolution error of 1% (typical)
- Four wire serial port interface (SPI)
- External interrupt output for motion detection
- Internal oscillator — no clock input needed
- Self-adjusting variable frame rate for optimum power performance in wireless application
- Customizable response time and downshift time for rest modes
- Enhanced programmability
  - Angle snapping
  - Angle tunability

Applications:

- Wired and Wireless Optical gaming mice
- Integrated input devices
- Battery-powered input devices

Key Chip Parameters:

Parameter	Value
Power supply Range	1.8V - 2.1V
Optical Lens	1:1
Interface	4 wire Serial Port Interface (SPI)
System Clock	70MHz
Frame Rate	Up to 12000 fps
Speed	250ips (typical)
Resolution	12000 cpi
Package Type	16 pin molded lead-frame DIP package with integrated IR LED

Ordering Information:

Part Number	Package Type
PMW3360DM-T2QU	16pin-DIP
LM19-LSI	Lens

RoHS compliant

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Contents

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

1.0 System Level Description

This section covers PMW3360's guidelines and recommendations in term of chip, lens & PCB assemblies.

1.1 Pin Configuration

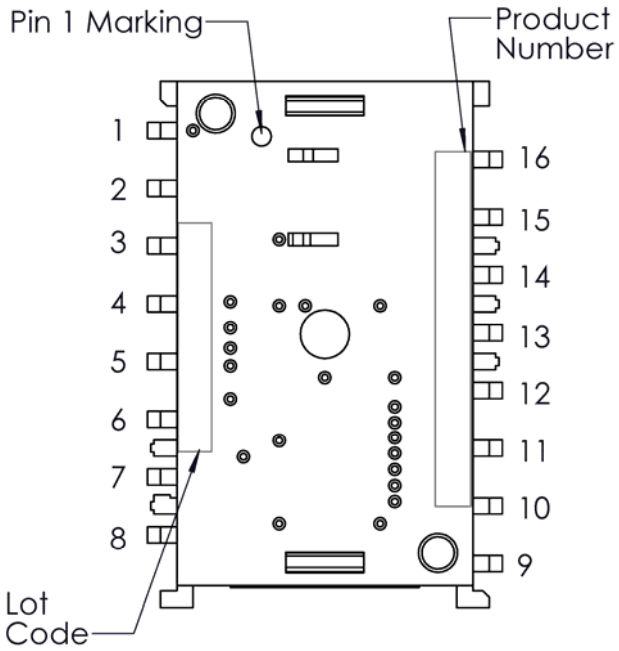


Figure 1. Device output pins

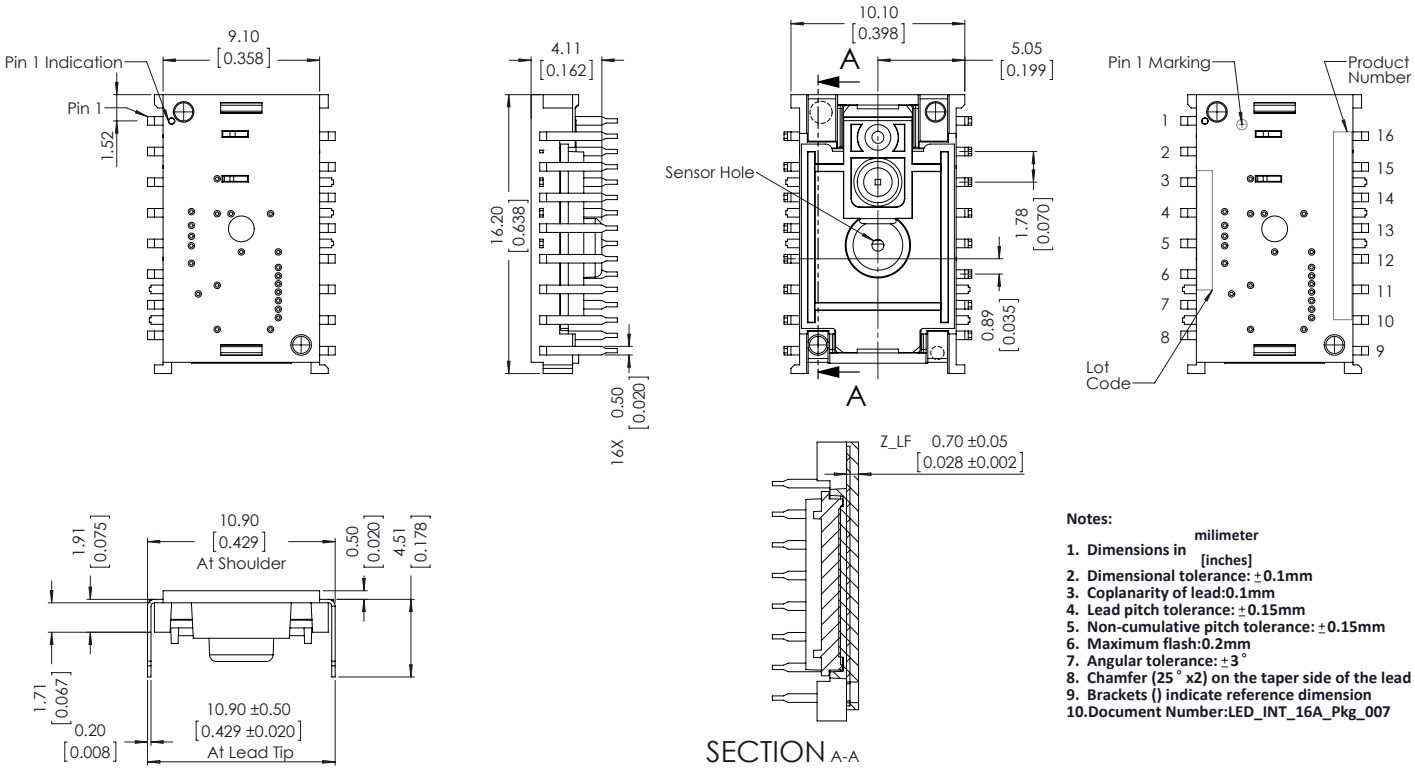
Pin No.	Function	Symbol	Type	Description
1	NA	NC	NC	(Float)
2	NA	NC	NC	(Float)
3	Supply Voltage and I/O Voltage	VDDPIX	Power	LDO output for selective analog circuit
4		VDD	Power	Input power supply
5		VDDIO	Power	I/O reference voltage
6	NA	NC	NC	(Float)
7	Reset control	NRESET	Input	Chip reset(active low)
8	Ground	GND	GND	Ground
9	Motion Output	MOTION	Output	Motion detect
10	4-wire spi communication	SCLK	Input	Serial data clock
11		MOSI	Input	Serial data input
12		MISO	Output	Serial data output
13		NCS	Input	Chip select(active low)
14	NA	NC	NC	(Float)
15	LED	LED_P	Input	LED Anode
16	NA	NC	NC	(Float)

Table 1. PMW3360DM-T2QU Pin Description

Items	Marking	Remark
Product Number	PMW3360DM-T2QU	
Lot Code	AYWWXXXXX	A : Assembly house Y: Year WW: Week XXXXX: PixArt reference

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

1.2 Package Outline Drawing



Notes:

1. Dimensions in milimeter [inches]
2. Dimensional tolerance: ±0.1mm
3. Coplanarity of lead:0.1mm
4. Lead pitch tolerance: ±0.15mm
5. Non-cumulative pitch tolerance: ±0.15mm
6. Maximum flash:0.2mm
7. Angular tolerance: ±3°
8. Chamfer (25° x2) on the taper side of the lead
9. Brackets () indicate reference dimension
10. Document Number:LED_INT_16A_Pkg_007

Figure 2. Package Outline Drawing

CAUTION: It is advised that normal static discharge precautions be taken in handling and assembling of this component to prevent damage and/or degradation which may be induced by ESD.

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

1.3 Assembly Drawings

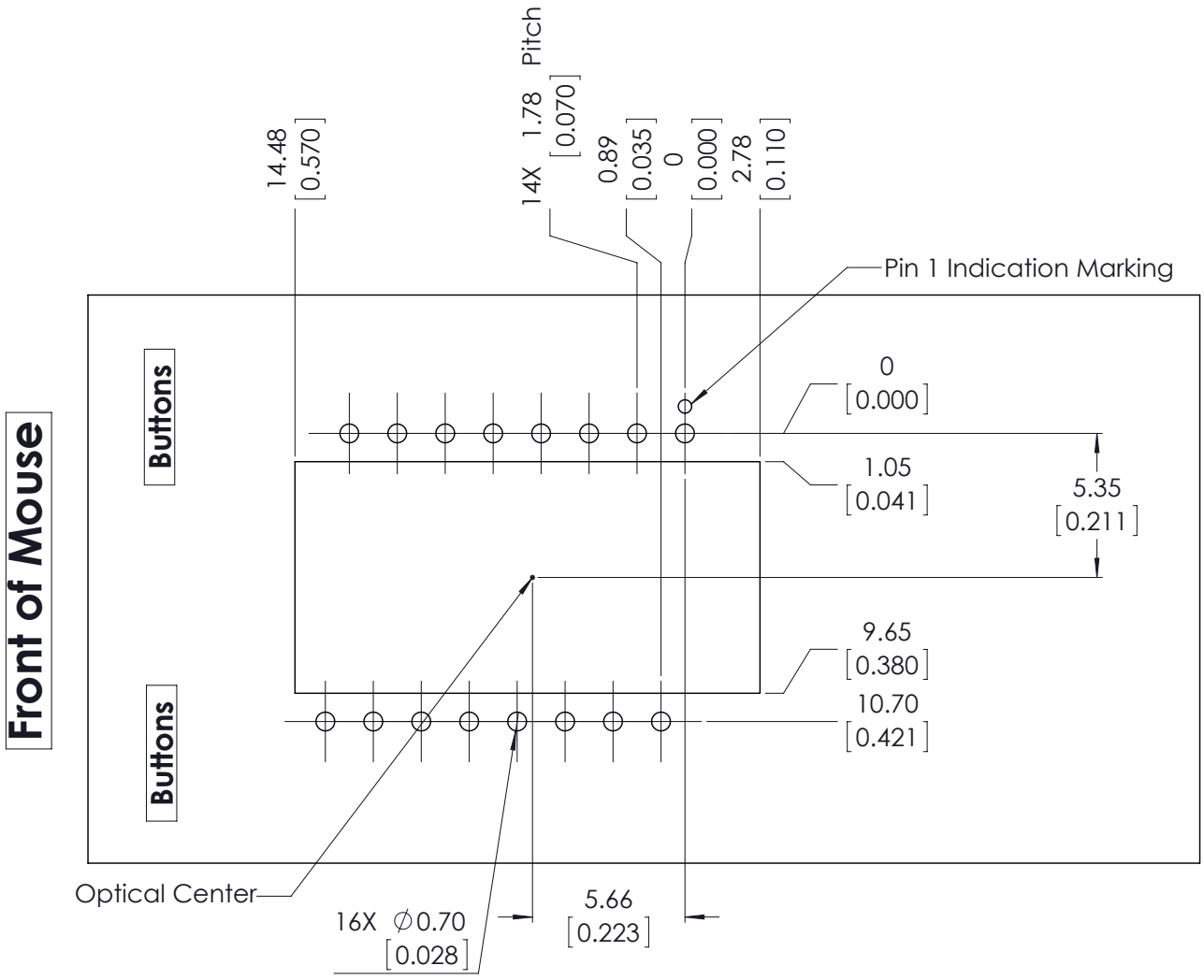


Figure 3. Recommended chip orientation, mechanical cutouts and spacing (Top View)

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

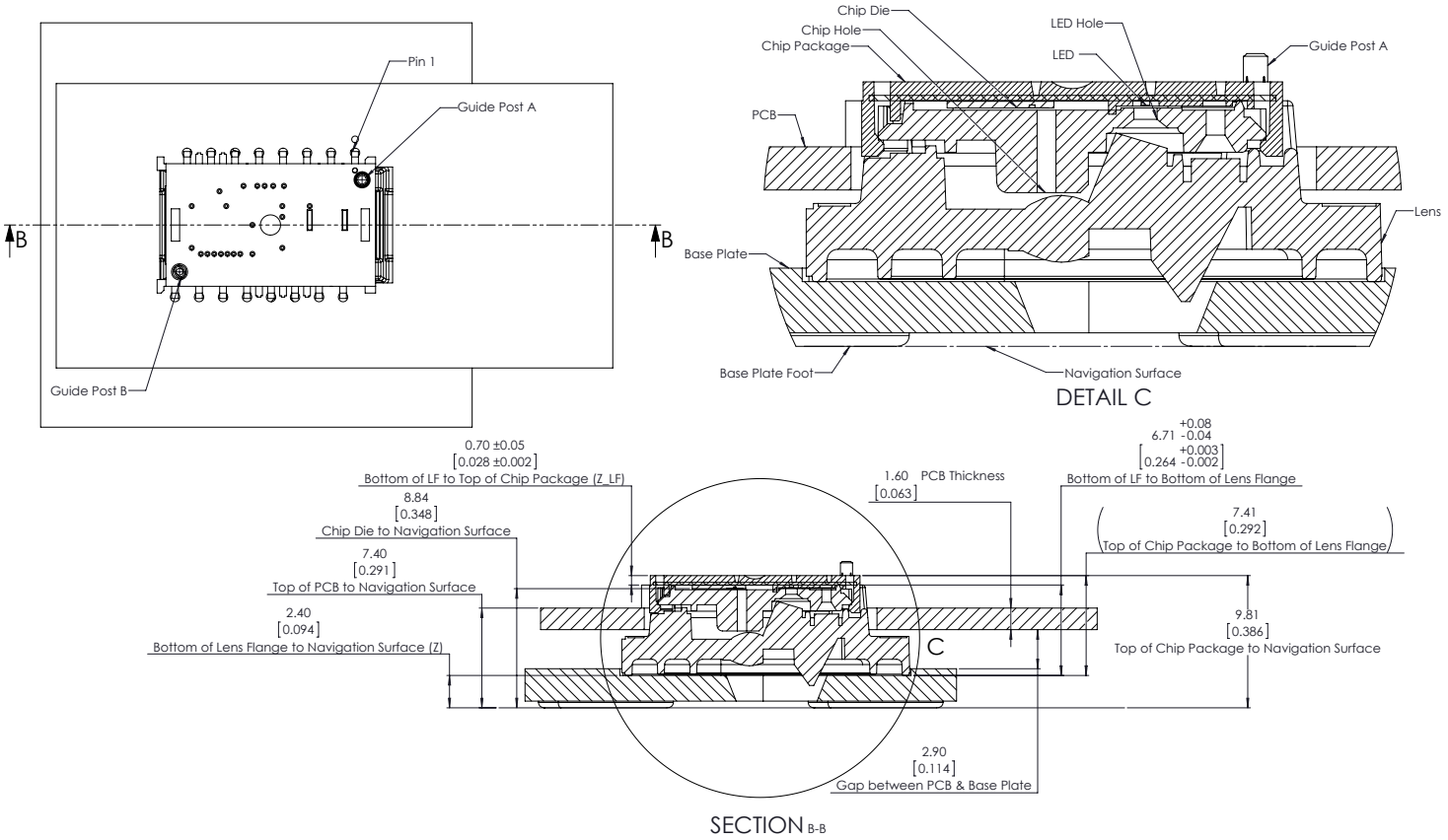


Figure 4. Assembly drawing of PMW3360DM-T2QU and distance from lens reference plane to tracking surface (Z)

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

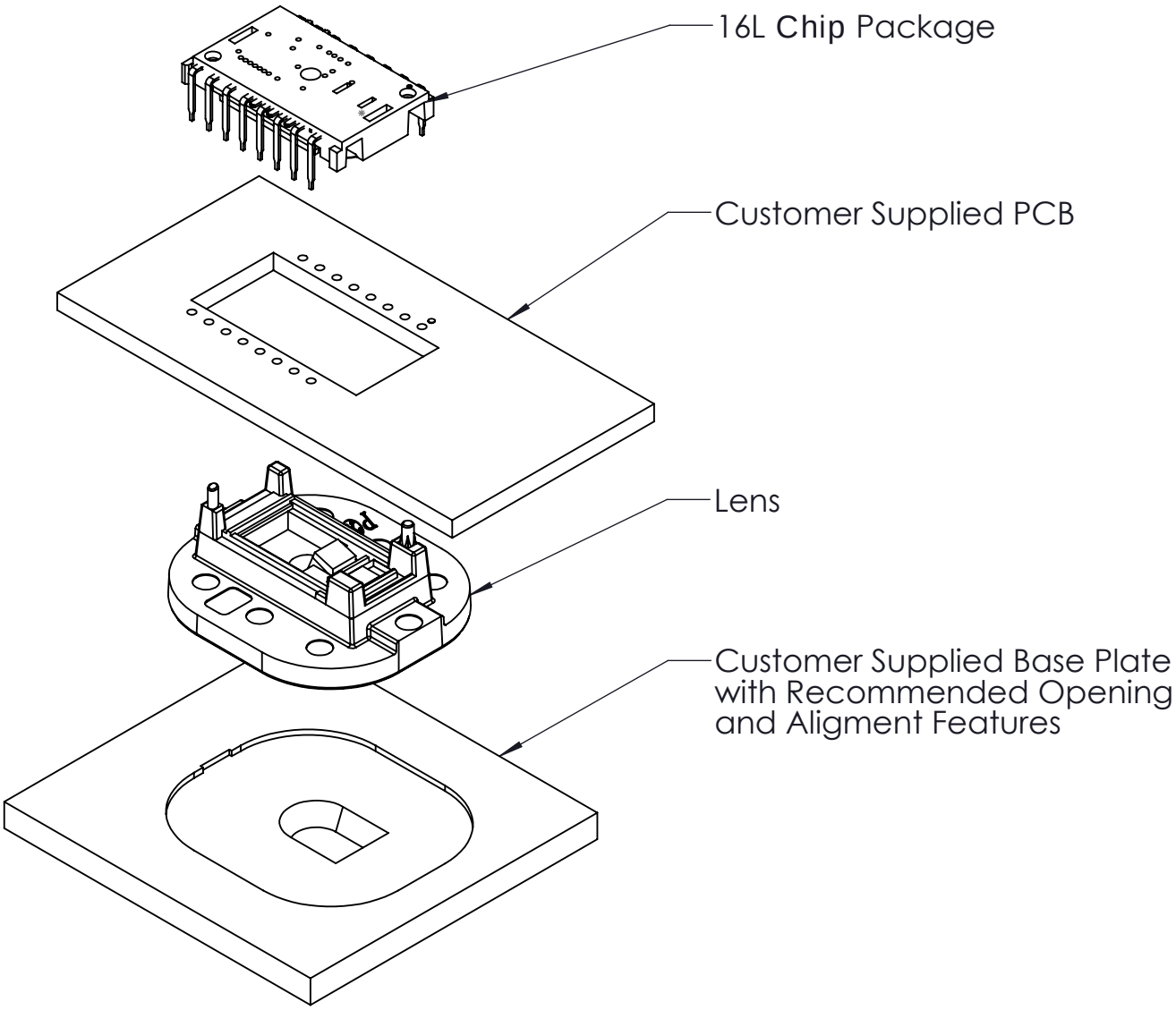


Figure 5. Exploded Assembly View

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

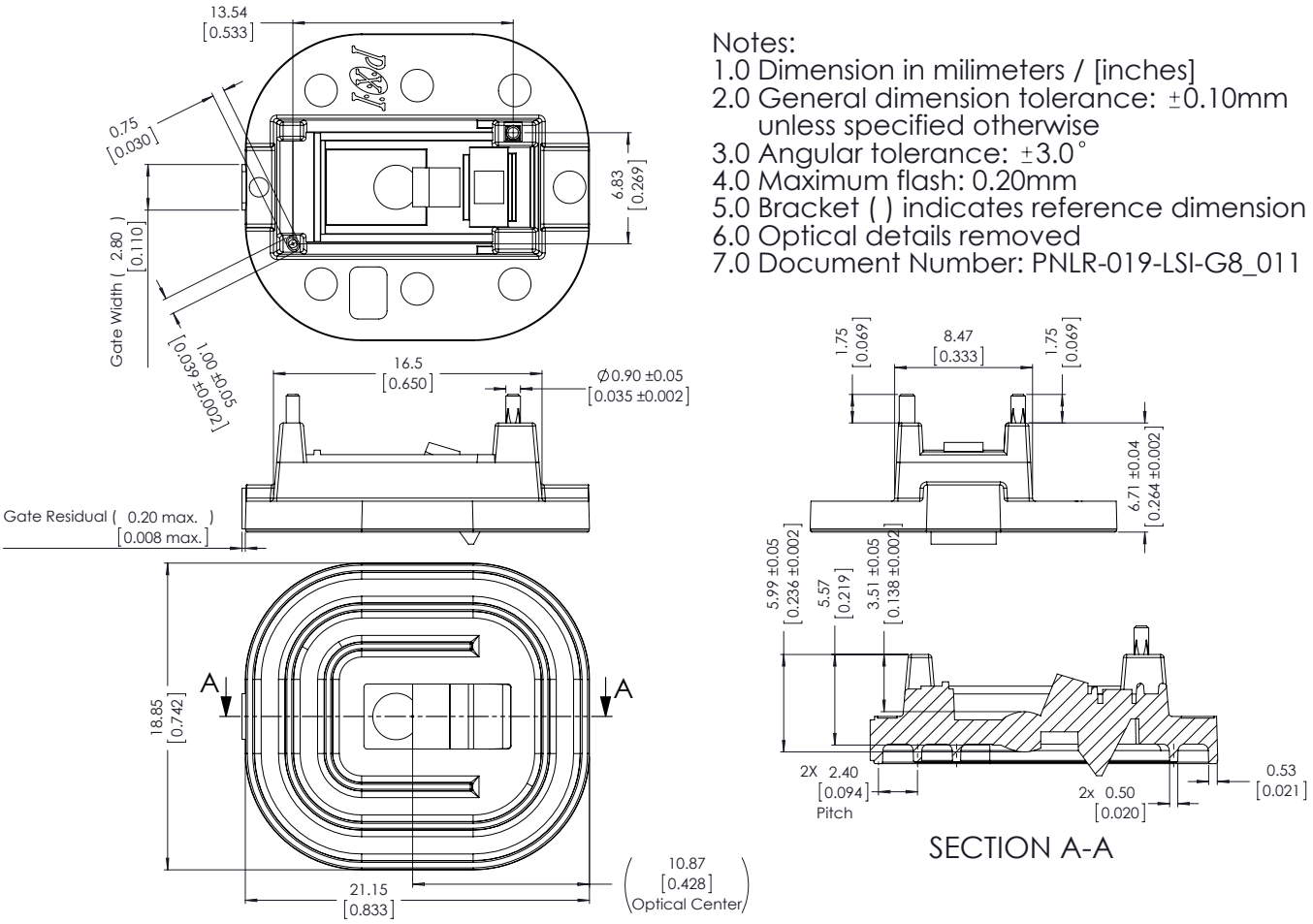


Figure 6. Lens Outline Drawing

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

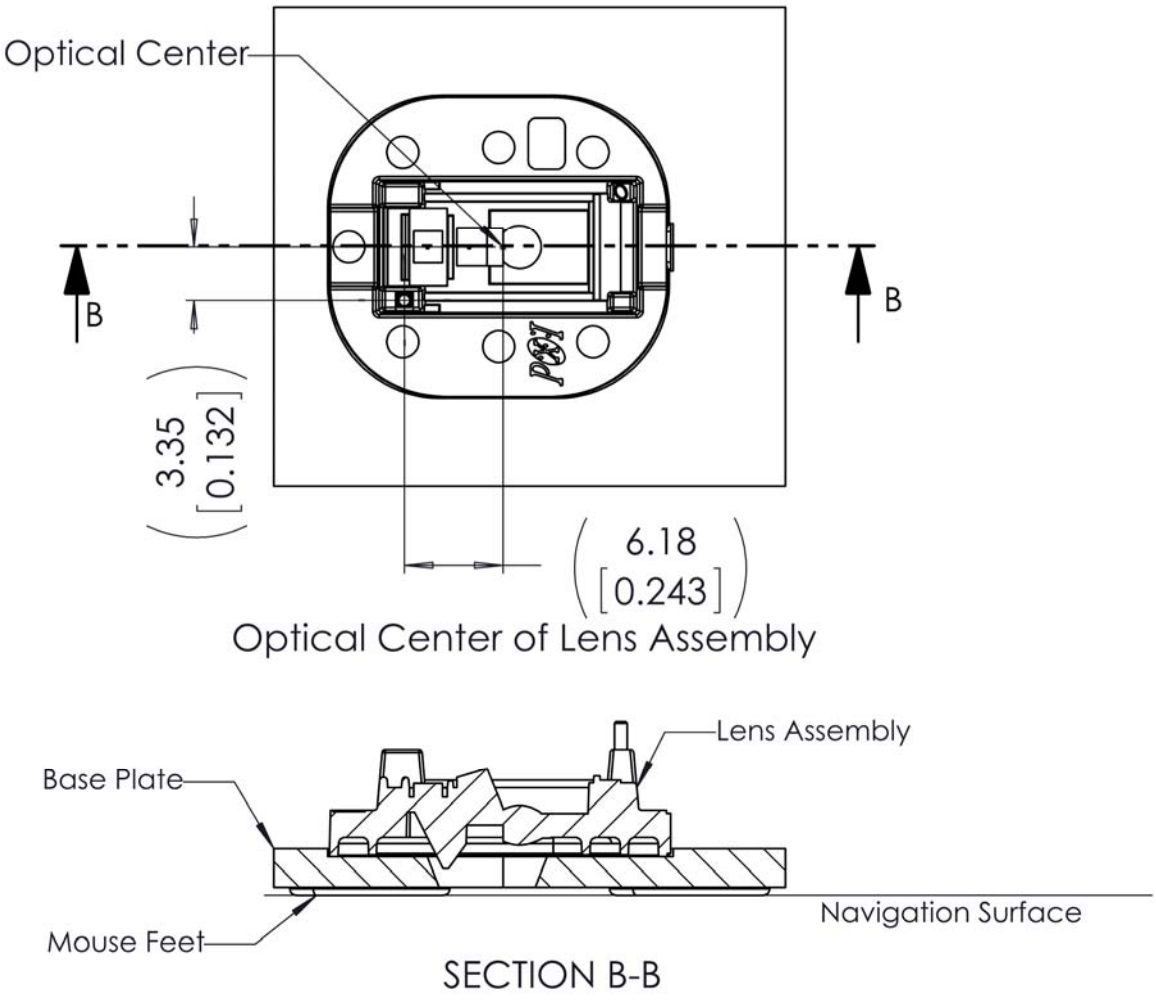


Figure 7. Cross section view of lens assembly

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

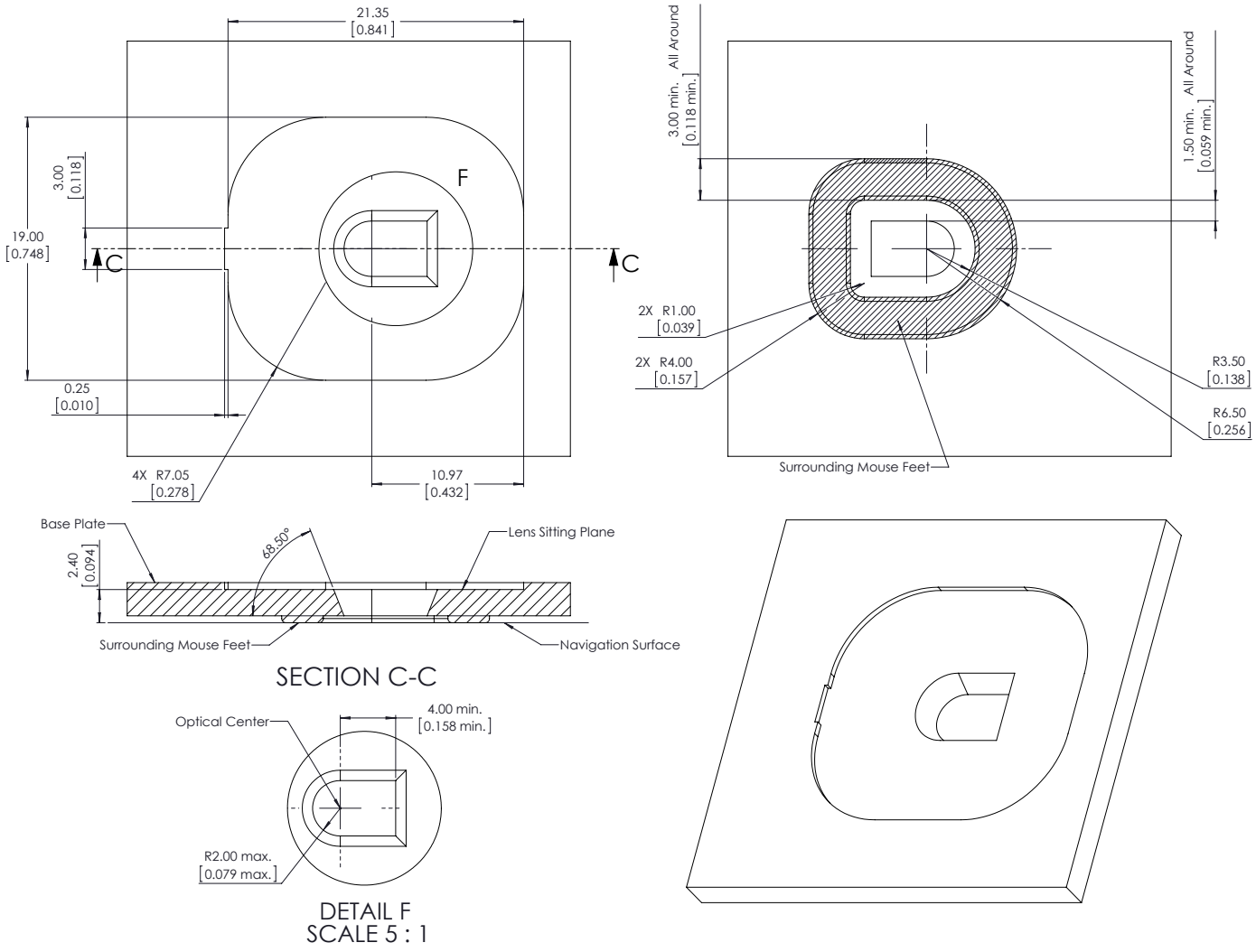


Figure 8. Recommended Base Plate Opening

Note: *Mouse feet should be placed close to the opening to stabilize the surface within the FOV of the chip.*

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

1.4 PCB Assembly Recommendation

1) Insert the integrated chip and all other electrical components into PCB.
2) Wave-solder the entire assembly in a no-wash solder process utilizing solder-fixture. A solder-fixture is required to protect the chip from flux spray and wave solder.
3) Avoid getting any solder flux onto the chip body as there is potential for flux to seep into the chip package, the solder fixture should be designed to expose only the chip leads to flux spray & molten solder while shielding the chip body and optical apertures. The fixture should also set the chip at the correct position and height on the PCB.
4) Place the lens onto the base plate. Care must be taken to avoid contamination on the optical surfaces.
5) Remove the protective kapton tapes from optical apertures of the chip. Care must be taken to prevent Contaminants from entering the apertures. Do not place the PCB with the chip facing up during the entire mouse assembly process. Hold the PCB vertically when removing kapton tape.
6) Insert PCB assembly over the lens onto the base plate aligning post to retain PCB assembly. The chip package will self-align to the lens via the guide posts. The optical position reference for the PCB is set by the base plate and lens. Note that the PCB motion due to button presses must be minimized to maintain optical alignment.
7) Recommendation: The lens can be permanently secured to the chip package by melting the lens' guide posts over the chip with heat staking process. Please refer to the application note PMS0122-LM19-LSI-AN for more details.
8) Install mouse top case. There must be a feature in the top case to press down onto the PCB assembly to ensure all components are stacked or interlocked to the correct vertical height.

Chip Block Diagram

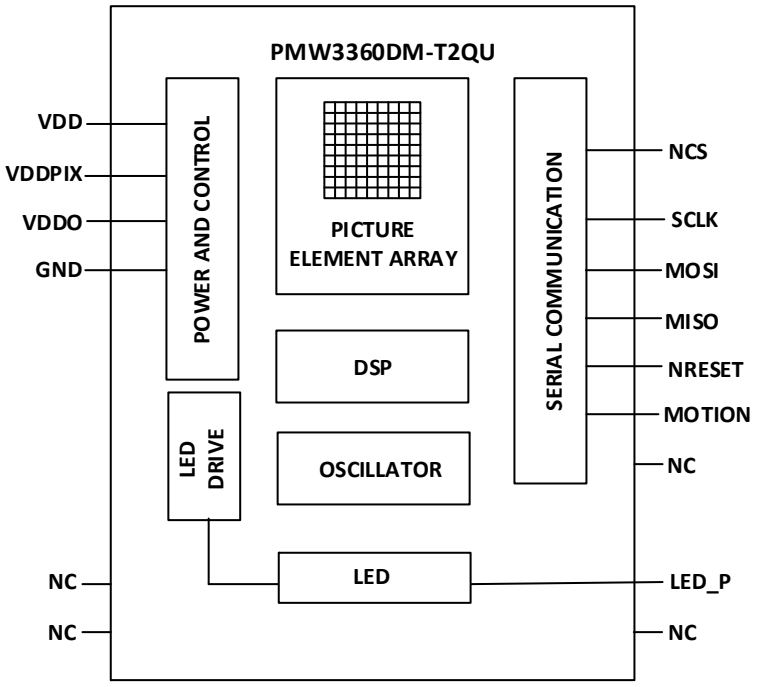


Figure 9. Block diagram of PMW3360DM-T2QU

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

1.5 Reference Schematics

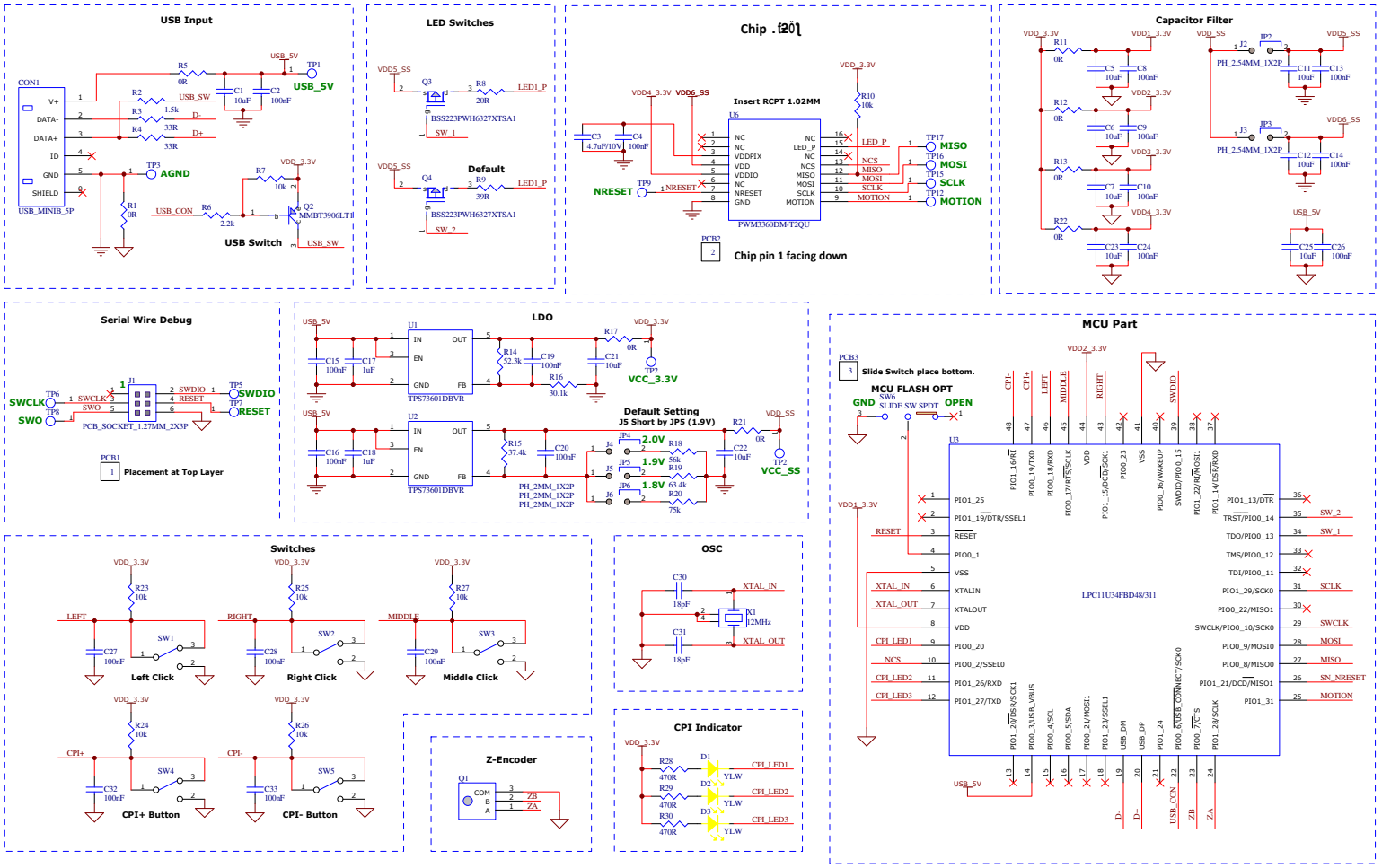


Figure 10. Schematic diagram for interface between PMW3360DM-T2QU and microcontroller on a wired solution

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

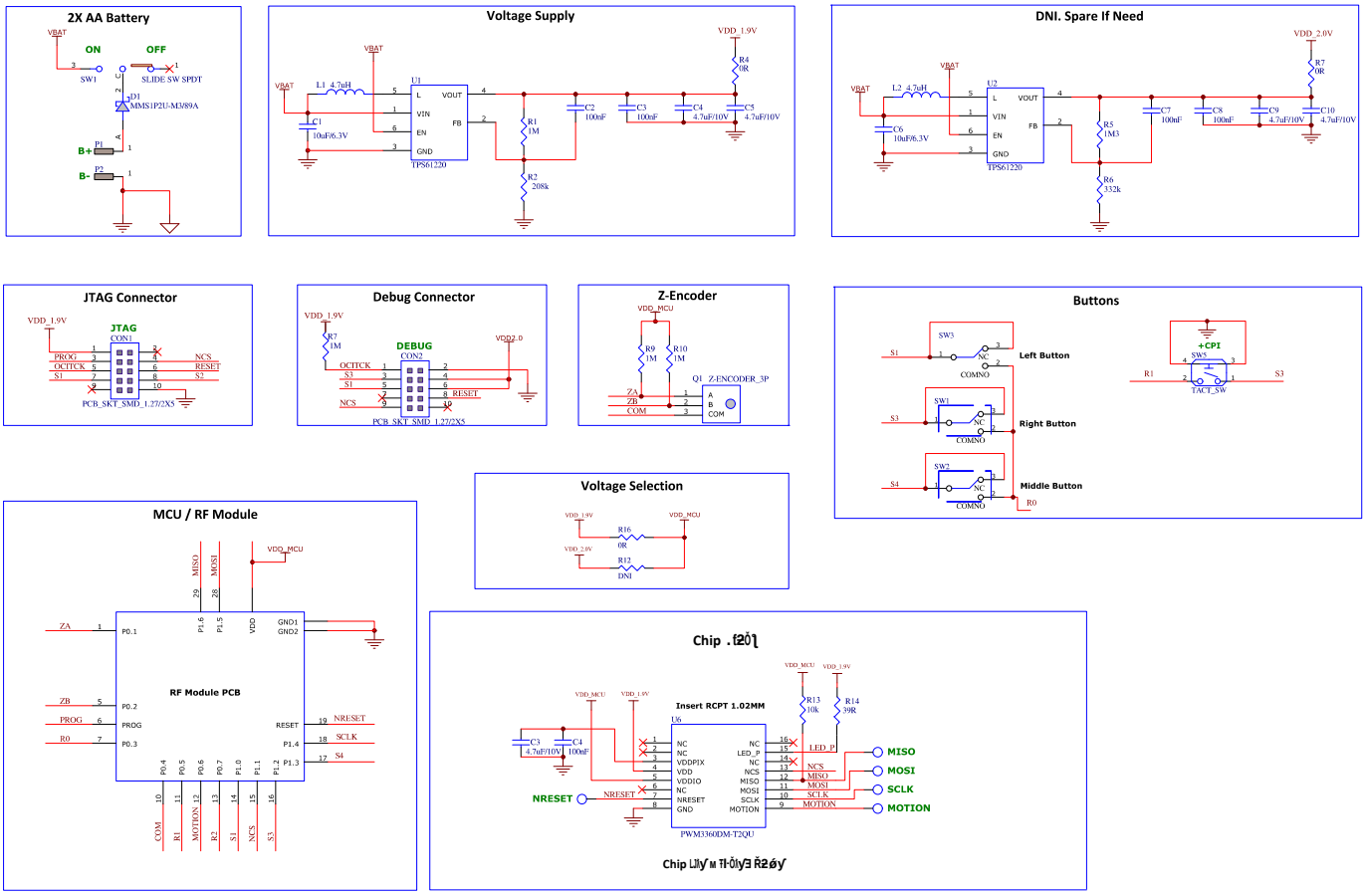


Figure 11. Schematic diagram for interface between PMW3360DM-T2QU and microcontroller on a wireless solution

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

2.0 Electrical Specifications

Regulatory Requirements

- Passes FCC "Part15, Subpart B, Class B", "CISPR 22 1997 Class B" and worldwide analogous emission limits when assembled into a mouse with shielded cable and following PixArt Imaging's recommendations.
- Passes IEC 62471: 2006 Photo biological safety of lamps and lamp systems

2.1 Absolute Maximum Ratings

Table 2: Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-40	85	°C	
Lead Solder Temperature	T_{SOLDER}		260	°C	For 7 seconds, 1.6mm below seating plane.
Supply Voltage	V_{DD}	-0.5	2.10	V	
	V_{DDIO}	-0.5	3.60	V	
ESD (Human Body Model)			2	kV	All pins
Input Voltage	V_{IN}	-0.5	3.6	V	All I/O pins.

2.2 Recommended Operating Conditions

Table 3: Recommended Operating Condition

Parameter	Symbol	Min	Typ.	Max	Units	Notes
Operating Temperature	T_A	0		40	°C	
Power Supply Voltage	V_{DD}	1.80	1.90	2.10	V	excluding supply noise
	V_{DDIO}	1.80	1.90	3.60	V	excluding supply noise. (VDDIO must be same or greater than VDD)
Power Supply Rise Time	t_{RT}	0.15		20	ms	0 to VDD min
Supply Noise (Sinusoidal)	V_{NA}			100	mVp-p	10 kHz —75 MHz
Serial Port Clock Frequency	f_{SCLK}			2.0	MHz	50% duty cycle
Distance from Lens Reference Plane to Tracking Surface	Z	2.2	2.4	2.6	mm	
Speed	S		250		ips	300ips on QCK, Vespula Speed, Vespula Control and FUNC 1030 surfaces
Resolution error	R_{esErr}		1		%	Up to 200ips on QCK with 5000 cpi
Acceleration	A			50	g	In run mode

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

2.3 AC Electrical Specifications

Table 4. AC Electrical Specifications

Electrical characteristics over recommended operating conditions. Typical values at 25 °C, V_{DD} = 1.9 V, V_{DDIO} = 1.9V.

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Motion Delay After Reset	$t_{MOT-RST}$	50			ms	From reset to valid motion, assuming motion is present
Shutdown	t_{STDWN}			500	µs	From Shutdown mode active to low current
Wake From Shutdown	t_{WAKEUP}	50			ms	From Shutdown mode inactive to valid motion. Notes: A RESET must be asserted after a shutdown. Refer to section "Notes on Shutdown", also note $t_{MOT-RST}$
MISO Rise Time	t_{r-MISO}		50		ns	C_L = 100pF
MISO Fall Time	t_{f-MISO}		50		ns	C_L = 100pF
MISO Delay After SCLK	$t_{DLY-MISO}$			90	ns	From SCLK falling edge to MISO data valid, no load conditions
MISO Hold Time	$t_{hold-MISO}$	200			ns	Data held until next falling SCLK edge
MOSI Hold Time	$t_{hold-MOSI}$	200			ns	Amount of time data is valid after SCLK rising edge
MOSI Setup Time	$t_{setup-MOSI}$	120			ns	From data valid to SCLK rising edge
SPI Time Between Write Commands	t_{SWW}	180			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte.
SPI Time Between Write And Read Commands	t_{SWR}	180			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second address byte.
SPI Time Between Read And Subsequent Commands	t_{SRW} t_{SRR}	20			µs	From rising SCLK for last bit of the first data byte, to falling SCLK for the first bit of the address byte of the next command.
SPI Read Address-Data Delay	t_{SRAD}	160			µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read.
SPI Read Address-Data Delay for Burst Mode Motion Read	t_{SRAD_MOTBR}	35			µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read. Applicable for Burst Mode Motion Read only.
NCS Inactive After Motion Burst	t_{BEXIT}	500			ns	Minimum NCS inactive time after motion burst before next SPI usage
NCS To SCLK Active	$t_{NCS-SCLK}$	120			ns	From last NCS falling edge to first SCLK rising edge

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
SCLK To NCS Inactive (For Read Operation)	$t_{SCLK-NCS}$	120			ns	From last SCLK rising edge to NCS rising edge, for valid MISO data transfer
SCLK To NCS Inactive (For Write Operation)	$t_{SCLK-NCS}$	35			µs	From last SCLK rising edge to NCS rising edge, for valid MOSI data transfer
NCS To MISO High-Z	$t_{NCS-MISO}$			500	ns	From NCS rising edge to MISO high-Z state
MOTION Rise Time	$t_{r-MOTION}$		50		ns	C_L = 100pF
MOTION Fall Time	$t_{f-MOTION}$		50		ns	C_L = 100pF
Input Capacitance	C_{in}		50		pF	SCLK, MOSI, NCS
Load Capacitance	C_L			100	pF	MISO, MOTION
Transient Supply Current	I_{DDT}			70	mA	Max supply current during the supply ramp from 0V to V_{DD} with min 150 us and max 20ms rise time. (Does not include charging currents for bypass capacitors)
	I_{DDTIO}			60	mA	Max supply current during the supply ramp from 0V to V_{DDIO} with min 150 us and max 20ms rise time. (Does not include charging currents for bypass capacitors)

2.4 DC Electrical Specifications

Table 5. DC Electrical Specifications

Electrical characteristics, over recommended operating conditions. Typical values at 25 °C, V_{DD} = 1.9 V, V_{DDIO} = 1.9V, LED current at 12mA, 70MHz (internal), and 1.1kHz (slow clock).

Parameter	Symbol	Min	Typ.	Max	Units	Notes
DC Supply Current	I_{DD_RUN1} I_{DD_RUN2} I_{DD_RUN3} I_{DD_RUN4} I_{DD_REST1} I_{DD_REST2} I_{DD_REST3}		16.3 18.6 21.6 37.0 2.8 61.0 32.0		mA mA mA mA mA uA uA	Average current consumption, including LED current with 1ms polling.
Power Down Current	I_{PD}		10		µA	
Input Low Voltage	V_{IL}			0.3 x V_{DDIO}	V	SCLK, MOSI, NCS
Input High Voltage	V_{IH}	0.7 x V_{DDIO}			V	SCLK, MOSI, NCS
Input Hysteresis	V_{I_HYS}		100		mV	SCLK, MOSI, NCS
Input Leakage Current	I_{leak}		±1	±10	µA	Vin=V_{DDIO} or 0V, SCLK, MOSI, NCS
Output Low Voltage	V_{OL}			0.45	V	Iout=1mA, MISO, MOTION
Output High Voltage	V_{OH}	V_{DDIO} - 0.45			V	Iout=-1mA, MISO, MOTION

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

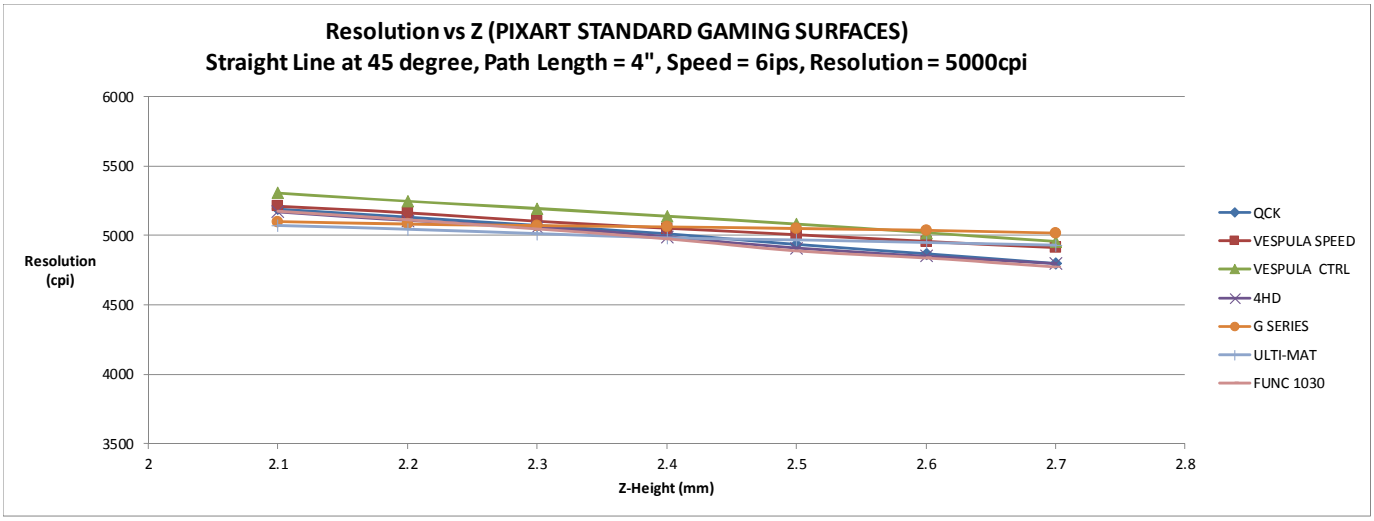


Figure 12 Mean Resolution vs. Z at default resolution at 5000cpi

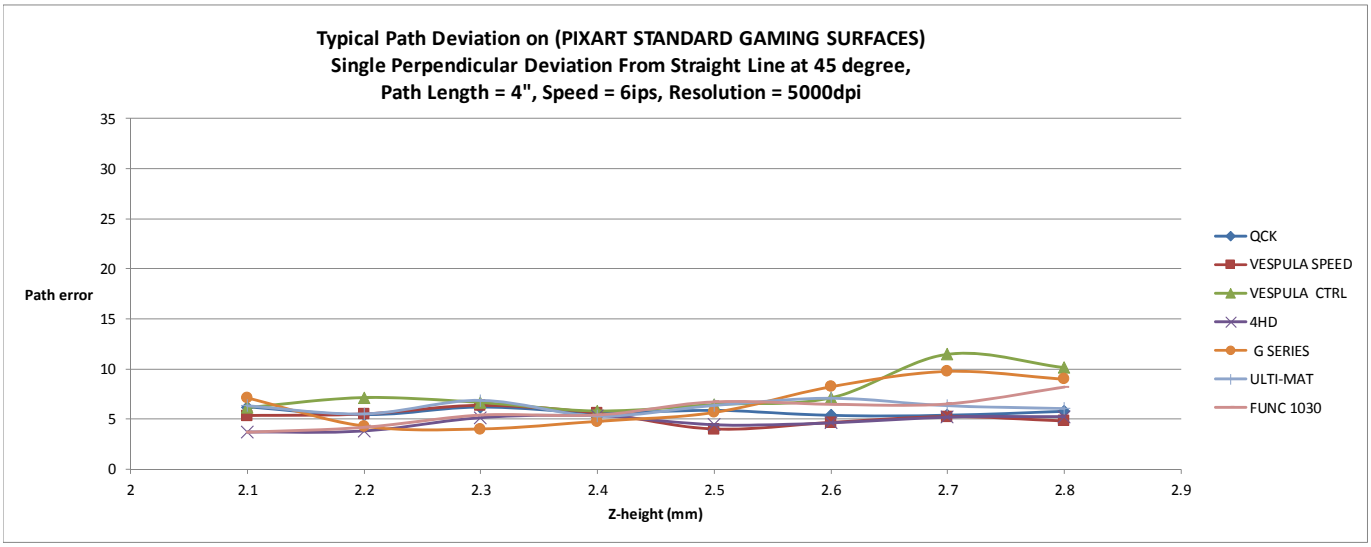


Figure 13 Path error vs. Z-height at default resolution at 5000cpi (mm)

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

3.0 Serial Peripheral Interface (SPI)

The synchronous serial port is used to set and read parameters in PMW3360DM-T2QU chip, and to read out the motion information. The serial port is also used to load SROM data into PMW3360DM-T2QU chip.

The port is a four wire port. The host microcontroller always initiates communication; PMW3360DM-T2QU chip never initiates data transfers. SCLK, MOSI, and NCS may be driven directly by a microcontroller. The port pins may be shared with other SPI slave devices. When the NCS pin is high, the inputs are ignored and the output is tri-stated.

The lines that comprise the SPI port are:

SCLK	Clock input, generated by the master (microcontroller).
MOSI	Input data. (Master Out/Slave In)
MISO	Output data. (Master In/Slave Out)
NCS	Chip select input (active low). NCS needs to be low to activate the serial port; otherwise, MISO will be high Z, and MOSI & SCLK will be ignored. NCS can also be used to reset the serial port in case of an error.

Motion Pin Timing

The motion pin is an active low output that signals the micro-controller when motion has occurred. The motion pin is lowered whenever the motion bit is set; in other words, whenever there is non-zero data in the Delta_X_L, Delta_X_H, Delta_Y_L or Delta_Y_H registers. Clearing the motion bit (by reading Delta_X_L, Delta_X_H, Delta_Y_L or Delta_Y_H registers) will put the motion pin high.

Chip Select Operation

The serial port is activated after NCS goes low. If NCS is raised during a transaction, the entire transaction is aborted and the serial port will be reset. This is true for all transactions including SROM download. After a transaction is aborted, the normal address-to-data or transaction-to-transaction delay is still required before beginning the next transaction. To improve communication reliability, all serial transactions should be framed by NCS. In other words, the port should not remain enabled during periods of non-use because ESD and EFT/B events could be interpreted as serial communication and put the chip into an unknown state. In addition, NCS must be raised after each burst-mode transaction is complete to terminate burst-mode. The port is not available for further use until burst-mode is terminated.

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Write Operation

Write operation, defined as data going from the micro-controller to PMW3360DM-T2QU chip, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. PMW3360DM-T2QU chip reads MOSI on rising edges of SCLK.

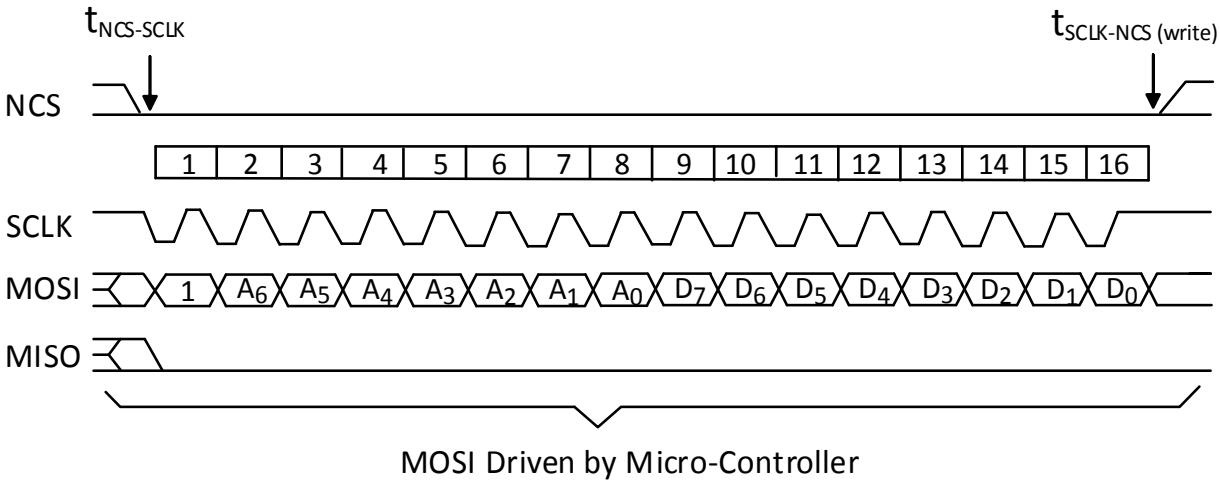


Figure 14. Write operation

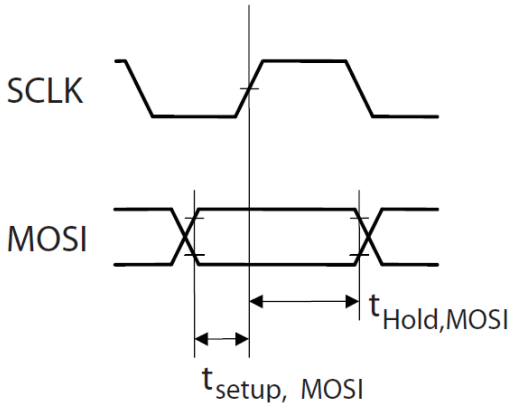


Figure 15. MOSI setup and hold time

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Read Operation

A read operation, defined as data going from PMW3360DM-T2QU chip to the micro-controller, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address, is sent by the micro-controller over MOSI, and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by PMW3360DM-T2QU chip over MISO. The chip outputs MISO bits on falling edges of SCLK and samples MOSI bits on every rising edge of SCLK.

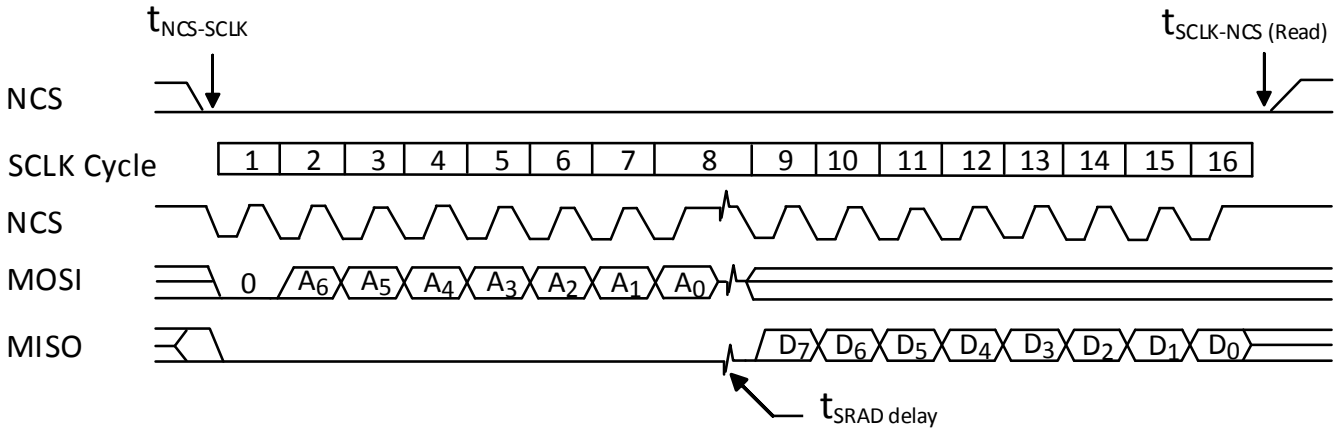


Figure 16. Read operation

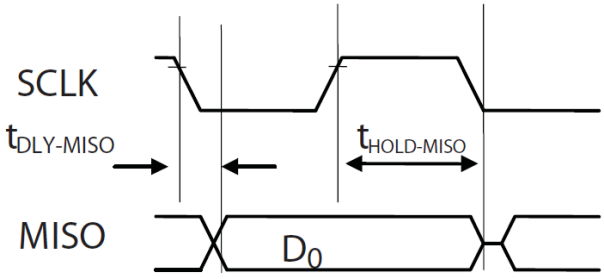


Figure 17. MISO Delay and hold time

Note: The minimum high state of SCLK is also the minimum MISO data hold time of PMW3360DM-T2QU chip. Since the falling edge of SCLK is actually the start of the next read or write command, PMW3360DM-T2QU chip will hold the state of data on MISO until the falling edge of SCLK.

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Required timing between Read and Write Commands (tsxx)

There are minimum timing requirements between read and write commands on the serial port.

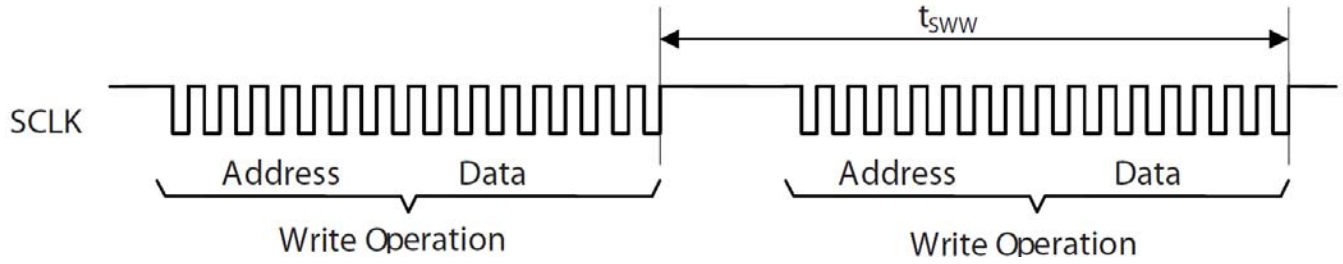


Figure 18. Timing between two write commands

If the rising edge of the SCLK for the last data bit of the second write command occurs before the t_{SWW} delay, then the first write command may not complete correctly.

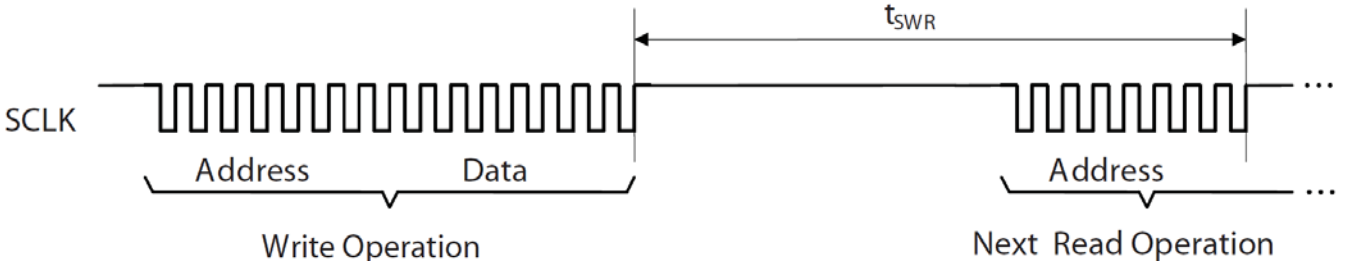


Figure 19. Timing between write and either write or subsequent read commands

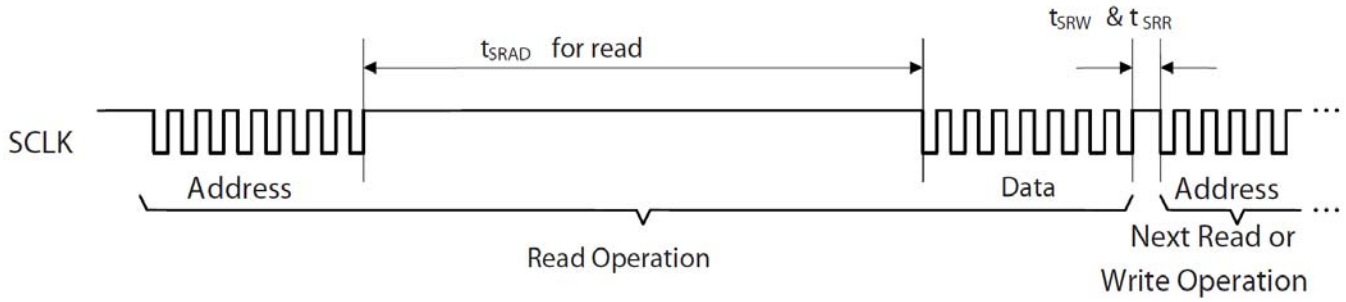


Figure 20. Timing between read and either write or subsequent read commands

If the rising edge of SCLK for the last address bit of the read command occurs before the t_{SWR} required delay, the write command may not complete correctly. During a read operation SCLK should be delayed at least t_{SRAD} after the last address data bit to ensure that the Chip has time to prepare the requested data.

The falling edge of SCLK for the first address bit of either the read or write command must be at least t_{SRR} or t_{SRW} after the last SCLK rising edge of the last data bit of the previous read operation. In addition, during a read operation SCLK should be delayed after the last address data bit to ensure that PMW3360DM-T2QU chip has time to prepare the requested data.

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

4.0 Burst mode operation

Burst Mode Operation

Burst mode is a special serial port operation mode which may be used to reduce the serial transaction time for three predefined operations: motion read and SROM download and frame capture. The speed improvement is achieved by continuous data clocking to or from multiple registers without the need to specify the register address, and by not requiring the normal delay period between data bytes.

Motion Read

Reading the Motion_Burst register activates this mode. PMW3360DM-T2QU chip will respond with the following motion burst report in order. Motion burst report:

BYTE[00] = Motion
BYTE[01] = Observation
BYTE[02] = Delta_X_L
BYTE[03] = Delta_X_H
BYTE[04] = Delta_Y_L
BYTE[05] = Delta_Y_H
BYTE[06] = SQUAL
BYTE[07] = Raw_Data_Sum
BYTE[08] = Maximum_Raw_Data
BYTE[09] = Minimum_Raw_Data
BYTE[10] = Shutter_Upper
BYTE[11] = Shutter_Lower

After sending the register address, the microcontroller must wait for t_{SRAD_MOTBR}, and then begin reading data. All data bits can be read with no delay between bytes by driving SCLK at the normal rate. The data are latched into the output buffer after the last address bit is received. After the burst transmission is complete, the microcontroller must raise the NCS line for at least t_{BEXIT} to terminate burst mode. The serial port is not available for use until it is reset with NCS, even for a second burst transmission.

Procedure to start motion burst:

1. Write any value to Motion_Burst register.
2. Lower NCS
3. Send Motion_Burst address (0x50).
4. Wait for t_{SRAD_MOTBR}
5. Start reading SPI Data continuously up to 12 bytes. Motion burst may be terminated by pulling NCS high for at least t_{BEXIT}.
6. To read new motion burst data, repeat from step 2.
7. If a non-burst register read operation was executed; then, to read new burst data, start from step 1 instead.

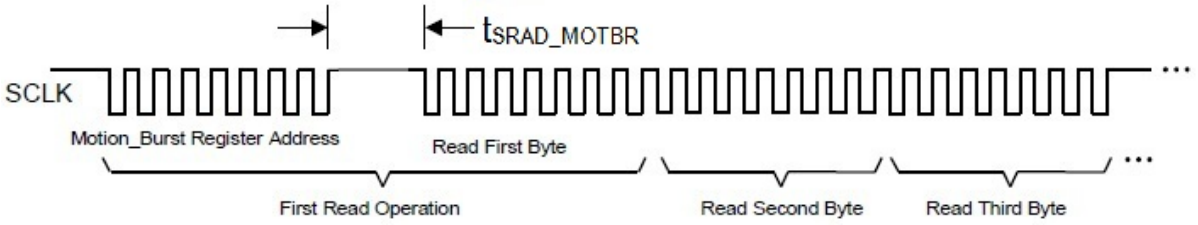


Figure 21. Motion Read sequence for step 3 to 5

Note: Motion burst data can be read from the Motion_Burst registers even in run or rest mode.

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

5.0 SROM Download

This function is used to load the supplied firmware file contents into PMW3360DM-T2QU after chip power up sequence. The firmware file is an ASCII text file.

SROM download procedure:

1. Perform the Power-Up sequence (steps 1 to 8)
2. Write 0 to Rest_En bit of Config2 register to disable Rest mode.
3. Write 0x1d to SROM_Enable register for initializing
4. Wait for 10 ms
5. Write 0x18 to SROM_Enable register again to start SROM Download
6. Write SROM file into SROM_Load_Burst register, 1st data must start with SROM_Load_Burst address. All the SROM data must be downloaded before SROM starts running.
7. Read the SROM_ID register to verify the ID before any other register reads or writes.
8. Write 0x00 to Config2 register for wired mouse or 0x20 for wireless mouse design.

The SROM download success may be verified in two ways. Once execution from SROM space begins, the SROM_ID register will report the firmware version. At any time, a self-test may be executed which performs a CRC on the SROM contents and reports the results in a register. Take note that the self-test does disrupt tracking performance and also reset registers to default value. The test is initiated by writing 0x15 to the SROM_Enable register and the result is placed in the Data_Out_Lower and Data_Out_Upper registers. See register description for more details.

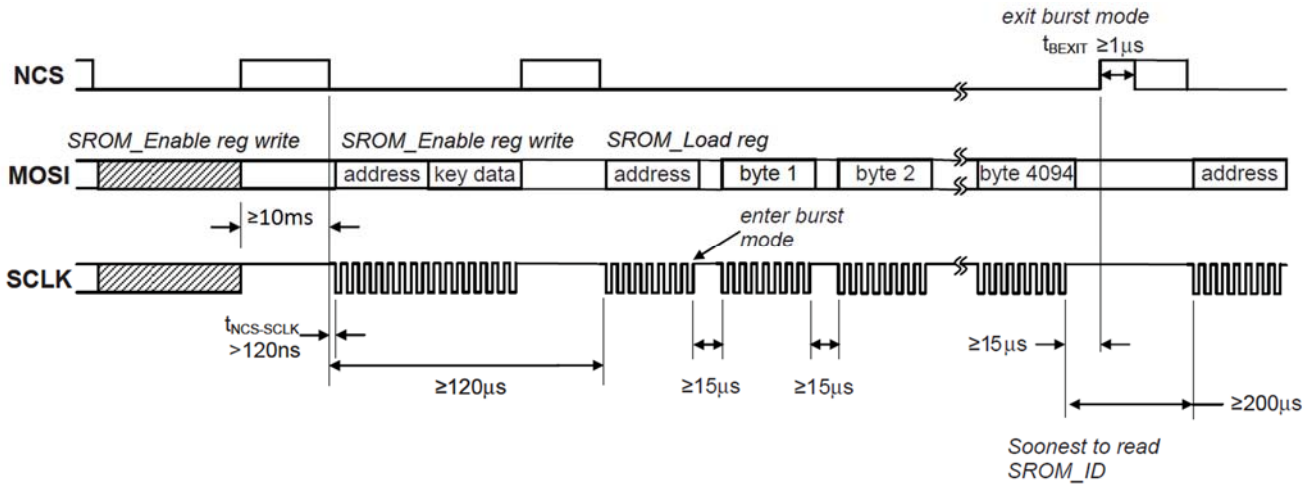


Figure 22. SROM Download Burst Mode

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

6.0 Frame Capture

This is a fast way to download a full array of raw data values from a single frame. This mode disables navigation and overwrites any downloaded firmware. A hardware reset is required to restore navigation, and the firmware must be reloaded.

To trigger the capture, write to the Frame_Capture register. The next available complete 1 frame image will be stored to memory. The data is retrieved by reading the Raw_Data_Burst register using burst read method per the waveform below. If the Raw_ Data_Burst register is read before the data is ready (step 6 below), it will return all zeros.

Frame Capture procedure:

1. The chip should be powered up and reset correctly (SROM download should be part of this powered up and reset sequence - refer to Power Up sequence in data sheet for more information).
2. Wait for 250ms.
3. Write 0 to Rest_En bit of Config2 register to disable Rest mode.
4. Write 0x83 to Frame_Capture register.
5. Write 0xC5 to Frame_Capture register.
6. Wait for 20ms.
7. Continue burst read from Raw_data_Burst register until all 1296 raw data are transferred.
8. Continue step 1-8 to capture another frame.

Note: Manual reset and SROM download are needed after frame capture to restore navigation.

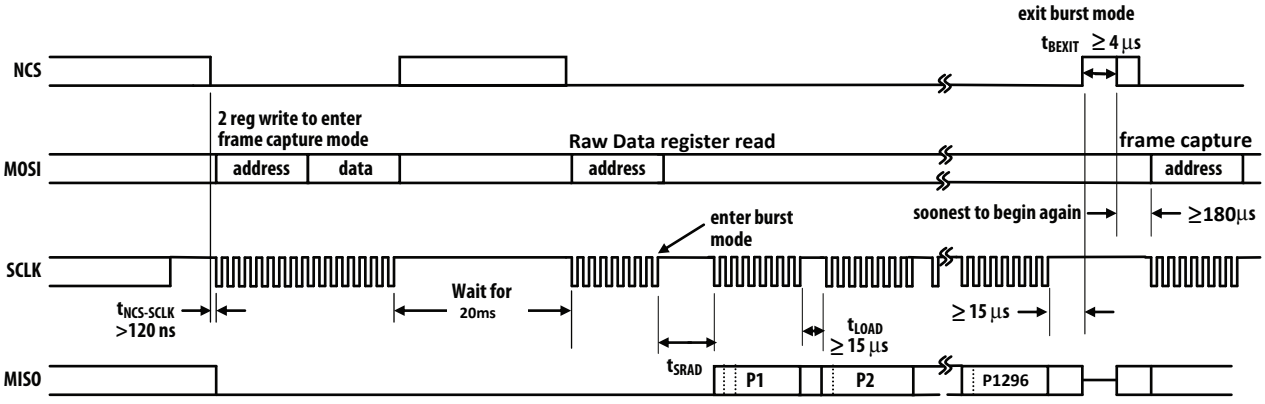
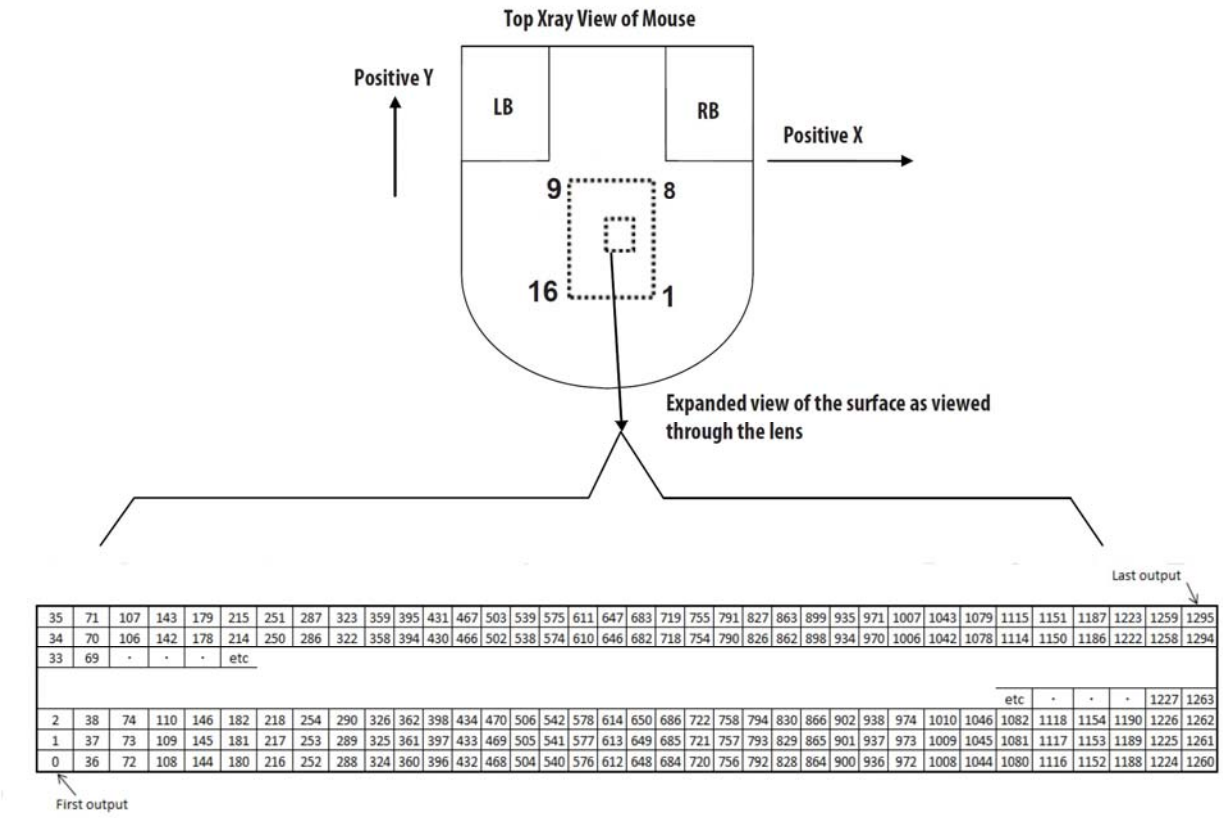


Figure 23. Frame Capture Burst Mode

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms



35	71	107	143	179	215	251	287	323	359	395	431	467	503	539	575	611	647	683	719	755	791	827	863	899	935	971	1007	1043	1079	1115	1151	1187	1223	1259	1295
34	70	106	142	178	214	250	286	322	358	394	430	466	502	538	574	610	646	682	718	754	790	826	862	898	934	970	1006	1042	1078	1114	1150	1186	1222	1258	1294
33	69	·	·	·	etc																														
																														etc	·	·	·	1227	1263
2	38	74	110	146	182	218	254	290	326	362	398	434	470	506	542	578	614	650	686	722	758	794	830	866	902	938	974	1010	1046	1082	1118	1154	1190	1226	1262
1	37	73	109	145	181	217	253	289	325	361	397	433	469	505	541	577	613	649	685	721	757	793	829	865	901	937	973	1009	1045	1081	1117	1153	1189	1225	1261
0	36	72	108	144	180	216	252	288	324	360	396	432	468	504	540	576	612	648	684	720	756	792	828	864	900	936	972	1008	1044	1080	1116	1152	1188	1224	1260

Figure 24. Raw data Map (Surface referenced)

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

7.0 Power Up

Although the chip performs an internal power up self reset, it is still recommend that the Power_Up_Reset register is written every time power is applied. The appropriate sequence is as follows:

1. Apply power to VDD and VDDIO in any order, with a delay of no more than 100ms in between each supply. Ensure all supplies are stable.
2. Drive NCS high, and then low to reset the SPI port.
3. Write 0x5A to Power_Up_Reset register (or, alternatively toggle the NRESET pin).
4. Wait for at least 50ms.
5. Read from registers 0x02, 0x03, 0x04, 0x05 and 0x06 one time regardless of the motion pin state.
6. Perform SROM download.
7. Load configuration for other registers.

During power-up there will be a period of time after the power supply is high but before normal operation. The table below shows the state of the various pins during power-up and reset.

State of Signal Pins After VDD is Valid		
Pin	During Reset	After Reset
NRESET	Functional	Functional
NCS	Ignored	Functional
MISO	Undefined	Depends on NCS
SCLK	Ignored	Depends on NCS
MOSI	Ignored	Depends on NCS
MOTION	Undefined	Functional

NRESET

The NRESET pin can be used to perform a full chip reset. When asserted, it performs the same reset function as the Power_Up_Reset_Register. The NRESET pin needs to be asserted (held to logic 0) for at least 100 ns.

Note:- NRESET pin has a built in weak pull up circuit. During active low reset phase, it can draw a static current of up to 600uA.

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

8.0 Shutdown

PMW3360DM-T2QU can be set in Shutdown mode by writing to Shutdown register. The SPI port should not be accessed when Shutdown mode is asserted, except the power-up command (writing 0x5a to register 0x3a). Other ICs on the same SPI bus can be accessed, as long as the chip's NCS pin is not asserted. The SROM download is required when wake up from Shutdown mode.

To de-assert Shutdown mode:

1. Drive NCS high, and then low to reset the SPI port.
2. Write 0x5A to Power_Up_Reset register (or, alternatively toggle the NRESET pin).
3. Wait for at least 50ms.
4. Read from registers 0x02, 0x03, 0x04, 0x05 and 0x06 one time regardless of the motion pin state.
5. Perform SROM download.
6. Load configuration for other registers.

Pin	Status when Shutdown Mode
NRESET	High
NCS	High*1
MISO	Hi-Z*2
SCLK	Ignore if NCS = 1*3
MOSI	Ignore if NCS = 1*4
MOTION	Output High

*1. NCS pin must be held to 1 (high) if SPI bus is shared with other devices. It is recommended to hold to 1 (high) during Shutdown unless powering up the chip. It must be held to 0 (low) if the chip is to be re-powered up from shutdown (writing 0x5a to register 0x3a).
*2. MISO should be either pull up or down during shutdown in order to meet the low power consumption specification in the datasheet.
*3. SCLK is ignored if NCS is 1 (high). It is functional if NCS is 0 (low).
*4. MOSI is ignored if NCS is 1 (high). If NCS is 0 (low), any command present on the MOSI pin will be ignored except power-up command (writing 0x5a to register 0x3a).

Note:- There are long wakeup times from shutdown. These features should not be used for power management during normal mouse motion.

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

9.0 Lift cut off calibration

This chip has the capability to optimize its lift performance by tuning internal parameters to the surface. This “Lift cut off calibration” feature involves user interaction.

Take note that the Lift cut off calibration procedure that follows references registers of seven Lift cut off calibration related registers: (i) LiftCutoff_Tune1, (ii) LiftCutoff_Tune2, (iii) LiftCutoff_Tune3, (iv) LiftCutoff_Tune_Timeout, (v) LiftCutoff_Tune_Min_Length, (vi) Raw data_Threshold and (vii) Min_SQ_Run.

1. Ensure that the chip is powered up according to the Power Up Sequence.
2. Ensure that Lift cut off calibration SROM*[1] is downloaded.
3. Delay for 30ms.
4. Prompt the user that the "Lift cut off calibration" procedure is about to begin to ensure that the mouse is placed nominally on the surface (mouse is not lifted).
5. Start the calibration procedure by setting RUN_CAL register bit to 1. The calibration procedure can be started by a SW prompt to the user or user-initiated through a mouse-click event.
6. Poll CAL_STAT[2:0] to check the status of the calibration procedure. There are three ways to successfully stop the calibration procedure: set RUN_CAL register bit to 0 if either:
   - CAL_STAT[2:0] = 0x02,
   - CAL_STAT[2:0] = 0x02 and user initiates a stop through a mouse-click event, or,
   - CAL_STAT[2:0] = 0x03.

   If CAL_STAT[2:0] = 0x04, the calibration procedure needs to be re-started.
7. Stop the calibration procedure by ensuring that the RUN_CAL register bit is 0, then wait 1msec before reading the recommended “Raw data Threshold” register value, RPTH[6:0] (lower 7 bits of LiftCutoff_Tune2 register). RPTH[6:0] recommends a raw data threshold value that replaces the default value in the tracking SROM’s Raw_data_Threshold register to improve lift performance. The Raw_ data_Threshold register requires the Tracking SROM*[2] to be loaded.
8. Read the recommended “Min SQUAL Run” register value, RMSQ[7:0] (entire 8 bits of LiftCutoff_Tune3 register). RMSQ[7:0] recommends a Min SQUAL Run value that replaces the default value in the tracking SROM’s Min_SQ_Run register to improve lift performance. The Min_SQ_Run register requires the Tracking SROM*[2] to be downloaded.
9. The Lift cut off calibration procedure is complete.

Note:
**[1] Lift cut off calibration SROM: SROM 0x81 or above (4KB).*
**[2] Tracking SROM: SROM 0x03 or above (4KB).*

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

10.0 Registers Table

PMW3360DM-T2QU registers are accessible via the serial port. The registers are used to read motion data and status as well as to set the device configuration.

Address	Register	Access (R = Read / W = Write or Read/Write= RW)	Default Value
0x00	Product_ID	R	0x42
0x01	Revision_ID	R	0x01
0x02	Motion	RW	0x20
0x03	Delta_X_L	R	0x00
0x04	Delta_X_H	R	0x00
0x05	Delta_Y_L	R	0x00
0x06	Delta_Y_H	R	0x00
0x07	SQUAL	R	0x00
0x08	Raw_Data_Sum	R	0x00
0x09	Maximum_Raw_data	R	0x00
0x0A	Minimum_Raw_data	R	0x00
0x0B	Shutter_Lower	R	0x12
0x0C	Shutter_Upper	R	0x00
0x0D	Control	RW	0x02
0x0F	Config1	RW	0x31
0x10	Config2	RW	0x20
0x11	Angle_Tune	RW	0x00
0x12	Frame_Capture	RW	0x00
0x13	SROM_Enable	W	N/A
0x14	Run_Downshift	RW	0x32
0x15	Rest1_Rate_Lower	RW	0x00
0x16	Rest1_Rate_Upper	RW	0x00
0x17	Rest1_Downshift	RW	0x1F
0x18	Rest2_Rate_Lower	RW	0x63
0x19	Rest2_Rate_Upper	RW	0x00
0x1A	Rest2_Downshift	RW	0xBC
0x1B	Rest3_Rate_Lower	RW	0xF3
0x1C	Rest3_Rate_Upper	RW	0x01
0x24	Observation	RW	0x00
0x25	Data_Out_Lower	R	0x00
0x26	Data_Out_Upper	R	0x00
0x29	Raw_Data_Dump	RW	0x00
0x2A	SROM_ID	R	0x00
0x2B	Min_SQ_Run	RW	0x10
0x2C	Raw_Data_Threshold	RW	0x0A
0x2F	Config5	RW	0x31
0x3A	Power_Up_Reset	W	N/A
0x3B	Shutdown	W	N/A
0x3F	Inverse_Product_ID	R	0xBD
0x41	LiftCutoff_Tune3	RW	0x00
0x42	Angle_Snap	RW	0x00
0x4A	LiftCutoff_Tune1	RW	0x00
0x50	Motion_Burst	RW	0x00
0x58	LiftCutoff_Tune_Timeout	RW	0x27
0x5A	LiftCutoff_Tune_Min_Length	RW	0x09
0x62	SROM_Load_Burst	W	N/A
0x63	Lift_Config	RW	0x02
0x64	Raw_Data_Burst	R	0x00
0x65	LiftCutoff_Tune2	R	0x00

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

11.0 Registers Description

Register: 0x00								
Name: Product_ID								
Bit	7	6	5	4	3	2	1	0
Field	PID_7	PID_6	PID_5	PID_4	PID_3	PID_2	PID_1	PID_0
	Reset Value: 0x42							
Access: R/W	Read Only							
Data Type:	8-bit unsigned integer							
Usage	This value is a unique identification assigned to this model only. The value in this register does not change; it can be used to verify that the serial communications link is functional.							

Register: 0x01								
Name: Revision_ID								
Bit	7	6	5	4	3	2	1	0
Field	RID_7	RID_6	RID_5	RID_4	RID_3	RID_2	RID_1	RID_0
	Reset Value: 0x01							
Access: R/W	Read Only							
Data Type:	8-bit unsigned integer							
Usage	This register contains the current IC revision, the revision of the permanent internal firmware. It is subject to change when new IC versions are released.							

Register: 0x02								
Name: Motion								
Bit	7	6	5	4	3	2	1	0
Field	MOT	Reserved	1	RData_1st	Lift_Stat	OP_MODE_1	OP_MODE_2	FRAME_RData_1st
	Reset Value: 0x20							
Access: R/W	Read/ Write							
Data Type:	8-bit Field							
Usage	This register allows the user to determine if motion has occurred since the last time it was read. The procedure to read the motion registers (Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H) is as follows: 1. Write any value to the Motion register. 2. Read the Motion register. This will freeze the Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H register values. 3. If the MOT bit is set, Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers should be read in the given sequence to get the accumulated motion. Note: if Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers are not read before the motion register is read for the second time, the data in Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H will be lost. 4. To read a new set of motion data (Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H), repeat from Step 2. 5. If any other register was read i.e. any other register besides Motion, Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H, then, to read a new set of motion data, repeat from Step 1 instead.							

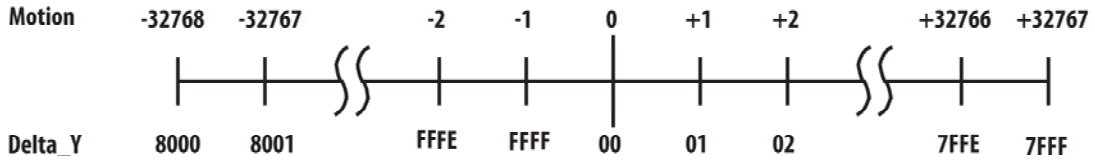
PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Field Name	Description
MOT	Motion since last report or PD **0 = No motion** 1 = Motion occurred, data ready for reading in Delta_X_L, Delta_X_H, Delta_Y_L and Delta_Y_H registers
[6]	Reserved.
[5]	1
RData_1st	This bit is set when the Raw_Data_Grab register is written to or when a complete raw data array has been read, initiating an increment to raw data 0,0. **0 = Raw_Data_Grab data not from raw data 0,0** 1 = Raw_Data_Grab data is from raw data 0,0
Lift_Stat	Indicate the lift status of Chip, **0 = Chip on surface.** 1 = Chip lifted.
OP_Mode[1:0]	**00 – Run mode** 01 – Rest 1 10 – Rest 2 11 – Rest 3
FRAME_RData_1st	This bit is set to indicate first raw data in frame capture. **0 = Frame capture data not from raw data 0,0** 1 = Frame capture data is from raw data 0,0

Register: 0x03								
Name: Delta_X_L								
Bit	7	6	5	4	3	2	1	0
Field	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0
	Reset Value: 0x00							
Access: R/W	Read Only							
Data Type:	16 bits 2's complement number. Lower 8 bits of Delta_X.							
Usage	X movement is counts since last report. Absolute value is determined by resolution. Reading it clears the register.							

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Register: 0x04								
Name: Delta_X_H								
Bit	7	6	5	4	3	2	1	0
Field	X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	X_8
	Reset Value: 0x04							
Access: R/W	Read Only							
Data Type:	16 bits 2's complement number. Lower 8 bits of Delta_X.							
Usage	Delta_X_H must be read after Delta_X_L to have the full motion data. Reading it clears the register.							

Register: 0x05								
Name: Delta_Y_L								
Bit	7	6	5	4	3	2	1	0
Field	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
	Reset Value: 0x00							
Access: R/W	Read Only							
Data Type:	16 bits 2's complement number. Lower 8 bits of Delta_Y.							
Usage	Y movement is counts since last report. Absolute value is determined by resolution. Reading it clears the register. 							

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Register: 0x06								
Name: Delta_Y_H								
Bit	7	6	Bit	7	6	Bit	7	6
Field	Y_{15}	Y_{14}	Y_{13}	Y_{12}	Y_{11}	Y_{10}	Y_9	Y_8
	Reset Value: 0x00							
Access: R/W	Read Only							
Data Type:	16 bits 2's complement number. Upper 8 bits of Delta_Y							
Usage	Delta_Y_H must be read after Delta_Y_L to have the full motion data. Reading it clears the register							

Register: 0x07								
Name: SQUAL								
Bit	7	6	5	4	3	2	1	0
Field	SQ_7	SQ_6	SQ_5	SQ_4	SQ_3	SQ_2	SQ_1	SQ_0
	Reset Value: 0x00							
Access: R/W	Read Only							
Data Type:	8-bit unsigned integer							
Usage	The SQUAL (Surface quality) register is a measure of the number of valid features visible by the chip in the current frame. Use the following formula to find the total number of valid features. Number of Features = SQUAL Register Value * 8 The maximum SQUAL register value is 0x80. Since small changes in the current frame can result in changes in SQUAL, variations in SQUAL when looking at a surface are expected. The graph below shows 883 sequentially acquired SQUAL values, while a chip was moved slowly over white paper. SQUAL values are only valid in run mode. Disable Rest mode before measuring SQUAL.							

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

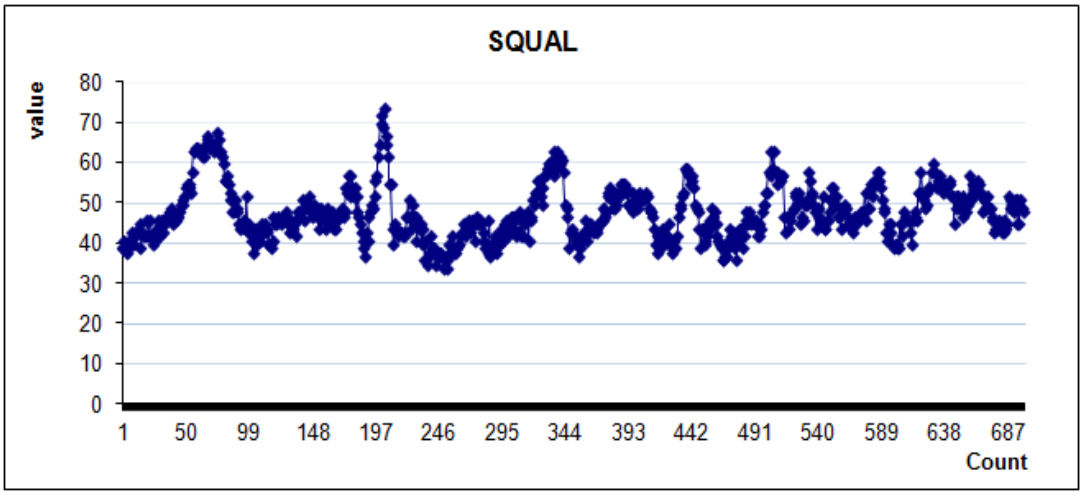


Figure 25. Average SQUAL on white paper

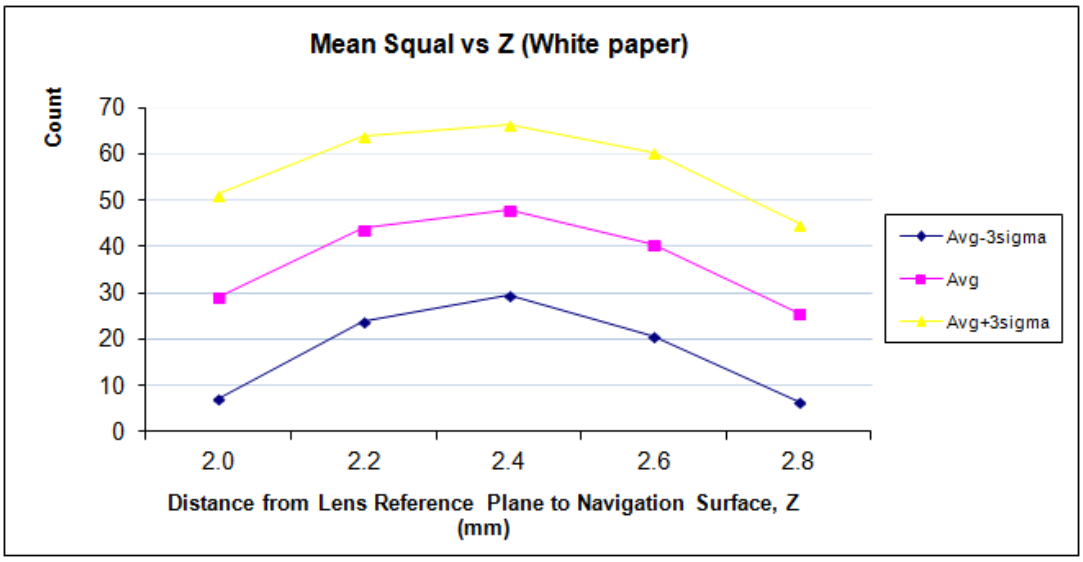


Figure 26. Mean SQUAL vs Z

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Register: 0x08								
Name: Raw_Data_Sum								
Bit	7	6	5	4	3	2	1	0
Field	AP_7	AP_6	AP_5	AP_4	AP_3	AP_2	AP_1	AP_0
	Reset Value: 0x00							
Access: R/W	Read Only							
Data Type:	8-bit unsigned integer							
Usage	This register is used to find the average raw data value. It reports the upper byte of an 18-bit counter which sums all 1296 raw data in the current frame. To find the average raw data values follow the formula below. Average Raw Data = Register Value * 1024 / 1296 The maximum register value is 160(Dec) (0xA0) (127 * 1296 / 1024 truncated to an integer). The minimum register value is 0. The raw data sum value can change every frame							

Register: 0x09								
Name: Maximum_Raw_Data								
Bit	7	6	5	4	3	2	1	0
Field	MRD_7	MRD_6	MRD_5	MRD_4	MRD_3	MRD_2	MRD_1	MRD_0
	Reset Value: 0x00							
Access: R/W	Read Only							
Data Type:	8-bit unsigned integer							
Usage	Maximum Raw data value in current frame. Minimum value = 0, maximum value = 127. The maximum raw data value can change every frame							

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Register: 0x0A								
Name: Minimum_Raw_Data								
Bit	7	6	5	4	3	2	1	0
Field	$MinRD_7$	$MinRD_6$	$MinRD_5$	$MinRD_4$	$MinRD_3$	$MinRD_2$	$MinRD_1$	$MinRD_0$
	Reset Value: 0x00							
Access: R/W	Read Only							
Data Type:	8-bit unsigned integer							
Usage	Minimum Raw data value in current frame. Minimum value = 0, maximum value = 127. The minimum raw data value can change every frame							

Register: 0x0B								
Name: Shutter_Lower								
Bit	7	6	5	4	3	2	1	0
Field	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0
	Reset Value: 0x12							
Access: R/W	Read Only							
Data Type:	16-bit unsigned number							
Usage	Lower byte of the 16bit Shutter register							

Register: 0x0C								
Name: Shutter_Upper								
Bit	7	6	5	4	3	2	1	0
Field	S_{15}	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8
	Reset Value: 0x00							
Access: R/W	Read Only							
Data Type:	16-bit unsigned number							
Usage	Units are clock cycles of the internal oscillator. Read Shutter_Upper first, then Shutter_Lower. They should be read consecutively. The shutter is adjusted to keep the average raw data values within normal operating ranges. The shutter value is checked and automatically adjusted to a new value if needed on every frame when operating in default mode.							

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

<table>
<tr><th colspan="9">Register: 0x0D</th></tr>
<tr><td colspan="9">Name: Control</td></tr>
<tr><td>Bit</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td rowspan="2">Field</td><td>CTRL1$_7$</td><td>CTRL1$_6$</td><td>CTRL1$_5$</td><td>Reserved</td><td>Reserved</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td colspan="8">Reset Value: 0x02</td></tr>
<tr><td>Access: R/W</td><td colspan="8">Read Write</td></tr>
<tr><td>Data Type:</td><td colspan="8">8-bit unsigned integer</td></tr>
<tr><td>Usage</td><td colspan="8">This register defines programmable invert able of XY register scheme.
<table>
<tr><th>Field Name</th><th>Description</th></tr>
<tr><td>CTRL1$_{[7:5]}$</td><td>000 - 0 degree
110 - 90 degree
011 – 180 degree
101 – 270 degree</td></tr>
<tr><td>Reserved$_{[4:0]}$</td><td>Reserved</td></tr>
</table>
Note: For CTRL1$_{[7:5]}$ please use 0 degree for best performance</td></tr>
</table>

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

<table>
<tr><th colspan="9">Register: 0x0F</th></tr>
<tr><td colspan="9">Name: Config1</td></tr>
<tr><td>Bit</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Field</td><td>RES_7</td><td>RES 1_6</td><td>RES_5</td><td>RES_4</td><td>RES_3</td><td>RES_2</td><td>RES_1</td><td>RES_0</td></tr>
<tr><td></td><td colspan="8">Reset Value: 0x31</td></tr>
<tr><td>Access: R/W</td><td colspan="8">Read/ Write</td></tr>
<tr><td>Data Type:</td><td colspan="8">Bit Field</td></tr>
<tr><td>Usage</td><td colspan="8">This register allows the user to change the X & Y or Y only resolution of the chip. Shown below are the bits, their default values, and optional values. The CPI of X & Y or Y only setting in this register depends on the Rpt_Mod register bit (refer to the description for Config2 register).
<table>
<tr><th>Field Name</th><th>Description</th></tr>
<tr><td>RES[7:0]</td><td>Set resolution with CPI step of 100 cpi
0x00: 100 cpi (Minimum cpi)
0x01: 200 cpi
0x02: 300 cpi
:
:
0x31: 5000 cpi (default cpi)
:
:
0x77: 12000 cpi (maximum cpi)</td></tr>
</table></td></tr>
</table>

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Register: 0x10								
Name: Config2								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Rest_En	Reserved	Reserved	Rpt_Mod	Reserved	O
	Reset Value: 0x20							
Access: R/W	Read/ Write							
Data Type:	Bit Field							

Usage

Field Name	Description
[7:6]	Reserved
Rest_En	0 = Normal operation without REST mode. **1 = REST mode enable.**
[4:3]	Reserved
Rpt_Mod	Select the X and Y CPI reporting mode. **= 0: Normal CPI setting affects both delta X and Y.** = 1: CPI setting for delta Y is defined by Config1 (address 0x0F). CPI setting for delta X is defined by Config5 (address 0x2F)
1	Reserved
Bit[0]	Must be set to 0

Register: 0x11								
Name: Angle_Tune								
Bit	7	6	5	4	3	2	1	0
Field	$Angle_7$	$Angle_6$	$Angle_5$	$Angle_4$	$Angle_3$	$Angle_2$	$Angle_1$	$Angle_0$
	Reset Value: 0x00							
Access: R/W	Read/ Write							
Data Type:	Bit Field							

Usage

Field Name	Description
Angle[7:0]	0xE2 -30 degree 0xF6 -10 degree **0x00 0 degree (default)** 0x0F +15 degree 0x1E +30 degree

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Register: 0x12								
Name: Frame_Capture								
Bit	7	6	5	4	3	2	1	0
Field	FC_7	FC_6	FC_5	FC_4	FC_3	FC_2	FC_1	FC_0
	Reset Value: 0x12							
Access: R/W	Read Only							
Data Type:	8-bit unsigned integer							
Usage	Used to capture the next available complete 1 frame of raw data values to be stored to RAM. Writing to this register will cause any firmware loaded to be overwritten and stops navigation. A hardware reset and SROM download are required to restore normal operation for motion reading. Refer to the Frame Capture section for use details.							

Register: 0x13								
Name: SROM_Enable								
Bit	7	6	5	4	3	2	1	0
Field	SE_7	SE_6	SE_5	SE_4	SE_3	SE_2	SE_1	SE_0
	Reset Value: N/A							
Access: R/W	Write Only							
Data Type:	8-bit unsigned integer							
Usage	Write to this register to start either SROM download or SROM CRC test. See SROM Download section for details. SROM CRC test can be performed to check if SROM download was successful. Navigation is halted and the SPI port should not be used during this SROM CRC test. Registers will be reset to default value after completion of CRC test. SROM CRC read procedure is as below: 1. Write 0x15 to SROM_Enable register. 2. Wait for at least 10ms. 3. Read register Data_Out_Upper and register Data_Out_Lower .							

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Register: 0x14								
Name: Run_Downshift								
Bit	7	6	5	4	3	2	1	0
Field	RD_7	RD_6	RD_5	RD_4	RD_3	RD_2	RD_1	RD_0
	Reset Value: 0x32							
Access: R/W	Read/ Write							
Data Type:	8-bit unsigned integer							
Usage	This register set the Run to Rest1 downshift time. Default value is 500ms. Use the formula below for calculation. The minimum register value is 0x01. A value of 0x00 will be internally clipped to 0x01. Run Downshift time (ms) = RD[7:0] x 10 ms Default = 50 x 10 = 500ms Max = 255x10 = 2550ms = 2.55s All the above values are expected to have a +40% and -20% of tolerance.							

Register: 0x15								
Name: Res1_Rate_Lower								
Bit	7	6	5	4	3	2	1	0
Field	$R1R_7$	$R1R_6$	$R1R_5$	$R1R_4$	$R1R_3$	$R1R_2$	$R1R_1$	$R1R_0$
	Reset Value: 0x00							
Access: R/W	Read/Write							
Data Type:	16-bit unsigned integer							
Usage	Lower byte of the Rest1 frame rate register.							

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Register: 0x16								
Name: Rest1_Rate_Upper								
Bit	7	6	5	4	3	2	1	0
Field	$R1R_{15}$	$R1R_{14}$	$R1R_{13}$	$R1R_{12}$	$R1R_{11}$	$R1R_{10}$	$R1R_{9}$	$R1R_{8}$
	Reset Value: 0x00							
Access: R/W	Read/Write							
Data Type:	16-bit unsigned integer							
Usage	Upper byte of the Rest1 frame rate register. This register sets the Rest1 frame rate duration. Default value is 1 ms. To write to the registers, write Lower first, followed by Upper. Register read can be in any order but must be consecutive. R1R[15:0] value must not exceed 0x09B0, otherwise an internal watchdog will trigger a reset. Use the formula below for calculation. Rest1 frame rate duration = (R1R[15:0] + 1) x 1 ms Default = (0 + 1) x 1 = 1 ms All the above values are expected to have a +40% and -20% of tolerance.							

Register: 0x17								
Name: Rest1_Downshift								
Bit	7	6	5	4	3	2	1	0
Field	$R1D_{7}$	$R1D_{6}$	$R1D_{5}$	$R1D_{4}$	$R1D_{3}$	$R1D_{2}$	$R1D_{1}$	$R1D_{0}$
	Reset Value: 0x1F							
Access: R/W	Read/Write							
Data Type:	8-bit unsigned integer							
Usage	This register set the Rest1 to Rest2 downshift time. Default value is 9.92 sec. Use the formula below for calculation. The minimum register value is 0x01. A value of 0x00 will be internally clipped to 0x01. The default multiplier value is defined through SROM. Rest1 Downshift time = R1D[7:0] x 320 x Rest1_Rate. Default = Rest1_Downshift x 320 x Rest1_Rate = 9.92s (default multiplier value is 320) All the above values are expected to have a +40% and -20% of tolerance.							

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Register: 0x18								
Name: Rest2_Rate_Lower								
Bit	7	6	5	4	3	2	1	0
Field	$R2R_7$	$R2R_6$	$R2R_5$	$R2R_4$	$R2R_3$	$R2R_2$	$R2R_1$	$R2R_0$
	Reset Value: 0x63							
Access: R/W	Read/Write							
Data Type:	16-bit unsigned integer							
Usage	Lower byte of the Rest2 frame rate register.							

Register: 0x19								
Name: Rest2_Rate_Upper								
Bit	7	6	5	4	3	2	1	0
Field	$R2R_{15}$	$R2R_{14}$	$R2R_{13}$	$R2R_{12}$	$R2R_{11}$	$R2R_{10}$	$R2R_9$	$R2R_8$
	Reset Value: 0x00							
Access: R/W	Read/Write							
Data Type:	16-bit unsigned integer							
Usage	Upper byte of the Rest2 frame rate register. This register sets the Rest2 frame rate duration. Default value is 100 ms. To write to the registers, write Lower first, followed by Upper. Register read can be in any order but must be consecutive. R2R[15:0] value must not exceed 0x09B0, otherwise an internal watchdog will trigger a reset. Use the formula below for calculation. Rest2 frame rate duration = (R2R[15:0] + 1) x 1 ms Default = (99 + 1) x 1 = 100 ms All the above values are expected to have a +40% and -20% of tolerance.							

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Register: 0x1A								
Name: Rest2_Downshift								
Bit	7	6	5	4	3	2	1	0
Field	$R2D_7$	$R2D_6$	$R2D_5$	$R2D_4$	$R2D_3$	$R2D_2$	$R2D_1$	$R2D_0$
	Reset Value: 0xBC							
Access: R/W	Read/Write							
Data Type:	8-bit unsigned integer							
Usage	This register set the Rest2 to Rest3 downshift time. Default value is 601.6s. Use the formula below for calculation. The minimum register value is 0x01. A value of 0x00 will be internally clipped to 0x01. Rest2 Downshift time = R2D[7:0] x 32 x Rest2_Rate. Default = 188 x 32 x 100 = 601.6s = 10mins All the above values are expected to have a +40% and -20% of tolerance.							

Register: 0x1B								
Name: Rest3_Rate_Lower								
Bit	7	6	5	4	3	2	1	0
Field	$R3R_7$	$R3R_6$	$R3R_5$	$R3R_4$	$R3R_3$	$R3R_2$	$R3R_1$	$R3R_0$
	Reset Value: 0xF3							
Access: R/W	Read/Write							
Data Type:	16-bit unsigned integer							
Usage	Lower byte of the Rest3 frame rate register.							

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Register: 0x1C								
Name: Res3_Rate_Upper								
Bit	7	6	5	4	3	2	1	0
Field	$R3R_{15}$	$R3R_{14}$	$R3R_{13}$	$R3R_{12}$	$R3R_{11}$	$R3R_{10}$	$R3R_{9}$	$R3R_{8}$
	Reset Value: 0x01							
Access: R/W	Read/Write							
Data Type:	16-bit unsigned integer							
Usage	Upper byte of the Rest3 frame rate register. This register sets the Rest3 frame rate duration. Default value is 500 ms. To write to the registers, write Lower first, followed by Upper. Register read can be in any order but must be consecutive. R3R[15:0] value must not exceed 0x09B0, otherwise an internal watchdog will trigger a reset. Use the formula below for calculation. Rest3 frame rate duration = (R3R[15:0] + 1) x 1 ms Default = (499 + 1) x 1 = 500 ms All the above values are expected to have a +40% and -20% of tolerance.							

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Register: 0x24								
Name: Observation								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	OB_6	OB_5	OB_4	OB_3	OB_2	OB_1	OB_0
	Reset Value: 0x00							
Access: R/W	Read/Write							
Data Type:	Bit Field							
Usage	The user must clear the register by writing 0x00, wait for minimum T_{dly_obs} msec, and read the register. The active process will have set their corresponding bit. The register may be used as part of recovery scheme to detect a problem caused by EFT/B or ESD. T_{dly_obs} is defined as the longest frame period + 0.5msec. The longest frame period is Rest3. Clock tolerance need to be taken into account. For e.g. if the default Rest3 rate of 500msec is used, then T_{dly_obs} = (500x1.4) + 0.5 = 700.5msec.							

Field Name	Description
OB6	SROM_RUN: Indicates whether SROM is running. **0 = SROM not running** 1 = SROM running
OB[5:0]	Set once per frame

Register: 0x25								
Name: Data_Out_Lower								
Bit	7	6	5	4	3	2	1	0
Field	DO_7	DO_6	DO_5	DO_4	DO_3	DO_2	DO_1	DO_0
	Reset Value: 0x00							
Access: R/W	Read Only							
Data Type:	16-bit unsigned integer							
Usage	Lower byte of the Data_Out register							

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Register: 0x26								
Name: Data_Out_Upper								
Bit	7	6	5	4	3	2	1	0
Field	DO_{15}	DO_{14}	DO_{13}	DO_{12}	DO_{11}	DO_{10}	DO_9	DO_8
	Reset Value: 0x00							
Access: R/W	Read Only							
Data Type:	16-bit unsigned integer							
Usage	Data in these registers come from the SROM CRC test. The data can be read out in any order. The SROM CRC test is initiated by writing 0x15 to SROM_Enable register.							

CRC Result	Data_Out_Upper	Data_Out_Lower
SROM CRC test	0xBE	0xEF

Register: 0x29								
Name: Raw_Data_Grab								
Bit	7	6	5	4	3	2	1	0
Field	Valid	RD_D_6	RD_D_5	RD_D_4	RD_D_3	RD_D_2	RD_D_1	RD_D_0
	Reset Value: 0x00							
Access: R/W	Read / Write							
Data Type:	8-bit unsigned integer							
Usage	Write any value to this register to initialize the raw data output. Read motion register to check if first raw data is ready, and then read data from this register for the raw data. 1. Write 0 to Bit [5] of register 0x10 (Config2) to disable Rest mode. 2. Write any value to Raw_Data_Grab register to reset the register. 3. Read MOTION register 0x02 & check for Bit [4] for first raw data in raw data grab to be ready. 4. Then continuously reading Raw_Data_Grab register for raw data for 1296 times. Ensure Bit [7] is valid for each raw data read. 5. Write 1 to Bit [5] of register 0x10 (Config2) to enable rest mode if required.							

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Register: 0x2A								
Name: SROM_ID								
Bit	7	6	5	4	3	2	1	0
Field	SR_7	SR_6	SR_5	SR_4	SR_3	SR_2	SR_1	SR_0
	0x00							
Access: R/W	Read Only							
Data Type:	8-bit unsigned integer							
Usage	Contains the revision of the downloaded Shadow ROM (SROM) firmware. If the firmware has been successfully downloaded and the chip is operating out of SROM, this register will contain the SROM firmware revision; otherwise it will contain 0x00.							

Register: 0x2B								
Name: Min_SQ_Run								
Bit	7	6	5	4	3	2	1	0
Field	$MSQR_7$	$MSQR_6$	$MSQR_5$	$MSQR_4$	$MSQR_3$	$MSQR_2$	$MSQR_1$	$MSQR_0$
	Reset Value: 0x10							
Access: R/W	Read/Write							
Data Type:	Bit Field							
Usage	This register defines the minimum Squal threshold below which the chip will produce motion delta values of zero. Typically, the default value of this register should only be modified as a result of Lift cut off calibration SROM. Min_SQ_Run is only available for Tracking SROM and above.							

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Register: 0x2C								
Name: Raw_Data_Threshold								
Bit	7	6	5	4	3	2	1	0
Field	$RDTH_7$	$RDTH_6$	$RDTH_5$	$RDTH_4$	$RDTH_3$	$RDTH_2$	$RDTH_1$	$RDTH_0$
	Reset Value: 0x0A							
Access: R/W	Read/ Write							
Data Type:	Bit Field							
Usage	This register affects the SQUAL value register value. The SQUAL is a measure of the number of valid features. The raw data threshold register defines what is considered a valid feature. A low threshold value will make it easier for a feature to be considered valid. Therefore, a low raw data threshold will increase SQUAL since more features will be considered valid and vice versa. If raw data threshold is set too high, it will invalidate features that are actually trackable, thus making SQUAL too low and degrades tracking. If raw data threshold is set too low, it will validate features that are not trackable. Typically, the default value of this register should only be modified as the result of Lift cut off calibration SROM. Raw_Data_Threshold is only available with tracking SROM.							

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Register: 0x2F								
Name: Config5								
Bit	7	6	5	4	3	2	1	0
Field	$RESX_7$	$RESX_6$	$RESX_5$	$RESX_4$	$RESX_3$	$RESX_2$	$RESX_1$	$RESX_0$
	Reset Value: 0x31							
Access: R/W	Read/ Write							
Data Type:	Bit Field							
Usage	This register allows the user to change the X-axis resolution when the chip is configured to have independent X-axis and Y-axis resolution reporting mode via Rpt_Mod bit = 1 in Config2 register. The setting in this register will be inactive if Rpt_Mod bit = 0.Shown below are the bits, their default values, and optional values.							

Field Name	Description
RESX [7:0]	Set resolution with CPI step of 100 cpi 0x00: 100 cpi (Minimum cpi) 0x01: 200 cpi 0x02: 300 cpi : : **0x31: 5000 cpi (default cpi)** : : 0x77: 12000 cpi (maximum cpi)

Register: 0x3A								
Name: Power_Up_Reset								
Bit	7	6	5	4	3	2	1	0
Field	PUR_7	PUR_6	PUR_5	PUR_4	PUR_3	PUR_2	PUR_1	PUR_0
	Reset Value: N/A							
Access: R/W	Write Only							
Data Type:	8-bit unsigned integer							
Usage	Write 0x5a to this register to reset the chip. All settings will revert to default values. Reset is required after recovering from shutdown mode and to restore normal operation after Frame Capture							

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Register: 0x3B								
Name: Shutdown								
Bit	7	6	5	4	3	2	1	0
Field	SD_7	SD_6	SD_5	SD_4	SD_3	SD_2	SD_1	SD_0
	Reset Value: N/A							
Access: R/W	Write Only							
Data Type:	8-bit unsigned integer							
Usage	Write 0xB6 to set the chip to shutdown mode. Refer to the Shutdown section for more details and on the recovery procedure.							

Register: 0x3F								
Name: Inverse_Product_ID								
Bit	7	6	5	4	3	2	1	0
Field	PID_7	PID_6	PID_5	PID_4	PID_3	PID_2	PID_1	PID_0
	Reset Value: 0xBD							
Access: R/W	Read Only							
Data Type:	Bit Field							
Usage	This value is the inverse of the Product_ID. It is used to test the SPI port hardware							

Register: 0x41								
Name: LiftCuttoff_Tune3								
Bit	7	6	5	4	3	2	1	0
Field	$RMSQ_7$	$RMSQ_6$	$RMSQ_5$	$RMSQ_4$	$RMSQ_3$	$RMSQ_3$	$RMSQ_1$	$RMSQ_0$
	Reset Value: 0x00							
Access: R/W	Read/Write							
Data Type:	Bit Field							
Usage	This register is valid only if the calibration procedure is stopped successfully. RMSQ[7:0] recommends a minimum Squal run value that replaces the default value in the Min_SQ_Run register to improve lift performance. LiftCutoff_Tune3 is only available if Lift cut off calibration SROM is used for Lift cut off calibration.							

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Register: 0x42								
Name: Angle_Snap								
Bit	7	6	5	4	3	2	1	0
Field	AS_EN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	Reset Value: 0x00							
Access: R/W	Read/Write							
Data Type:	Bit Field							
Usage	The AS_EN bit in this register enables or disables the Angle Snap feature. AS_EN = 0 (Angle snap disabled. This is the default value.) AS_EN = 1 (Angle snap enabled with 5° snap setting.)							

Register: 0x4A								
Name: LiftCuttoff_Tune1								
Bit	7	6	5	4	3	2	1	0
Field	RUN_CAL	Reserved	Reserved	Reserved	Reserved	CAL_STAT2	CAL_STAT1	CAL_STAT0
	Reset Value: 0x00							
Access: R/W	Read/Write							
Data Type:	Bit Field							
Usage	This register is used to start either the Shutter Calibration or the SQUAL Calibration Lift cut off calibration procedure. It is also used to check the status of either procedure. Refer to the Lift cut off calibration section for more details.							

Field Name	Description
RUN_CAL	0 = Stop Shutter Calibration procedure (default) 1 = Start Shutter Calibration procedure
Bit [6:3]	Reserved
CAL_STAT[2:0]	0x00 = Reserved 0x01 = Calibration in progress. 0x02 = Calibration successfully completed (minimum length met). Surface data collection continues until timeout. Registers LiftCutoff_Tune_Min_Length and LiftCutoff_Tune_Timeout define the minimum length threshold and timeout respectively. 0x03 = Calibration successfully completed (minimum length met) and timeout has triggered. Surface data collection stops automatically. 0x04 = Calibration unsuccessful (minimum length not met) and timeout has triggered. 0x05 - 0x07 = Reserved

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Register: 0x50								
Name: Motion_Burst								
Bit	7	6	5	4	3	2	1	0
Field	MB_7	MB_6	MB_5	MB_4	MB_3	MB_2	MB_1	MB_0
	Reset Value: 0x00							
Access: R/W	Read/Write							
Data Type:	8-Bit unsigned integer							
Usage	The Motion_Burst register is used for high-speed access of up to 12 register bytes. See the Burst Mode-Motion Read section for full details of operation.							

Register: 0x58								
Name: LiftCuttoff_Tune_Timeout								
Bit	7	6	5	4	3	2	1	0
Field	$RMSQ_7$	$RMSQ_6$	$RMSQ_5$	$RMSQ_4$	$RMSQ_3$	$RMSQ_3$	$RMSQ_1$	$RMSQ_0$
	Reset Value: 0x27							
Access: R/W	Read/Write							
Data Type:	Bit Field							
Usage	This register sets the minimum Lift cut off calibration timeout threshold. Timeout (sec) = (TIMEOUT[7:0] + 1) x 0.5 sec Default = (39 + 1) x 0.5 = 20 sec Allowed TIMEOUT[7:0] range is 0x00 (0.5 sec) to 0xF9 (125 sec). All the above values are expected to have a +40% and -20% of tolerance.							

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Register: 0x5A								
Name: LiftCuttoff_Tune_Min_Length								
Bit	7	6	5	4	3	2	1	0
Field	$MINL_7$	$MINL_6$	$MINL_5$	$MINL_4$	$MINL_3$	$MINL_3$	$MINL_1$	$MINL_0$
	Reset Value: 0x09							
Access: R/W	Read/Write							
Data Type:	Bit Field							
Usage	This register sets the minimum Lift cut off calibration length threshold. Minimum Length (inches) = (MINL[7:0] + 1) x 2 inches Default = (9 + 1) x 2 = 20 inches Allowed MINL [7:0] range is 0x00 (2 inches) to 0xF9 (500 inches). Actual distance is expected to have a tolerance that is strongly dependent on MINL. The tolerance is approximately 40% for MINL = 0x04 (10 inches) and above. It is not recommended to set a MINL that is lower because the tolerance can potentially increase to 100%.							

Register: 0x62								
Name: SROM_Load_Burst								
Bit	7	6	5	4	3	2	1	0
Field	SL_7	SL_6	SL_5	SL_4	SL_3	SL_2	SL_1	SL_0
	Reset Value: N/A							
Access: R/W	Write Only							
Data Type:	8-Bit unsigned integer							
Usage	The SROM_Load_Burst register is used for high-speed programming SROM from an external PROM or microcontroller. See the SROM Download section for use details.							

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Register: 0x63								
Name: Lift_Config								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LIFC1	LIFC0
	Reset Value: 0X02							
Access: R/W	Read/Write							
Data Type:	Bit Field							
Usage	This register defines the lift detection height threshold. The lift status bit is asserted when the chip is above the threshold. LIFC[1:0] — Description 00 — Reserved 10 — Lift detection height = nominal height + 2 mm (default value). 11 — Lift detection height = nominal height + 3 mm.							

Register: 0x64								
Name: Raw_Data_Burst								
Bit	7	6	5	4	3	2	1	0
Field	RDB_7	RDB_6	RDB_5	RDB_4	RDB_3	RDB_2	RDB_1	RDB_0
	Reset Value: 0X00							
Access: R/W	Read Only							
Data Type:	8-Bit unsigned integer							
Usage	The Raw_Data_Burst register is used for high-speed access to all the raw data values for one complete frame capture, without having to write to the register address to obtain each raw data. The data pointer is automatically incremented after each read so all 1296 raw data values may be obtained by reading this register 1296 times. See the Frame Capture section for details. **Note**: Maximum raw data value is 127. PB7 is always zero.							

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

Register: 0x65								
Name: LiftCuttoff_Tune2								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	$RPTH_6$	$RPTH_5$	$RPTH_4$	$RPTH_3$	$RPTH_3$	$RPTH_1$	$RPTH_0$
	Reset Value:0x00							
Access: R/W	Read Only							
Data Type:	Bit Field							
Usage	This register provides Lift cut off calibration related readout registers. See the Lift cut off calibration section for more details. Field Name: RPTH[6:0] Description: These bits are valid only if calibration procedure is stopped successfully. RPTH[6:0] recommends a raw data threshold value that replaces the default value in the Raw_Data_Threshold register to improve lift performance.							

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms

12.0 Document Revision History

Revision Number	Date	Description
1.00	19 Aug 2014	- Initial creation
1.10	26 Nov 2015	- pg8 update Fig6 Lens Outline Drawing - pg10 update Fig8 Recommended Base Plate Opening - pg28 add item #3 Delay for 30mis
1.20	25 Feb 2016	- pg23 add point #8 Write 0x00 to Config2 register for wired mouse or 0x20 for wireless mouse design
1.30	6 Apr 2016	- pg47 add Register 0x29 Pix_Grab information
1.40	3 Aug 2016	- pg55 modify Register 0x63 Lift_Config register information. Removed setting 0x00
1.50	26 Sep 2016	- Update document. Change “sensor” to “chip”& “pixel” to “raw data” - Change PixArt RoH Logo - Change Image Array to Picture Element Array

PixArt Imaging Inc. All rights reserved. Any portion in this paper shall not be reproduced, copied, or transformed to any other forms