UNIVERSITY OF TEHRAN

Electrical and Computer Engineering Department

Digital Logic Design, ECE 367 / Digital Systems I, ECE 894

Fall 1402

Homework 9

Counters and Registers

Name:	**Date:**
Username:	

1. Show how a JK flip-flop can be built using a D flip-flop.

2. Write Verilog code for an n-bit shift register with right-shift and load control inputs. Provide an asynchronous reset input.

3. A) Write Verilog code for a T flip-flop with active low clock enable and a T input. Use Verilog always statement. B) Using Verilog **generate** statement, write Verilog code for an 8-bit asynchronous counter that is made of 8 flip-flops of Part A. C) Using flip-flop of Part A and and AND gate, write a Verilog module for a slice that can be used for a synchronous binary counter. D) Using Verilog **generate** statement, write Verilog code for an 8-bit synchronous counter that is made of 8 modules of Part C.

4. Draw the circuit represented by the code shown below. What is its count sequence?

```
module myCounter (input [2:0]R, input L, input Clock, output reg [2:0] Q)
  always @ (posedge Clock)
    if (L)
      Q <= R;
    else
      Q <= {~Q[0], Q[0]^Q[2], Q[1]};
endmodule
```

5. For the following circuit, show Verilog code and write the serial output and the register contents after 9 clock cycles with *Si* having 10010101 (right most bit first).