UNIVERSITY OF TEHRAN

Electrical and Computer Engineering Department

Digital Logic Design, ECE 367 / Digital Systems I, ECE 894

Fall 1402

Homework 5, 6

Logic Synthesis, Basic RTL Combinational Parts

Name:	**Date:**
Username:	

1. A 2's complement circuit can be described in SystemVerilog using ~ (complement) and the + (add) operators, i.e., **assign** compA = ~A + 1'b1. Alternatively, you can build a 2's complementor circuit using iterative logic.
   a. Using an **assign** statement write a SystemVerilog description for an 8-bit 2's complement circuit and synthesize it to standard logic gates library using Yosys.
   b. Using iterative logic, design an 8-bit 2's complement circuit.
   c. Compare gates used in Part a and Part b of this problem.

2. In this problem, you are to synthesize an adder using Yosys.
   a. Write a Verilog description of a full-adder using the following assignment:
      ```
      assign {co,sum} = a+b+ci;
      ```
      Using Yosys and using the library provided to you for the synthesis target, synthesize your Verilog description to a netlist of the library components.
   b. Take the netlist output of Yosys and show its corresponding circuit diagram. Show that the output circuit is indeed functions as a full-adder.
   c. Write a description for a 4-bit adder in Verilog. Synthesize this description using Yosys. Write the number of cells and gates used as the result of synthesis. Compare these with the same numbers reposted for the full-adder of Part b.
   d. Based on Part c, you should be able to know the structure used for the implementation of the 4-bit adder. Show a block diagram of the synthesized circuit.

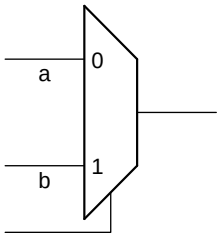
3. Function *f (a,b,c,d)* shown below is a four-variable function.
   a. Using QM tabular minimization method, show the complete list of Prime Implicants of this function in the cubical form.
   b. Show the complete list of Essential Prime Implicants in the cubical form.
   c. Show the minimal two-level logic realization of this function in Boolean form. Show all alternatives if the implementation of the function if it is not unique.

$$f(a,b,c,d) = \sum_m (2, 3, 4, 6, 7, 8, 9, 12, 13)$$

4. Show SystemVerilog description for a 3-to-8 binary decoder with active high outputs, and an active low enable input (EN). Use nesting of SystemVerilog condition operator, i.e., ?:.

5. Implement function shown with as few 2-to-1 multiplexers as possible.

$$f(a, b, c, d) = \Sigma_m(0, 2, 3, 4, 5, 6, 8, 9, 13, 14), d(5, 11, 14)$$



6. Using multiplexers for random logic realization.
    a. Write SystemVerilog code for a 4-to-1 multiplexer with an active high and an active low enable input.
    b. Use the module of Part a and as few extra gates as possible, to create a module for a 16-to-1 multiplexer.
    c. In a SystemVerilog module, use the module of Part b to implement the 5-variable function given below.

$$f\,(a, b, c, d, e) = \Sigma_m(1, 2, 3, 5, 6, 8, 9, 14, 15, 17, 18, 21, 22, 24, 27, 28, 30, 31)$$

7. Show the design of a cascadable comparator. The final outputs are to come from the most-significant bits of the comparator.
    a. Show a two-level logic circuit for each of the outputs of this circuit.
    b. Given 5NS delay for a two-input gate and adding 2NS for an additional input, find the worst-case delay of this circuit.
    c. Write SystemVerilog code for a 1-bit magnitude comparator with *a, b, l, e, g* inputs and *lt, eq*, and *gt* outputs.
    d. In a SystemVerilog module wire eight of comparators of Part a to build an 8-bit comparator. Assign constants to the right-most *l, e*, and *g* inputs as appropriate.

8. Show the design of a 2-bit cascadable comparator. The final outputs are to come from the most-significant bits of the comparator.
    a. Show a two-level logic circuit for each of the outputs of this circuit.
    b. Given 5NS delay for a two-input gate and adding 2NS for an additional input, find the worst-case delay of this circuit.
    c. Write SystemVerilog code for a 1-bit magnitude comparator with *a, b, l, e, g* inputs and *lt, eq*, and *gt* outputs.
    d. In a SystemVerilog module wire eight of comparators of Part a to build an 8-bit comparator. Assign constants to the right-most *l, e*, and *g* inputs as appropriate.

9. A circuit is to be designed to generate the value of the position of the most-significant bit of its 8-bit input that has a 1 value. For example if the input *A* is 00101101, the output *N* becomes 5. The design of this circuit consists of a part that first identifies the bit position and then it encodes it into a binary number (this was a hint). Make this circuit by cascading smaller modules.
    a. Show gate level schematic of a slice.
    b. Show how eight of these slices are cascaded to generate the 3-bit *N* bit position for its 8-bit *A* input.
    c. Given 5 NS for a two-input gate structure, find the worst-case delay of the circuit of Part B.