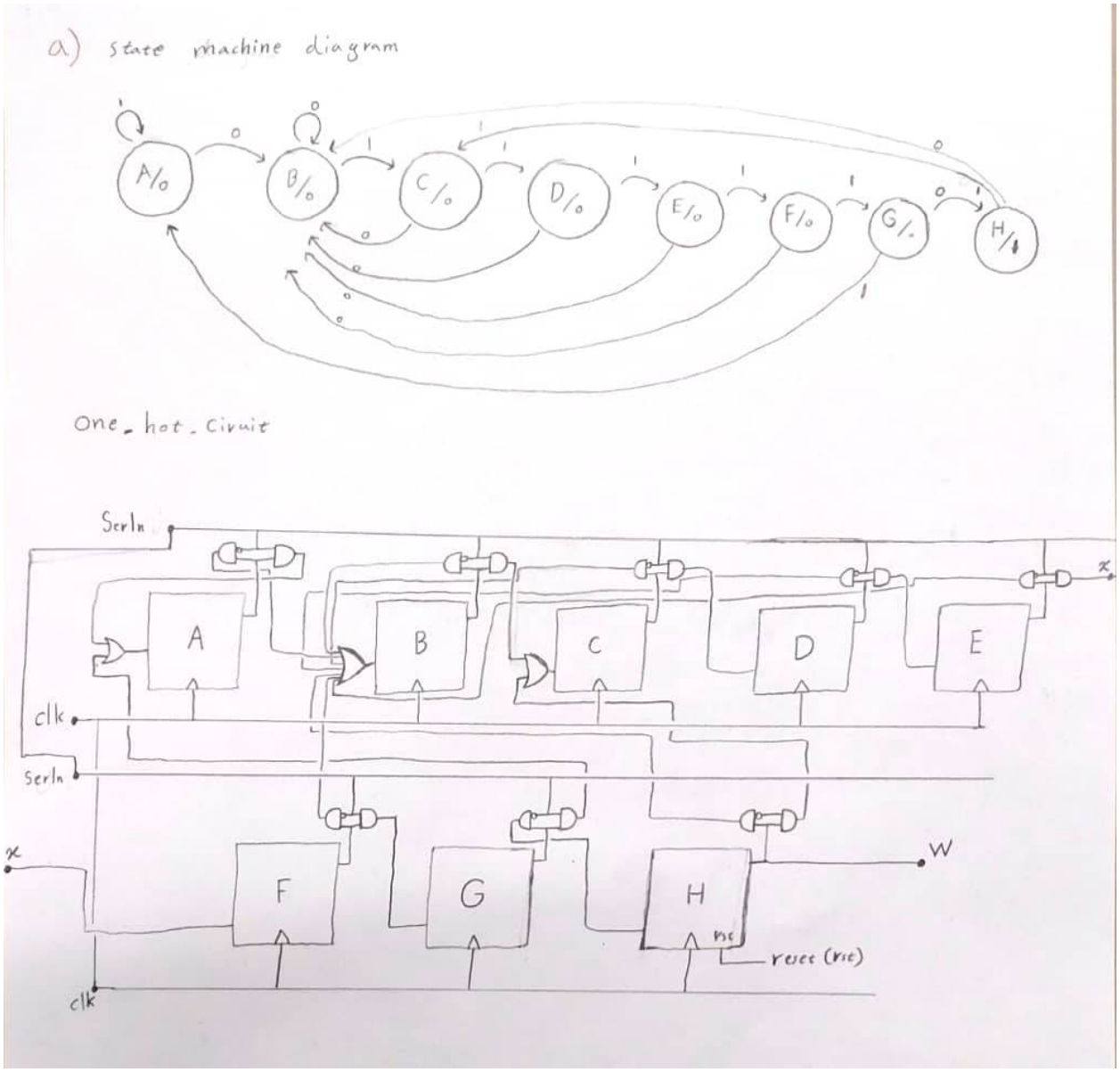
Q_a:

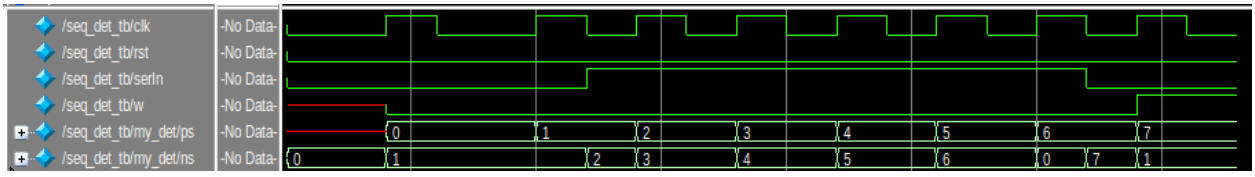
i)


a) state machine diagram
A/0
B/0
C/0
D/0
E/0
F/0
G/0
H/1
one_hot_circuit
SerIn
A
B
C
D
E
x
clk
SerIn
x
F
G
H
W
rst
reset (rst)
clk

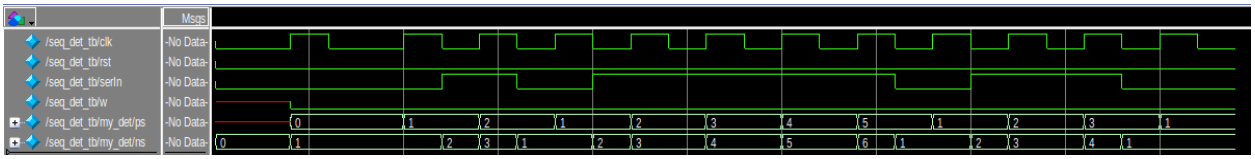
Here is sequence_detector verilog description.

```
module seq_det (input clk, rst, serIn, output w);
   logic [2:0] ps,ns;
   parameter [2:0] A = 3'd0, B = 3'd1, C = 3'd2, D = 3'd3, E = 3'd4, F =
3'd5, G = 3'd6, H = 3'd7;

   always @(ps, serIn) begin
       ns = A;
       case (ps)
           A: ns = serIn ? A : B;
           B: ns = serIn ? C : B;
           C: ns = serIn ? D : B;
           D: ns = serIn ? E : B;
           E: ns = serIn ? F : B;
           F: ns = serIn ? G : B;
           G: ns = serIn ? A : H;
           H: ns = serIn ? C : B;
           default: ns = A;
       endcase

   end

   assign w = (ps == H) ? 1'b1 : 1'b0;

   always @(posedge clk, posedge rst) begin
       if (rst)
           ps <= A;
       else
           ps <= ns;
   end

endmodule
```

Waveform transitions directly to the H state, resulting in the output.



Another waveform when Some state transitions result in the previous states.

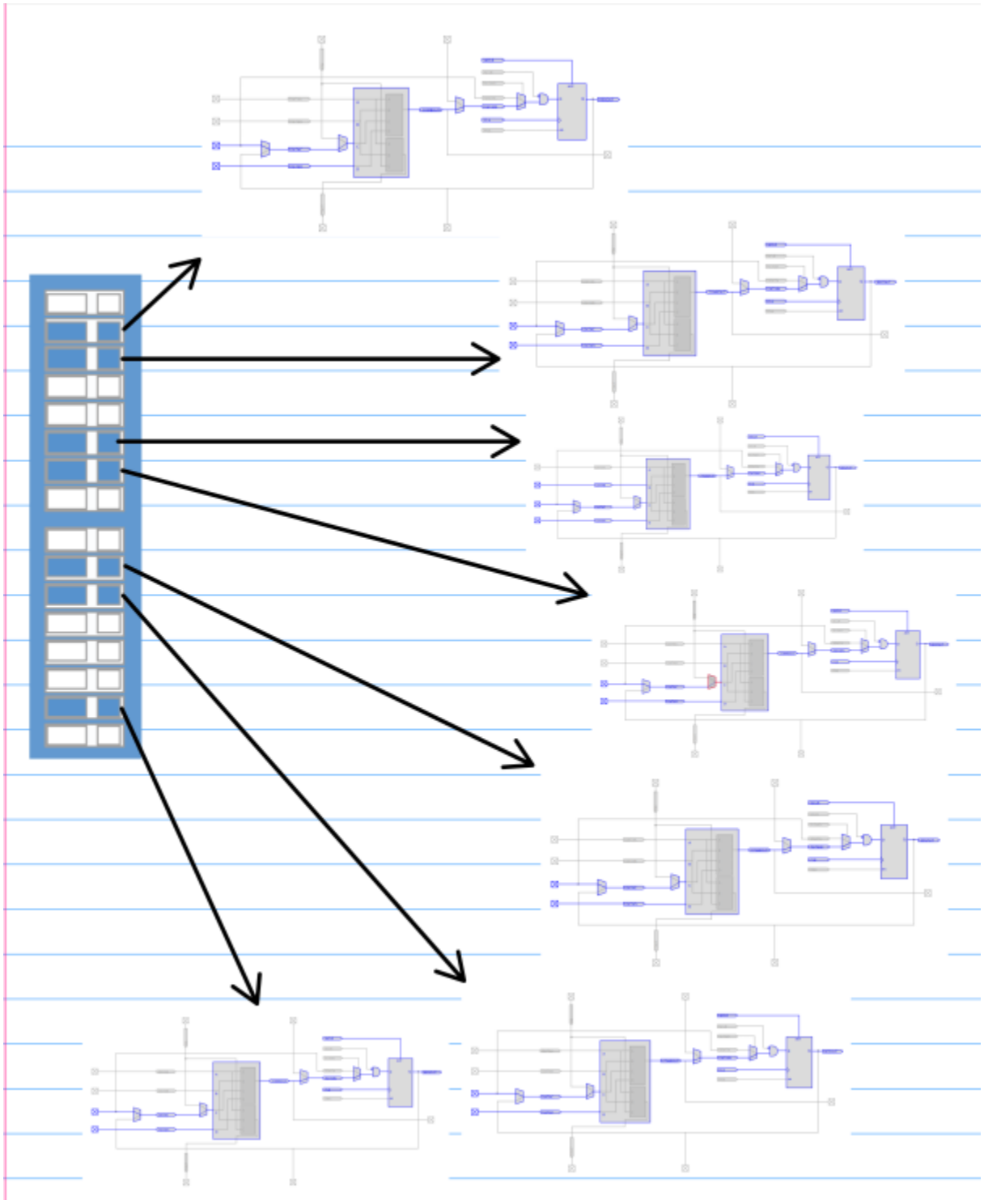


ii)

We imported our code into the quartez and compiled it.

Fitter Status	Successful - Mon Jan 1 14:54:29 2024
Quartus Prime Version	23.1std.0 Build 991 11/28/2023 SC Lite Edition
Revision Name	seq_det
Top-level Entity Name	seq_det
Family	Cyclone IV GX
Device	EP4CGX15BF14A7
Timing Models	Final
Total logic elements	7 / 14,400 (< 1 %)
Total registers	7
Total pins	4 / 81 (5 %)
Total virtual pins	0
Total memory bits	0 / 552,960 (0 %)
Embedded Multiplier 9-bit elements	0
Total GXB Receiver Channel PCS	0 / 2 (0 %)
Total GXB Receiver Channel PMA	0 / 2 (0 %)
Total GXB Transmitter Channel PCS	0 / 2 (0 %)
Total GXB Transmitter Channel PMA	0 / 2 (0 %)
Total PLLs	0 / 3 (0 %)

Floor plan



Minimum and maximum temperature

Timing at 125C:

Slow 1200mV 125C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	934.58 MHz	250.0 MHz	clk	limit due to minimum period restriction (max I/O toggle rate)

T_hold & T_setup in this tempreture:

Slow 1200mV 125C Model Setup Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	clk	-0.070	-0.070

Slow 1200mV 125C Model Hold Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	clk	0.439	0.000

At -40C:

Slow 1200mV -40C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	1103.75 MHz	250.0 MHz	clk	limit due to minimum period restriction (max I/O toggle rate)

T_hold & T_setup in this tempreture:

Slow 1200mV -40C Model Setup Summary

<<Filter>>

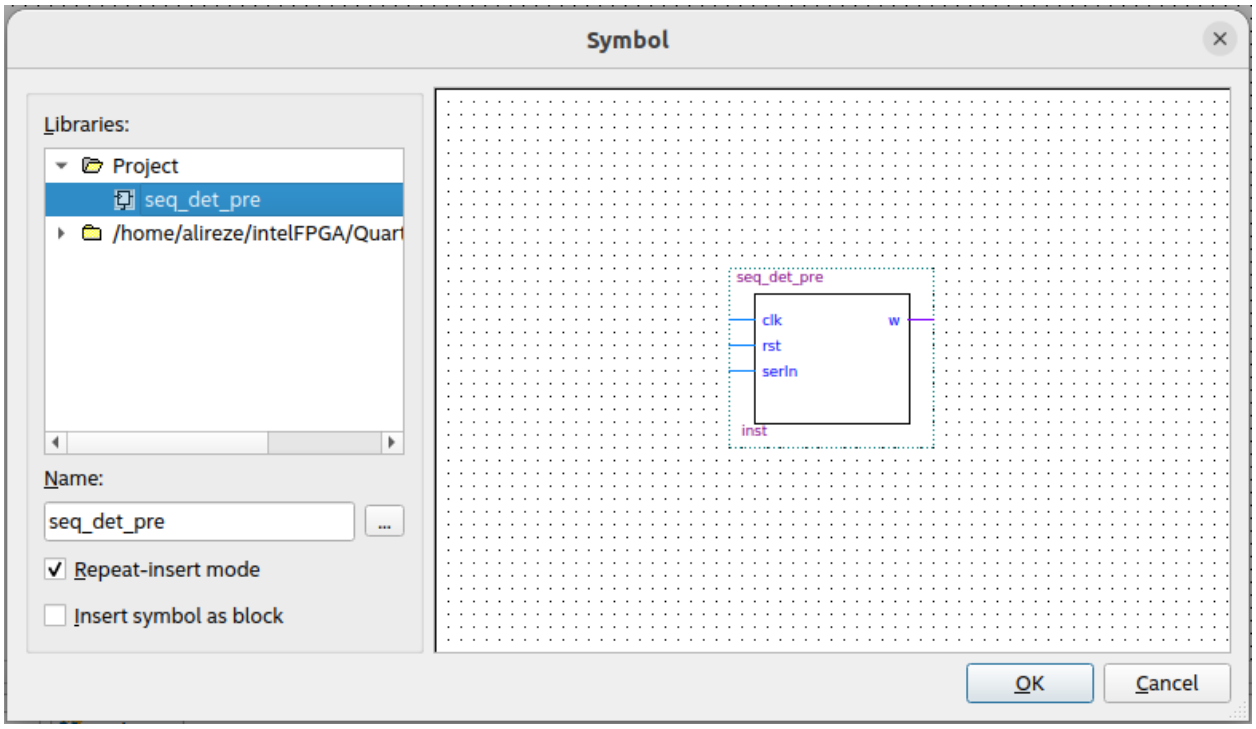
	Clock	Slack	End Point TNS
1	clk	0.094	0.000

Slow 1200mV -40C Model Hold Summary

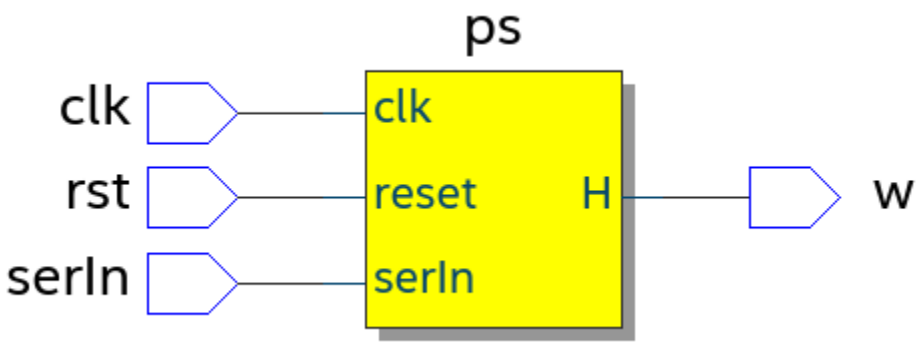
<<Filter>>

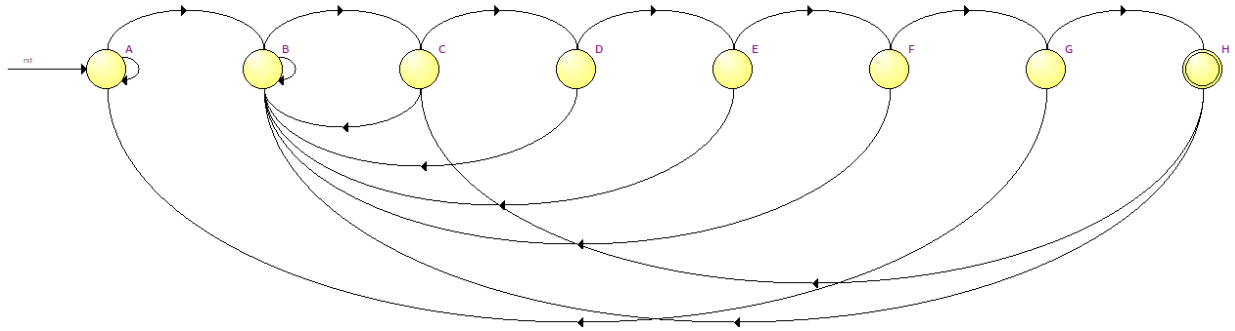
	Clock	Slack	End Point TNS
1	clk	0.378	0.000

Symbol



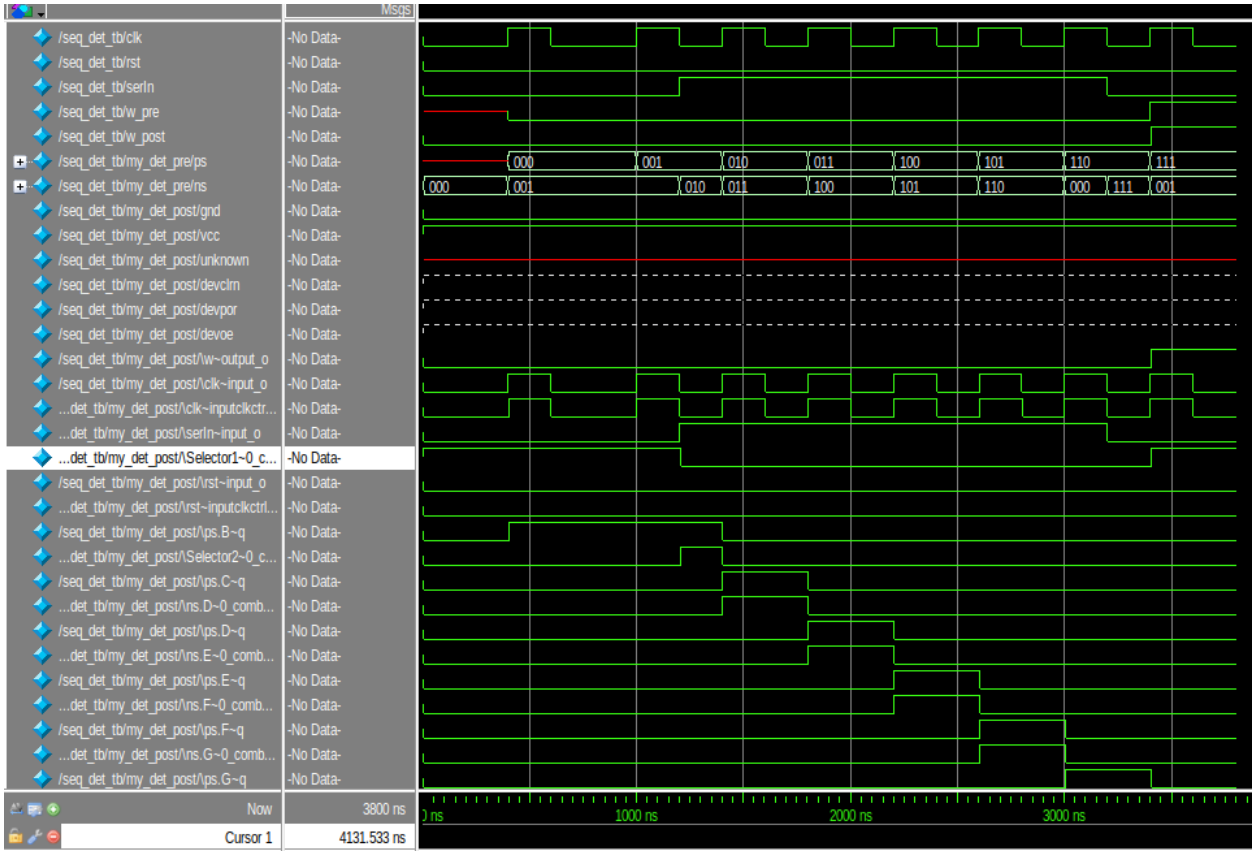
Rtl view



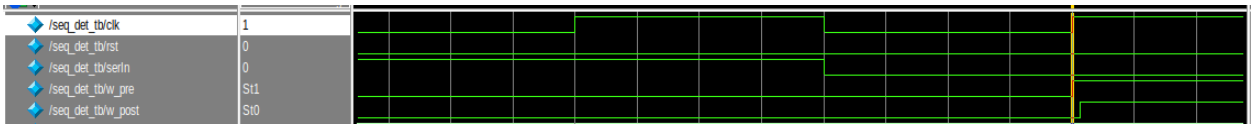


	Name	H	G	F	E	D	C	B	A
1	A	0	0	0	0	0	0	0	0
2	B	0	0	0	0	0	0	1	1
3	C	0	0	0	0	0	1	0	1
4	D	0	0	0	0	1	0	0	1
5	E	0	0	0	1	0	0	0	1
6	F	0	0	1	0	0	0	0	1
7	G	0	1	0	0	0	0	0	1
8	H	1	0	0	0	0	0	0	1

iii)



If we zoom on the output transition, we can see the delay of the post_synthesized_module:



Which is 6.608 ns after the clk posedge.

Q_B)

i)

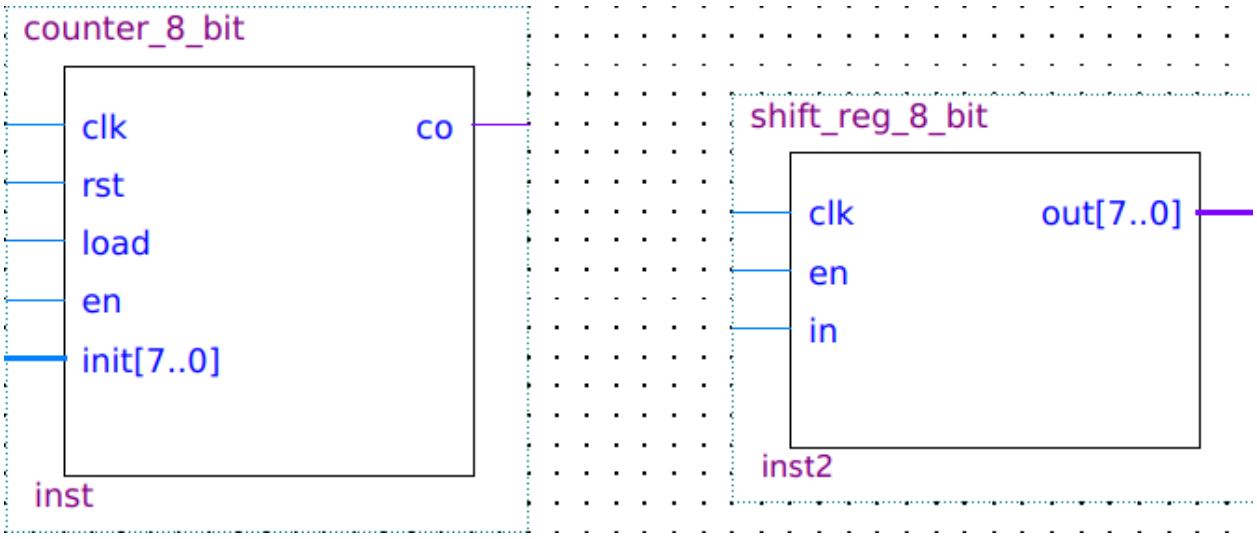
Counter and register

verolig

We are using them for all parts of the project.

```
module counter_8_bit (input clk, rst, load, en, input [7:0] init, output
co);

   logic [7:0] count_num;

   always @(posedge clk, posedge rst) begin
       if (rst)
           count_num = 8'b0;
       else if (load)
           count_num = init;
       else if (en)
           count_num <= count_num - 1;
   end

   assign co = (en && (|count_num == 0)) ? 1'b1 : 1'b0;

endmodule

module shift_reg_8_bit (input clk, en, in, output logic [7:0] out);
   always @(posedge clk) begin
       if (en)
           out = {in, out[7:1]};
   end
endmodule
```

Symbol

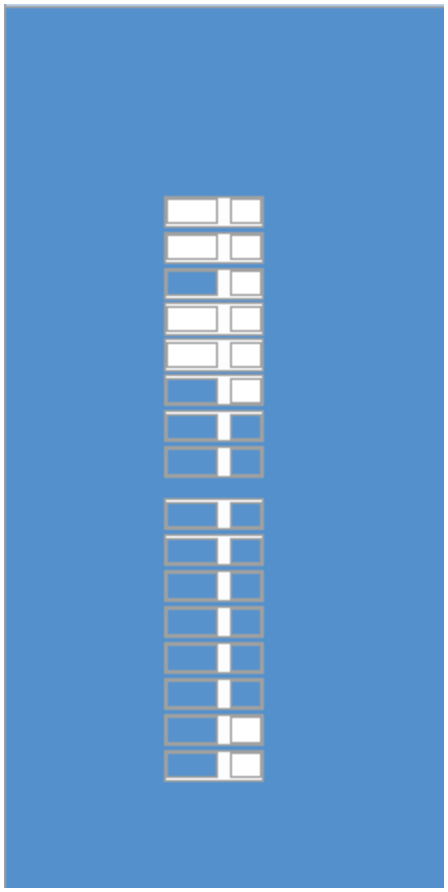


Synthesized counter

Flow Summary

<<Filter>>

Flow Status	Successful - Tue Jan 2 17:12:37 2024
Quartus Prime Version	23.1std.0 Build 991 11/28/2023 SC Lite Edition
Revision Name	part_b
Top-level Entity Name	counter_8_bit
Family	Cyclone IV GX
Device	EP4CGX15BF14A7
Timing Models	Final
Total logic elements	12 / 14,400 (< 1 %)
Total registers	8
Total pins	13 / 81 (16 %)
Total virtual pins	0
Total memory bits	0 / 552,960 (0 %)
Embedded Multiplier 9-bit elements	0
Total GXB Receiver Channel PCS	0 / 2 (0 %)
Total GXB Receiver Channel PMA	0 / 2 (0 %)
Total GXB Transmitter Channel PCS	0 / 2 (0 %)
Total GXB Transmitter Channel PMA	0 / 2 (0 %)
Total PLLs	0 / 3 (0 %)



Minimum and maximum temperature

125C:

Slow 1200mV 125C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	492.85 MHz	250.0 MHz	clk	limit due to minimum period restriction (max I/O toggle rate)

Slow 1200mV 125C Model Setup Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	clk	-1.029	-6.398

Slow 1200mV 125C Model Hold Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	clk	0.599	0.000

-40:

Slow 1200mV -40C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	583.43 MHz	250.0 MHz	clk	limit due to minimum period restriction (max I/O toggle rate)

Slow 1200mV -40C Model Setup Summary

<<Filter>>

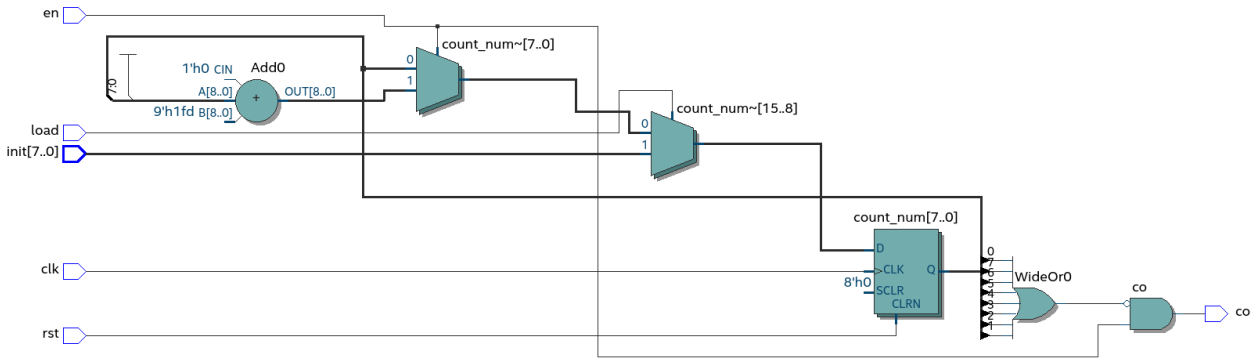
	Clock	Slack	End Point TNS
1	clk	-0.714	-4.100

Slow 1200mV -40C Model Hold Summary

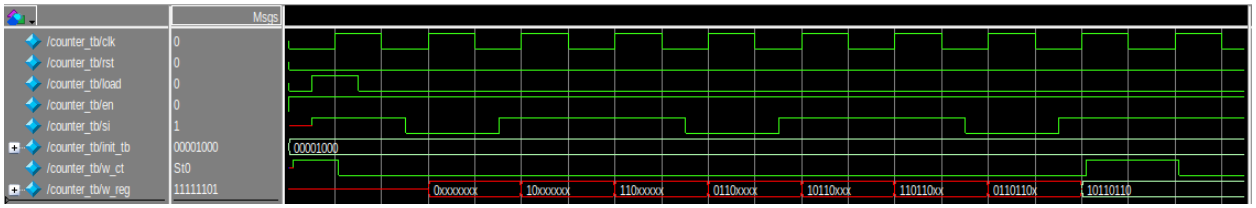
<<Filter>>

	Clock	Slack	End Point TNS
1	clk	0.515	0.000

Rtl view:



Simulation:

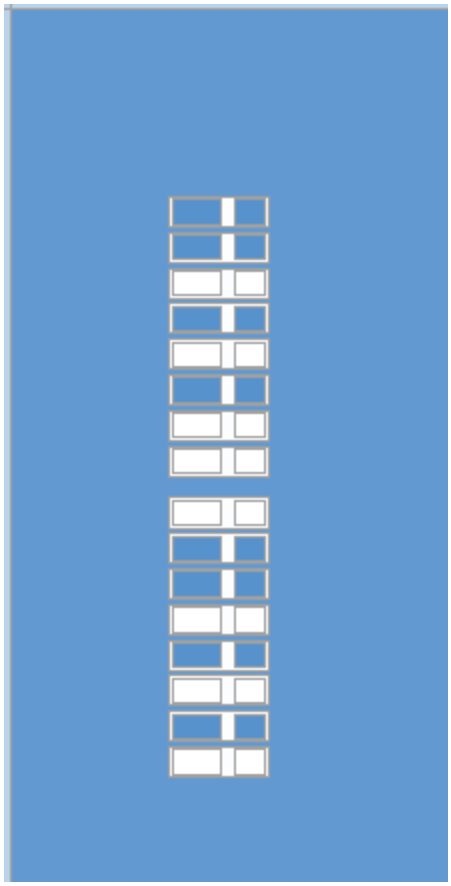


Synthesized shift register

Flow Summary

<<Filter>>

Flow Status	Successful - Tue Jan 2 17:54:56 2024
Quartus Prime Version	23.1std.0 Build 991 11/28/2023 SC Lite Edition
Revision Name	part_b
Top-level Entity Name	shift_reg_8_bit
Family	Cyclone IV GX
Device	EP4CGX15BF14A7
Timing Models	Final
Total logic elements	8 / 14,400 (< 1 %)
Total registers	8
Total pins	11 / 81 (14 %)
Total virtual pins	0
Total memory bits	0 / 552,960 (0 %)
Embedded Multiplier 9-bit elements	0
Total GXB Receiver Channel PCS	0 / 2 (0 %)
Total GXB Receiver Channel PMA	0 / 2 (0 %)
Total GXB Transmitter Channel PCS	0 / 2 (0 %)
Total GXB Transmitter Channel PMA	0 / 2 (0 %)
Total PLLs	0 / 3 (0 %)



Minimum and maximum temperature:

125C:

Slow 1200mV 125C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	1100.11 MHz	250.0 MHz	clk	limit due to minimum period restriction (max I/O toggle rate)

Slow 1200mV 125C Model Setup Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	clk	0.091	0.000

Slow 1200mV 125C Model Hold Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	clk	0.461	0.000

-40:

Slow 1200mV -40C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	1307.19 MHz	250.0 MHz	clk	limit due to minimum period restriction (max I/O toggle rate)

Slow 1200mV -40C Model Setup Summary

<<Filter>>

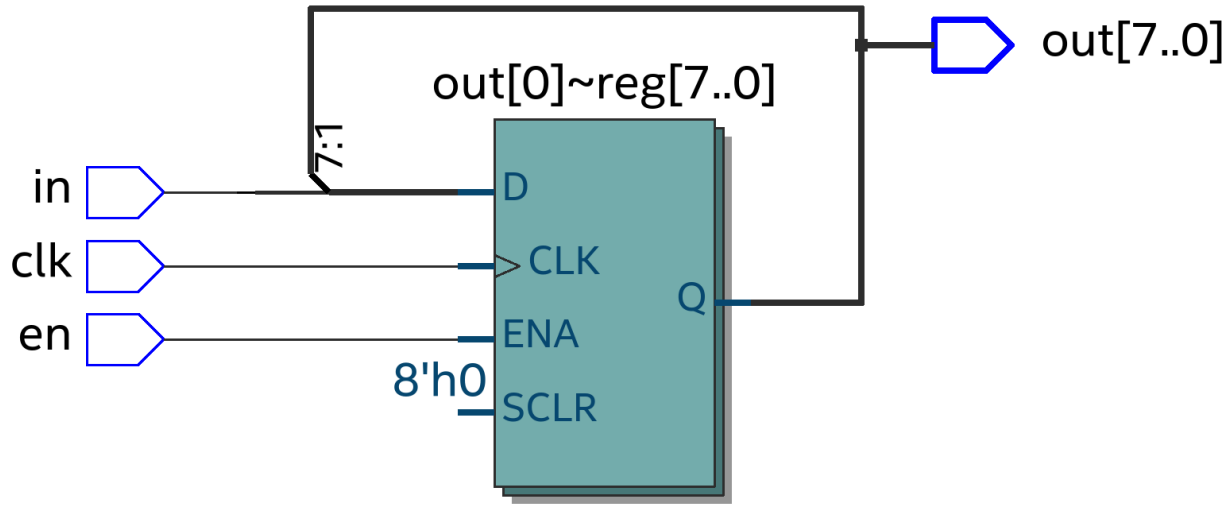
	Clock	Slack	End Point TNS
1	clk	0.235	0.000

Slow 1200mV -40C Model Hold Summary

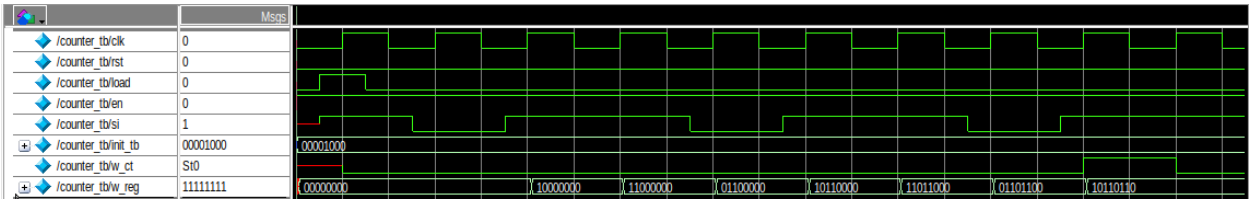
<<Filter>>

	Clock	Slack	End Point TNS
1	clk	0.408	0.000

Rtl view:



Simulation:



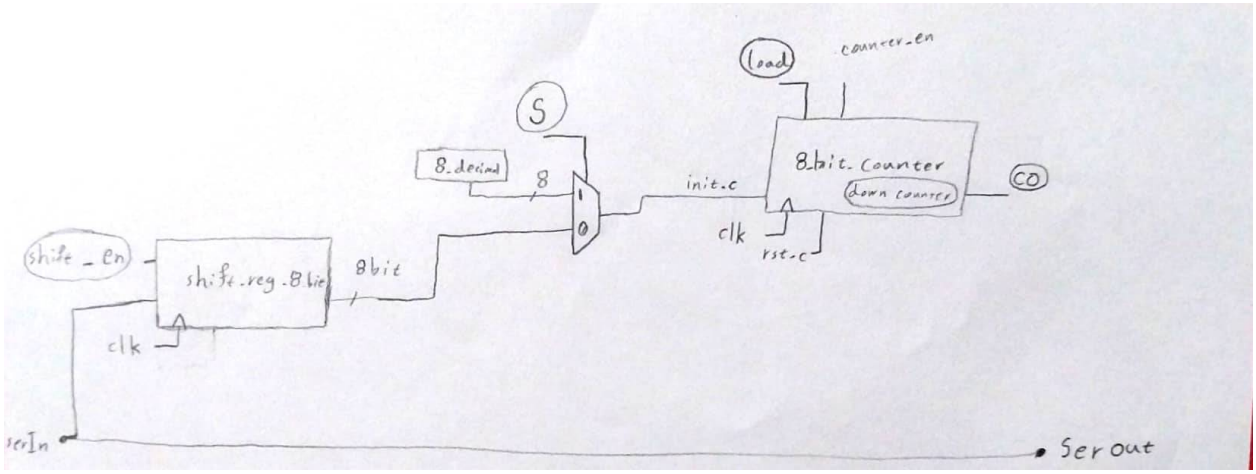
Q_C)

Design:

The whole idea of our project is based on this:

WHAT??:

This part of our design will answer this question, WHAT?.



In our project we had 2 parts that we needed counters, one for counting 8 and another one for counting nt, which we combined them together.

Verilog:

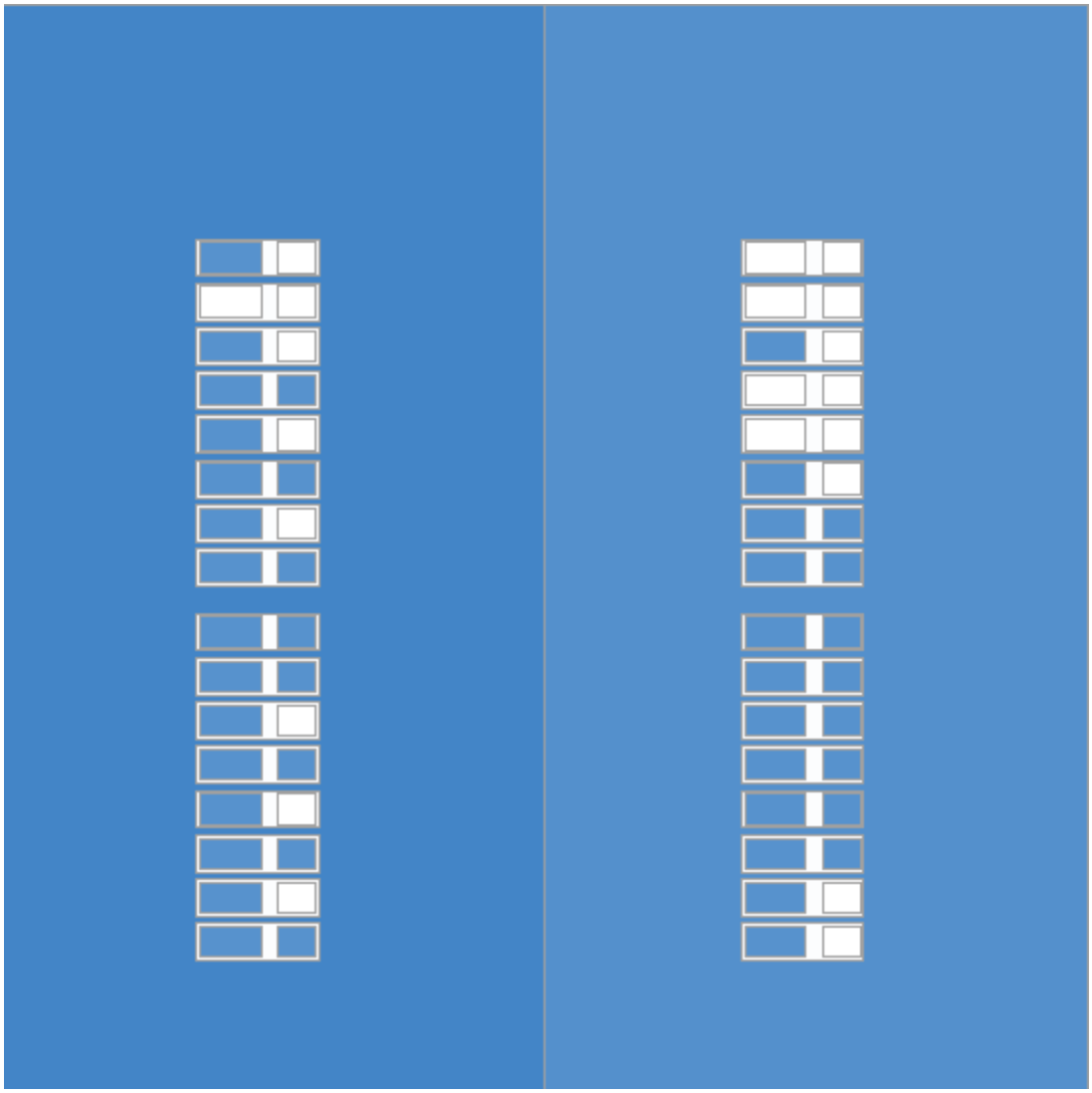
```
module combin_test (input clk, rst, serIn, shift_en, counter_en, load, S,
output co, serOut, serOutValid);
   wire [7:0] init_c, outShifter;

   counter_8_bit mycounter (clk, rst, load, counter_en, init_c, co);
   pre_shift_reg_8_bit myshifter (clk, shift_en, serIn, outShifter);

   assign init_c = S ? 8'd8 : outShifter;
   assign serOut = serIn;

endmodule
```

Syntheized:

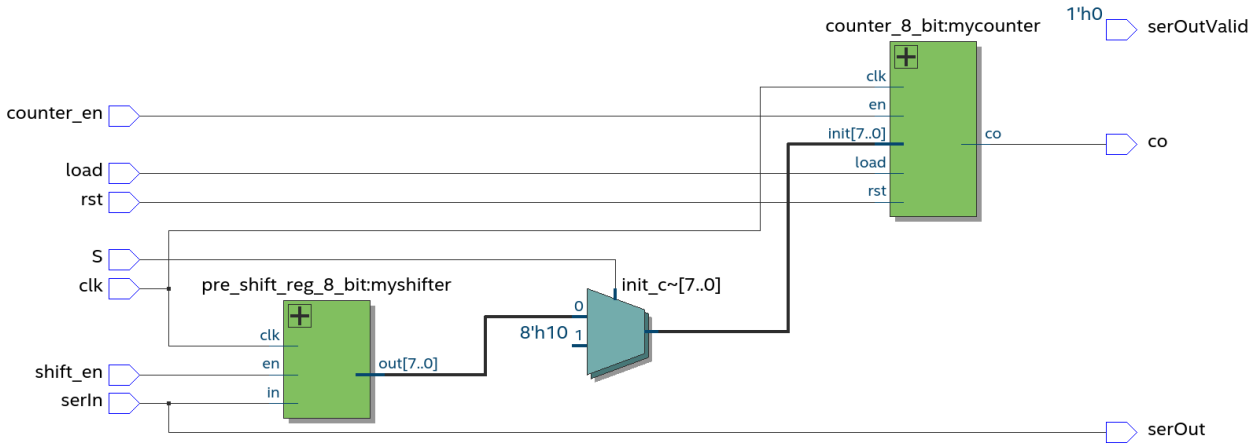
Flow Summary

<<Filter>>

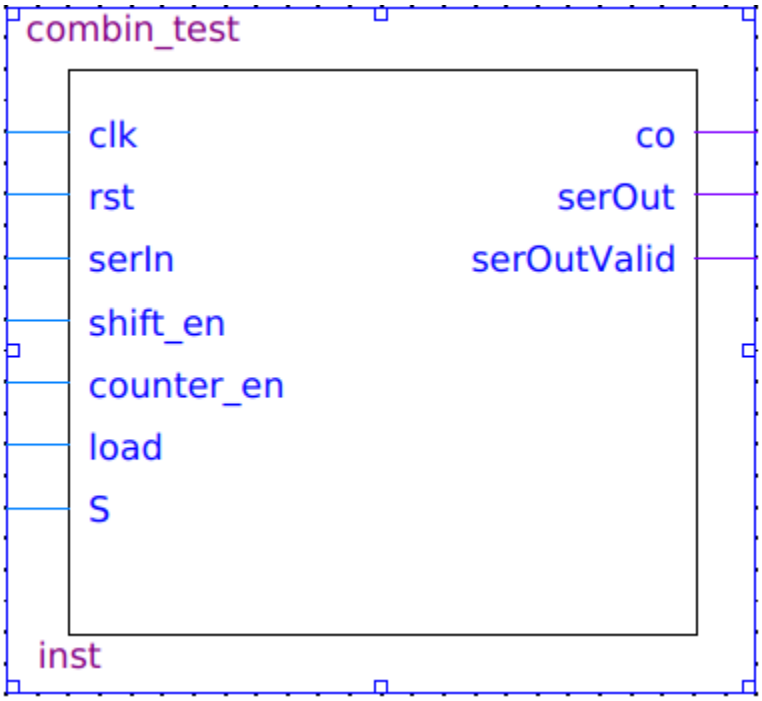
Flow Status	Successful - Wed Jan 3 06:29:24 2024
Quartus Prime Version	23.1std.0 Build 991 11/28/2023 SC Lite Edition
Revision Name	combin
Top-level Entity Name	combin_test
Family	Cyclone IV GX
Device	EP4CGX15BF14A7
Timing Models	Final
Total logic elements	27 / 14,400 (< 1 %)
Total registers	16
Total pins	10 / 81 (12 %)
Total virtual pins	0
Total memory bits	0 / 552,960 (0 %)
Embedded Multiplier 9-bit elements	0
Total GXB Receiver Channel PCS	0 / 2 (0 %)
Total GXB Receiver Channel PMA	0 / 2 (0 %)
Total GXB Transmitter Channel PCS	0 / 2 (0 %)
Total GXB Transmitter Channel PMA	0 / 2 (0 %)
Total PLLs	0 / 3 (0 %)



Rtl view:


counter_8_bit:mycounter
1'h0
serOutValid
clk
en
init[7..0]
co
load
rst
counter_en
load
rst
S
clk
pre_shift_reg_8_bit:myshifter
init_c~[7..0]
0
8'h10
1
clk
en
in
out[7..0]
shift_en
serIn
co
serOut

Symbol:



Minimum and maximum temperature:

125C:

Slow 1200mV 125C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	493.1 MHz	250.0 MHz	clk	limit due to minimum period restriction (max I/O toggle rate)

Slow 1200mV 125C Model Setup Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	clk	-1.028	-7.120

Slow 1200mV 125C Model Hold Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	clk	0.447	0.000

-40C:

Slow 1200mV -40C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	583.43 MHz	250.0 MHz	clk	limit due to minimum period restriction (max I/O toggle rate)

Slow 1200mV -40C Model Setup Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	clk	-0.714	-4.582

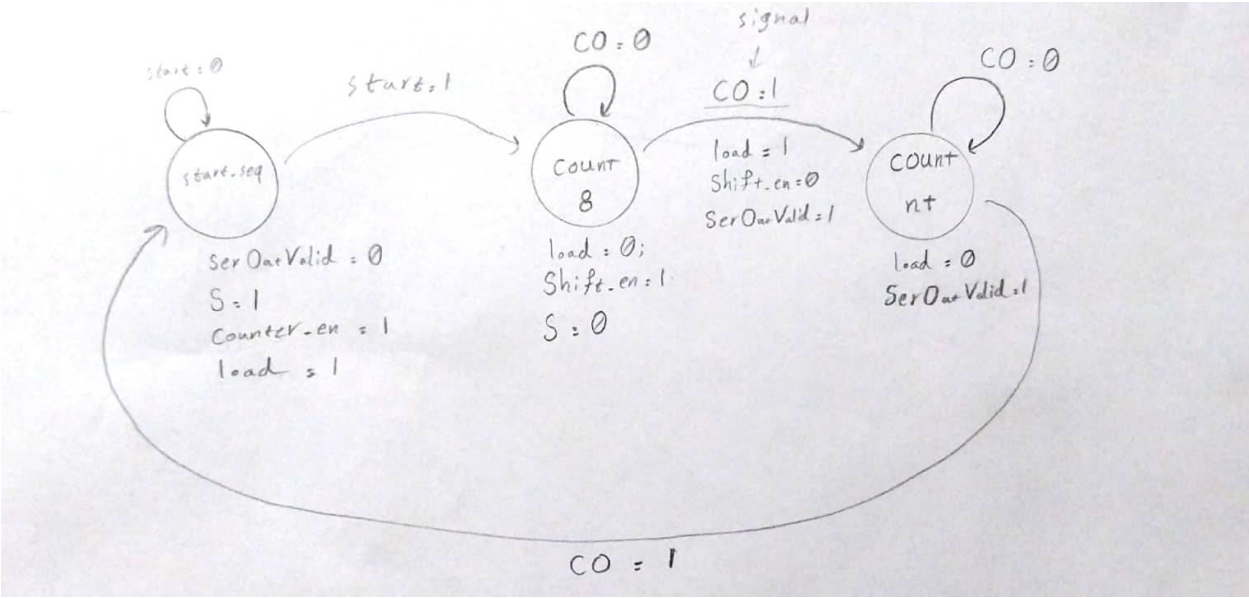
Slow 1200mV -40C Model Hold Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	clk	0.394	0.000

WHEN??:

And in this part, we will answer another question, WHEN??.



This part will control and conduct the previous part.
As you can see we have 3 states here, and each one of them are corresponding to a part of our project.

Verilog:

```
module main_state (input clk, rst, co, serIn, output logic load, S,
shift_en, counter_en, serOutValid);
   logic [2:0] ps, ns;
   wire start;
   parameter [2:0] START_SEQUENCE = 3'd0, COUNT_8 = 3'd1, COUNT_NT = 3'd2;
```

```
seq_det_pre start_seq(clk, rst, serIn, start);

always @(ps, co, start) begin
    ns = START_SEQUENCE;
    case (ps)
        START_SEQUENCE: begin
            ns = start ? COUNT_8 : START_SEQUENCE;
            serOutValid = 1'b0;
            S = 1'b1;
            counter_en = 1;
            load = 1'b1;
        end

        COUNT_8: begin
            if (co == 1) begin
                ns = COUNT_NT;
                load = 1;
                shift_en = 0;
                serOutValid = 1;
            end
            else begin
                ns = COUNT_8;
                load = 1'b0;
                shift_en = 1'b1;
                S = 1'b0;
            end

        end
        COUNT_NT: begin
            ns = co ? START_SEQUENCE : COUNT_NT;
            serOutValid = 1;
            shift_en = 0;
            load = 0;
        end

        default: ns = START_SEQUENCE;
    endcase

end
```

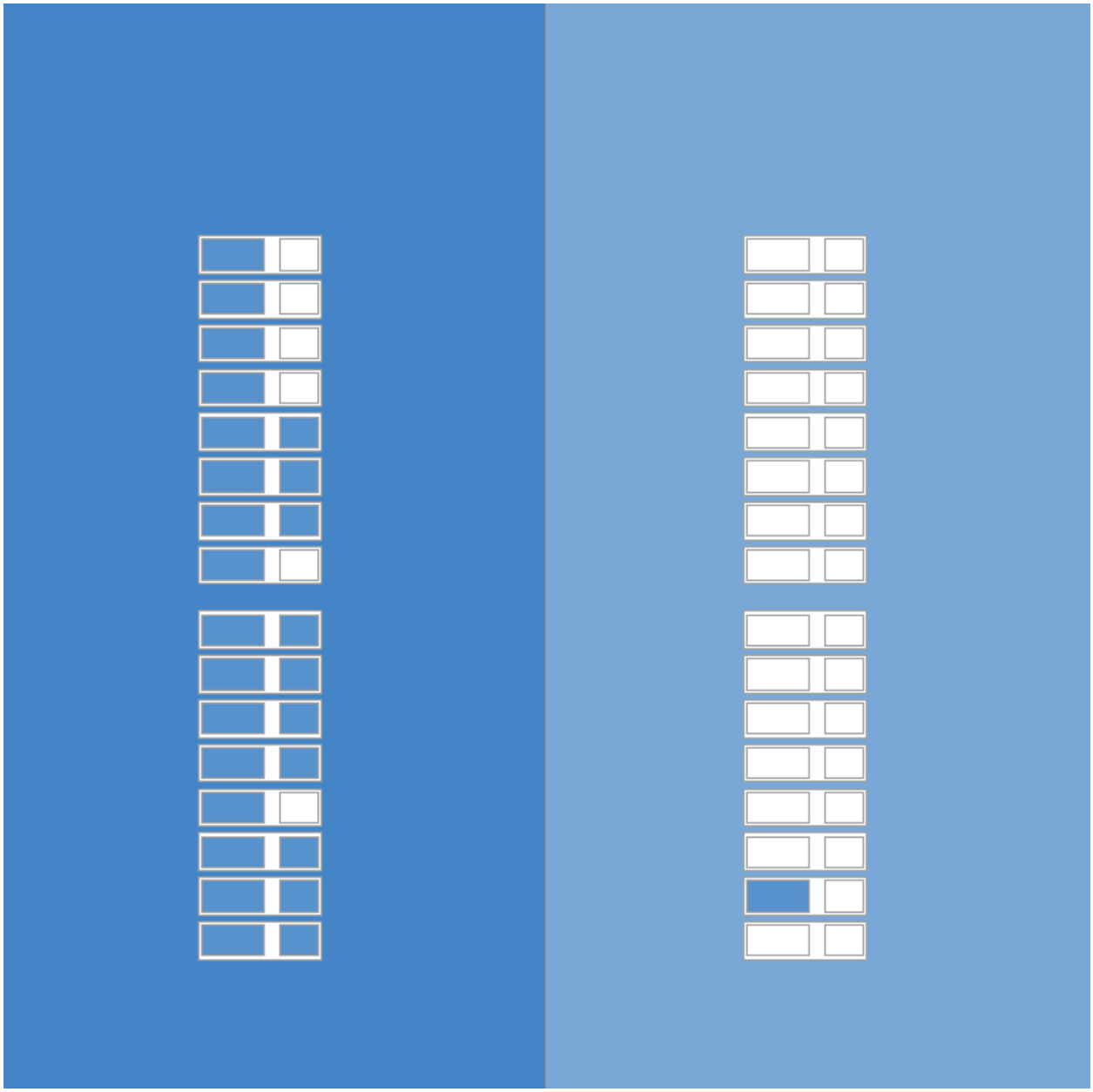
```
   always @(posedge clk, posedge rst) begin
       if (rst)
           ps <= START_SEQUENCE;
       else
           ps <= ns;
   end
endmodule
```

Syntheized:

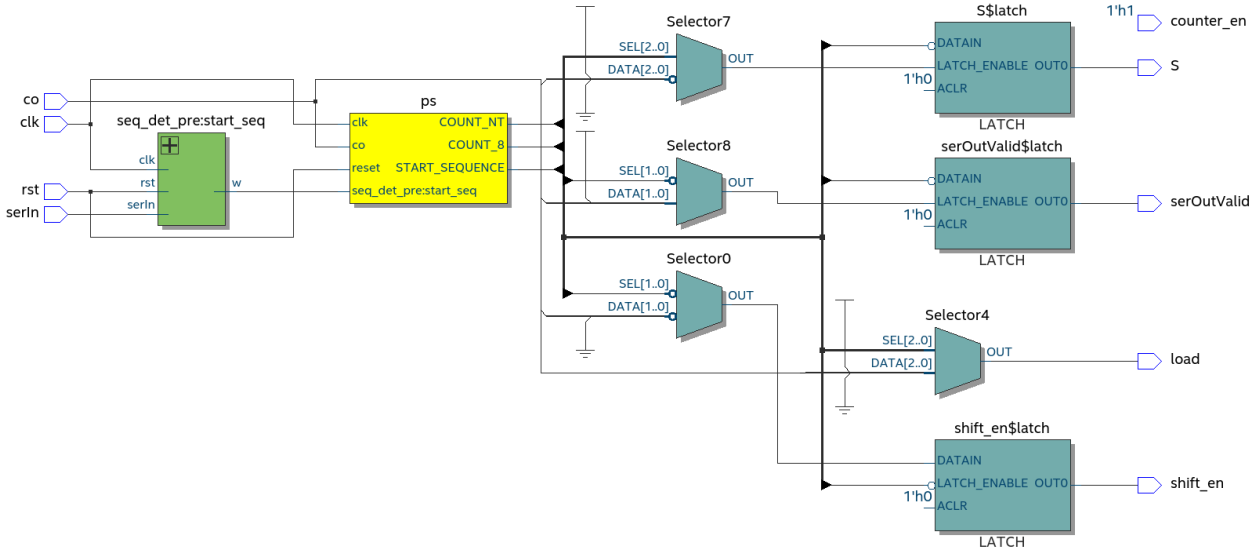
Flow Summary

<<Filter>>

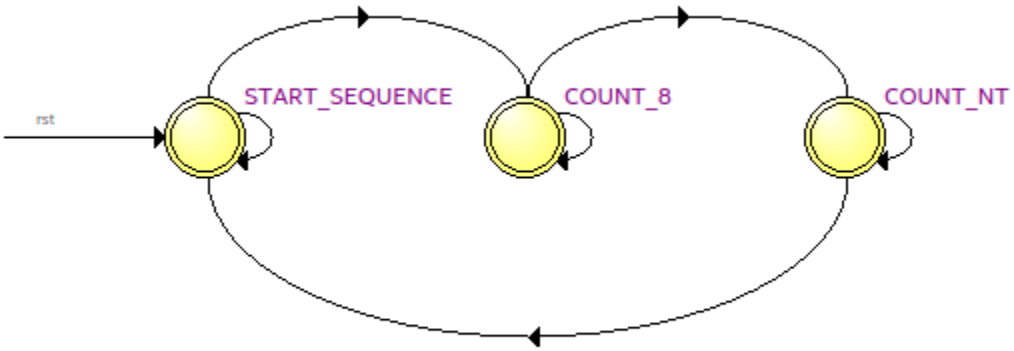
Flow Status	Successful - Wed Jan 3 06:47:50 2024
Quartus Prime Version	23.1std.0 Build 991 11/28/2023 SC Lite Edition
Revision Name	main_state
Top-level Entity Name	main_state
Family	Cyclone IV GX
Device	EP4CGX15BF14A7
Timing Models	Final
Total logic elements	17 / 14,400 (< 1 %)
Total registers	10
Total pins	9 / 81 (11 %)
Total virtual pins	0
Total memory bits	0 / 552,960 (0 %)
Embedded Multiplier 9-bit elements	0
Total GXB Receiver Channel PCS	0 / 2 (0 %)
Total GXB Receiver Channel PMA	0 / 2 (0 %)
Total GXB Transmitter Channel PCS	0 / 2 (0 %)
Total GXB Transmitter Channel PMA	0 / 2 (0 %)
Total PLLs	0 / 3 (0 %)



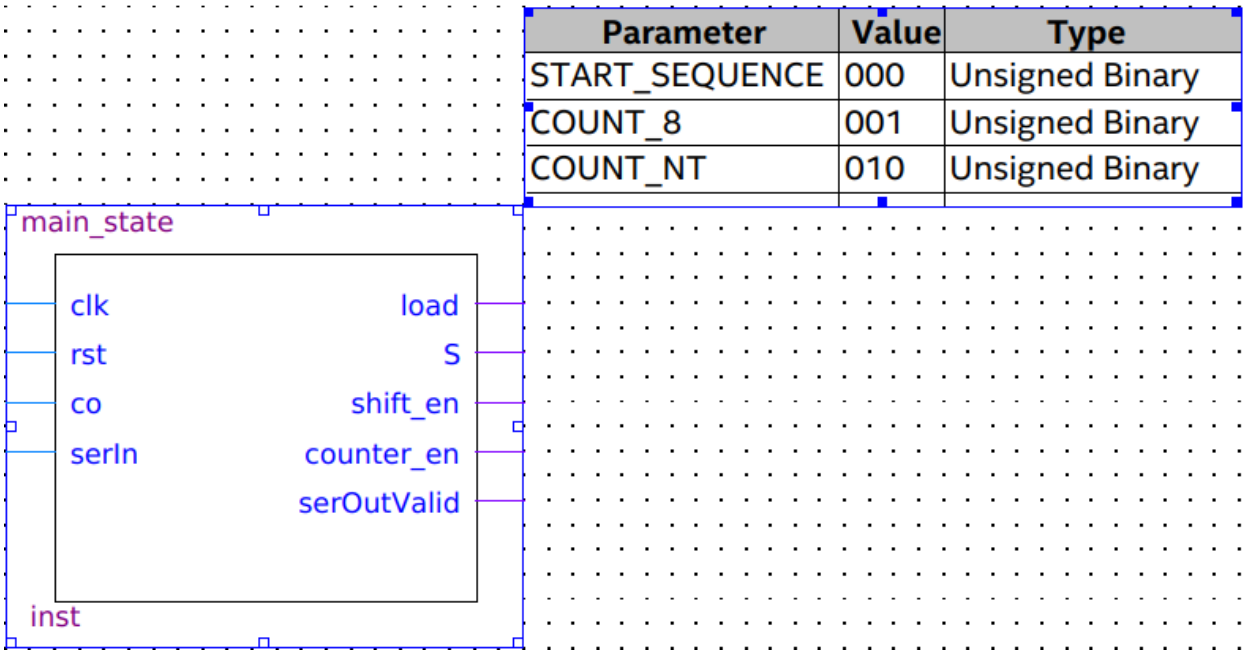
Rtl view:



state_plan:



Symbol:



Parameter	Value	Type
START_SEQUENCE	000	Unsigned Binary
COUNT_8	001	Unsigned Binary
COUNT_NT	010	Unsigned Binary

Minimum and maximum temperature:

125C:

Slow 1200mV 125C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	392.93 MHz	250.0 MHz	clk	limit due to minimum period restriction (max I/O toggle rate)

Slow 1200mV 125C Model Setup Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	ps...CE	-3.543	-5.769
2	co	-1.920	-2.493
3	clk	-1.662	-5.695

Slow 1200mV 125C Model Hold Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	clk	-0.120	-0.120
2	co	0.321	0.000
3	ps...CE	1.819	0.000

-40C:

Slow 1200mV -40C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	434.97 MHz	250.0 MHz	clk	limit due to minimum period restriction (max I/O toggle rate)

Slow 1200mV -40C Model Setup Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	ps...CE	-2.998	-4.768
2	co	-1.832	-2.139
3	clk	-1.408	-3.660

Slow 1200mV -40C Model Hold Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	clk	-0.109	-0.109
2	co	0.242	0.000
3	ps...CE	1.570	0.000

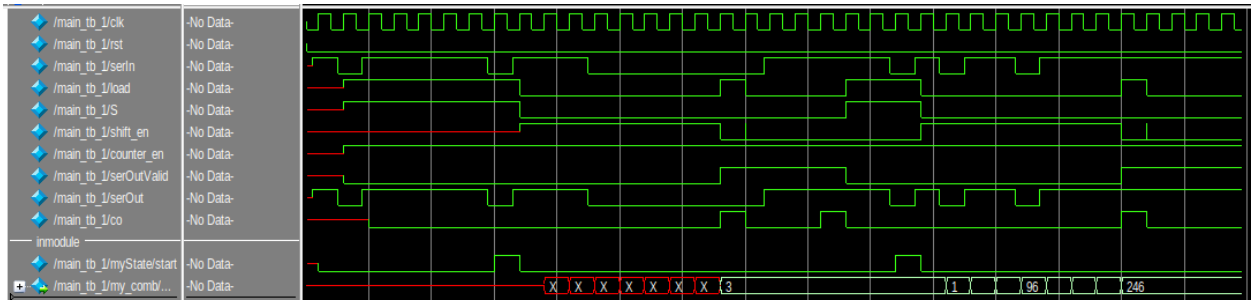
Simulation:

Here's a testbench for this circuit.

```
module main_tb_1 ();

   logic clk, rst, serIn;
   wire load, S, shift_en, counter_en, serOutValid, serOut;

   main_state myState (clk, rst, co, serIn, load, S, shift_en, counter_en,
serOutValid);
   combin_test my_comb (clk, rst, serIn, shift_en, counter_en, load, S,
co, serOut, serOutValid);

   initial {clk, rst} = 2'b0;

   always #100 clk = ~clk;

   initial begin
       #50  serIn = 1;

       #200 serIn = 0;
       #200 serIn = 1;
       #200 serIn = 1;
       #200 serIn = 1;
       #200 serIn = 1;
       #200 serIn = 1;
       #200 serIn = 0;


       #200 serIn = 1;
```

```
        #200 serIn = 1;
        #200 serIn = 1;
        #200 serIn = 0;
        #200 serIn = 0;
        #200 serIn = 0;
        #200 serIn = 0;
        #200 serIn = 0;
        #200 serIn = 0;

        #200 serIn = 0;
        #200 serIn = 1;
        #200 serIn = 1;
        #200 serIn = 1;
        #200 serIn = 1;
        #200 serIn = 1;
        #200 serIn = 0;

        #200 serIn = 1;
        #200 serIn = 0;
        #200 serIn = 1;
        #200 serIn = 1;
        #200 serIn = 0;
        #200 serIn = 1;
        #200 serIn = 1;
        #200 serIn = 1;
        #200 serIn = 1;
        #200 serIn = 1;
        #200 serIn = 1;
        #200 serIn = 1;
        #200 $stop;
    end
endmodule
```

Lets see the waveform:
Note: it's not synthesized yet so there's nothing going on with delays.


/main_tb_1/clk
/main_tb_1/rst
/main_tb_1/serIn
/main_tb_1/load
/main_tb_1/S
/main_tb_1/shift_en
/main_tb_1/counter_en
/main_tb_1/serOutValid
/main_tb_1/serOut
/main_tb_1/co
inmodule
/main_tb_1/myState/start
/main_tb_1/my_comb/...
-No Data-
X
3
1
96
246