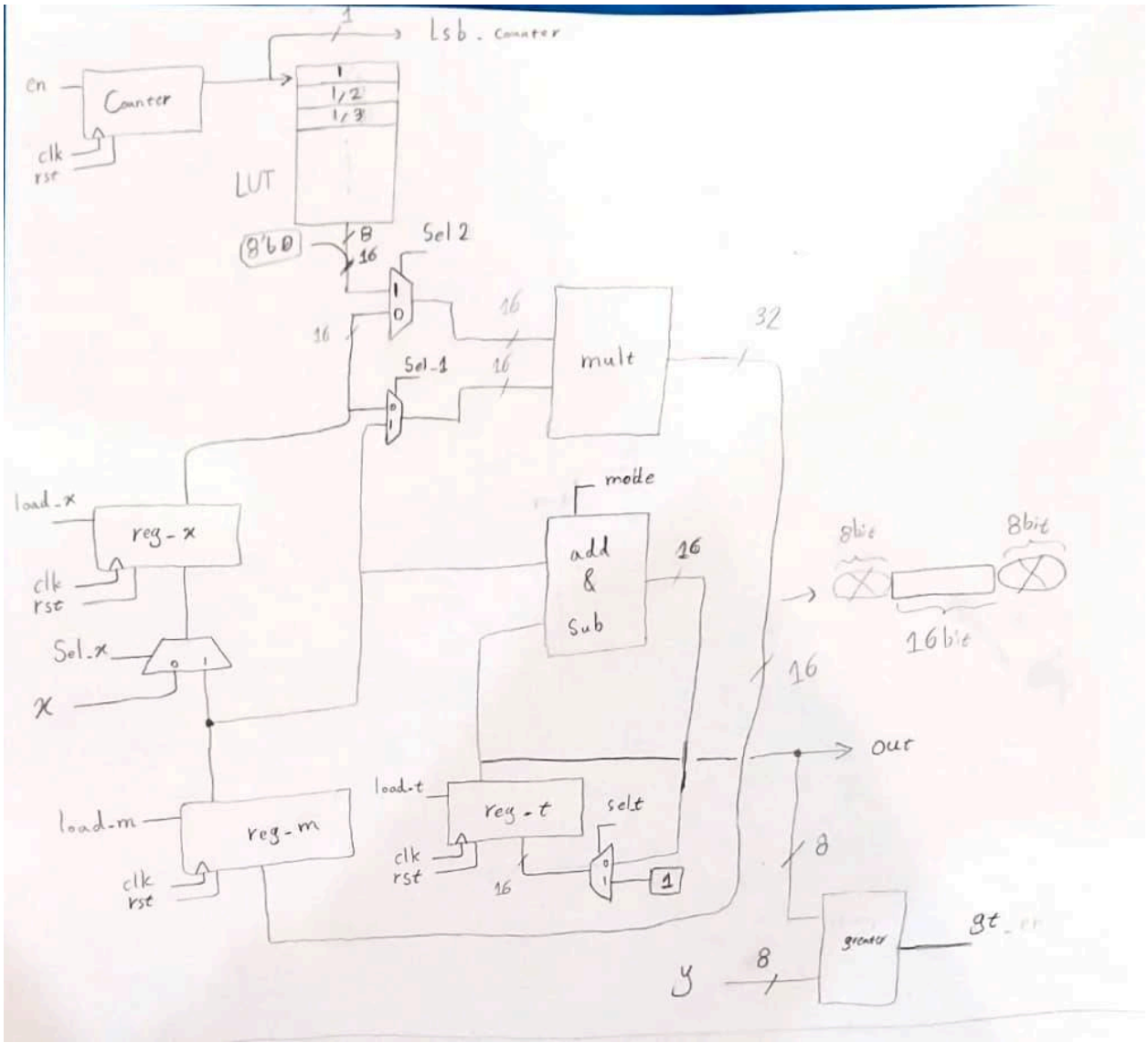
Datapath:

Description of our combinatorial part.



Components:

Verilog:

```
module my_counter #(parameter BIT_NUM = 8) (input clk, rst, en, output
logic [BIT_NUM - 1:0] out);

   always @(posedge clk, posedge rst) begin
       if (rst)
           out <= {BIT_NUM{1'b0}};
       else if (en)
           out <= out + 1'b1;
   end


endmodule

module register_16_bit (input clk, rst, load, input [15:0] init, output
logic [15:0] out);

   always @(posedge clk, posedge rst) begin
       if (rst)
           out <= 16'b0;
       else if (load)
           out <= init;
   end


endmodule

module sub_add_16_bit (input [15:0] A, B, input mode, output logic [15:0]
out, output logic CO);

   always @(A, B, mode) begin

       if (mode == 1'b1)
           {CO, out} = A + B;
       else
           out = A - B;
```

```
   end

endmodule

module multiplier_16_bit (input [15:0] A, B, output [31:0] out);

   assign out = A * B;

endmodule

module greater_8_bit (input [7:0] A, B, output gt);

   assign gt = (A > B) ? 1'b1 : 1'b0;

endmodule

module mux_2_to_1 (input [15:0] in0, in1, input sel, output [15:0] out);

   assign out = (sel == 0) ? in0 : in1;

endmodule

module LUT_8_bit (input[3:0] address , output[7:0] data);

   logic [7:0] ddata;

   always@(address) begin

       case(address)
           0:ddata = 8'hFF; //1
           1:ddata = 8'h80; //1/2
           2:ddata = 8'h55; //1/3
           3:ddata = 8'h40; //1/4
           4:ddata = 8'h33;  //1/5
           5:ddata = 8'h2A; //1/6
           6:ddata = 8'h24; //1/7
           7:ddata = 8'h20; //1/8
           8:ddata = 8'h1c; //1/9
           9:ddata = 8'h19; //1/10
           10:ddata = 8'h17; //1/11
```

```
            11:ddata = 8'h15; //1/12
            12:ddata = 8'h13; //1/13
            13:ddata = 8'h12; //1/14
            14:ddata = 8'h11; //1/15
            15:ddata = 8'h10; //1/16
        endcase
    end

    assign data = ddata;

endmodule
```

Assembled:

Verilog:

```
module comb_part (input clk, rst, counter_en, sel_1, sel_2, sel_x, sel_t,
load_x, load_m, load_t, mode, input [15:0] inX, input [7:0] inY, output
[15:0] out, output gt, lsb_counter);

    wire [7:0] lut_w;
    wire [31:0] mult_w;
    wire [15:0] add_w;
    wire [15:0] mux_1_w, mux_2_w, mux_x_w, mux_t_w;
    wire [15:0] reg_x_w, reg_m_w, reg_t_w;
    wire [3:0] cntr_w;

    my_counter #(4) cntr (clk, rst, counter_en, cntr_w);

    LUT_8_bit lut (cntr_w, lut_w);

    mux_2_to_1 mux_2 (reg_x_w, {8'b0, lut_w}, sel_2, mux_2_w);
    mux_2_to_1 mux_1 (reg_x_w, reg_m_w, sel_1, mux_1_w);
    mux_2_to_1 mux_x (inX, reg_m_w, sel_x, mux_x_w);
    mux_2_to_1 mux_t (16'b0000000011111111, add_w, sel_t, mux_t_w);

    register_16_bit reg_x (clk, rst, load_x, mux_x_w, reg_x_w);
    register_16_bit reg_m (clk, rst, load_m, mult_w[23:8], reg_m_w);
    register_16_bit reg_t (clk, rst, load_t, mux_t_w, reg_t_w);
```

```
   sub_add_16_bit sub_add (reg_t_w, reg_m_w, mode, add_w);

   multiplier_16_bit mult (mux_1_w, mux_2_w, mult_w);

   greater_8_bit greater (inY, out[7:0], gt);

   assign out = reg_t_w;
   assign lsb_counter = cntr_w[0];

endmodule
```

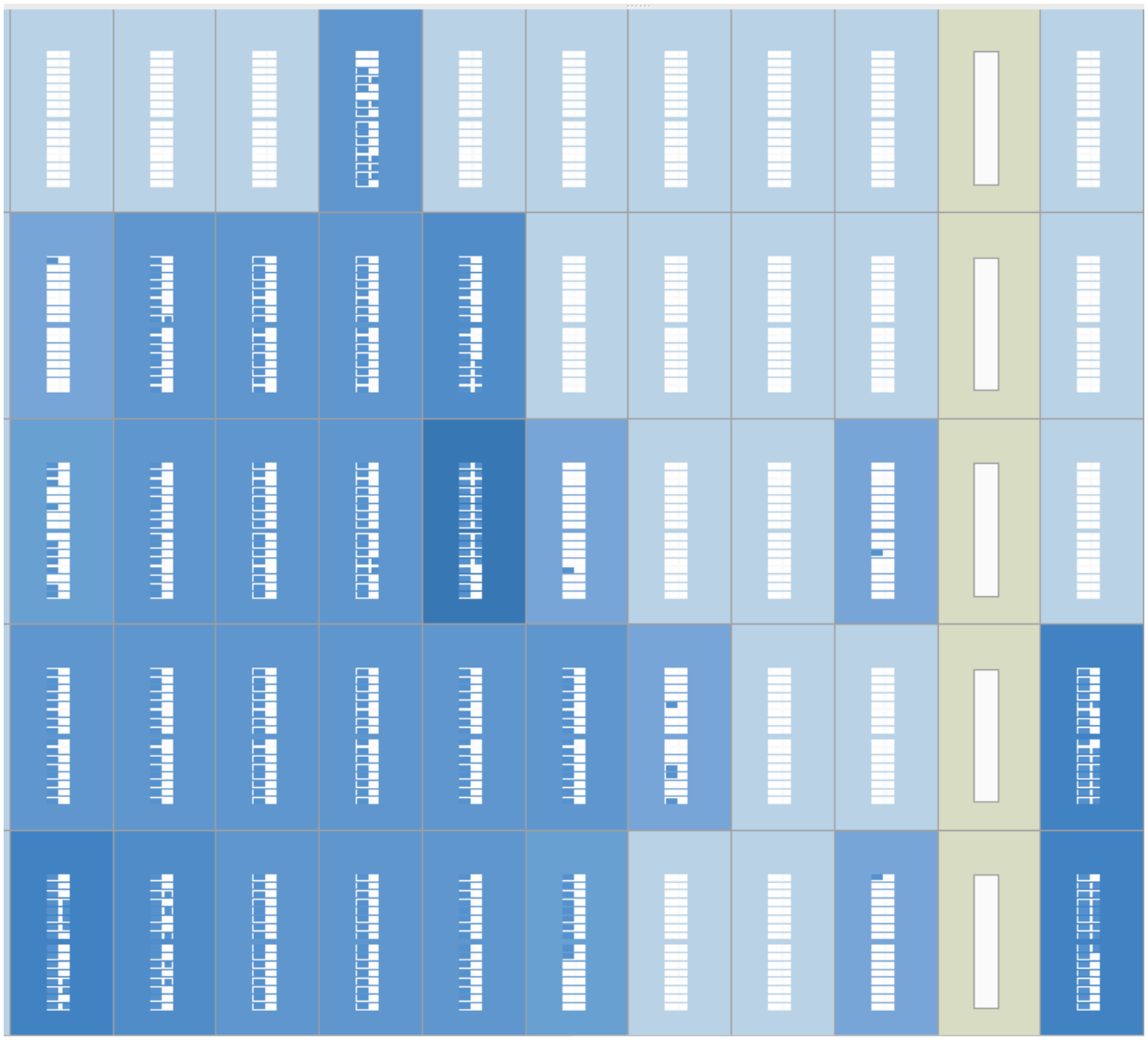
Synthesized:

Flow Summary

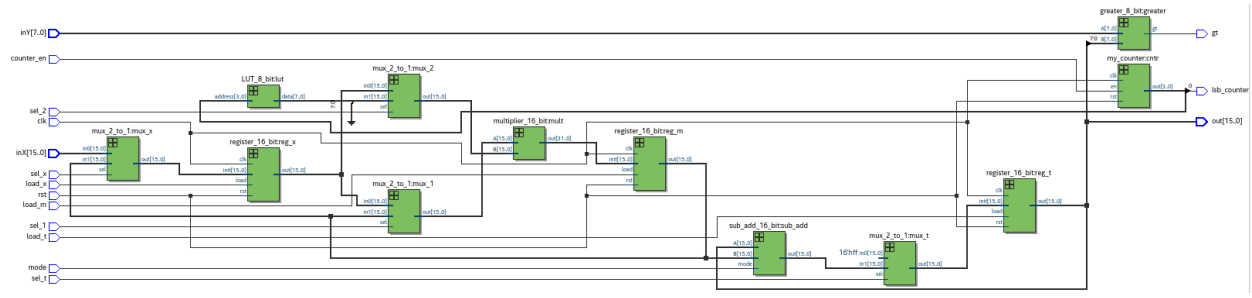
<<Filter>>

Flow Status	Successful - Wed Jan 10 04:33:25 2024
Quartus Prime Version	23.1std.0 Build 991 11/28/2023 SC Lite Edition
Revision Name	combin_part
Top-level Entity Name	comb_part
Family	Cyclone IV GX
Device	EP4CGX15BF14A7
Timing Models	Final
Total logic elements	385 / 14,400 (3 %)
Total registers	52
Total pins	53 / 81 (65 %)
Total virtual pins	0
Total memory bits	0 / 552,960 (0 %)
Embedded Multiplier 9-bit elements	0
Total GXB Receiver Channel PCS	0 / 2 (0 %)
Total GXB Receiver Channel PMA	0 / 2 (0 %)
Total GXB Transmitter Channel PCS	0 / 2 (0 %)
Total GXB Transmitter Channel PMA	0 / 2 (0 %)
Total PLLs	0 / 3 (0 %)

Floor plan:



Rtl view:



Timing:

125C:

Slow 1200mV 125C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	95.08 MHz	95.08 MHz	clk	

Slow 1200mV 125C Model Setup Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	clk	-9.517	-217.369

Slow 1200mV 125C Model Hold Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	clk	0.424	0.000

-40C:

Slow 1200mV -40C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	110.64 MHz	110.64 MHz	clk	

Slow 1200mV -40C Model Setup Summary

<<Filter>>

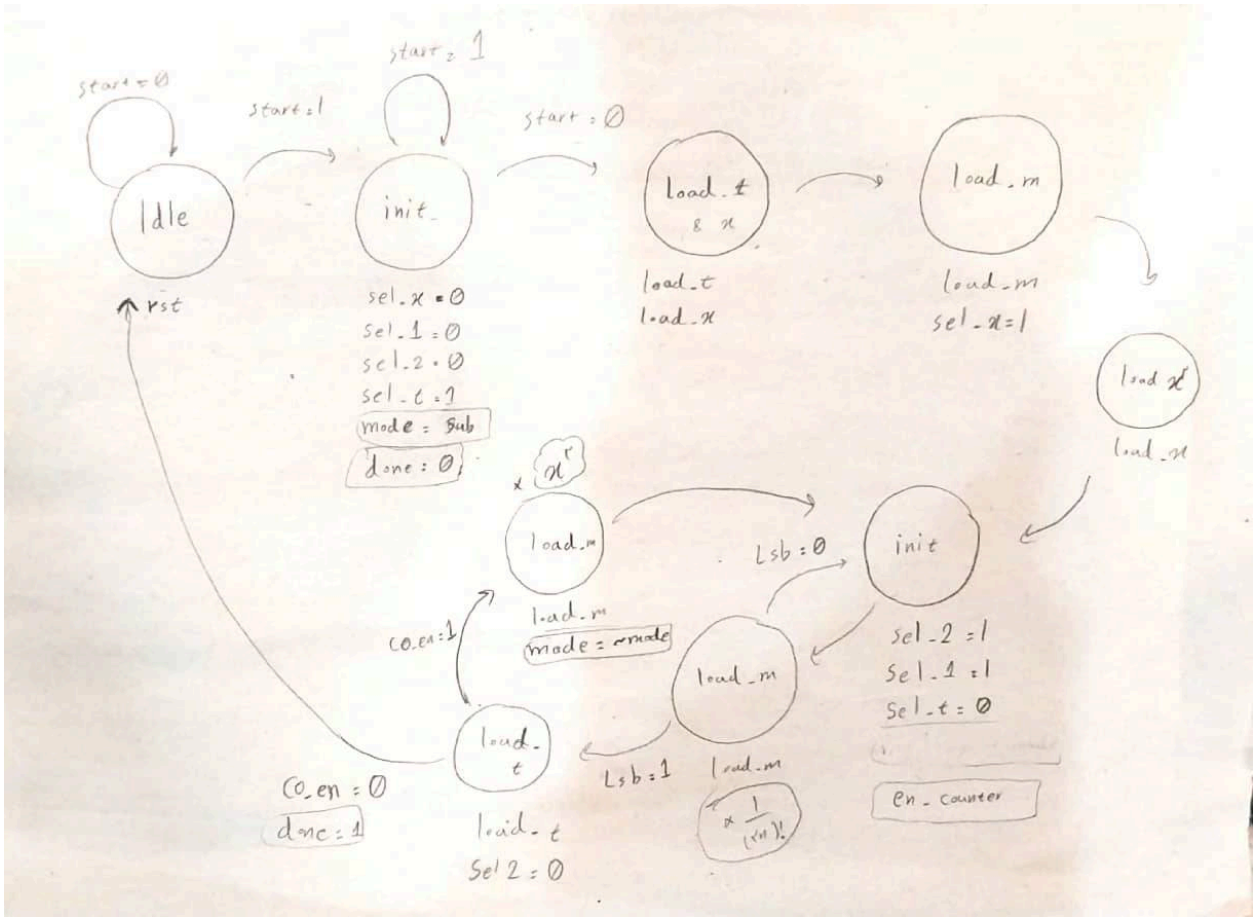
	Clock	Slack	End Point TNS
1	clk	-8.038	-180.967

Slow 1200mV -40C Model Hold Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	clk	0.342	0.000

State machine:



Verilog:

```
module controller (input clk, rst, start, gt, lsb_counter, output logic
counter_en, sel_1, sel_2, sel_x, sel_t, load_x, load_m, load_t, mode,
done, rst_w);
   logic [3:0] ps, ns;
   parameter [3:0] IDLE = 4'd0, INIT_X = 4'd1, LOAD_XT = 4'd2,
LOAD_X2_IN_M = 4'd3, LOAD_X2 = 4'd4,
   INIT_FRAC = 4'd5, LOAD_FRAC = 4'd6, LOAD_SUB_ADD = 4'd7, LOAD_MULTI =
4'd8;

   always @(ps, gt, lsb_counter, start) begin
       ns = IDLE;
```

```
        counter_en = 1'b0; load_m = 1'b0; load_x = 1'b0; load_t = 1'b0;
mode = 1'b0;
        rst_w = 1'b0;

        case (ps)
            IDLE: begin
                ns = start ? INIT_X : IDLE;
                rst_w = 1'b1;
            end

            INIT_X: begin
                ns = start ? INIT_X : LOAD_XT;

                sel_x = 1'b0; sel_t = 1'b0; sel_1 = 1'b0; sel_2 = 1'b0;
                mode = 1'b0; done = 1'b0;
            end

            LOAD_XT: begin
                ns = LOAD_X2_IN_M;

                load_t = 1'b1; load_x = 1'b1;
            end

            LOAD_X2_IN_M: begin
                ns = LOAD_X2;

                load_m = 1'b1; sel_x = 1'b1;
            end

            LOAD_X2: begin
                ns = INIT_FRAC;

                load_x = 1'b1;
            end

            INIT_FRAC: begin
                ns = LOAD_FRAC;

                sel_1 = 1'b1; sel_2 = 1'b1; sel_t = 1'b1;
                counter_en = 1'b1;
```

```
            end

            LOAD_FRAC: begin
                ns = lsb_counter ? LOAD_SUB_ADD : INIT_FRAC;

                load_m = 1'b1;
            end

            LOAD_SUB_ADD: begin
                if (gt == 1'b1) begin
                    ns = IDLE;

                    done = 1'b1;
                end
                else
                    ns = LOAD_MULTI;

                load_t = 1'b1;
                sel_2 = 1'b0;
            end

            LOAD_MULTI: begin
                ns = INIT_FRAC;

                load_m = 1'b1;
                mode = ~mode;
            end

            default: ns = IDLE;
        endcase
    end

    always @(posedge clk, posedge rst) begin
        if (rst)
            ps <= IDLE;
        else
            ps <= ns;
    end

endmodule
```

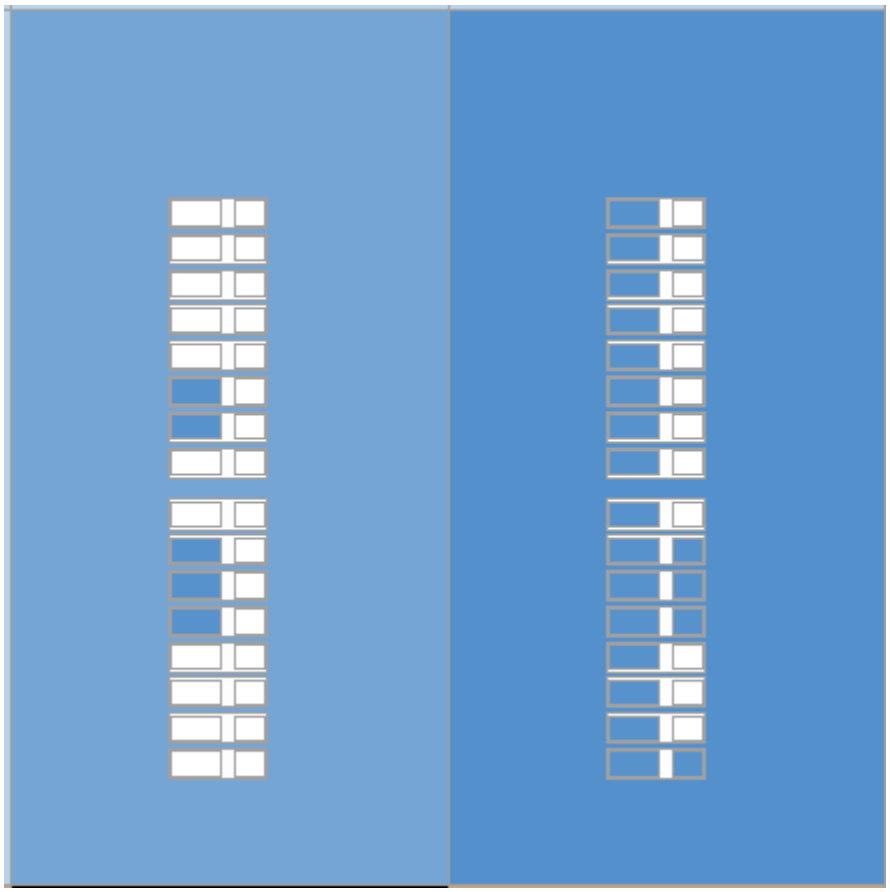
Synthesized:

Flow Summary

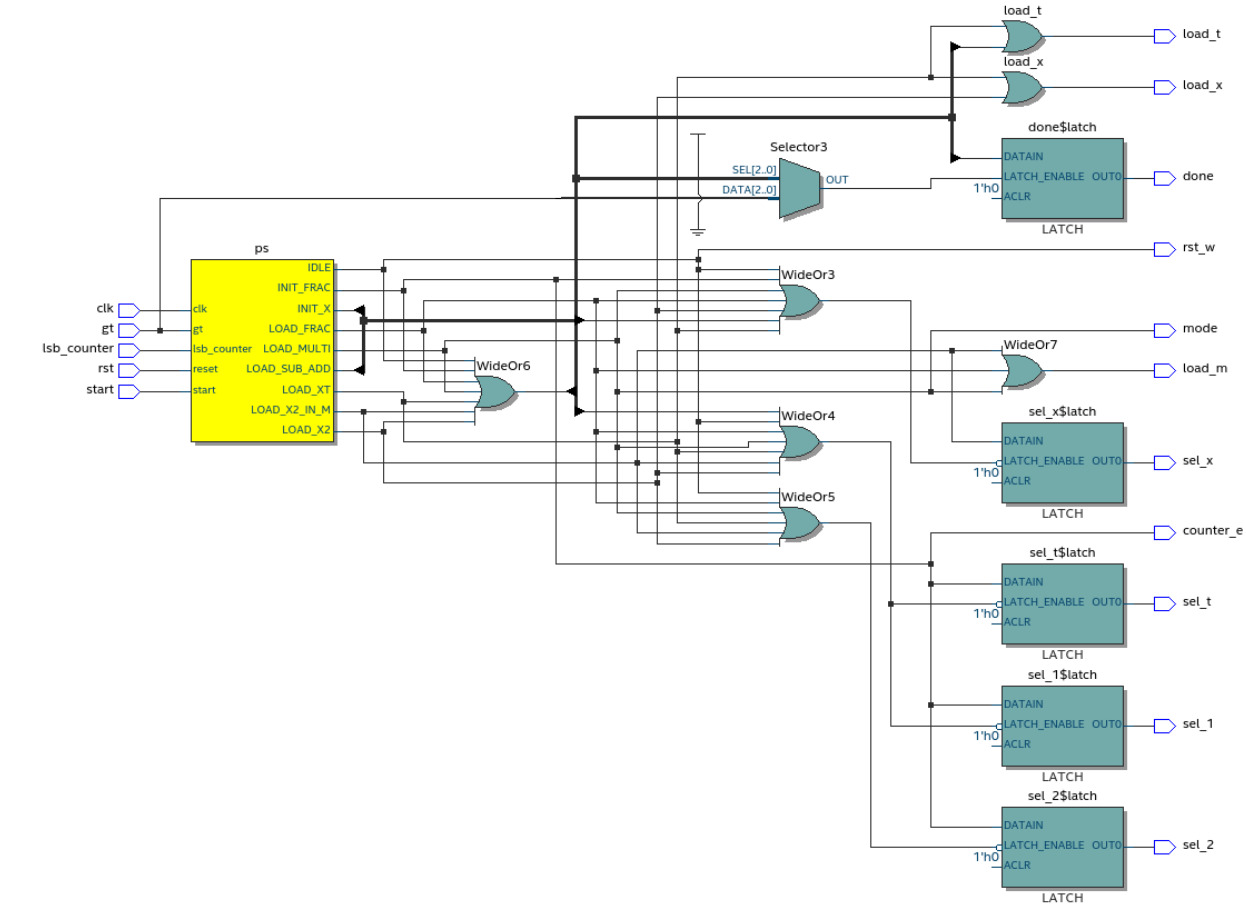
<<Filter>>

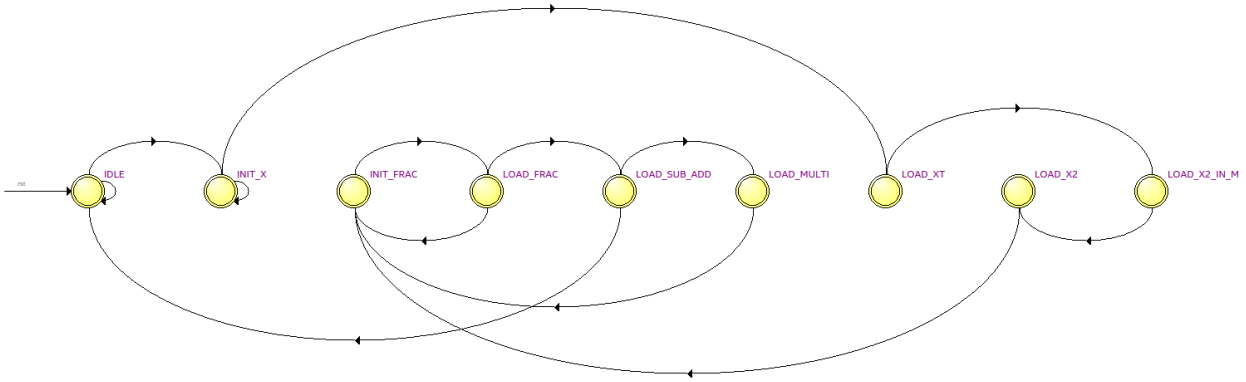
Flow Status	Successful - Wed Jan 10 04:51:30 2024
Quartus Prime Version	23.1std.0 Build 991 11/28/2023 SC Lite Edition
Revision Name	controller
Top-level Entity Name	controller
Family	Cyclone IV GX
Device	EP4CGX15BF14A7
Timing Models	Final
Total logic elements	21 / 14,400 (< 1 %)
Total registers	4
Total pins	16 / 81 (20 %)
Total virtual pins	0
Total memory bits	0 / 552,960 (0 %)
Embedded Multiplier 9-bit elements	0
Total GXB Receiver Channel PCS	0 / 2 (0 %)
Total GXB Receiver Channel PMA	0 / 2 (0 %)
Total GXB Transmitter Channel PCS	0 / 2 (0 %)
Total GXB Transmitter Channel PMA	0 / 2 (0 %)
Total PLLs	0 / 3 (0 %)

Floor plan:



Rtl view:


load_t
load_x
done$latch
Selector3
SEL[2..0]
DATA[2..0]
OUT
DATAIN
LATCH_ENABLE
OUT0
ACLR
1'h0
LATCH
done
rst_w
ps
IDLE
INIT_FRAC
INIT_X
LOAD_FRAC
LOAD_MULTI
LOAD_SUB_ADD
LOAD_XT
LOAD_X2_IN_M
LOAD_X2
clk
gt
lsb_counter
rst
start
reset
WideOr3
WideOr6
WideOr4
WideOr5
WideOr7
mode
load_m
sel_x$latch
sel_x
counter_e
sel_t$latch
sel_t
sel_1$latch
sel_1
sel_2$latch
sel_2


IDLE
INIT_X
INIT_FRAC
LOAD_FRAC
LOAD_SUB_ADD
LOAD_MULTI
LOAD_XT
LOAD_X2
LOAD_X2_IN_M

Timing:

125C:

Slow 1200mV 125C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	316.66 MHz	316.66 MHz	ps~4	
2	391.08 MHz	250.0 MHz	clk	limit due to minimum period restriction (max I/O toggle rate)

Slow 1200mV 125C Model Setup Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	ps~4	-3.350	-12.517
2	clk	-1.557	-4.925

Slow 1200mV 125C Model Hold Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	ps~4	0.352	0.000
2	clk	0.454	0.000

-40C:

Slow 1200mV -40C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	343.64 MHz	343.64 MHz	ps~4	
2	437.45 MHz	250.0 MHz	clk	limit due to minimum period restriction (max I/O toggle rate)

Slow 1200mV -40C Model Setup Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	ps~4	-2.864	-10.750
2	clk	-1.286	-3.818

Slow 1200mV -40C Model Hold Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	ps~4	0.280	0.000
2	clk	0.368	0.000

Main circuit:

Verilog:

```
module cos_x (input clk, rst, start, input [15:0] inX, input [7:0] inY,
output [15:0] out, output done);

   wire counter_en, sel_1, sel_2, sel_t, sel_x,
   load_m, load_t, load_x, mode, gt, lsb_counter, rst_w;
```

```
   comb_part datapath (clk, rst_w, counter_en, sel_1, sel_2, sel_x, sel_t,
load_x, load_m, load_t, mode, inX, inY, out, gt, lsb_counter);
   controller controller_ (clk, rst, start, gt, lsb_counter, counter_en,
sel_1, sel_2, sel_x, sel_t, load_x, load_m, load_t, mode, done, rst_w);

endmodule
```

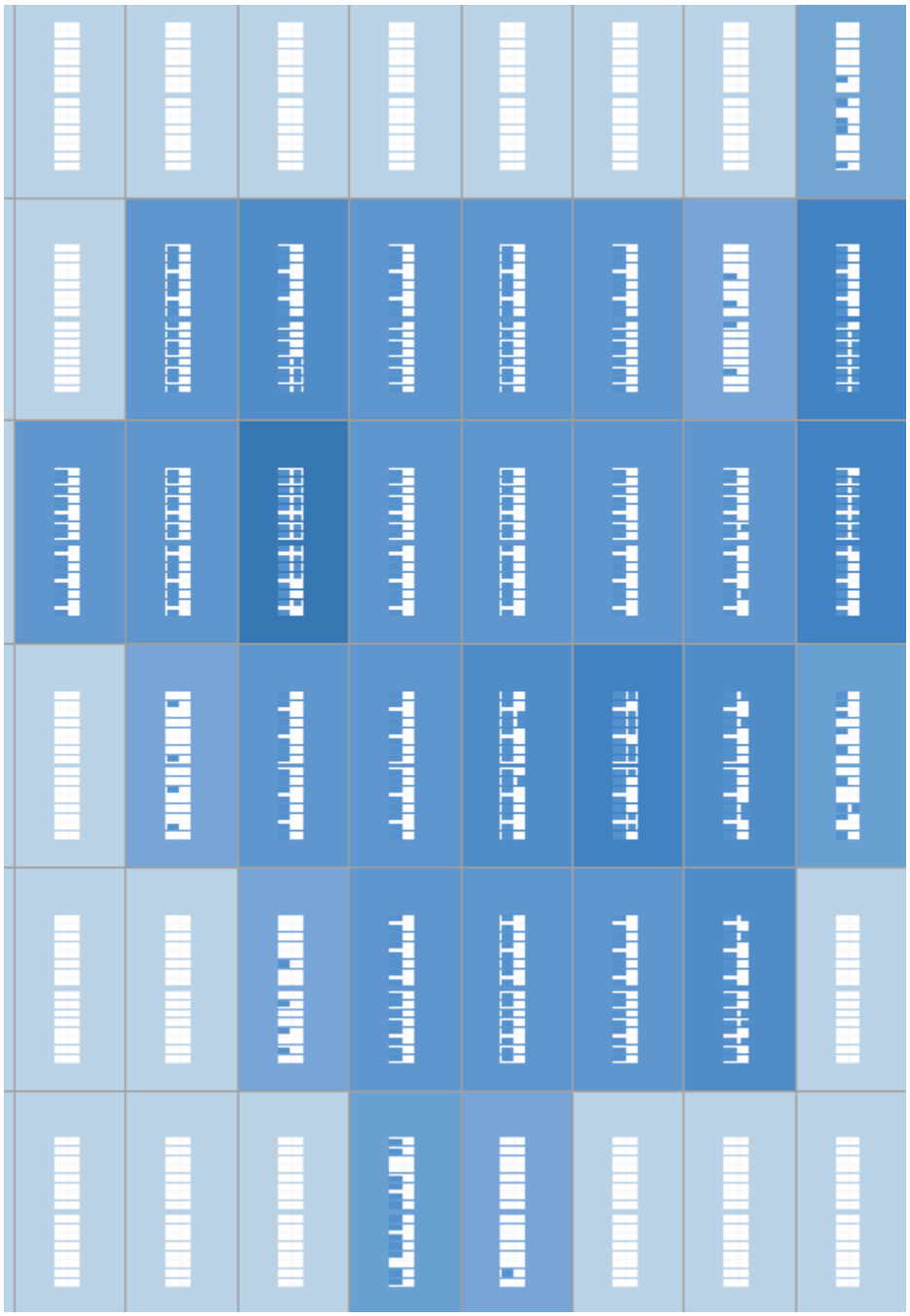
Synthesized:

Flow Summary

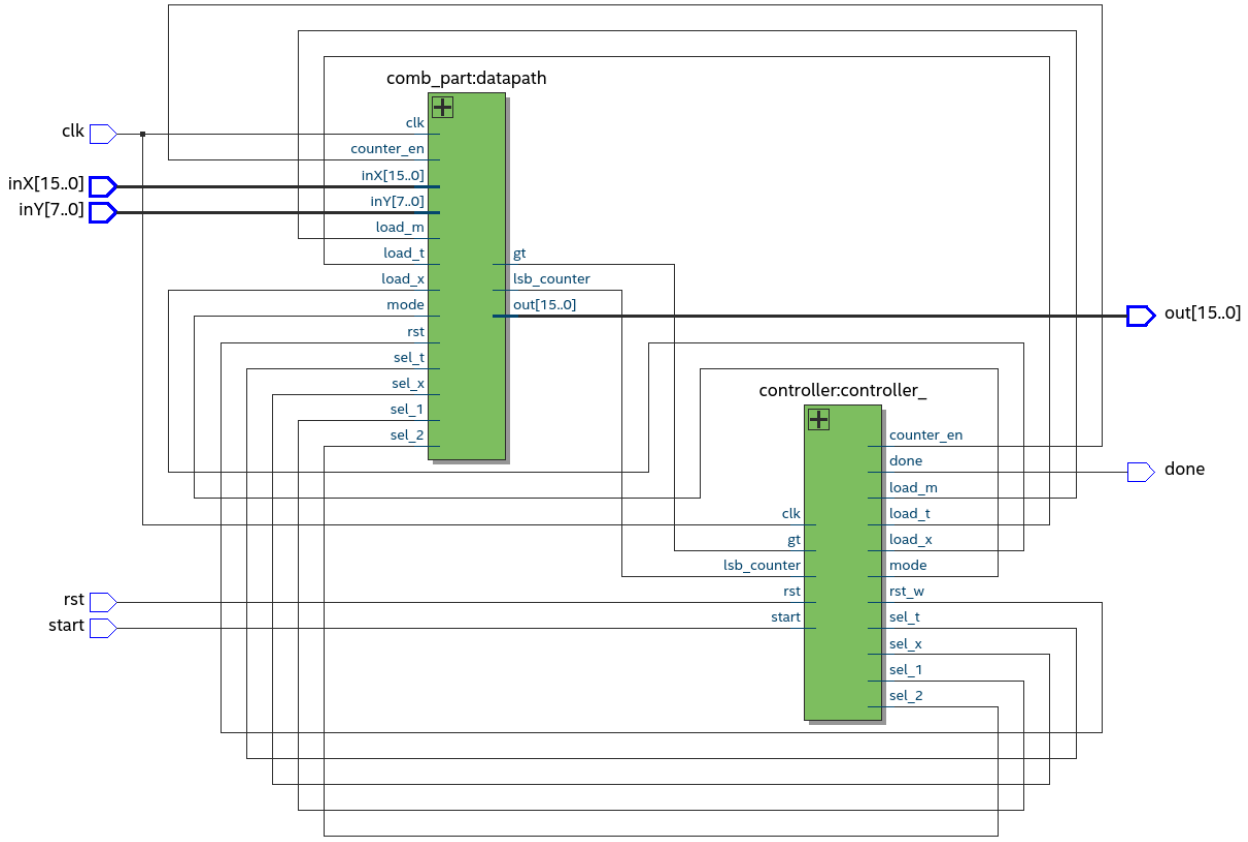
<<Filter>>

Flow Status	Successful - Wed Jan 10 05:25:25 2024
Quartus Prime Version	23.1std.0 Build 991 11/28/2023 SC Lite Edition
Revision Name	cos_x
Top-level Entity Name	cos_x
Family	Cyclone IV GX
Device	EP4CGX15BF14A7
Timing Models	Final
Total logic elements	408 / 14,400 (3 %)
Total registers	56
Total pins	44 / 81 (54 %)
Total virtual pins	0
Total memory bits	0 / 552,960 (0 %)
Embedded Multiplier 9-bit elements	0
Total GXB Receiver Channel PCS	0 / 2 (0 %)
Total GXB Receiver Channel PMA	0 / 2 (0 %)
Total GXB Transmitter Channel PCS	0 / 2 (0 %)
Total GXB Transmitter Channel PMA	0 / 2 (0 %)
Total PLLs	0 / 3 (0 %)

Floor plan:



Rtl view:



Timing:

125C:

Slow 1200mV 125C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	88.75 MHz	88.75 MHz	clk	
2	211.86 MHz	211.86 MHz	contr...|ps~4	

Slow 1200mV 125C Model Setup Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	clk	-10.267	-283.104
2	co...~4	-5.266	-16.418

Slow 1200mV 125C Model Hold Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	co...~4	0.072	0.000
2	clk	0.425	0.000

-40C:

Slow 1200mV -40C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	103.2 MHz	103.2 MHz	clk	
2	225.84 MHz	225.84 MHz	contr...|ps~4	

Slow 1200mV -40C Model Setup Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	clk	-8.690	-240.179
2	co...~4	-4.647	-14.267

Slow 1200mV -40C Model Hold Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	co...~4	0.038	0.000
2	clk	0.343	0.000