Question 1:

Verilog description for ALU:

`timescale 1ns/1ns

module ALU(input signed [15:0] inA, inB, output reg [15:0] outW, input inC, input [2:0] opc, output reg zer, neg);

    always @ (inA, inB, opc) begin

        outW = 16'b0;

        zer = 1'b0;

        neg = 1'b0;

        case (opc)

            3'b000: outW = ~inA + 1;

            3'b001: outW = inA + 1;

            3'b010: outW = inA + inB + inC;

            3'b011: outW = inA + inB >>> 1;

            3'b100: outW = inA & inB;

            3'b101: outW = inA | inB;

            3'b110: outW = {inA[7:0], inB[7:0]};

            default: outW = 16'b0;

        endcase

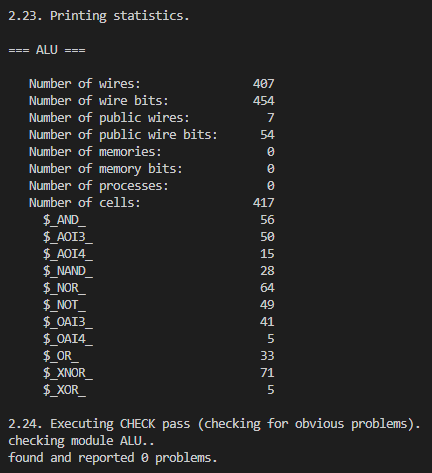
        zer = outW == 16'b0 ? 1'b1: 1'b0;

        neg = outW[15] == 1'b1 ? 1'b1: 1'b0;

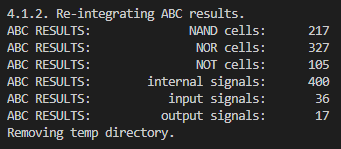
    end

endmodule

Then we synthesized the code using Yosys default cells, and the result is in below:



And then we used our own cells lib for our circuit.



Finally we wrote the Verilog description using Verilog and write a testbench for them.

`timescale 1ns/1ns

module tb();

    reg [15:0] aa, bb;

    reg [2:0] opc;

    reg cc;

    wire [15:0] ww, ww\_y;

    wire zer, neg, zer\_y, neg\_y;

    ALU alu(.inA(aa), .inB(bb), .inC(cc), .outW(ww), .opc(opc), .zer(zer), .neg(neg));

    ALU\_synth alu\_y(.inA(aa), .inB(bb), .inC(cc), .outW(ww\_y), .opc(opc), .zer(zer\_y), .neg(neg\_y));

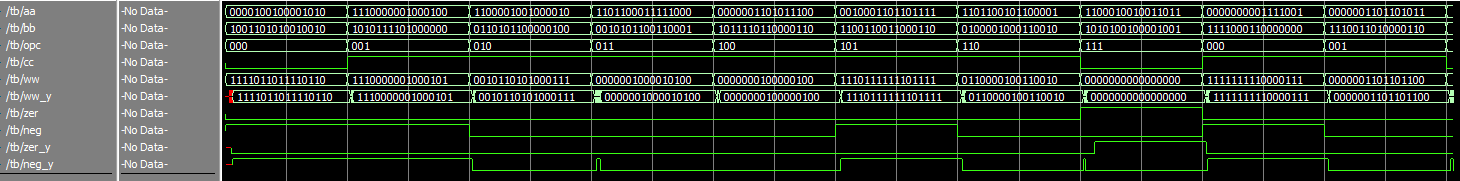
    initial opc = 3'b0;

    initial {aa, bb, cc} = $random;

    initial repeat (10) #1000 {aa, bb, cc} = $random;

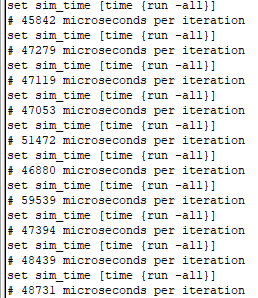
    initial repeat (10) #1000 opc = opc + 3'b001;

endmodule

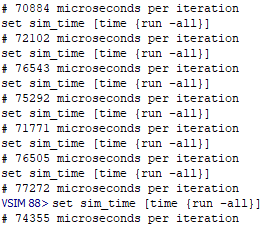
Here’s the wayform. 

We used this command “set sim\_time [time {run -all}]” at modelsim and compared the simulation speed of the two descriptions.

Our description:



Synthesized description:



Question 2:

