Task -2(i)

Team- 2

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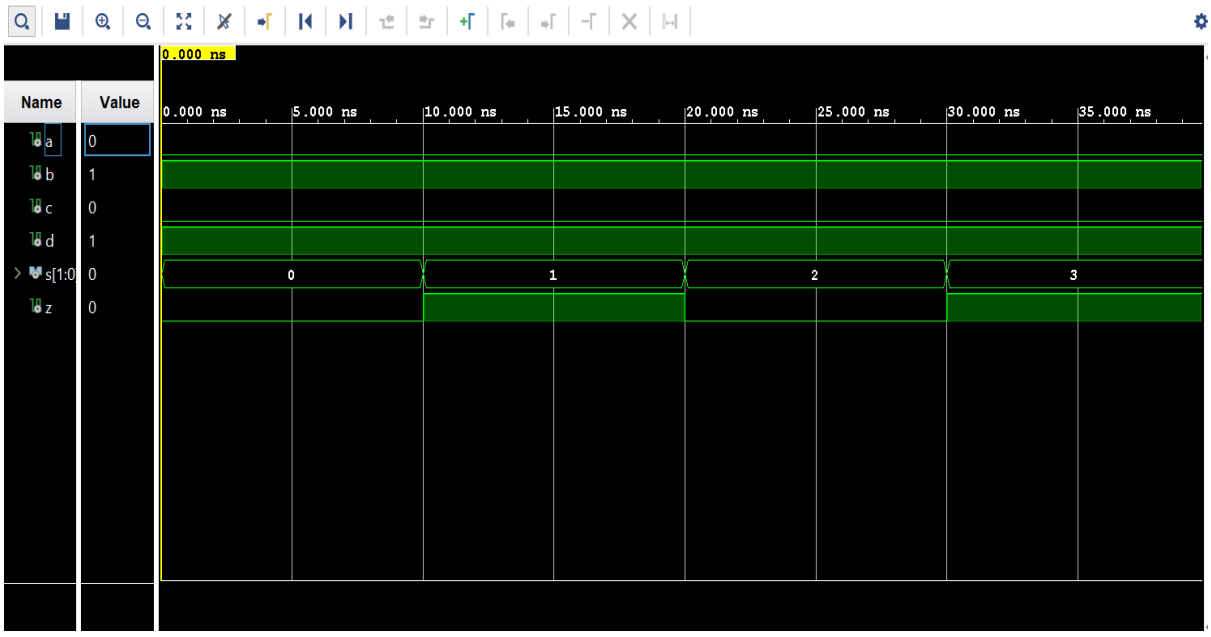
1. 4x1 MUX VHDL behavioural model

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity mux4_1 is
Port (a: in STD_logic;
b: in STD_logic;
c: in STD_logic;
d: in STD_logic;
s: in std_logic_vector (1 downto 0) ;
z: out STD_logic);

end mux4_1;
architecture Behavioral of mux4_1 is
begin
process (s)
begin

if( s <= "00") then
z <= a;
elsif( s <= "01") then
```

```
z <= b;
elsif( s <= "10") then
z <= c;
elsif( s <= "11") then
z <= d;
end if;
end process;
end Behavioral;
```



1. 4x1 MUX Verilog behavioural model

```
module mux4_1( OUT ,I0 ,I1, I2, I3, S0, S1 );
input I0, I1, I2, I3, S0, S1;
output reg OUT;

always @(*)
begin
 case({S1,S0})
 00: OUT = I0;
 01: OUT = I1;
 10: OUT = I2;
 11: OUT = I3;
 default : OUT = I0;
endcase
end
endmodule
```