

Team - 6

Ankush, Abhinay, Disha, Supriya, Madhulatha, Parikshit

Smart Actuators in Distributed Propulsion Systems

The IC Architecture referred in the article is: SOC

Aim :

The aim of this article is to present the development and validation of a high-temperature System on Chip (SOC) ASIC chipset designed for Smart Actuators in Distributed Propulsion Systems. The focus is on the transition from FPGA to ASIC to enhance reliability, modularity, and cost-effectiveness in aerospace control systems, under the Air Force SBIR contract by Embedded Systems LLC. The analog portion of the SOC chipset has been fabricated using high-temperature SOI (Silicon On Insulator) technology by Honeywell, while the digital portion is currently implemented in a commercial temperature FPGA and performs important computational functions for reconfiguring the SOC and executing complex control tasks. The risk reduction task focused on verifying and validating these key functions in a real environment before converting the design into an ASIC. The ultimate goal is to implement the complete SOC chipset in ASIC form for high-temperature applications.

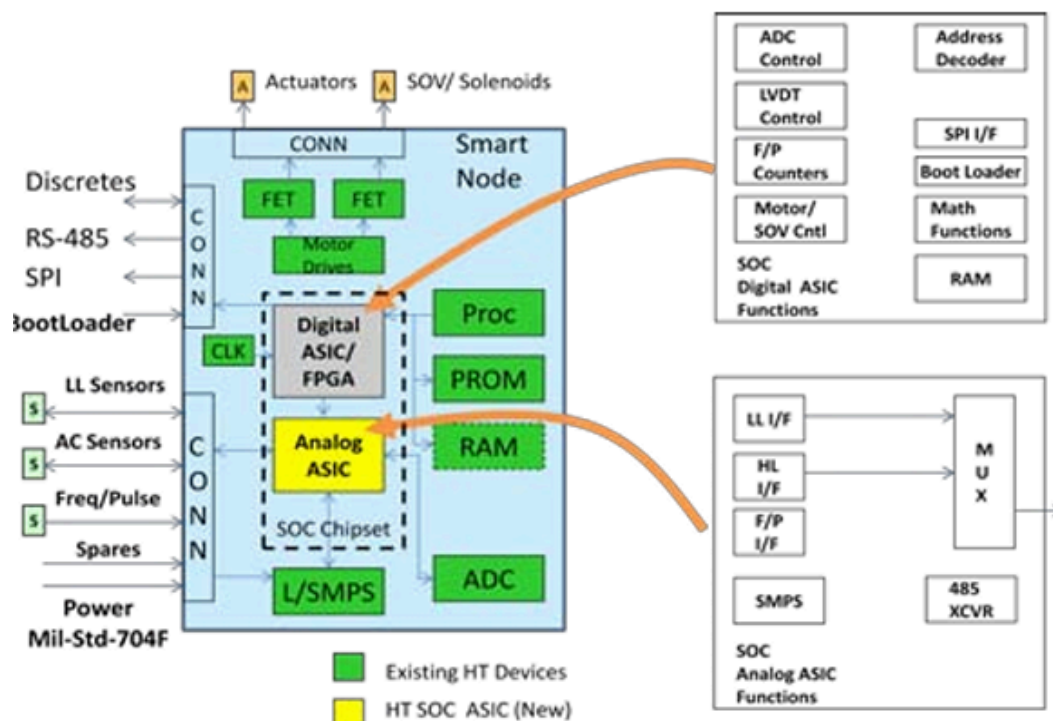


Fig. 1. Smart Node and SOC building block

Functional Description

The detailed process flow of the solution provided in the article involves several stages, from the initial design to the validation and implementation of the System On Chip (SOC) ASIC chipset for Smart Actuators in Distributed Propulsion Systems. Below is the step-by-step process flow:

1. Design and Development

Objective Definition: The project begins with defining the objective, which is to develop a hierarchical, distributed architecture for future propulsion FADEC systems with flexible, scalable, and reconfigurable Smart Nodes. **SOC Chipset Design:** Design the SOC chipset to include both analog and digital portions. The analog portion handles I/O interfaces for sensors and actuators, while the digital portion performs computational functions.

2. Fabrication of Analog SOC

High-Temperature SOI Technology: The analog portion of the SOC chipset is fabricated using high-temperature SOI technology by Honeywell. **Testing of Analog SOC:** The fabricated analog SOC undergoes thorough testing to ensure it operates correctly under high temperatures and interfaces properly with various sensors and actuators.

3. Implementation of Digital SOC in FPGA

FPGA Implementation: The digital portion of the SOC is initially implemented in a commercial temperature FPGA. This FPGA contains the computational functions needed for reconfiguring the SOC and performing complex control tasks. **Development of Control Functions:** Develop standalone control and math functions within the digital SOC to handle tasks such as actuator control, digital demodulation, PI control, and PWM generation.

4. Risk Reduction Testing

Setup: Use a high-performance, aerospace production-grade hydraulic actuator with dual redundant channels for testing. Integrate the SOC chipset with the actuator and a PAT (Production Acceptance Test) rig **Testing Steps:**

- **Calibration and Checkout:** Validate the setup by ensuring the PAT rig fully controls the actuator, calibrating tracking errors between LVDT channels, and checking signal connectivity.
- **Smart Node as Monitor:** Use the Smart Node to provide excitation to LVDT Channel B while the PAT rig closes the actuator loop with Channel A. Compare LVDT position readings from the PAT rig and Smart Node.
- **Smart Node in Control:** The Smart Node closes the actuator loop in real time using its own excitation and LVDT signals. Perform real-time control functions and generate the metering valve current command.
- **Transitions:** Command the actuator through discrete steps and alternate control between the PAT rig and Smart Node. Observe and analyze the transients and control performance.

5. Analysis of Results

Comparison of LVDT Readings: Analyze the LVDT tracking errors and compare the actuator position readings from the PAT rig and Smart Node. Performance Validation: Validate that the Smart Node can accurately control the actuator in real time without degrading performance compared to the PAT rig.

6. Conversion to ASIC

- Minimize Risks: Use the results from risk reduction testing to minimize risks associated with converting the FPGA-based digital SOC into an ASIC.
- Digital ASIC Implementation: Design and fabricate the digital portion of the SOC as an ASIC, incorporating all validated control and computational functions.

7. Final Testing and Validation

- Integration and Testing: Integrate the complete high-temperature SOC chipset (both analog and digital ASIC portions) and conduct comprehensive testing in a real environment.
- Operational Validation: Validate the SOC chipset's performance in distributed propulsion control systems, ensuring reliability, scalability, and reconfigurability.

8. Deployment

Production: Finalize the design for production and deploy the SOC chipset in various aerospace control systems, enhancing the modularity, reliability, and performance of FADEC systems.

Features of IC

Based on the information from the paper, the features of the System On Chip (SOC) ASIC chipset designed for Smart Actuators in Distributed Propulsion Systems include:

- High-Temperature SOI Technology: The analog portion of the SOC is fabricated using high-temperature Silicon On Insulator (SOI) technology, which ensures reliable operation in extreme temperature environments.
- Integrated Analog and Digital Functions: The SOC chipset combines both analog and digital functions in a single chip, facilitating compact and efficient design.
- Flexible and Scalable Architecture: The SOC is designed to be flexible and scalable, allowing it to be used in various configurations and applications within distributed propulsion systems.

- **Reconfigurability:** The SOC can be reconfigured to adapt to different control tasks and sensor/actuator interfaces, enhancing its versatility in different scenarios.
- **Standalone Control and Math Functions:** The digital portion of the SOC includes standalone control and math functions, such as actuator control, digital demodulation, Proportional-Integral (PI) control, and Pulse Width Modulation (PWM) generation.
- **FPGA Implementation for Risk Reduction:** Initially implemented in a commercial temperature FPGA for testing and validation, the digital SOC demonstrated its key functions before being converted to an ASIC.
- **Real-Time Actuator Control:** The SOC chipset can control actuators in real time, performing necessary computations and adjustments on-the-fly.
- **Dual Redundant Channels:** The SOC can interface with dual redundant LVDT (Linear Variable Differential Transformer) channels, ensuring reliable position sensing and control.
- **Excitation and Signal Processing:** Provides excitation to sensors (like LVDTs) and processes their signals for accurate control tasks.
- **Calibration and Tracking:** Capable of calibrating and tracking errors between redundant channels to maintain accuracy and reliability.
- **Modularity:** The SOC's modular design allows it to be integrated into various aerospace systems with minimal modifications.
- **Reduced Development Costs:** By using an FPGA for initial testing and validation, the development costs and risks associated with designing the ASIC are significantly reduced.
- **Production-Grade Testing:** The SOC has been tested in a high-performance aerospace production environment, ensuring its readiness for deployment in real-world applications.
- **Enhanced Reliability:** The design and testing processes ensure that the SOC chipset offers high reliability for critical aerospace control systems.

Mapping between IC, its features using EDA

Types	Features	EDA tools
FPGA	Reconfigurability, Rapid Prototyping, parallel processing	Schematic capture: Cadence virtuoso
	High-Speed I/O, Scalability	HDL Entry: VHDL/VERILOG
		Simulation: ModelSim, Xilinx Vivado
		Place and Route: Xilinx Vivado, Intel Quartus
ASIC	Custom Design, High Efficiency, Compact Size	Logic Synthesis: Synopsys Design Compiler
	High Reliability, Cost-Effective at Scale	Place and Route: Cadence Innovus, Synopsys IC Compiler
		Formal Verification: Cadence JasperGold
		Timing Analysis: Synopsys Prime Time
SOC	Integration, Versatility, Reconfigurability	High-Level Synthesis: Cadence Stratus
	Scalability, High Performance	Power Analysis : Cadence Voltus
		DFT : Mentor Tessent
		Fabrication: Cadence Virtuoso Layout Suite