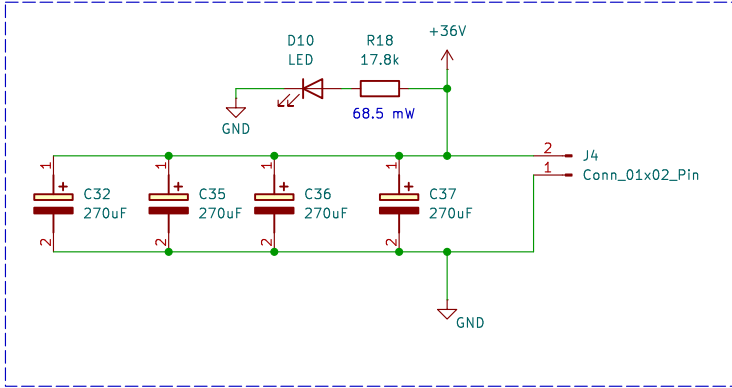
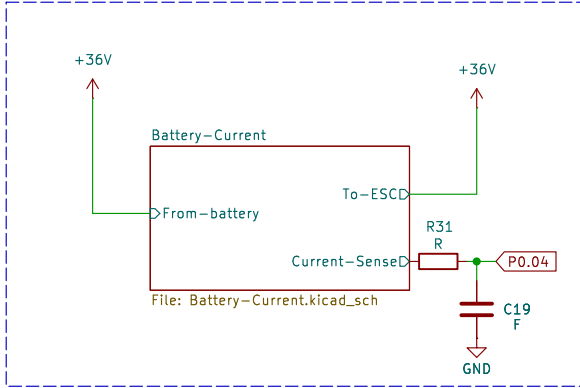


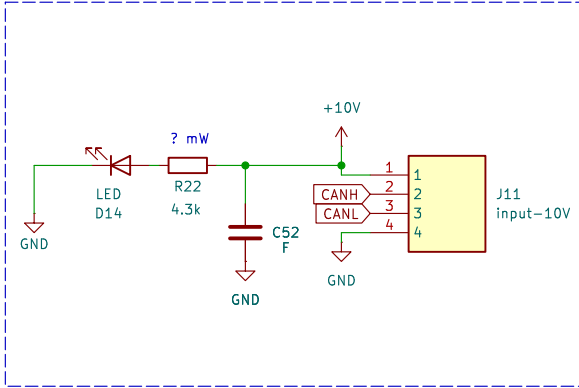
Battery input



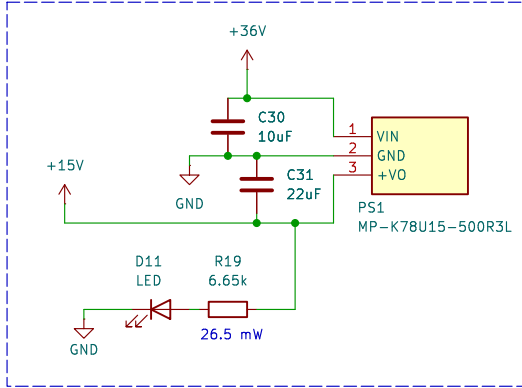
36 V Current measurement



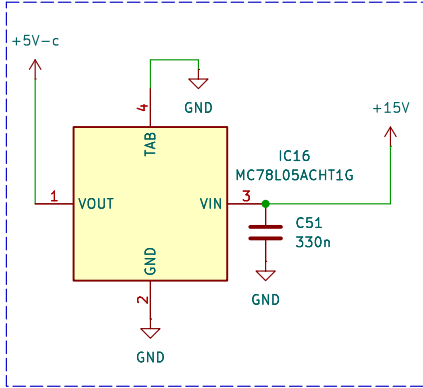
10 V and CAN Input



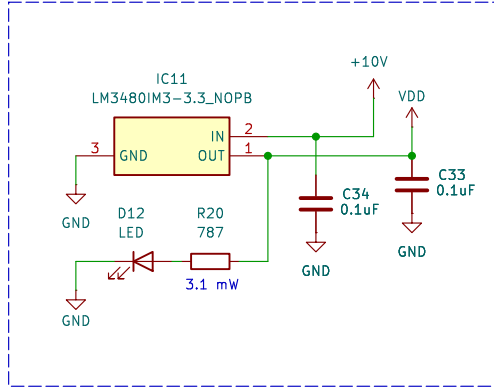
15 V regulator



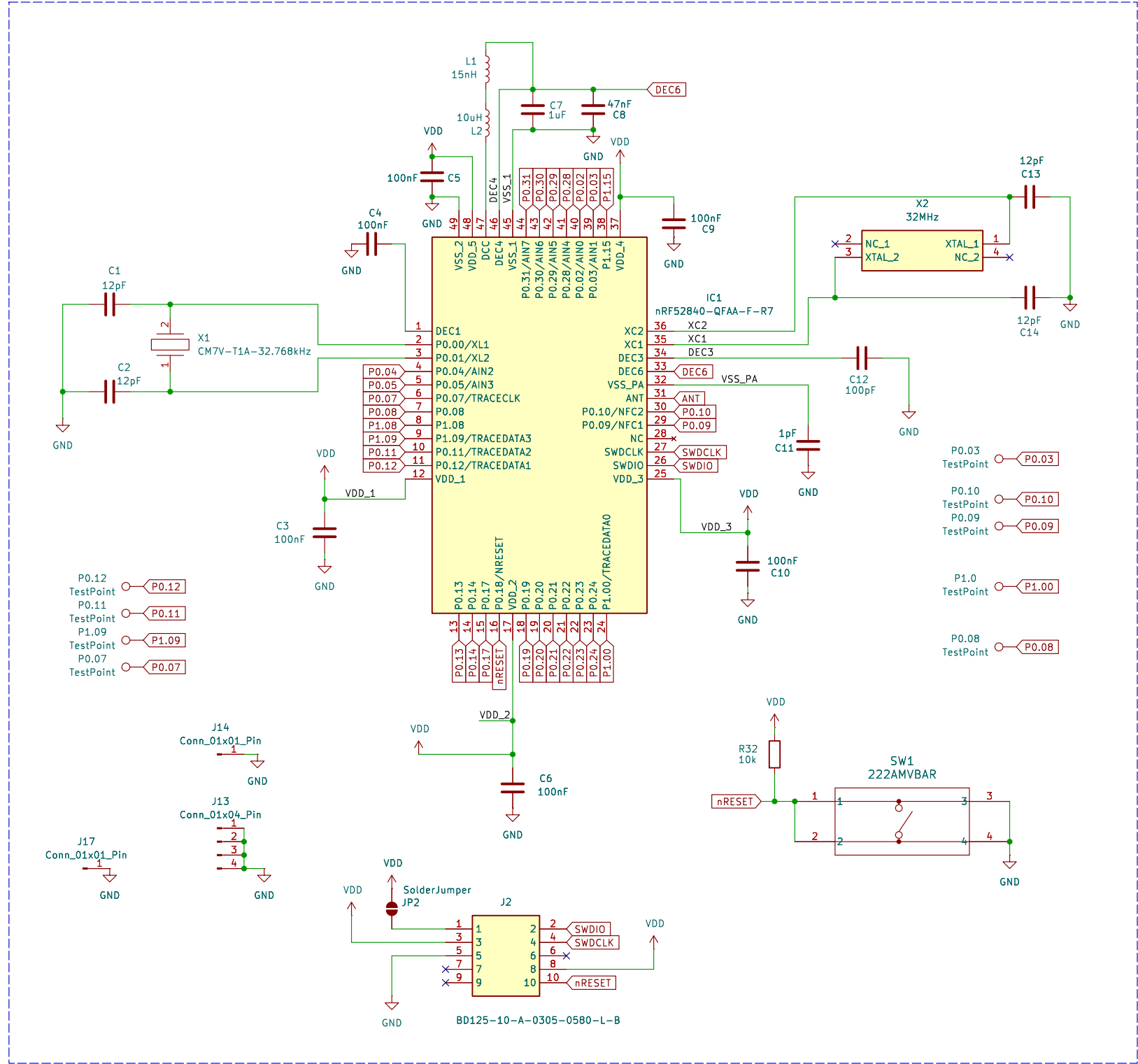
5 V regulator



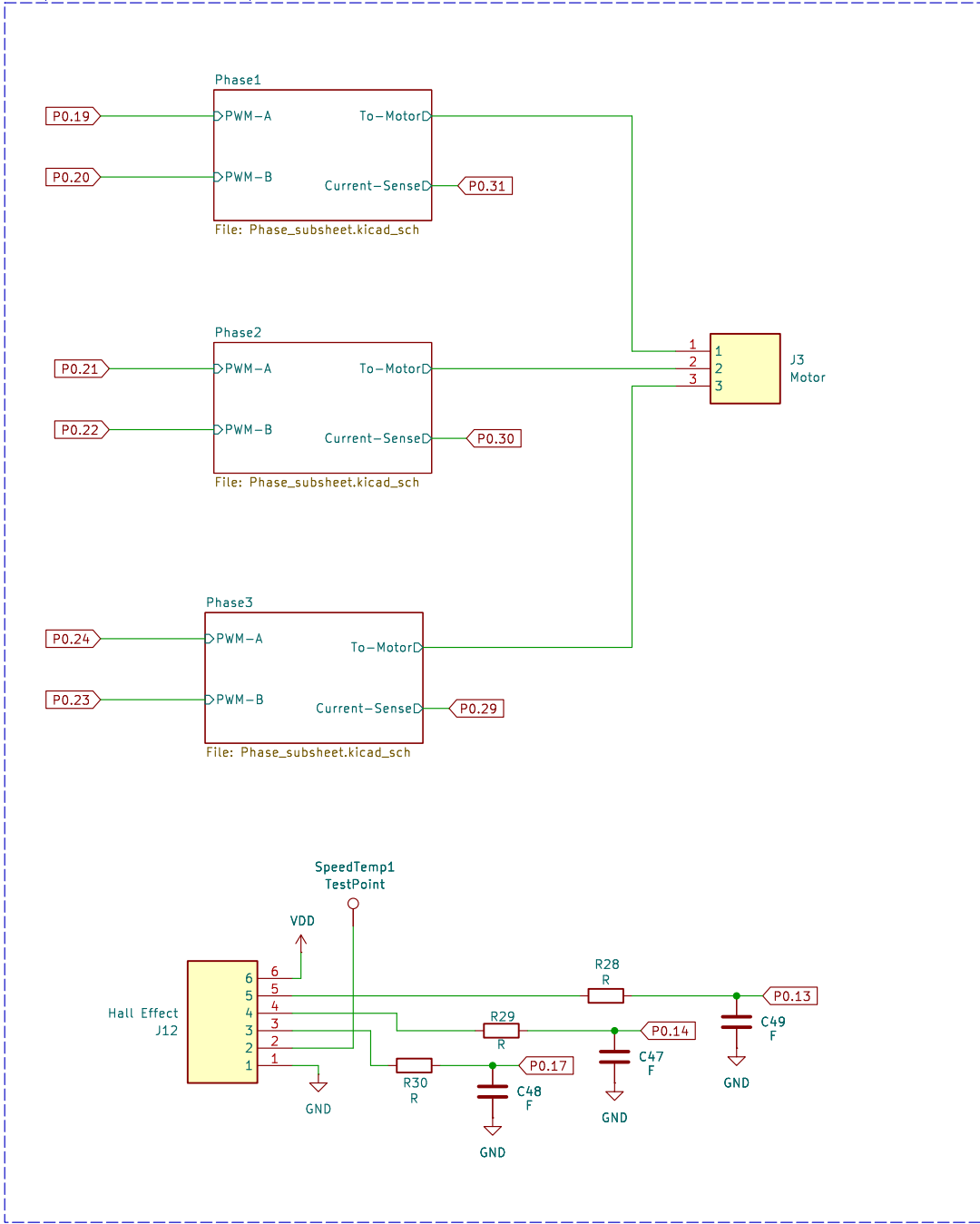
3.3 V regulator nRF



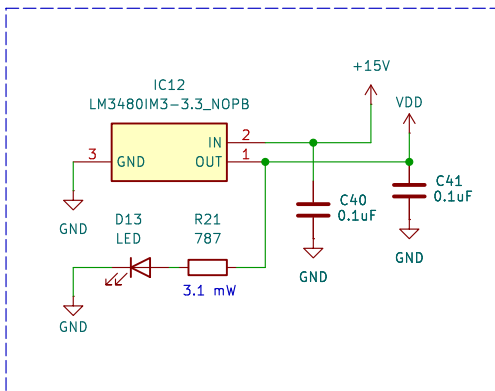
nRF52840 Circuit



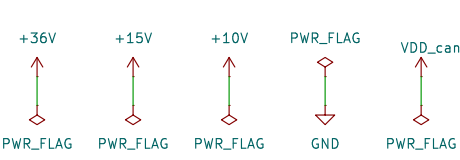
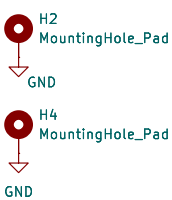
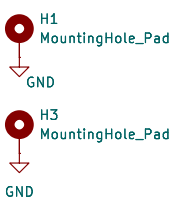
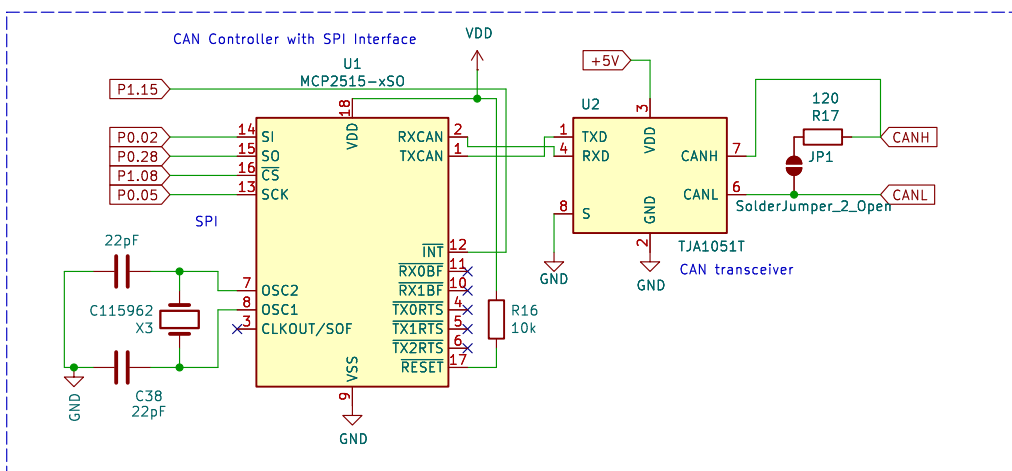
Input/Output to the motor



3.3 V regulator Drivers



CAN-module



8.2.2.7.3 Select a VDDB Capacitor  
 ChaneL B has the same current requirements as Channel A. Therefore, a VDDB capacitor (shown as CVDD in Figure 8–1) is needed. In this example with a bootstrap configuration, the VDDB capacitor will also supply current for VDDA through the bootstrap diode. A 50–V, 10– $\mu$ F MLCC and a 50–V, 220–nF MLCC are chosen for CVDD. If the bias power supply output is a relatively long distance from the VDDB pin, a tantalum or electrolytic capacitor, with a value over 10  $\mu$ F, should be used in parallel with CVDD.

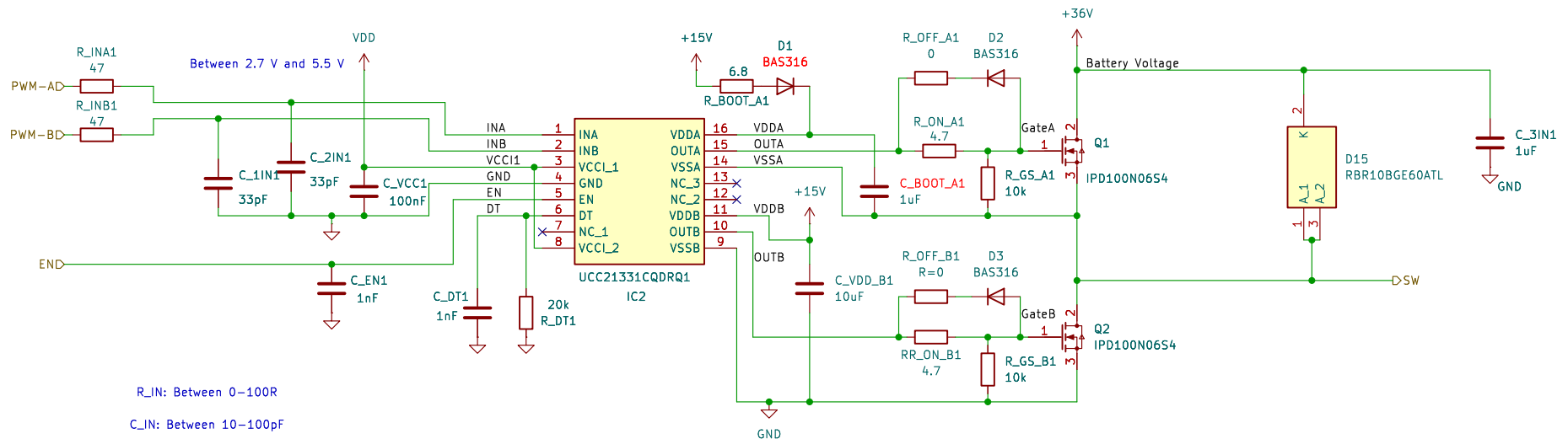
R<sub>GS</sub>: 5.1k – 20k  
 R<sub>GS</sub> = 10K

R<sub>ON</sub> High: 5R, Page 8  
 R<sub>ON</sub> = 4.7

R<sub>BOOT</sub>: 1–20R, Page 25

R<sub>BOOT</sub> = 6.8 Ohm

C<sub>BOOT</sub>: 1.1– $\mu$ F capacitance from VDDA and VDDB to VSSA and VSSB  
 Page 8



R<sub>IN</sub>: Between 0–100R

C<sub>IN</sub>: Between 10–100pF

It is recommended to use an RC filter on EN pin to filter high frequency noise, with R = 0  $\Omega$  to 100  $\Omega$  and C = 100 pF to 1000 pF

C<sub>VDD</sub>: Low-ESR and low-ESL capacitors must be connected close to the device between the VCCI and GND pins and between the VDD and VSS pins to support high peak currents when turning on the external power transistor

R<sub>DT</sub>, C<sub>DT</sub>: It is recommended to place the dead-time setting resistor, RDT, and its bypassing capacitor close to DT pin of the UCC21331.

C<sub>VCC</sub>: Similarly, a bypass capacitor should also be placed between the VCCI and GND pins. Given the small amount of current drawn by the logic circuitry within the input side of the UCC21331, this bypass capacitor has a minimum recommended value of 100 nF.

C<sub>EN</sub>: It is recommended to bypass using a  $\approx$ 1nF low ESR/ESL capacitor, CEN, close to EN pin when connecting to a  $\mu$ C with distance

Red text on component name means high current path

Pay attention to high current path that includes the bootstrap capacitor, bootstrap diode, local VSSB-referenced bypass capacitor, and the low-side transistor body/anti-parallel diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode by the VDD bypass capacitor. This recharging occurs in a short time interval and involves a high peak current. Minimizing this loop length and area on the circuit board is important for ensuring reliable operation.

The gate driver must be placed as close as possible to the transistors.

Sheet: /Phase1/Driver\_subsheet\_1/  
 File: Driver\_subsheet.kicad\_sch

**Title:**

Size: A4

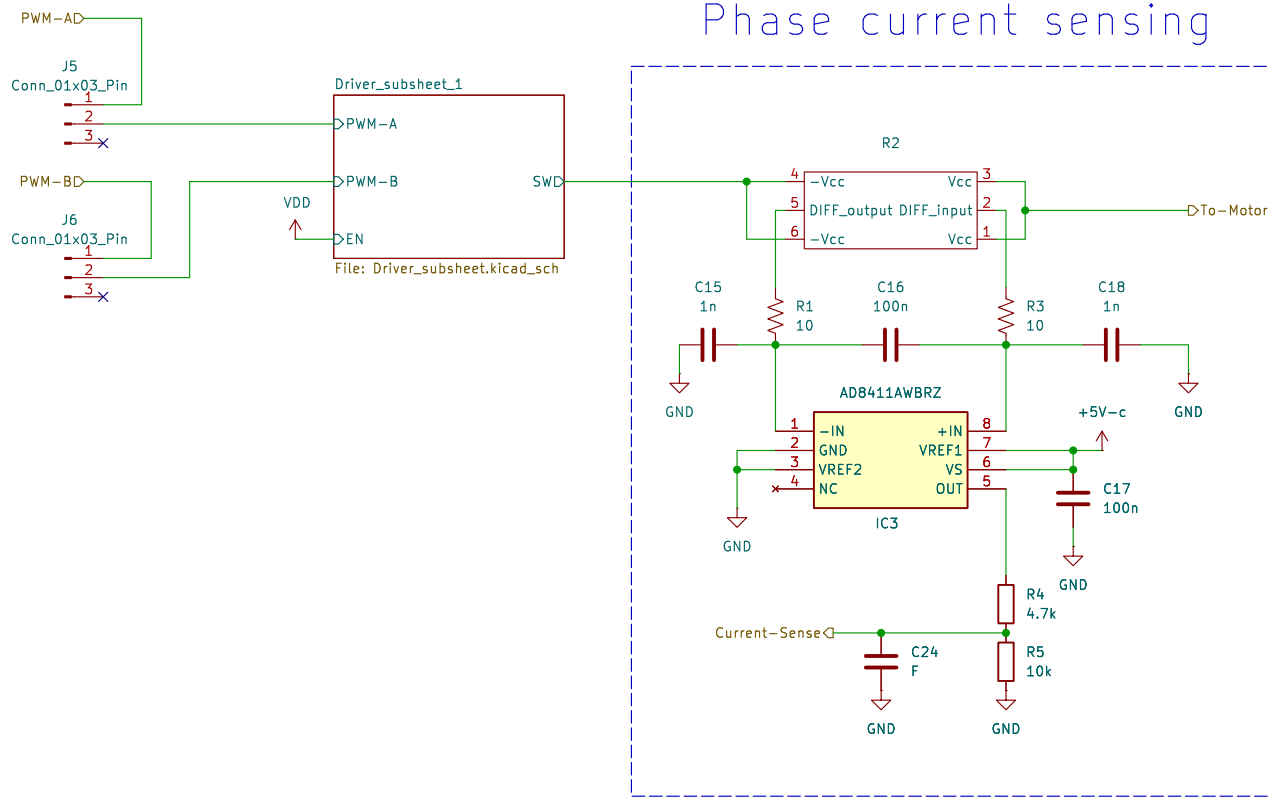
Date:

KiCad E.D.A. 8.0.5

**Rev:**

Id: 2/8

Phase current sensing



Sheet: /Phase1/  
File: Phase\_subsheet.kicad\_sch

Title:

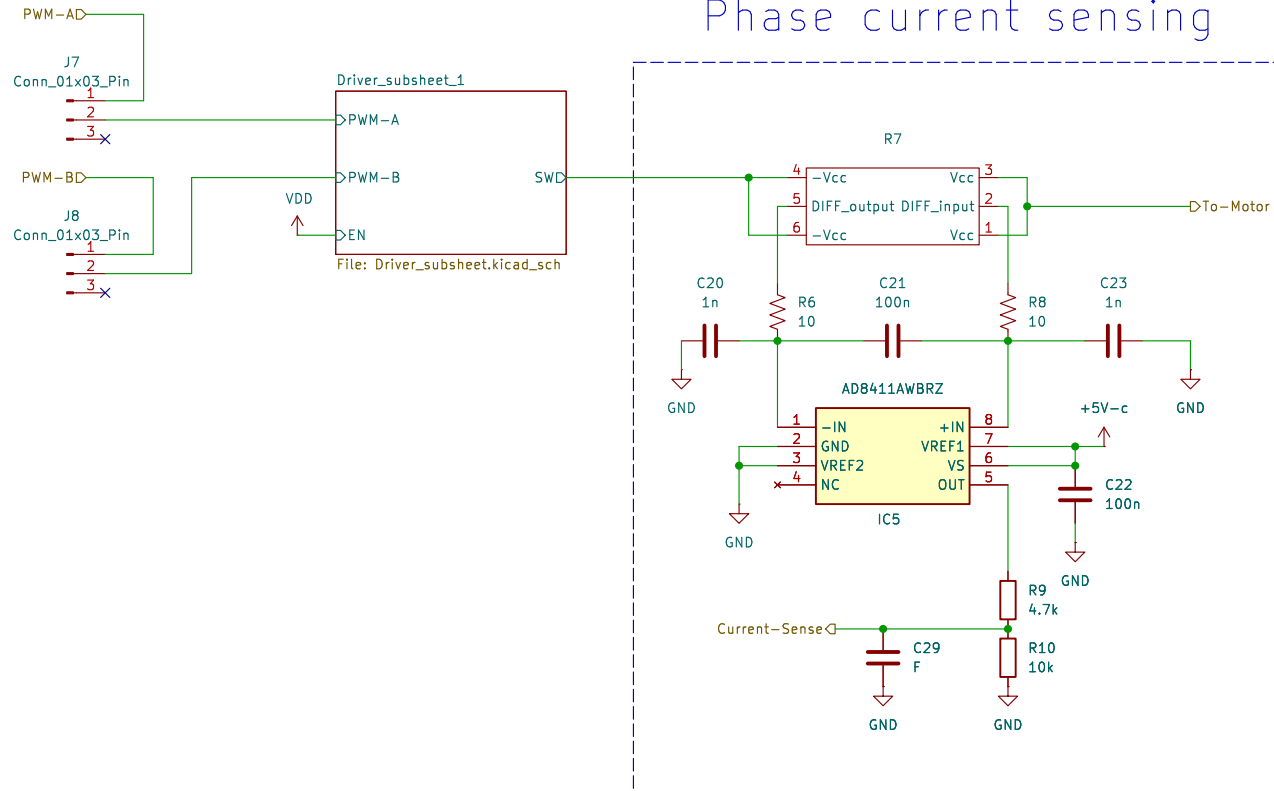
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KiCad E.D.A. 8.0.5

Date:

Rev:

Id: 3/8

## Phase current sensing



Sheet: /Phase2/  
File: Phase\_subsheet.kicad\_sch

### Title:

Size: A4 Date:

KiCad E.D.A. 8.0.5

Rev:

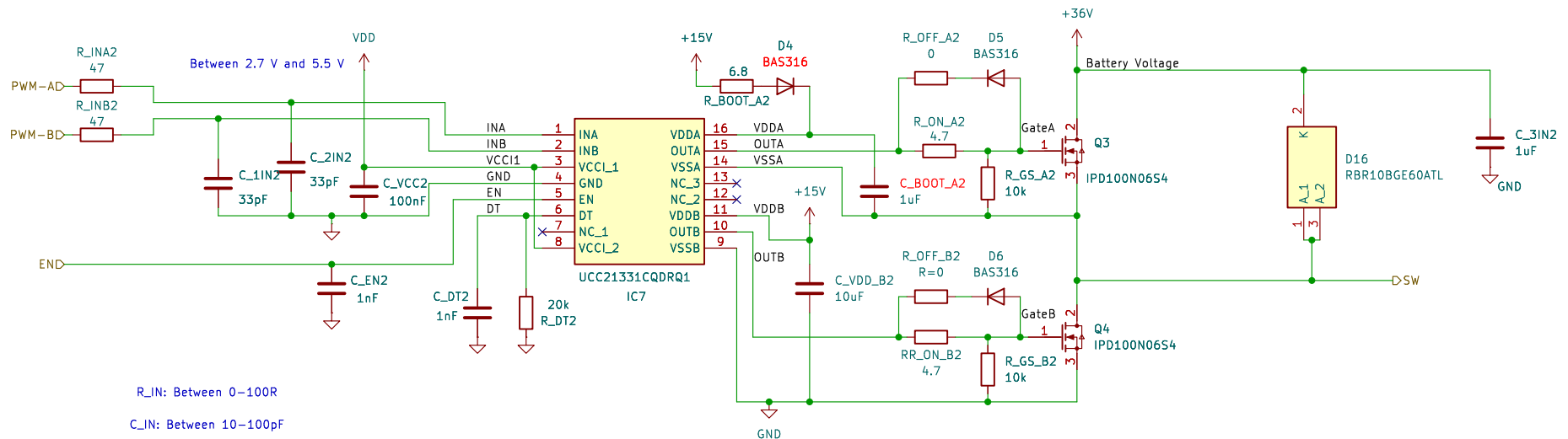
Id: 4/8

8.2.2.7.3 Select a VDDB Capacitor  
Chanel B has the same current requirements as Channel A. Therefore, a VDDB capacitor (shown as CVDD in Figure 8-1) is needed. In this example with a bootstrap configuration, the VDDB capacitor will also supply current for VDDA through the bootstrap diode. A 50-V, 10-μF MLCC and a 50-V, 220-nF MLCC are chosen for CVDD. If the bias power supply output is a relatively long distance from the VDDB pin, a tantalum or electrolytic capacitor, with a value over 10 μF, should be used in parallel with CVDD.

R<sub>GS</sub>: 5.1k – 20k  
R<sub>GS</sub> = 10K

R<sub>ON</sub> High: 5R, Page 8  
R<sub>ON</sub> = 4.7

R<sub>BOOT</sub>: 1–20R, Page 25  
R<sub>BOOT</sub> = 6.8 Ohm C<sub>BOOT</sub>: 1.1–μF capacitance from VDDA and VDDB to VSSA and VSSB  
Page 8



R<sub>IN</sub>: Between 0–100R

C<sub>IN</sub>: Between 10–100pF

It is recommended to use an RC filter on EN pin to filter high frequency noise, with R = 0 Ω to 100 Ω and C = 100 pF to 1000 pF

C<sub>VDD</sub>: Low-ESR and low-ESL capacitors must be connected close to the device between the VCCI and GND pins and between the VDD and VSS pins to support high peak currents when turning on the external power transistor

R<sub>DT</sub>, C<sub>DT</sub>: It is recommended to place the dead-time setting resistor, RDT, and its bypassing capacitor close to DT pin of the UCC21331.

C<sub>VCC</sub>: Similarly, a bypass capacitor should also be placed between the VCCI and GND pins. Given the small amount of current drawn by the logic circuitry within the input side of the UCC21331, this bypass capacitor has a minimum recommended value of 100 nF.

C<sub>EN</sub>: It is recommended to bypass using a ≈1nF low ESR/ESL capacitor, CEN, close to EN pin when connecting to a μC with distance

Red text on component name means high current path

Pay attention to high current path that includes the bootstrap capacitor, bootstrap diode, local VSSB-referenced bypass capacitor, and the low-side transistor body/anti-parallel diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode by the VDD bypass capacitor. This recharging occurs in a short time interval and involves a high peak current. Minimizing this loop length and area on the circuit board is important for ensuring reliable operation.

The gate driver must be placed as close as possible to the transistors.

Sheet: /Phase2/Driver\_subsheet\_1/  
File: Driver\_subsheet.kicad\_sch

Title:

Size: A4

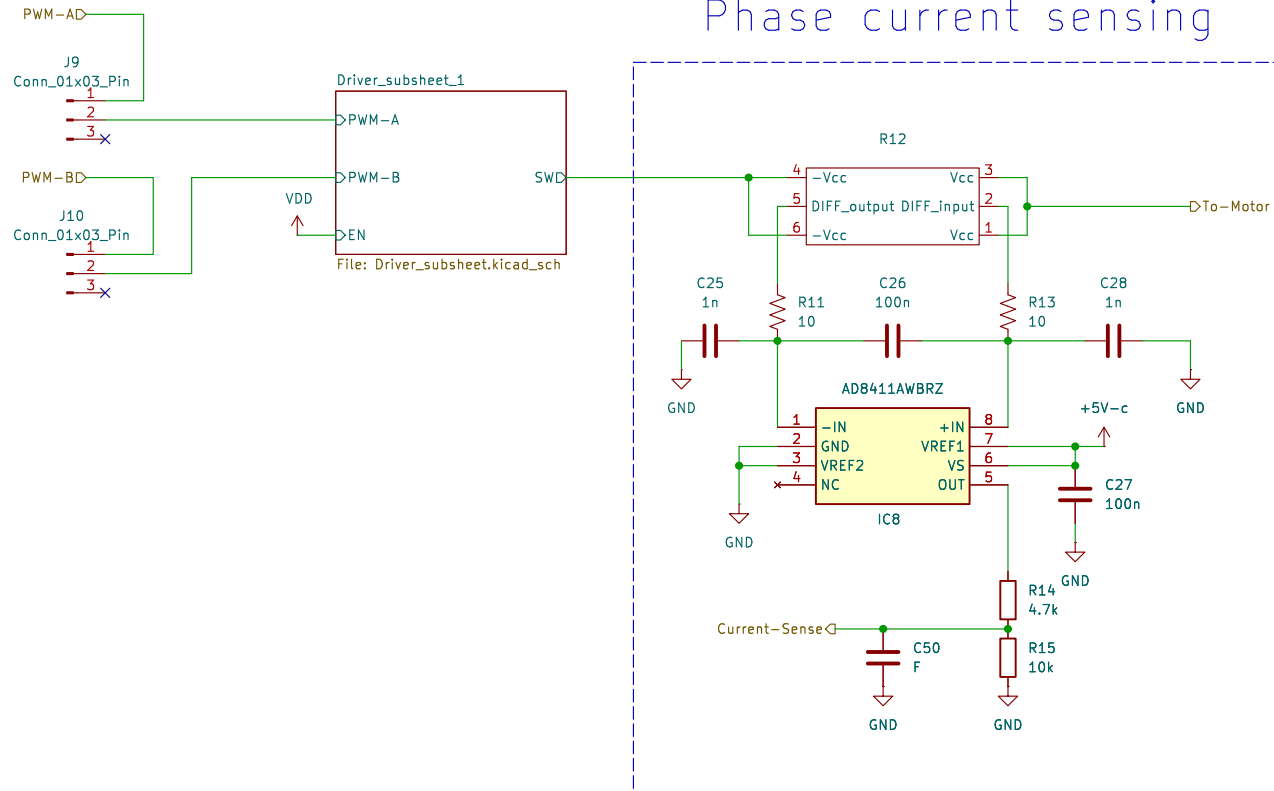
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KiCad E.D.A. 8.0.5

Rev:

Id: 5/8

# Phase current sensing



Sheet: /Phase3/  
File: Phase\_subsheet.kicad\_sch

## Title:

Size: A4  
KiCad E.D.A. 8.0.5

Date:

Rev:  
Id: 6/8

#### 8.2.2.7.3 Select a VDDDB Capacitor

R\_ON High: 5R. Page 8  
R\_ON = 4.7

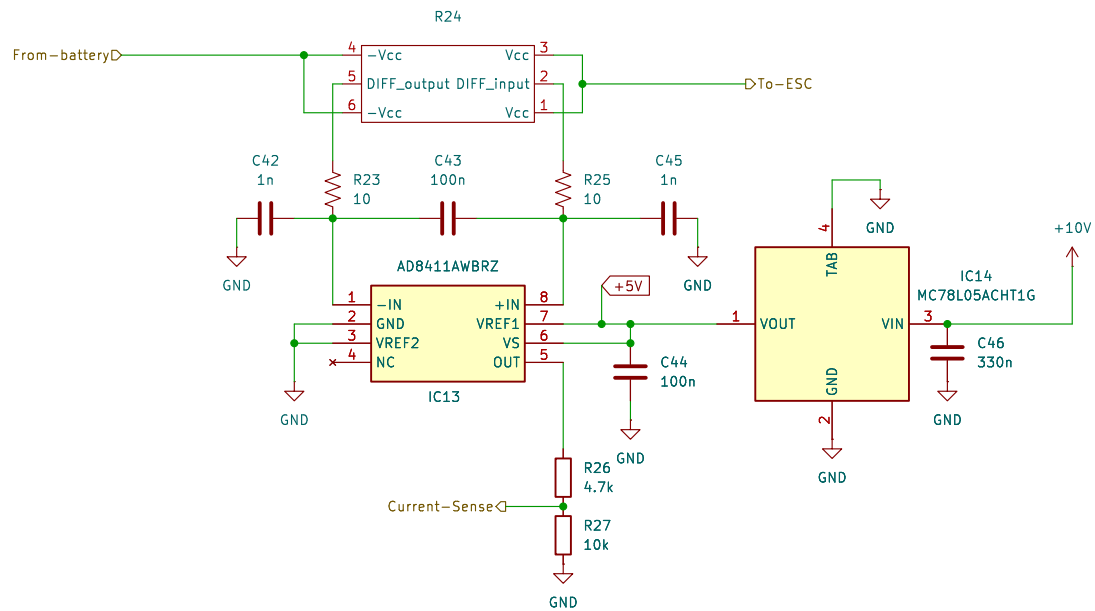
$$R_{BOOT} = 6.8 \text{ Ohm}$$

Page 8



The gate driver must be placed as close as possible to the transistors.

Sheet: /Phase3/Driver_subsheet_1/		D
File: Driver_subsheet.kicad_sch		
<b>Title:</b>		
Size: A4	Date:	<b>Rev:</b>
KiCad E.D.A. 8.0.5		Id: 7/8



AD8411AWBRZ:SOIC127P600X175-8N

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**Title:**

Size: A4

Date:

KiCad E.D.A. 8.0.5

**Rev:**

Id: 8/8