11 JTAG (IEEE 1149.1) Test Access Port

11.1 INTRODUCTION

The DSP56300 Core provides a dedicated user-accessible test access port (TAP) that is fully compatible with the IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture. Problems associated with testing high density circuit boards have led to development of this proposed standard under the sponsorship of the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The DSP56300 Core implementation supports circuit-board test strategies based on this standard.

The test logic includes a test access port (TAP) consisting of four dedicated signal pins, a 16-state controller, and three test data registers. A boundary scan register links all device signal pins into a single shift register. The test logic, implemented utilizing static logic design, is independent of the device system logic. The DSP56300 Core implementation provides the following capabilities:

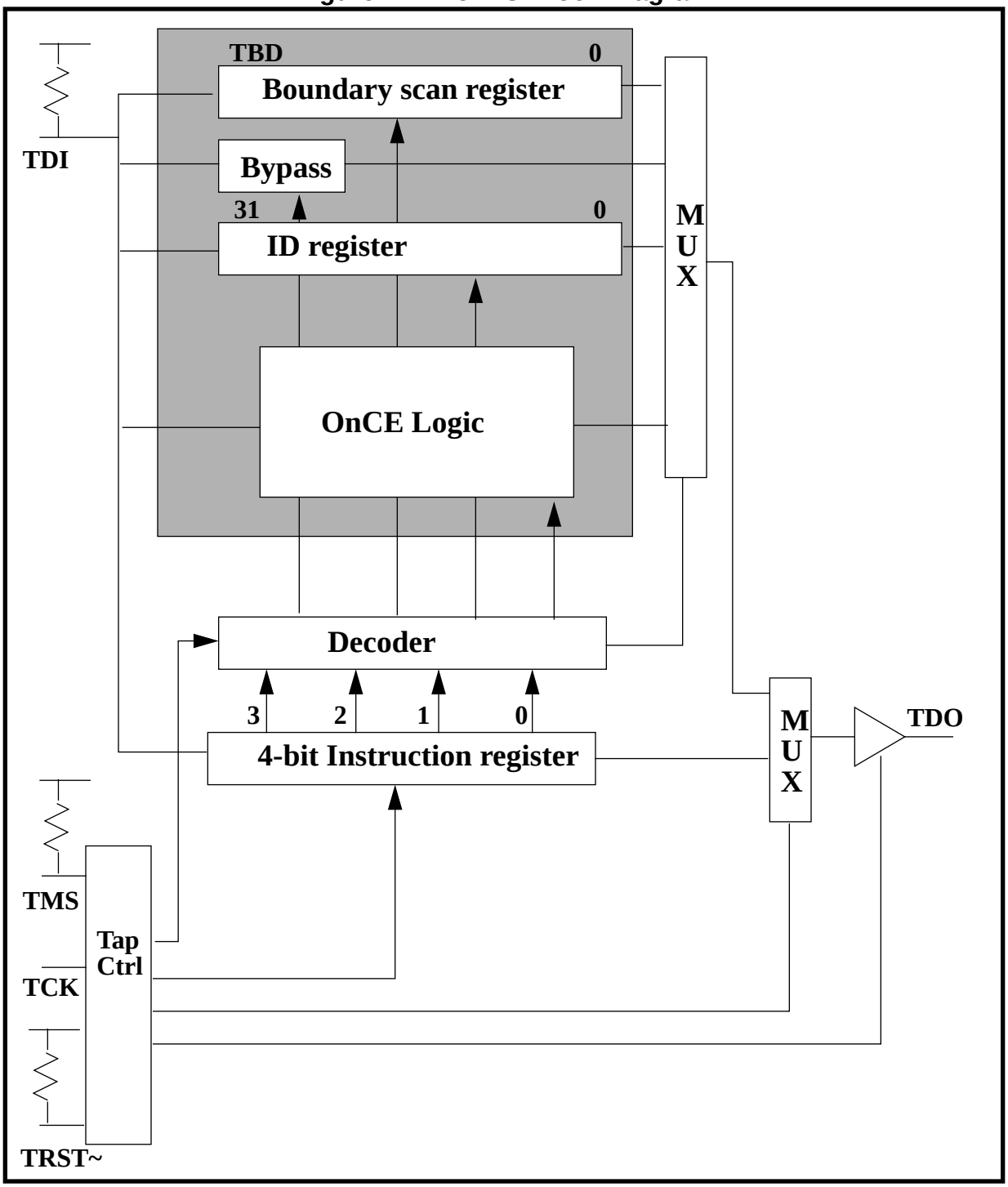
1. Perform boundary scan operations to test circuit-board electrical continuity (EXTEST).
2. Bypass the DSP56300 Core for a given circuit-board test by effectively reducing the boundary scan register to a single cell (BYPASS).
3. Sample the DSP56300 Core based device system pins during operation and transparently shift out the result in the boundary scan register. Preload values to output pins prior to invoking the EXTEST instruction (SAMPLE/PRELOAD).
4. Disable the output drive to pins during circuit-board testing (HIGHZ).
5. Provide a means of accessing the OnCE controller and circuits to control a target system (ENABLE_ONCE).
6. Provide a means of entering the Debug Mode of operation (DEBUG_REQUEST).
7. Query identification information (manufacturer, part number and version) from an DSP56300 Core based device (IDCODE).
8. Force test data onto the outputs of an DSP56300 Core based device while replacing its boundary-scan register in the serial data path with a single bit register (CLAMP).

11.2 OVERVIEW

This section, which includes aspects of the JTAG implementation that are specific to the

DSP56300 Core, is intended to be used with the supporting IEEE 1149.1 document. The discussion includes those items required by the standard to be defined and, in certain cases, provides additional information specific to the DSP56300 Core implementation. For internal details and applications of the standard, refer to the IEEE 1149.1 document. The block diagram of the DSP56300 Core implementation of JTAG is shown in Figure 11-1.

Figure 11-1. JTAG Block Diagram



The DSP56300 Core implementation includes a 4-bit instruction register and three test registers: a 1-bit bypass register, a 32-bit identification register and a TBD-bit boundary scan register. This implementation includes a dedicated TAP and four pins.

11.2.1 JTAG PINS

11.2.1.1 Test Clock (TCK)

The test clock input (TCK) pin is used to synchronize the test logic.

11.2.1.2 Test Mode Select (TMS)

The test mode select input (TMS) pin is used to sequence the test controller's state machine. The TMS is sampled on the rising edge of TCK and it has an internal pullup resistor.

11.2.1.3 Test Data Input (TDI)

Serial test instruction and data are received through the test data input (TDI) pin. TDI is sampled on the rising edge of TCK and it has an internal pullup resistor.

11.2.1.4 Test Data Output (TDO)

The test data output TDO pin is the serial output for test instructions and data. TDO is three-stateable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK.

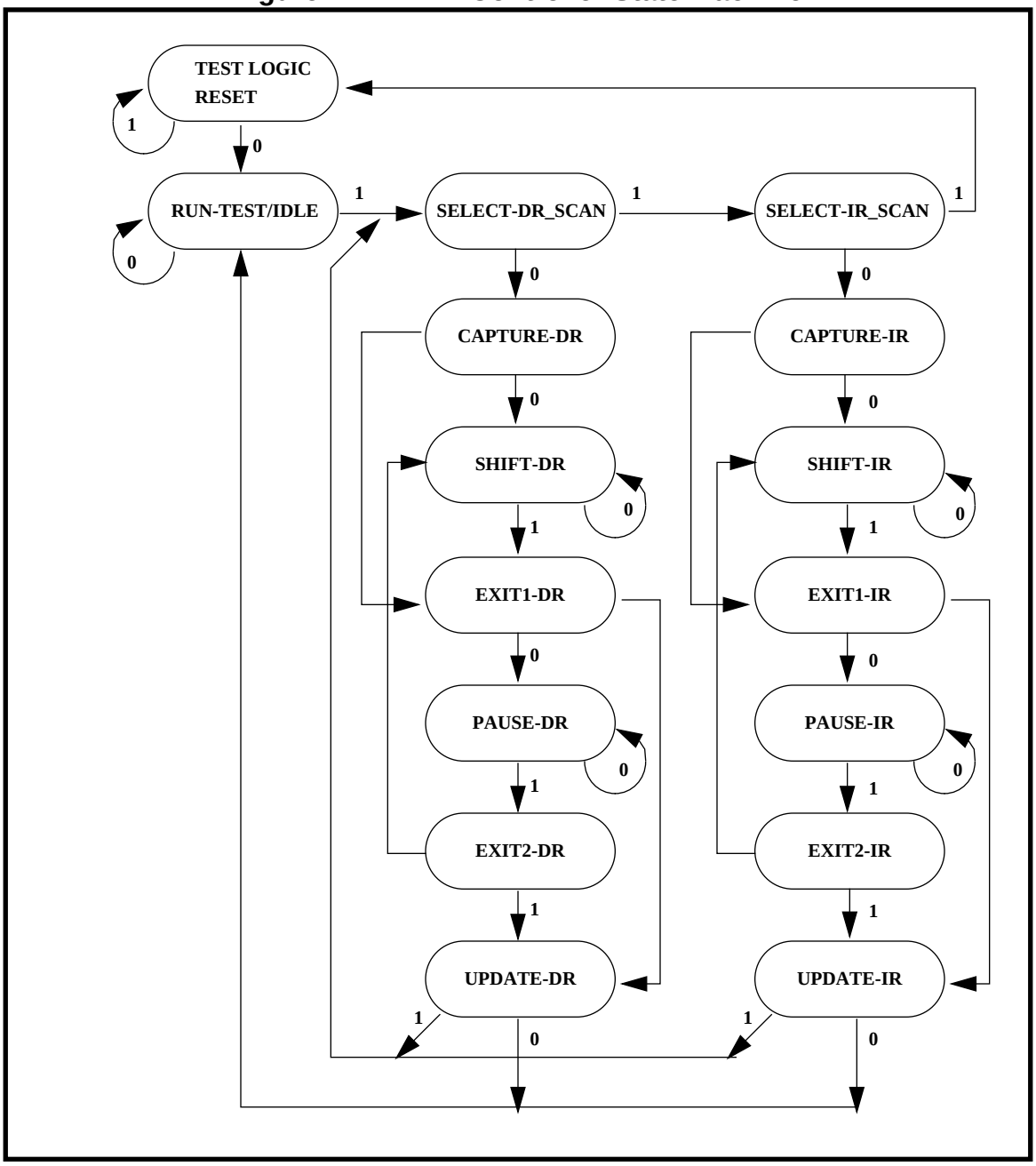
11.2.1.5 Test Reset (TRST~)

The test reset input (TRST~) pin is used to asynchronously initialize the test controller.The TRST~ has an internal pullup resistor.

11.2.2 TAP CONTROLLER

The TAP controller is responsible for interpreting the sequence of logical values on the TMS signal. It is a synchronous state machine that controls the operation of the JTAG logic. The state machine is shown in Figure . The value shown adjacent to each arc represents the value of the TMS signal sampled on the rising edge of TCK signal. For a description of the TAP controller states, please refer to the IEEE 1149.1 document.

Figure 11-2. TAP Controller State Machine



11.2.3 BOUNDARY SCAN REGISTER

The boundary scan register (BSR) in the DSP56300 Core JTAG implementation contains bits for all device signal and clock pins and associated control signals. All DSP56300 Core bidirectional pins have a single register bit in the boundary scan register for pin data, and are controlled by an associated control bit in the boundary scan register.

The boundary scan bit definitions varies according to the specific chip implementation of the DSP56300 core and is described in it's specification document.

11.2.4 INSTRUCTION REGISTER

The DSP56300 Core JTAG implementation includes the three mandatory public instructions (EXTEST, SAMPLE/PRELOAD, and BYPASS), and also supports the optional CLAMP instruction defined by IEEE 1149.1. The public instruction (HI-Z) provides the capability for disabling all device output drivers. The public instruction (ENABLE_ONCE) enables the JTAG port to communicate with the OnCE circuitry. The public instruction (DEBUG_REQUEST) enables the JTAG port to force the DSP56300 Core into the Debug Mode of operation. The DSP56300 Core includes a 4-bit instruction register without parity consisting of a shift register with four parallel outputs. Data is transferred from the shift register to the parallel outputs during the update-IR controller state. The four bits are used to decode the eight unique instructions shown in Table 11-1. All other encodings are reserved for future enhancements and will be decoded as BYPASS.

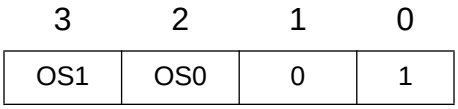
Table 11-1. JTAG Instructions

Code				Instruction
B3	B2	B1	B0	
0	0	0	0	EXTEST
0	0	0	1	SAMPLE/PRELOAD
0	0	1	0	IDCODE
0	0	1	1	CLAMP
0	1	0	0	HI-Z
0	1	0	1	RESERVED
0	1	1	0	ENABLE_ONCE
0	1	1	1	DEBUG_REQUEST
1	x	x	x	BYPASS

The parallel output of the instruction register is reset to 0010 in the test-logic-reset controller state which is equivalent to the IDCODE instruction.

During the capture-IR controller state, the parallel inputs to the instruction shift register are loaded with the code 01 in the least significant bits as required by the standard. The two most significant bits are loaded with the values of the core status bits OS1 and OS0 from the OnCE controller. See Chapter 10 ON-CHIP EMULATOR (OnCE™) for a description of the status bits. Figure 11-3 shows the Instruction Register configuration.

Figure 11-3. Instruction Register



11.2.4.1 EXTEST

The external test (EXTEST) instruction selects the TBD-bit boundary scan register. EXTEST also asserts internal reset for the DSP56300 Core system logic to force a predictable internal state while performing external boundary scan operations.

By using the TAP, the register is capable of:

1. scanning user-defined values into the output buffers,
2. capturing values presented to input pins
3. controlling the direction of bidirectional pins,
4. controlling the output drive of three-stateable output pins.

For more details on the function and use of EXTEST, please refer to the IEEE 1149.1 document.

11.2.4.2 SAMPLE/PRELOAD

The SAMPLE/PRELOAD instruction provides two separate functions. First, it provides a means to obtain a snapshot of system data and control signals. The snapshot occurs on the rising edge of TCK in the capture-DR controller state. The data can be observed by shifting it transparently through the boundary scan register.

Note: Since there is no internal synchronization between the JTAG clock (TCK) and the system clock (CLK), the user must provide some form of external synchronization to achieve meaningful results.

The second function of SAMPLE/PRELOAD is to initialize the boundary scan register output cells prior to selection of EXTEST. This initialization ensures that known data will appear on the outputs when entering the EXTEST instruction.

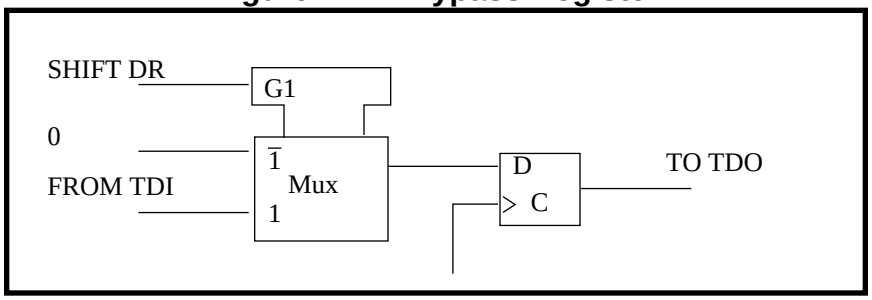
11.2.4.3 BYPASS

The BYPASS instruction selects the single-bit bypass register as shown in Figure 11-4. This creates a shift-register path from TDI to the bypass register and, finally, to TDO, circumventing the TBD-bit boundary scan register. This instruction is used to enhance test efficiency when a component other than the DSP56300 Core based device becomes the device under test.

When the bypass register is selected by the current instruction, the shift-register stage is set to a logic zero on the rising edge of TCK in the capture-DR controller state. Therefore,

the first bit to be shifted out after selecting the bypass register will always be a logic zero.

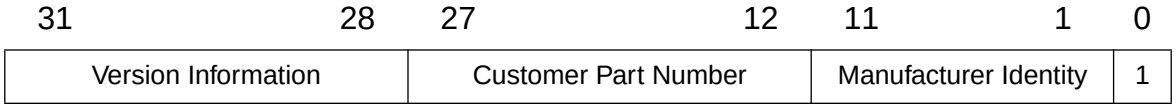
Figure 11-4. Bypass Register



11.2.4.4 IDCODE

The IDCODE instruction selects the ID register. This instruction is provided as a public instruction to allow the manufacturer, part number and version of a component to be determined through the TAP. Figure 11-3 shows the ID register configuration.

Figure 11-5. Identification Register Configuration



One application of the ID register is to distinguish the manufacturer(s) of components on a board when multiple sourcing is used. As more components emerge which conform to the IEEE 1149.1 standard, it is desirable to allow for a system diagnostic controller unit to blindly interrogate a board design in order to determine the type of each component in each location. This information is also available for factory process monitoring and for failure mode analysis of assembled boards.

Motorola's Manufacturer Identity is 00000001110. The Customer Part Number consists of two parts: Motorola Design Center Number (bits 27:22) and a sequence number (bits 21:12). MSIL Design Center Number is 000110.

Once the IDCODE instruction is decoded, it will select the ID register which is a 32-bit data register. Since the bypass register loads a logic 0 at the start of a scan cycle, whereas the ID register loads a logic 1 into its least significant bit, examination of the first bit of data shifted out of a component during a test data scan sequence immediate following exit from Test-Logic-Reset controller state will show whether such a register is included in the design. When the IDCODE instruction is selected, the operation of the test logic shall have no effect on the operation of the on-chip system logic as required by the IEEE 1149.1 standard.

11.2.4.5 HI-Z

The HI-Z instruction is not included in the IEEE 1149.1 standard. It is provided as a manufacturer's optional public instruction to prevent having to backdrive the output pins during circuit-board testing. When HI-Z is invoked, all output drivers, including the

two-state drivers, are turned off (i.e., high impedance). The instruction selects the bypass register. The HI-Z instruction also asserts internal reset for the DSP56300 Core system logic to force a predictable internal state while performing external boundary scan operations

11.2.4.6 CLAMP

The CLAMP instruction is not included in the IEEE 1149.1 standard. It is provided as a public instruction that selects the 1-bit bypass register as the serial path between TDI and TDO while allowing signals driven from the component pins to be determined from the boundary scan register. During testing of ICs on PCB, it may be necessary to place static guarding values on signals that control operation of logic not involved in the test. The EXTEST instruction could be used for this purpose, but since it selects the boundary-scan register the required guarding signals would be loaded as part of the complete serial data stream shifted in, both at the start of the test and each time a new test pattern is entered. Since the CLAMP instruction allows guarding values to be applied using the boundary-scan register of the appropriate ICs while selecting their bypass registers, it allows much faster testing than does the EXTEST instruction. Data in the boundary scan cell remains unchanged until a new instruction is shifted in or the JTAG state machine is set to its reset state. The CLAMP instruction also asserts internal reset for the DSP56300 Core system logic to force a predictable internal state while performing external boundary scan operations.

11.2.4.7 ENABLE_ONCE

The ENABLE_ONCE instruction is not included in the IEEE 1149.1 standard. It is provided as a public instruction to allow the user to perform system debug functions. When the ENABLE_ONCE instruction is decoded the TDI and TDO pins are connected directly to the OnCE registers. The particular OnCE register connected between TDI and TDO at a given time is selected by the OnCE controller depending on the OnCE instruction being currently executed. All communication with the OnCE controller is done through the Select-DR-Scan path of the JTAG TAP Controller. See Chapter 10 ON-CHIP EMULATOR (OnCE™) for more information.

11.2.4.8 DEBUG_REQUEST

The DEBUG_REQUEST instruction is not included in the IEEE 1149.1 standard. It is provided as a public instruction to allow the user to generate a debug request signal to the DSP56300 Core. When the DEBUG_REQUEST instruction is decoded the TDI and TDO pins are connected to the Instruction Registers. Due to the fact that in the capture-IR state of the TAP the OnCE status bits are captured in the Instruction shift register, the external JTAG controller must continue to shift-in the DEBUG_REQUEST instruction while polling the status bits that are shifted-out until the Debug Mode of operation is entered (acknowledged by the combination 11 on OS1-OS0). After the acknowledgment of the Debug Mode is received, the external JTAG controller must issue the ENABLE_ONCE instruction to allow the user to perform system debug functions. See Chapter 10 ON-CHIP EMULATOR (OnCE™) for more information.

11.3 DSP56300 RESTRICTIONS

The control afforded by the output enable signals using the boundary scan register and the EXTEST instruction requires a compatible circuit-board test environment to avoid device-destructive configurations. The user must avoid situations in which the DSP56300 Core output drivers are enabled into actively driven networks.

There are two constraints related to the JTAG interface. First, the TCK input does not include an internal pullup resistor and should not be left unconnected to preclude mid-level inputs. The second constraint is to ensure that the JTAG test logic is kept transparent to the system logic by forcing TAP into the test-logic-reset controller state, using either of two methods. During power-up, TRST~ must be externally asserted to force the TAP controller into this state. After power-up is concluded, TMS must be sampled as a logic one for five consecutive TCK rising edges. If TMS either remains unconnected or is connected to VCC, then the TAP controller cannot leave the test-logic-reset state, regardless of the state of TCK.

The DSP56300 Core features a low-power stop mode, which is invoked using an instruction called STOP. The interaction of the JTAG interface with low-power stop mode is as follows:

1. The TAP controller must be in the test-logic-reset state to either enter or remain in the low-power stop mode. Leaving the TAP controller test-logic-reset state negates the ability to achieve low-power, but does not otherwise affect device functionality.
2. The TCK input is not blocked in low-power stop mode. To consume minimal power, the TCK input should be externally connected to VCC or ground.
3. The TMS and TDI pins include on-chip pullup resistors. In low-power stop mode, these two pins should remain either unconnected or connected to VCC to achieve minimal power consumption.

Since during STOP state all DSP56300 Core clocks are disabled, the JTAG interface provides the means of polling the device status (sampled in the capture-IR state). For an DSP56300 derivative that does not include the $\overline{\text{DE}}$ pin, the JTAG interface provides the software means of entering the Debug Mode by executing the DEBUG_REQUEST instruction.