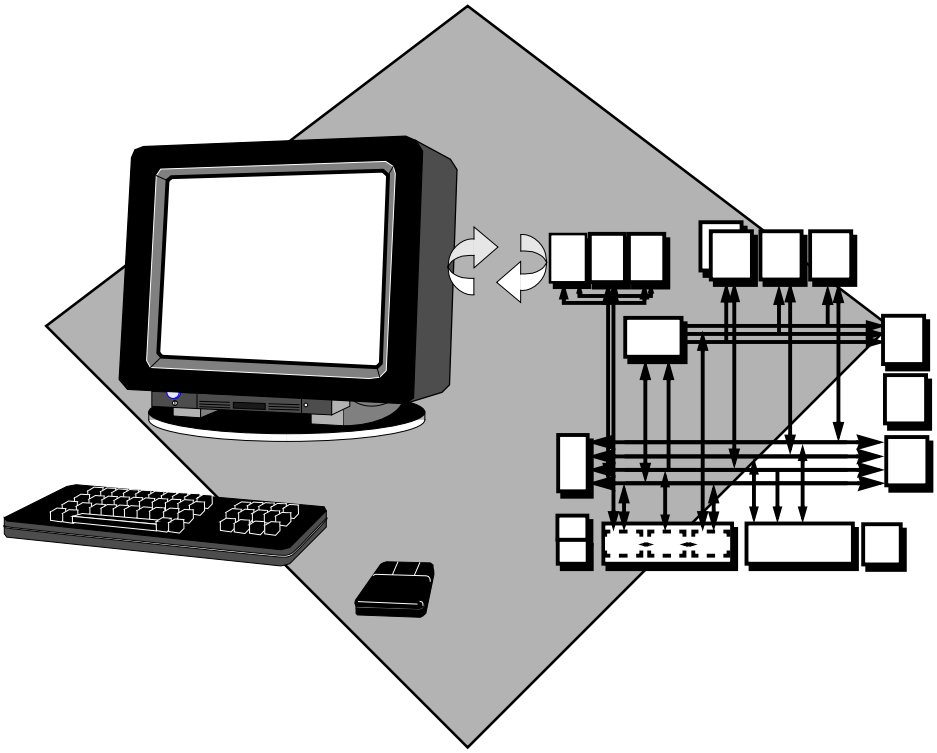
SECTION 5

GENERAL-PURPOSE INPUT/OUTPUT



5.1 INTRODUCTION

The DSP56307 provides 34 bidirectional signals that can be configured as GPIO signals or as peripheral dedicated signals. No dedicated GPIO signals are provided. All of these signals are GPIO by default after reset. The control register settings of the DSP56307 peripherals determine whether these signals function as GPIO or as peripheral dedicated signals. This section tells how signals can be used as GPIO.

5.2 PROGRAMMING MODEL

Section 2 Signal/Connection Descriptions of this manual documents in detail the special uses of the 34 bidirection signals. These signals fall into five groups and are controlled separately or as the following groups.

- Port B: 16 GPIO signals (shared with the HI08 signals)
- Port C: six GPIO signals (shared with the ESSI0 signals)
- Port D: six GPIO signals (shared with the ESSI1 signals)
- Port E: three GPIO signals (shared with the SCI signals)
- Timers: three GPIO signals (shared with the triple timer signals)

5.2.1 Port B Signals and Registers

Each of the 16 Port B signals not used as an HI08 signal can be configured as a GPIO signal. The GPIO functionality of Port B is controlled by three registers: host control register (HCR), host port GPIO data register (HDR), and host port GPIO direction register (HDDR). These registers are documented in **Section 6 Host Interface (HI08)** of this manual.

5.2.2 Port C Signals and Registers

Each of the six Port C signals not used as an ESSI0 signal can be configured as a GPIO signal. The GPIO functionality of Port C is controlled by three registers: Port C control register (PCRC), Port C direction register (PRRC), and Port C data register (PDRC). These registers are documented in **Section 7 Enhanced Synchronous Serial Interface** of this manual.

5.2.3 Port D Signals and Registers

Each of the six Port D signals not used as an ESSI1 signal can be configured as a GPIO signal. The GPIO functionality of Port D is controlled by three registers: Port D control register (PCRD), Port D direction register (PRRD), and Port D data register (PDRD). These registers are documented in **Section 7 Enhanced Synchronous Serial Interface** of this manual.

5.2.4 Port E Signals and Registers

Each of the three Port E signals not used as an SCI signal can be configured as a GPIO signal. The GPIO functionality of Port E is controlled by three registers: Port E control register (PCRE), Port E direction register (PRRE) and Port E data register (PDRE). These registers are documented in **Section 8 Serial Communication Interface** of this manual.

5.2.5 Triple Timer Signals

Each of the three triple timer interface signals (TIO0–TIO2) not used as a timer signal can be configured as a GPIO signal. Each signal is controlled by the appropriate timer control status register (TCSR0–TCSR2). These registers are documented in **Section 9 Triple Timer Module** of this manual.