8 DMA CONTROLLER

The Direct Memory Access (DMA) Controller is an on-chip device that permits data transfers between internal/external memory and/or internal/external I/O in any combination, without intervention of the program. Due to dedicated DMA address and data buses as well as internal memories partition, a high level of isolation is achieved where the DMA operation does not interfere or slow down the core operation.

The DMA Controller has six channels, each one having its own register set. All the registers are memory-mapped in the internal I/O memory space.

Table 8-1 shows the various types of data transfers that the DMA Controller can perform.

Table 8-1. DMA Controller Data Transfers

			Clock cycles per single word transfer
Internal Memory	→	Internal Memory	2
External Memory	↔	Internal Memory	2+wait states
External Memory	→	External Memory	2+wait states
Internal Memory	↔	Internal I/O	2
External Memory	↔	Internal I/O	2+wait states
Internal I/O	→	Internal I/O	2

Data transfer for one channel takes minimum two clock cycles per single word.

The DMA can execute data transfers with various types of address generation schemes such as:

1. constant addressing, where the address is unchanged throughout the data transfer.
2. uni-dimensional addressing, where one block is transferred using consecutive addresses.
3. two-dimensional addressing, where equally spaced blocks are transferred, using consecutive addresses within each block. The spacing between the blocks is programmed into an offset register.
4. three-dimensional addressing, where equally spaced groups of equally spaced blocks are transferred, using consecutive addresses within each block. The two spacings are programmed into two offset registers.

5. special cases of the above mentioned modes allow many other address generation patterns such as linear buffers with non-unit stride, circular buffers, etc.

8.1 DMA CONTROLLER PROGRAMMING MODEL

The registers comprising the DMA Controller are shown in Table 8-2 through Table 8-8.

Table 8-2. DMA Controller Programming Model - Channel 0

DSR0 - DMA Source Address Register for channel 0
DDR0 - DMA Destination Address Register for channel 0
DCO0 - DMA Counter for channel 0
DCR0 - DMA Control Register for channel 0

Table 8-3. DMA Controller Programming Model - Channel 1

DSR1 - DMA Source Address Register for channel 1
DDR1 - DMA Destination Address Register for channel 1
DCO1 - DMA Counter for channel 1
DCR1 - DMA Control Register for channel 1

Table 8-4. DMA Controller Programming Model - Channel 2

DSR2 - DMA Source Address Register for channel 2
DDR2 - DMA Destination Address Register for channel 2
DCO2 - DMA Counter for channel 2
DCR2 - DMA Control Register for channel 2

Table 8-5. DMA Controller Programming Model - Channel 3

DSR3 - DMA Source Address Register for channel 3
DDR3 - DMA Destination Address Register for channel 3
DCO3 - DMA Counter for channel 3
DCR3 - DMA Control Register for channel 3

Table 8-6. DMA Controller Programming Model - Channel 4

DSR4 - DMA Source Address Register for channel 4
DDR4 - DMA Destination Address Register for channel 4
DCO4 - DMA Counter for channel 4
DCR4 - DMA Control Register for channel 4

Table 8-7. DMA Controller Programming Model - Channel 5

DSR5 - DMA Source Address Register for channel 5
DDR5 - DMA Destination Address Register for channel 5
DCO5 - DMA Counter for channel 5
DCR5 - DMA Control Register for channel 5

Table 8-8. DMA Offset Registers

DOR0 - DMA Offset Register 0
DOR1 - DMA Offset Register 1
DOR2 - DMA Offset Register 2
DOR3 - DMA Offset Register 3

Table 8-9. DMA Status Register

DSTR - DMA Status Register

8.1.1 DMA Source Address Register (DSR)

The DMA Source Address Register (DSR) is a 24-bit read/write register that contains the source address for the next DMA transfer. The DMA controller has one source address register for each DMA channel - DSR0, DSR1, DSR2, DSR3, DSR4 and DSR5.

8.1.2 DMA Destination Address Register (DDR)

The DMA Destination Address Register (DDR) is a 24-bit read/write register that contains the destination address for the next DMA transfer. The DMA controller has one destination address register for each DMA channel - DDR0, DDR1, DDR2, DDR3, DDR4 and DDR5.

8.1.3 DMA Offset Register (DOR)

The DMA Offset Register is a 24-bit read/write register that contains the offset value to be used in some of the DMA addressing modes. The DMA controller has four common offset registers (DOR0, DOR1, DOR2 and DOR3) that can be used by all the channels according to their address generation mode.

8.1.4 DMA Counter (DCO)

The DMA Counter is a 24-bit read/write register that contains the number of DMA data transfers to be done. The DCO has five modes of operations determined by the DMA channel's address generation mode that are defined in the DMA channel's Control Register.

The following paragraphs explains the various modes of the DMA Counter. During DMA operation, a Source Address Register (DSR) is associated with one of the counter modes, while the Destination Address Register (DDR) can be associated with another counter mode. The examples below use DSR as an example of the address register used, but the same example is valid for the destination register also.

8.1.4.1 DMA counter mode A - single counter

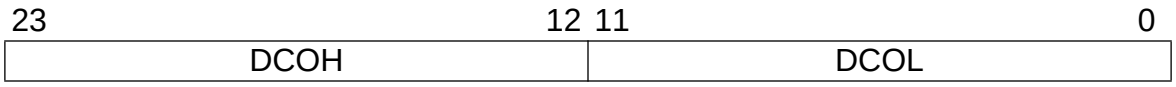
In this mode of operation, the number of transfers is equal to the value loaded into DCO plus one (DCO+1). Before each DMA transfer, the DCO is tested for zero, and the following actions occur based on the test result:

- DCO > 0: A transfer is initiated with an address equal to the address register, then DCO is decremented by one and the address register is updated according to the address generation mode.
- DCO = 0: The last transfer is initiated with an address equal to the address register, the address register is updated according to the address generation mode and DCO is loaded with its preloaded value.

If, for example, DCO is preloaded with the value 5, DSR is loaded with the value S and the address generation mode is postincrement by 1, the following DMA transfers will be initiated by the DMA controller:

before the transfer			after the transfer	
DSR	DCO	transfer source address	DSR	DCO
S	5	S	S+1	4
S+1	4	S+1	S+2	3
S+2	3	S+2	S+3	2
S+3	2	S+3	S+4	1
S+4	1	S+4	S+5	0
S+5	0	S+5	S+6	5

8.1.4.2 DMA counter mode B - dual counter



In this mode of operation, which is useful for two dimensional block transfers, the DCO is separated to two sections: DCOL (bits 0-11) and DCOH (bits 12-23). Before each DMA transfer the DCO is tested for zero and the following actions occur based on the test result:

- DCOL > 0: A transfer is initiated with an address equal to the address register, then DCOL is decremented by one and the address register is incremented by one.
- DCOH > 0; DCOL = 0: A transfer is initiated with an address equal to the address register, the address register is incremented with the specified offset register, DCOH is decremented by one and DCOL is loaded with its preloaded value.
- DCOH = 0; DCOL = 0: The last transfer is initiated with an address equal to the address register, the address register is incremented with the specified offset register and both DCOH and DCOL are loaded with their preloaded value.

The number of transfers in this mode is equal to (DCOL+1) x (DCOH+1).

If, for example, DCOH is preloaded with the value 1, DCOL is preloaded with the value 2, DOR is preloaded with the value O and DSR with the value S, the following DMA transfers will be initiated by the DMA controller:

before the transfer			after the transfer	
DSR	DCO	transfer source address	DSR	DCO
S	1:2	S	S+1	1:1
S+1	1:1	S+1	S+2	1:0
S+2	1:0	S+2	S+O+2	0:2
S+O+2	0:2	S+O+2	S+O+3	0:1
S+O+3	0:1	S+O+3	S+O+4	0:0
S+O+4	0:0	S+O+4	S+2O+4	1:2

8.1.4.3 DMA counter modes C, D and E- triple counter

In this mode of operation, which is useful for three dimensional block transfers, the DCO is separated to three sections: DCOL, DCOM and DCOH. Before each DMA transfer the

DCO is tested for zero and the following actions occur based on the test result:

- DCOL > 0: A transfer is initiated with an address equal to the address register, then DCOL is decremented by one and the address register is incremented by one.

- DCOM > 0; DCOL = 0: A transfer is initiated with an address equal to the address register, the address register is incremented with the first specified offset register, DCOM is decremented by one and DCOL is loaded with its preloaded value.

- DCOH > 0; DCOM = 0; DCOL = 0: A transfer is initiated with an address equal to the address register, the address register is then incremented with the second specified offset register, DCOH is decremented by one and both DCOM and DCOL are loaded with their preloaded value.

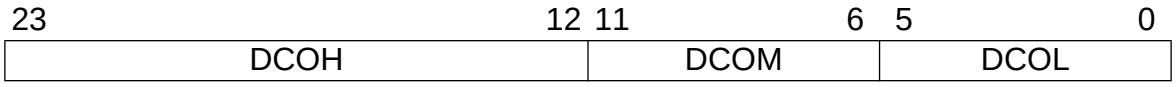
- DCOH = 0; DCOM = 0; DCOL = 0: The last transfer is initiated with an address equal to the address register, the address register is then incremented with the second specified offset register and both DCOH, DCOM and DCOL are loaded with their preloaded value.

The number of transfers in this mode is equal to (DCOL+1) x (DCOM+1) x (DCOH+1).

If, for example, DCOH is preloaded with the value 1, DCOM is also preloaded with the value 1, DCOL is preloaded with the value 2, DOR0 is preloaded with the value O0, DOR1 is preloaded with the value O1 and DSR with the value S, the following DMA transfers will be initiated by the DMA controller:

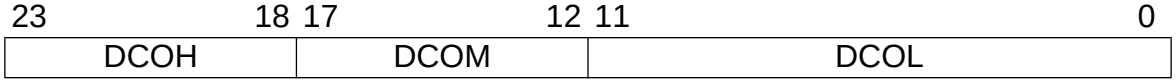
before the transfer			after the transfer	
DSR	DCO	transfer source address	DSR	DCO
S	1:1:2	S	S+1	1:1:1
S+1	1:1:1	S+1	S+2	1:1:0
S+2	1:1:0	S+2	S+O0+2	1:0:2
S+O0+2	1:0:2	S+O0+2	S+O0+3	1:0:1
S+O0+3	1:0:1	S+O0+3	S+O0+4	1:0:0
S+O0+4	1:0:0	S+O0+4	S+O0+O1+4	0:1:2
S+O0+O1+4	0:1:2	S+O0+O1+4	S+O0+O1+5	0:1:1
S+O0+O1+5	0:1:1	S+O0+O1+5	S+O0+O1+6	0:1:0
S+O0+O1+6	0:1:0	S+O0+O1+6	S+2O0+O1+6	0:0:2
S+2O0+O1+6	0:0:2	S+2O0+O1+6	S+2O0+O1+7	0:0:1
S+2O0+O1+7	0:0:1	S+2O0+O1+7	S+2O0+O1+8	0:0:0
S+2O0+O1+8	0:0:0	S+2O0+O1+8	S+2O0+2O1+8	1:1:2

1. DMA counter mode C structure:
   The structure of DMA counter mode C is as follows: DCOL (bits 0-5), DCOM (bits 6-11) and DCOH (bits 12-23).



2. DMA counter mode D structure:
   The structure of DMA counter mode D is as follows: DCOL (bits 0-5), DCOM (bits 6-17) and DCOH (bits 18-23).

3. DMA counter mode E structure:
   The structure of DMA counter mode E is as follows: DCOL (bits 0-11), DCOM (bits 12-17) and DCOH (bits 18-23).



8.1.5 DMA Control Register (DCR)

The DMA Control Register (DCR) is a 24-bit read/write register that controls the DMA operation. Each bit is shown in Figure 8-1 and described in the following paragraphs. All DCR bits are cleared during processor reset.

Figure 8-1. DMA Control Register

23	22	21	20	19	18	17	16	15	14	13	12
DE	DIE	DTM2	DTM1	DTM0	DPR1	DPR0	DCON	DRS4	DRS3	DRS2	DRS1

11	10	9	8	7	6	5	4	3	2	1	0
DRS0	D3D	DAM5	DAM4	DAM3	DAM2	DAM1	DAM0	DDS1	DDS0	DSS1	DSS0

8.1.5.1 DCR DMA Channel Enable Bit (DE) Bit 23

The DE bit enables the channel operation. Setting DE will trigger a single block DMA transfer in the DMA transfer mode that uses DE as a trigger, and will enable a single block, a single “line” or a single word DMA transfer in the transfer modes which use a requesting device as a trigger. DE is cleared by Hardware Reset, and by the end of DMA transfer in some of the transfer modes as defined by the DTM(2:0) bits. Clearing DE explicitly by software during a DMA operation will stop the channel operation only after the current DMA transfer has been completed (the current word has been stored into the destination).

DE	DMA Operation
0	Disabled
1	Enabled

8.1.5.2 DCR DMA Interrupt Enable Bit (DIE) Bit 22

When the DMA Interrupt Enable bit is set, a DMA interrupt will be generated at the end of a DMA block transfer, that is after the counter is loaded with its preloaded value and the DTD bit in the DMA status register is set. A DMA interrupt will also be generated when DE is cleared explicitly by software during a DMA operation, as described in Section 8.1.5.1.

When DIE is cleared, the DMA interrupt is disabled.

DIE	DMA Interrupt
0	Disabled
1	Enabled

8.1.5.3 DCR DMA Transfer Mode (DTM2-DTM0)- bits 21:19

DMA Transfer mode bits specify the modes of operation of the DMA channel.

When DTM2-DTM0=000, a block of data is transferred, the length of the block is determined by the counter, the transfer is enabled by DE and initiated by the first DMA request. The transfer is completed after the counter decrements to zero, then it reloads itself with the original value and clears the DE bit.

Table 8-10. DMA Transfer Mode (DTM2-DTM0) Bits

DTM(2:0)	triggered by	DE cleared at end of block	Transfer Mode
000	request	yes	block transfer
001	request	yes	word transfer
010	request	yes	line transfer
011	DE	yes	block transfer
100	request	no	block transfer
101	request	no	word transfer
110	reserved		
111	reserved		

When DTM2-DTM0=001, a block of data is transferred, the length of the block is determined by the counter and each DMA request will transfer a single word while enabled by DE. The transfer is completed after the counter decrements to zero, then it reloads itself with the original value and clears the DE bit.

When DTM2-DTM0=010, a block of data is transferred, the length of the block is determined by the counter and each DMA request will transfer a "line", i.e. the number of words as defined at DCOL, while enabled by DE. The transfer is completed after the whole counter decrements to zero, then it reloads itself with the original value and clears the DE bit.

When DTM2-DTM0=011, a block of data is transferred, the length of the block is determined by the counter and the transfer is initiated by setting DE. The transfer is completed when the counter decrements to zero, then it reloads itself with the original value and clears the DE bit.

When DTM2-DTM0=100, a block of data is transferred, the length of the block is determined by the counter, the transfer is enabled by DE and initiated by the first DMA request. The transfer is completed when the counter decrements to zero, then it reloads itself with the original value. The DE bit is not cleared at the end of the block, therefore the DMA channel is waiting for a new request.

When DTM2-DTM0=101, a single word transfer is enabled by DE and initiated by every DMA request. When the counter decrements to zero, it is reloaded with its original value. The DE bit is not automatically cleared, therefore the DMA channel is waiting for a new request.

8.1.5.4 DCR DMA Channel priority(DPR1-DPR0) - bits 18:17

The DMA Channel Priority control bits define the priority level of the DMA channel relative to the other DMA channels as well as to the priority level of the core when external bus access is required. When DMA transfers are pending, the DMA channel priority level of all the channels are compared to decide which channel will be activated in the next word transfer. This decision must be made since all channels use common resources such as the DMA address generation logic, the address and data buses etc.

Table 8-11. DCR DMA Channel priority(DPR1-DPR0) Bits

DPR(1:0)	Channel Priority
00	Priority Level 0 (lowest)
01	Priority Level 1
10	Priority Level 2
11	Priority Level 3 (highest)

If all or some of the channels have the same priority, then the channels will be activated in a round-robin fashion: channel 0 will be activated to transfer one word out of its programmed stream, followed by channel 1, followed be channel 2 and so on.

If the channel priorities are different, the channel with the highest priority will start executing DMA transfers and will remain doing so as long as there are DMA transfers pending. In the event that a lower priority channel is executing DMA transfers when a higher priority channel receives a transfer request, the lower priority channel will finish the transfer of the current word and arbitration will start again. If some channels with the same priority are activated in a round-robin fashion and a new channel with higher priority interferes, then after this channel finishes its pending transfers the order of the transfers in the round-robin mode may change, but the algorithm remains the same.

The DPR(1:0) bits are also used to determine the DMA priority relative to the core priority when an external bus access is required. This function involves the DMA priority level defined by the current active DMA channel, the core priority defined by bits CP1-CP0 in the DSP56300 Core Status Register (SR) and the core-DMA priority defined by bits CDP1-CDP0 in the DSP56300 Core Operating Mode Register (OMR).

When the priority of the DMA is higher than the priority of the core (CDP=01; CDP=00 and

DPR > CP) and both the DMA and the core require an external access, the DMA will perform the external bus access and the core will wait for the DMA to complete the programmed current transfer.

When the priority of the DMA is equal to the priority of the core (CDP=10; CDP=00 and DPR = CP) and both the DMA and the core require an external access, the core will perform all its external accesses pertaining to the current instruction and than the DMA will perform its access.

When the priority of the DMA is lower than the priority of the core (CDP=11; CDP=00 and DPR < CP) and both the DMA and the core require an external access, the core will always perform its external accesses and the DMA will wait for a free slot in which the core does not require the external bus.

In the dynamic priority mode (CDP=00), it is possible that a DMA channel will be halted before executing both the source and destination accesses when the core has higher priority over the external bus. In this case, if another, higher priority DMA channel will request an access, the halted channel will finish its previous access with the new higher priority before the new requesting DMA channel will be serviced.

8.1.5.5 DCR DMA Continuous Mode (DCON) - bit 16

When DMA Continuous Mode bit is set the channel will enter the continuous transfer mode, in which it will not be interrupted throughout the transfer by any other DMA channel of equal priority. The DMA transfers in Continuous Mode of operation can be interrupted if a DMA channel of higher priority has been enabled after the Continuous Mode transfer was started. If the priority of the DMA is higher than the priority of the core (CDP=01; CDP=00 and DPR>CP) and DCON bit is set, than if the DMA requires an external access, it will get the external bus and the core will not be able to use the external bus in the next cycle after the DMA access even if the DMA does not need the bus in this cycle. However, if a refresh cycle from the DRAM controller is requested in such a case, the DMA will be interrupted by the refresh cycle.
When the DCON bit is cleared the priority algorithm operates as described in the Section 8.1.5.4.

8.1.5.6 DCR DMA Request Source (DRS0-DRS4) Bits 15-11

The DMA Request Source bits encode the source of DMA requests used to trigger the DMA transfers. The DMA request sources may be the internal peripherals, external devices requesting service through the $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$ and $\overline{\text{IRQD}}$ pins or triggering by transfer done from a DMA channel. All the request sources behave as edge-triggered synchronous inputs.

Peripheral requests 18-21 (DRS[4:0]=111xx) are special because in addition to the regular behavior of all the requesting devices, they can serve as “fast request sources”. In a regular request from a peripheral, the trigger to the DMA remains set until the appropriate register at the peripheral is accessed by the DMA, therefore the peripheral

cannot generate a second request until the first one was served. Another method is when the peripheral (i.e. timer) gives a triggering pulse without taking care whether the DMA served this trigger. The “fast peripheral” has a full duplex handshake to the DMA, enabling a maximum throughput of a trigger every two clock cycles. This mode is functional only in the “word transfer mode” (DTM = 001 or 101). In the “fast request mode” the DMA sets an “enable line” to the peripheral. If the peripheral wants, he sends the DMA a one cycle triggering pulse.This pulse resets the enable line. If the DMA decides by the priority algorithm that this trigger will be served in the next cycle, the enable line is set again even before the corresponding register in the peripheral is accessed.

DMA Request Source Bits DRS(4:0)	Requesting Device
00000	External ($\overline{\text{IRQA}}$ pin)
00001	External ($\overline{\text{IRQB}}$ pin)
00010	External ($\overline{\text{IRQC}}$ pin)
00011	External ($\overline{\text{IRQD}}$ pin)
00100	Transfer Done from channel 0
00101	Transfer Done from channel 1
00110	Transfer Done from channel 2
00111	Transfer Done from channel 3
01000	Transfer Done from channel 4
01001	Transfer Done from channel 5
01010	Peripheral Request MDRQ0
...	...
11111	Peripheral Request MDRQ21

8.1.5.7 DCR DMA three Dimensional mode (D3D)- bit 10

When this bit is set the addressing mode, determined by DAM(5:0) is three-dimensional. When this bit is cleared the addressing mode is non three-dimensional.

8.1.5.8 DCR DMA Address Mode (DAM5-DAM0)- bits 9:4

These bits define the address generation mode for the DMA transfer. These bits are encoded in two different ways according to D3D bit.

Non three dimensional modes (D3D = 0).

In this case DAM bits are separated into two groups: DAM(5:3), that defines the address generation mode for destination transfers and DAM(2:0), that defines the address generation mode for source transfers.The encoding is defined in Table 8-12 and in Table 8-13. The address generation mode can be no update, postincrement by 1 or two-dimensional.

In the no update addressing mode the DMA is accessing a constant address for the entire transfer. This addressing mode is useful when accessing peripheral devices as well as other single address devices such as FIFOs.

In the postincrement by one addressing mode the DMA is accessing consecutive addresses. This addressing mode is useful when accessing data structures in memories, when the data elements are placed in successive memory locations.

In the two-dimensional addressing mode of operation the DMA is accessing data at consecutive addresses for a given number of times (DCOL) and then an offset register is added to the generated address. The entire process is repeated for another given number of times (DCOH). DCOL and DCOH are the two sections of the DCO counter. See Section 8.1.4 for a detailed description of the DCO operation. This addressing mode is useful when accessing two dimensional arrays of data.

Table 8-12. Source Address Generation Mode (D3D = 0)

DAM(2:0)	addressing mode	counter mode	offset select
000	two-dimensional	B	DOR0
001	two-dimensional	B	DOR1
010	two-dimensional	B	DOR2
011	two-dimensional	B	DOR3
100	no update	A	N/A
101	post increment by 1	A	N/A
110	reserved		
111	reserved		

Note: if the source address generation mode specify different counter mode than the destination address generation mode, then the counter mode is B.

Table 8-13. Destination Address Generation Mode (D3D = 0)

DAM(5:3)	addressing mode	counter mode	offset select
000	two-dimensional	B	DOR0
001	two-dimensional	B	DOR1
010	two-dimensional	B	DOR2
011	two-dimensional	B	DOR3
100	no update	A	N/A
101	post increment by 1	A	N/A
110	reserved		
111	reserved		

Note: if the destination address generation mode specify different counter mode than the source address generation mode, then the counter mode is B.

Three dimensional modes (D3D = 1).

In this case DAM bits are separated into three groups: DAM(1:0) that defines the DMA counter mode, DAM2 that is the address mode select and DAM(5:3) that defines the address generation mode. The encoding is defined in Table 8-14, Table 8-15 and Table 8-16. When D3D equals one, either the source addressing mode or the destination addressing mode or both are three-dimensional.
In the three-dimensional address generation mode of operation the DMA is accessing data at consecutive addresses for a given number of times (DCOL) and then an offset register is added to the generated address. This process is repeated for another given number of times (DCOM) after which another offset is added to the generated address. The entire process is repeated for a given number of times (DCOH). DCOL, DCOM and DCOH are the three sections of the DCO counter. See Section 8.1.4 for a detailed description of the DCO operation. This addressing mode is useful when accessing a number of two dimensional arrays of data.

Table 8-14. Counter Mode (D3D = 1)

DAM(1:0)	counter mode
00	mode C
01	mode D
10	mode E
11	reserved

Table 8-15. Address Mode Select (D3D = 1)

DAM2	addressing mode	offset select
0	source: three-dimensional	source: DOR0 : DOR1
	destination: defined by DAM(5:3)	destination: defined by DAM(5:3)
1	source: defined by DAM(5:3)	source: defined by DAM(5:3)
	destination: three-dimensional	destination: DOR2 : DOR3

Table 8-16. Address Generation Mode (D3D = 1)

DAM(5:3)	addressing mode	offset select
000	two-dimensional	DOR0
001	two-dimensional	DOR1
010	two-dimensional	DOR2
011	two-dimensional	DOR3
100	no update	none
101	post increment by 1	none
110	three-dimensional	DOR0 : DOR1
111	three-dimensional	DOR2 : DOR3

The offset select in Tables 8-12, 8-13, 8-15 and 8-16 defines the offset registers that are selected to increment the address register, when DCOL or DCOM:DCOL equals zero. In two-dimensional mode only one offset register is needed to increment the address register when DCOL equals zero. In three dimensional mode, two offset registers are needed, DORi:DORj. When DCOL equals zero and DCOM does not equal zero, then DORi is used to increment the address register. If both DCOL and DCOM equal zero, then DORj is used to increment the address register.

8.1.5.9 DCR DMA Destination Space (DDS0-DDS1) Bits 3, 2

The DMA Destination Space control bits specify the memory space that will be referenced as destination by the DMA.

DDS1	DDS0	DMA Destination Memory Space
0	0	X Memory Space
0	1	Y Memory Space
1	0	P Memory Space
1	1	Reserved

Note: In Cache Mode, a DMA to P Memory Space has some limitations (as described in Chapter 5).

8.1.5.10 DCR DMA Source Space (DSS0-DSS1) Bits 1, 0

The DMA Source Space control bits specify the memory that will be referenced as source by the DMA.

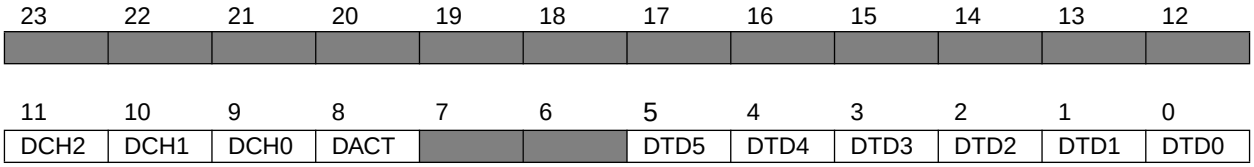
DSS1	DSS0	DMA Source Memory Space
0	0	X Memory Space
0	1	Y Memory Space
1	0	P Memory Space
1	1	Reserved

Note: In Cache Mode, a DMA from P Memory Space has some limitations (as described in Chapter 5).

8.1.6 DMA Status Register (DSTR)

The DMA Status Register (DSTR) is a 24-bit read only register that reflects the status of the DMA operation. Each bit is shown in Figure 8-2 and described in the following paragraphs.

Figure 8-2. DMA Status Register



8.1.6.1 DSTR DMA Channel Transfer Done Status (DTD)- bits 5-0

The DMA Transfer Done status bits (DTD5-DTD0) are set when the last word during a single block transfer is stored in the destination, stopping channel operation. At the same time, the DE bit in the related DCR register, may be cleared according to the transfer mode as defined by DTM(2:0). The last transfer is defined as the one where the DMA counter reloads to its initial value, or when DE is explicitly cleared by software. If the DIE bit in the related DCR is set, then the assertion of the DTD bit will cause a DMA interrupt request. When the DMA Interrupt is disabled, the core may verify the channel status by polling this bit. DTD bits are set by Hardware Reset. The DTD bit is reset by explicitly setting bit DE at the corresponding DCR register by software.

Note1: Due to pipeline dependencies, after setting DE in a DCR register, the corresponding DTD bit will be affected only after additional two instruction cycles.

Note2: If the DMA channel works in a word transfer mode, than clearing DE will set the corresponding DTD bit only after a trigger that was already captured by the DMA is handled.

8.1.6.2 DSTR reserved bits - bits 23:12 and 7:6

These bits are reserved and are read as zero.

8.1.6.3 DSTR DMA Active state (DACT) - bit 8

The DMA Active state status bit is set if the DMA is in the middle of a transfer. This bit is cleared if all the DMA channels are disabled or wait for DMA requests. This bit should be polled and tested for zero before entering to a low power mode by executing a STOP instruction. The DACT status bit is cleared by Hardware Reset

8.1.6.4 DSTR DMA Active Channel (DCH2-DCH0) - bits 11:9

The DMA Active Channel status bits are the encoding of the current active channel. These bits are cleared at Hardware Reset. Their value is valid only if DACT=1.

Table 8-17. DCH Status bits encoding

DCH(2:0)	Active channel
000	DMA Channel 0
001	DMA Channel 1
010	DMA Channel 2
011	DMA Channel 3
100	DMA Channel 4
101	DMA Channel 5
110	reserved
111	reserved

8.2 DMA Restrictions

The following are some restrictions that apply to the DMA operation:

1. The user should take care when he needs to enter into the STOP processing state. Before executing the STOP instruction, the Dma ACTive (DACT) status bit should be polled until it is read as ‘0’. When the chip enters the STOP state all the DMA triggers that were previously latched are cleared.
2. The core will exit the WAIT processing state when a DMA channel accepts a trigger that is programmed as the selected source trigger. The DMA will prevent the core from entering WAIT processing state if the DMA is active.
3. Only the Transmit/Receive Data registers of the peripheral interfaces may be accessed by the DMA Controller when specifying source or destination in the internal I/O space.
4. If one of the DMA channels is accessing external memory and the access is delayed due to bus arbitration or memory wait, the other DMA channels will also stop, since the DMA mechanism does not distinguish between the different channels.
5. The internal RAM is divided into 256-word banks. If the Core and DMA are accessing different banks they will not interfere one with another, i.e. each will continue operations at its maximum speed. If both Core and DMA are accessing the same bank then the Core will always have priority and the DMA will be delayed until a free slot will be available.
6. The DMA Address Registers (DSR, DDR, DOR) and the DMA Counter

(DCO) should be written only when the channel that uses them is disabled (DE=0 and DTD=1). The operation of the DMA controller cannot be guaranteed if one of these registers is written while the DMA channel that uses them is busy.

7. A change in the request source should be initiated only when the corresponding DMA channel is idle. If the channel is forced to enter the idle state by clearing the Dma Enable (DE) control bit, the corresponding Dma Transfer Done (DTD) status bit should be polled until it is read as '1'.
8. If a DMA channel is programmed to perform accesses in the word transfer mode, the corresponding DTD status bit will be set only after the current captured request will be serviced by an appropriate transfer. This will assure that the last captured request will not be lost. Note that if this channel's priority is low, the DTD will be set only when it receives the priority to perform its accesses. In order to shorten this time, the channel's priority may be raised before DE is cleared.
9. While a DMA channel is enabled (DE=1) the user should not modify any of the channel's DCR bits, but for the DE bit itself.
10. Due to the DSP56300 Core pipeline, after DE bit in DCRx is set, the corresponding DTDx bit in DSTR will be cleared only after two instruction cycles.