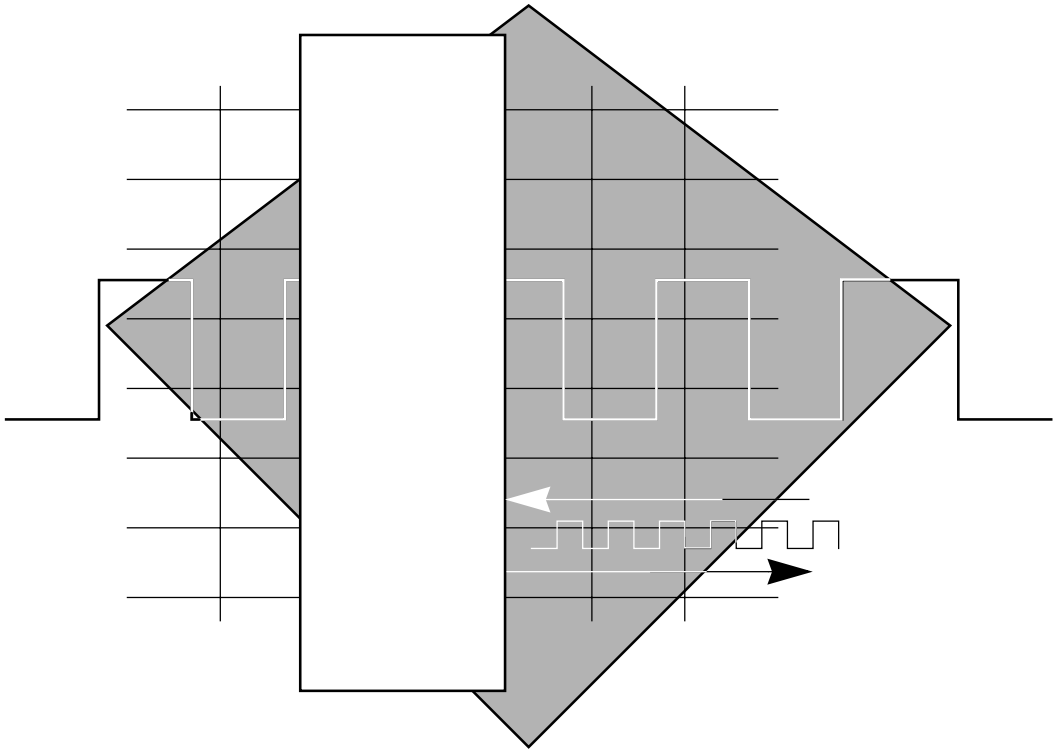
SECTION 7

ENHANCED SYNCHRONOUS SERIAL INTERFACE



7.1 INTRODUCTION

The ESSI provides a full-duplex serial port for serial communication with a variety of serial devices, including one or more industry-standard codecs, other DSPs, microprocessors, and peripherals that implement the Motorola serial peripheral interface (SPI). The ESSI consists of independent transmitter and receiver sections and a common ESSI clock generator.

There are two independent and identical ESSIs in the DSP56307: ESSI0 and ESSI1. For the sake of simplicity, a single generic ESSI is described here.

The ESSI block diagram is shown in **Figure 7-1**. This interface is synchronous because all serial transfers are synchronized to one clock.

Note: This synchronous interface should not be confused with the asynchronous channels mode of the ESSI, in which separate clocks are used for the receiver and transmitter. In that mode, the ESSI is still a synchronous device because all transfers are synchronized to these clocks.

Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is similar in that it is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. The network mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for nonperiodic transfers of data. This mode can be used to transfer data serially at high speed when the data become available. This mode offers a subset of the SPI protocol.

Since each ESSI unit can be configured with one receiver and three transmitters, the two units can be used together for surround sound applications (which need two digital input channels and six digital output channels).

7.2 ENHANCEMENTS TO THE ESSI

The SSI used in the DSP56000 family has been enhanced in the following ways to make the ESSI:

- Network enhancements
  - Time slot mask registers (receive and transmit)
  - End-of-frame interrupt
  - Drive enable signal (to be used with transmitter 0)

- Audio enhancements
  - Three transmitters per ESSI (for six-channel surround sound)
- General enhancements
  - Can trigger DMA interrupts (receive or transmit)
  - Separate exception enable bits
- Other changes
  - One divide-by-2 removed from the internal clock source chain
  - Control register A prescaler range (CRA(PSR)) bit definition is reversed
  - Gated clock mode not available

7.3 ESSI DATA AND CONTROL SIGNALS

Three to six signals are required for ESSI operation, depending on the operating mode selected. The serial transmit data (STD) signal and serial control (SC0 and SC1) signals are fully synchronized to the clock if they are programmed as transmit-data signals.

7.3.1 Serial Transmit Data Signal (STD)

The STD signal transmits data from the serial transmit shift register. STD is an output when data is being transmitted from the TX0 shift register. With an internally-generated bit clock, the STD signal becomes a high impedance output signal for a full clock period after the last data bit is transmitted if another data word does not follow immediately. If sequential data words are transmitted, the STD signal does not assume a high-impedance state. The STD signal can be programmed as a GPIO signal (P5) when the ESSI STD function is not is use.

7.3.2 Serial Receive Data Signal (SRD)

The SRD signal receives serial data and transfers the data to the ESSI receive shift register. SRD can be programmed as a GPIO signal (P4) when the ESSI SRD function is not in use.

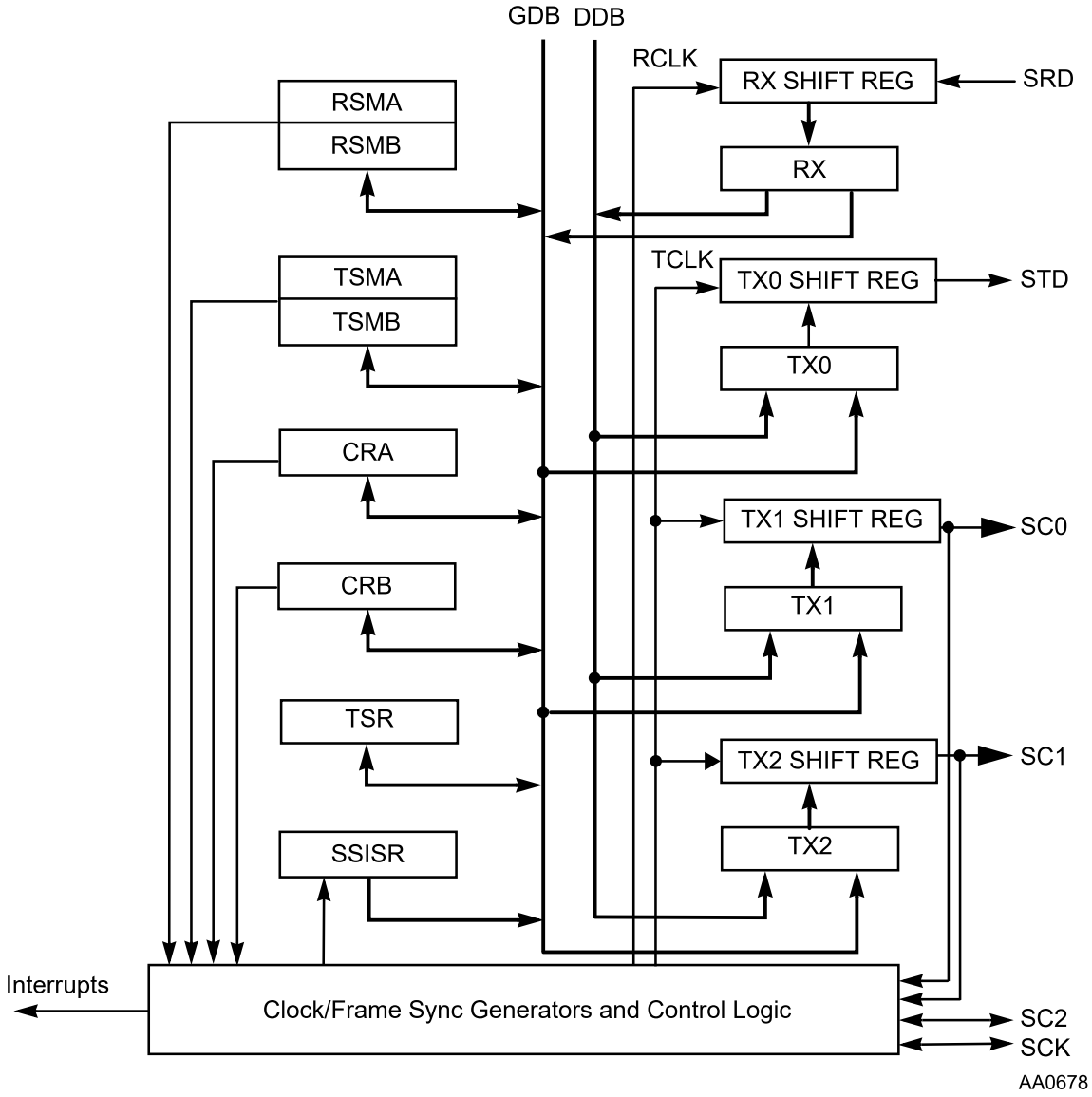


Figure 7-1 ESSI Block Diagram

7.3.3 Serial Clock (SCK)

The SCK signal is a bidirectional signal providing the serial bit rate clock for the ESSI interface. The SCK signal is a clock input or output used by all the enabled transmitters and receiver in synchronous modes or by all the enabled transmitters in asynchronous

modes. See **Table 7-1** on page 7-8 for details. SCK can be programmed as a GPIO signal (P3) when the ESSI SCK function is not in use.

Notes: **1.** Although an external serial clock can be independent of and asynchronous to the DSP system clock, the external ESSI clock frequency must not exceed $F_{core}/3$, and each ESSI phase must exceed the minimum of 1.5 CLKOUT cycles.

2. The internally sourced ESSI clock frequency must not exceed $F_{core}/4$.

7.3.4 Serial Control Signal (SC0)

ESSI0: SC00; ESSI1: SC10

The programmer determines the function of this signal by selecting either synchronous or asynchronous mode, according to **Table 7-4** on page 7-24. In asynchronous mode, this signal is used for the receive clock I/O. In synchronous mode, this signal is used as the transmitter data out signal for transmit shift register TX1 or for serial flag I/O. A typical application of serial flag I/O would be multiple device selection for addressing in codec systems.

If SC0 is configured as a serial flag signal or receive clock signal, its direction is determined by the serial control direction 0 (SCD0) bit in ESSI control register B (CRB). When configured as an output, SC0 functions as the serial output flag 0 (OF0) or as a receive shift register clock output. If SC0 is used as the serial output flag 0, its value is determined by the value of the serial output flag 0 (OF0) bit in the CRB.

If SC0 is an input, it functions as either serial Input Flag 0 or a receive shift register clock input. As serial input flag 0, SC0 controls the state of the serial input flag 0 (IF0) bit in the ESSI status register (SSISR).

When SC0 is configured as a transmit data signal, it is always an output signal, regardless of the SCD0 bit value. SC0 is fully synchronized with the other transmit data signals (STD and SC1).

SC0 can be programmed as a GPIO signal (P0) when the ESSI SC0 function is not in use.

Note: The ESSI can operate with more than one active transmitter only in synchronous mode.

7.3.5 Serial Control Signal (SC1)

ESSI0:SC01; ESSI1: SCI11

The programmer determines the function of this signal by selecting either synchronous or asynchronous mode, according to**Table 7-4** on page 7-24. In asynchronous mode (such as a single codec with asynchronous transmit and receive), SC1 is the receiver frame sync I/O. In synchronous mode, SC1 is used for the transmitter data out signal of transmit shift register TX2, for the transmitter 0 drive-enabled signal, or for serial flag I/O.

When used as serial flag I/O, it operates like SC0. SC0 and SC1 are independent flags, but can be used together for multiple serial device selection. SC0 and SC1 can be unencoded to select up to two codecs or decoded externally to select up to four codecs. If SC1 is configured as a serial flag signal, its direction is determined by the SCD1 bit in the CRB.

If SC1 is configured as a serial flag or receive frame sync signal, its direction is determined by the serial control direction 1 (SCD1) bit in the CRB.

When configured as an output, the SC1 signal functions as a serial output flag, as the transmitter 0 drive-enabled signal, or as the receive frame sync signal output. If SC1 is used as serial output flag 1, its value is determined by the value of the serial output flag 1 (OF1) bit in the CRB.

When configured as an input, this signal can receive frame sync signals from an external source, or it acts as a serial input flag. As a serial input flag, SC1controls status bit IF1 in the SSISR.

When this signal is configured as a transmit data signal, it is always an output signal, regardless of the SCD1 bit value. As an output, it is fully synchronized with the other ESSI transmit data signals (STD and SC0).

SC1 can be programmed as a GPIO signal (P1) when the ESSI SC1 function is not in use.

Table 7-1 ESSI Clock Sources

SYN	SCKD	SCD0	RX Clock Source	RX Clock Out	TX Clock Source	TX Clock Out
Asynchronous						
0	0	0	EXT, SC0	—	EXT, SCK	—
0	0	1	INT	SC0	EXT, SCK	—
0	1	0	EXT, SC0	—	INT	SCK
0	1	1	INT	SC0	INT	SCK
Synchronous						
1	0	0/1	EXT, SCK	—	EXT, SCK	—
1	1	0/1	INT	SCK	INT	SCK

7.3.6 Serial Control Signal (SC2)

ESSI0:SC02; ESSI1:SC02

This signal is used for frame sync I/O. The frame sync is SC2 for both the transmitter and receiver in synchronous mode and for the transmitter only in asynchronous mode. The direction of this signal is determined by the SCD2 bit in the CRB.

When configured as an output, this signal outputs the internally generated frame sync signal.

When configured as an input, this signal receives an external frame sync signal for the transmitter in asynchronous mode and for both the transmitter and receiver when in synchronous mode.

SC2 can be programmed as a GPIO signal (P2) when the ESSI SC2 function is not in use.

7.4 ESSI PROGRAMMING MODEL

The ESSI is composed of the following registers:

- Two control registers (CRA, CRB)
- One status register (SSISR)
- Three transmit data registers (TX0, TX1, TX2)
- One receive data register (RX)
- Two transmit slot mask registers (TSMA, TSMB)
- Two receive slot mask registers (RSMA, RSMB)
- One special-purpose time slot register (TSR)

The following paragraphs document each of the bits in the ESSI registers. **Section 7.6** documents the GPIO of the ESSI.

11	10	9	8	7	6	5	4	3	2	1	0
PSR				PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

23	22	21	20	19	18	17	16	15	14	13	12
	SSC1	WL2	WL1	WL0	ALC		DC4	DC3	DC2	DC1	DC0

AA0857

Figure 7-2 ESSI Control Register A (CRA)
(ESSI0 X:$FFFFB5, ESSI1 X:$FFFFA5)

11	10	9	8	7	6	5	4	3	2	1	0
CKP	FSP	FSR	FSL1	FSL0	SHFD	SCKD	SCD2	SCD1	SCD0	OF1	OF0

23	22	21	20	19	18	17	16	15	14	13	12
REIE	TEIE	RLIE	TLIE	RIE	TIE	RE	TE0	TE1	TE2	MOD	SYN

AA0858

Figure 7-3 ESSI Control Register B (CRB)
(ESSI0 X:$FFFFB6, ESSI1 X:$FFFFA6)

11	10	9	8	7	6	5	4	3	2	1	0
				RDF	TDE	ROE	TUE	RFS	TFS	IF1	IF0

23	22	21	20	19	18	17	16	15	14	13	12

AA0859

Figure 7-4 ESSI Status Register (SSISR)
(ESSI0 X:$FFFFB7, ESSI1 X:$FFFFA7)

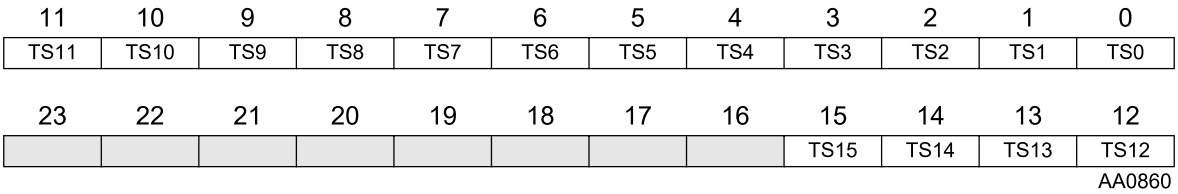


Figure 7-5 ESSI Transmit Slot Mask Register A (TSMA)
(ESSI0 X:$FFFFB4, ESSI1 X:$FFFFA4)

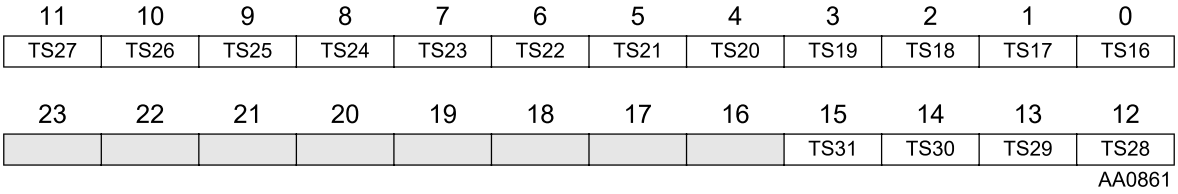


Figure 7-6 ESSI Transmit Slot Mask Register B (TSMB)
(ESSI0 X:$FFFFB3, ESSI1 X:$FFFFA3)

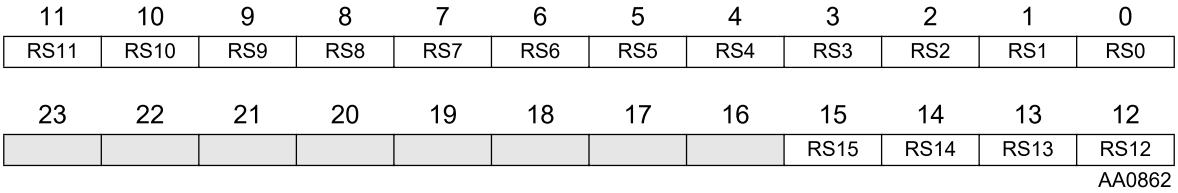


Figure 7-7 ESSI Receive Slot Mask Register A (RSMA)
(ESSI0 X:$FFFFB2, ESSI1 X:$FFFFA2)

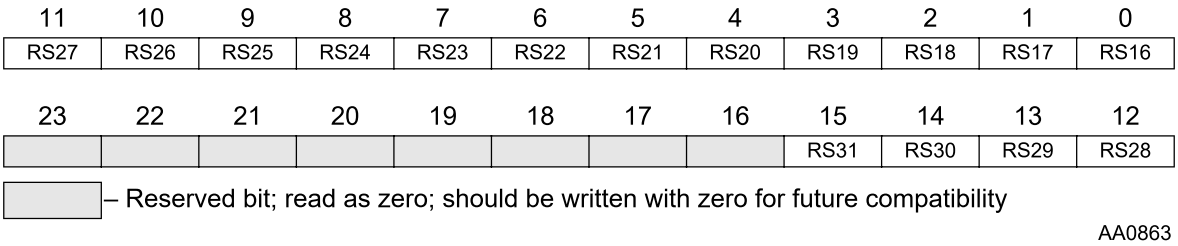


Figure 7-8 ESSI Receive Slot Mask Register B (RSMB)
(ESSI0 X:$FFFFB1, ESSI1 X:$FFFFA1)

7.4.1 ESSI Control Register A (CRA)

The ESSI Control Register A (CRA) is one of two 24-bit read/write control registers used to direct the operation of the ESSI. CRA controls the ESSI clock generator bit and frame sync rates, word length, and number of words per frame for serial data. The CRA control bits are documented in the following paragraphs and in **Figure 7-2**.

7.4.1.1 CRA Prescale Modulus Select PM[7:0] Bits 7–0

The PM[7:0] bits specify the divide ratio of the prescale divider in the ESSI clock generator. A divide ratio from 1 to 256 (PM = $0 to $FF) can be selected. The bit clock output is available at the transmit clock signal (SCK) and/or the receive clock (SC0) signal of the DSP. The bit clock output is also available internally for use as the bit clock to shift the transmit and receive shift registers. The ESSI clock generator functional diagram is shown in **Figure 7-9**. F_{core} is the DSP56307 core clock frequency (the same frequency as the CLKOUT signal when that signal is enabled). Careful choice of the crystal oscillator frequency and the prescaler modulus generates the industry-standard codec master clock frequencies of 2.048 MHz, 1.544 MHz, and 1.536 MHz.

Both the hardware $\overline{\text{RESET}}$ signal and the software RESET instruction clear PM[7:0].

7.4.1.2 CRA Reserved Bits 8–10

These bits are reserved. They are read as 0 and should be written with 0.

7.4.1.3 CRA Prescaler Range (PSR) Bit 11

The PSR controls a fixed divide-by-eight prescaler in series with the variable prescaler. This bit is used to extend the range of the prescaler for those cases where a slower bit clock is needed. When PSR is set, the fixed prescaler is bypassed. When PSR is cleared, the fixed divide-by-eight prescaler is operational, as in **Figure 7-9**.

This definition is reversed from that of the SSI in other members of the DSP56000 family.

The maximum allowed internally generated bit clock frequency is the internal DSP56307 clock frequency divided by 4; the minimum possible internally generated bit clock frequency is the DSP56307 internal clock frequency divided by 4096.

Both the hardware $\overline{\text{RESET}}$ signal and the software RESET instruction clear PSR.

Note: The combination PSR = 1 and PM[7:0] = $00 (dividing F_{core} by 2) can cause synchronization problems and thus should not be used.

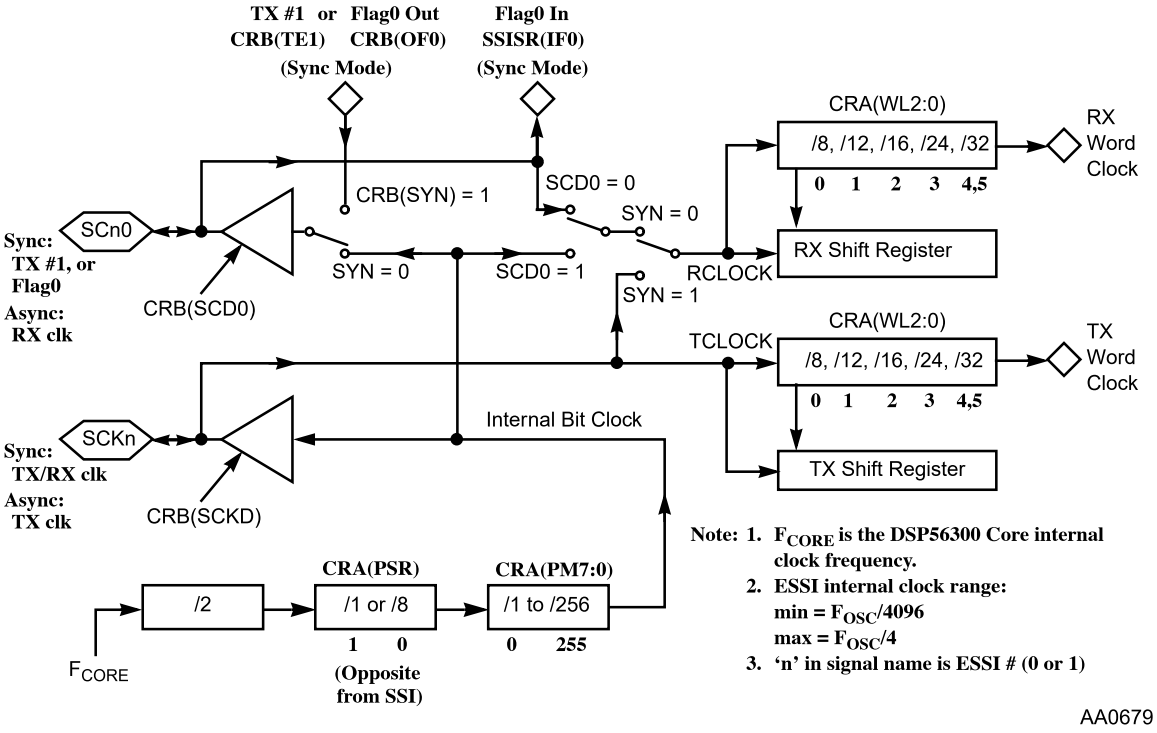


Figure 7-9 ESSI Clock Generator Functional Block Diagram

7.4.1.4 CRA Frame Rate Divider Control DC[4:0] Bits 16–12

The values of the DC[4:0] bits control the divide ratio for the programmable frame rate dividers used to generate the frame clocks. In network mode, this ratio can be interpreted as the number of words per frame minus one. In normal mode, this ratio determines the word transfer rate.

The divide ratio can range from 1 to 32 (DC = 00000 to 11111) for normal mode and 2 to 32 (DC = 00001 to 11111) for network mode. A divide ratio of one (DC = 00000) in network mode is a special case known as on-demand mode. In normal mode, a divide ratio of one (DC = 00000) provides continuous periodic data word transfers. A bit-length frame sync must be used in this case; you select it by setting the FSL[1:0] bits in the CRA to (01).

Both the hardware $\overline{\text{RESET}}$ signal and the software RESET instruction clear DC[4:0].

The ESSI frame sync generator functional diagram is shown in **Figure 7-10**.

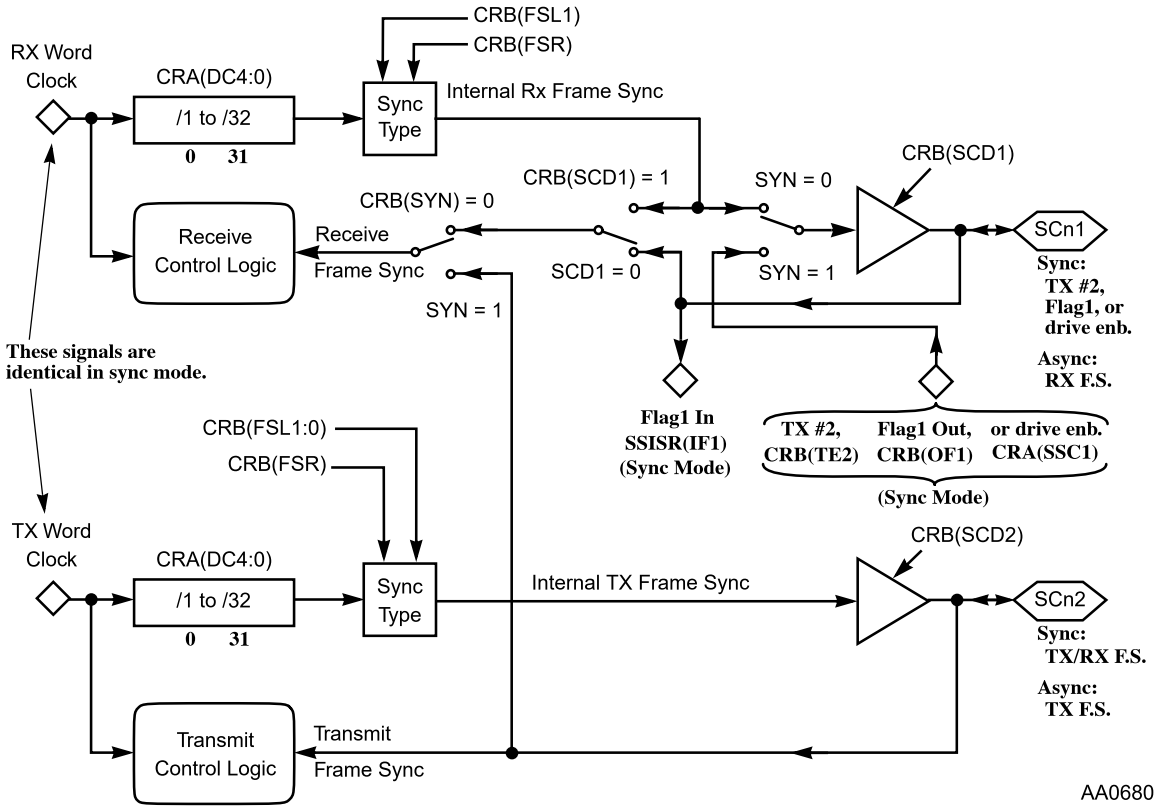


Figure 7-10 ESSI Frame Sync Generator Functional Block Diagram

7.4.1.5 CRA Reserved Bit 17

This bit is reserved. It is read as 0 and should be written with 0.

7.4.1.6 CRA Alignment Control (ALC) Bit 18

The ESSI handles 24-bit fractional data. Shorter data words are left-aligned to the MSB, bit 23. For applications that use 16-bit fractional data, shorter data words are left-aligned to bit 15. The ALC bit supports shorter data words. If ALC is set, received words are left-aligned to bit 15 in the receive shift register. Transmitted words must be left-aligned to bit 15 in the transmit shift register. If the ALC bit is cleared, received words are left-aligned to bit 23 in the receive shift register. Transmitted words must be left-aligned to bit 23 in the transmit shift register. The ALC bit is cleared by either a hardware $\overline{\text{RESET}}$ signal or a software RESET instruction.

Note: If the ALC bit is set, only 8-, 12-, or 16-bit words should be used. The use of 24- or 32-bit words leads to unpredictable results.

7.4.1.7 CRA Word Length Control (WL[2:0]) Bits 21–19

The WL[2:0] bits select the length of the data words transferred via the ESSI. Word lengths of 8-, 12-, 16-, 24-, or 32-bits can be selected, as in **Table 7-2**. The ESSI data path programming model in **Figure 7-16** and **Figure 7-17** shows additional information about how to select different length data words. The ESSI data registers are 24 bits long. The ESSI transmits 32-bit words either by duplicating the last bit 8 times when WL[2:0] = 100, or by duplicating the first bit 8 times when WL[2:0] = 101. The WL[2:0] bits are cleared by a hardware $\overline{\text{RESET}}$ signal or by a software RESET instruction.

Table 7-2 ESSI Word Length Selection

WL2	WL1	WL0	Number of Bits/Word
0	0	0	8
0	0	1	12
0	1	0	16
0	1	1	24
1	0	0	32 (valid data in the first 24 bits)
1	0	1	32 (valid data in the last 24 bits)
1	1	0	Reserved
1	1	1	Reserved

7.4.1.8 CRA Select SC1 (SSC1) Bit 22

The SSC1 bit controls the functionality of the SC1 signal. If SSC1 is set, the ESSI is configured in Synchronous mode (the CRB synchronous/asynchronous bit (SYN) is set), and transmitter 2 is disabled (transmit enable (TE2) = 0)), then the SC1 signal acts as the transmitter 0 driver-enabled signal while the SC1 signal is configured as output (SCD1 = 1). This configuration enables an external buffer for the transmitter 0 output.

If SSC1 is cleared, the ESSI is configured in synchronous mode (SYN = 1), and transmitter 2 is disabled (TE2 = 0), then the SC1 acts as the serial I/O flag while the SC1 signal is configured as output (SCD1 = 1).

7.4.1.9 CRA Reserved Bit 23

This bit is reserved. It is read as 0 and should be written with 0.

7.4.2 ESSI Control Register B (CRB)

Control Register B (CRB) is one of two 24-bit read/write control registers that direct the operation of the ESSI, as shown in **Figure 7-3** on page 7-9. CRB controls the ESSI multifunction signals, SC[2:0], which can be used as clock inputs or outputs, frame synchronization signals, transmit data signals, or serial I/O flag signals.

The serial output flag control bits and the direction control bits for the serial control signals are in the ESSI CRB. Interrupt enable bits for the receiver and the transmitter are also in the CRB. The bit setting of the CRB also determines how many transmitters are enabled; 0, 1, 2, or 3 transmitters can be enabled. The CRB settings also determine the ESSI operating mode.

Either a hardware $\overline{\text{RESET}}$ signal or a software RESET instruction clear all the bits in the CRB.

The relationship between the ESSI signals SC[2:0], SCK, and the CRB bits is summarized in **Table 7-4** on page 7-24. The ESSI CRB bits are described in the following paragraphs.

7.4.2.1 CRB Serial Output Flags (OF0, OF1) Bits 0, 1

The ESSI has two serial output flag bits, OF1 and OF0. The normal sequence follows for setting output flags when transmitting data (by transmitter 0 through the STD signal only).

1. Wait for TDE (TX0 empty) to be set.
2. Write the flags.
3. Write the transmit data to the TX register.

Bits OF0 and OF1 are double-buffered so that the flag states appear on the signals when the TX data is transferred to the transmit shift register. The flag bit values are synchronized with the data transfer.

Note: The timing of the optional serial output signals SC[2:0] is controlled by the frame timing and is not affected by the settings of TE2, TE1, TE0, or the receive enable (RE) bit of the CRB.

7.4.2.1.1 CRB Serial Output Flag 0 (OF0) Bit 0

When the ESSI is in synchronous mode and transmitter 1 is disabled (TE1 = 0), the SC0 signal is configured as ESSI flag 0. If the serial control direction bit (SCD0) is set, the SC0 signal is an output. Data present in Bit OF0 is written to SC0 at the beginning of the frame in normal mode or at the beginning of the next time slot in network mode.

Bit OF0 is cleared by a hardware $\overline{\text{RESET}}$ signal or by a software RESET instruction.

7.4.2.1.2 CRB Serial Output Flag 1 (OF1) Bit 1

When the ESSI is in synchronous mode and transmitter 2 is disabled (TE2 = 0), the SC1 signal is configured as ESSI flag 1. If the serial control direction bit (SCD1) is set, the SC1 signal is an output. Data present in bit OF1 is written to SC1 at the beginning of the frame in normal mode or at the beginning of the next time slot in network mode.

Bit OF1 is cleared by a hardware $\overline{\text{RESET}}$ signal or by a software RESET instruction.

7.4.2.2 CRB Serial Control Direction 0 (SCD0) Bit 2

In synchronous mode (SYN = 1) when transmitter 1 is disabled (TE1 = 0), or in asynchronous mode (SYN = 0), SCD0 controls the direction of the SC0 I/O signal. When SCD0 is set, SC0 is an output; when SCD0 is cleared, SC0 is an input.

When TE1 is set, the value of SCD0 is ignored and the SC0 signal is always an output.

Bit SCD0 is cleared by a hardware $\overline{\text{RESET}}$ signal or by a software RESET instruction.

7.4.2.3 CRB Serial Control Direction 1 (SCD1) Bit 3

In synchronous mode (SYN = 1) when transmitter 2 is disabled (TE2 = 0), or in asynchronous mode (SYN = 0), SCD1 controls the direction of the SC1 I/O signal. When SCD1 is set, SC1 is an output; when SCD1 is cleared, SC1 is an input.

When TE2 is set, the value of SCD1 is ignored and the SC1 signal is always an output.

Bit SCD1 is cleared by a hardware $\overline{\text{RESET}}$ signal or by a software RESET instruction.

7.4.2.4 CRB Serial Control Direction 2 (SCD2) Bit 4

SCD2 controls the direction of the SC2 I/O signal. When SCD2 is set, SC2 is an output; when SCD2 is cleared, SC2 is an input. SCD2 is cleared by a hardware $\overline{\text{RESET}}$ signal or by a software RESET instruction.

7.4.2.5 CRB Clock Source Direction (SCKD) Bit 5

SCKD selects the source of the clock signal that clocks the transmit shift register in asynchronous mode and both the transmit and receive shift registers in synchronous mode. If SCKD is set and the ESSI is in synchronous mode, the internal clock is the source of the clock signal used for all the transmit shift registers and the receive shift register. If SCKD is set and the ESSI is in asynchronous mode, the internal clock source becomes the bit clock for the transmit shift register and word length divider. The internal clock is output on the SCK signal.

When SCKD is cleared, the external clock source is selected. The internal clock generator is disconnected from the SCK signal, and an external clock source may drive this signal.

Either a hardware $\overline{\text{RESET}}$ signal or a software RESET instruction clears SCKD.

7.4.2.6 CRB Shift Direction (SHFD) Bit 6

The SHFD bit determines the shift direction of the transmit or receive shift register. If SHFD is set, data is shifted in and out with the LSB first. If SHFD is cleared, data is shifted in and out with the MSB first, as in **Figure 7-16** on page 7-30 and **Figure 7-17** on page 7-31.

Either a hardware $\overline{\text{RESET}}$ signal or a software RESET instruction clears SHFD.

7.4.2.7 CRB Frame Sync Length FSL[1:0] Bits 7 and 8

These bits select the length of frame sync to be generated or recognized, as in **Figure 7-11** on page 7-19, **Figure 7-14** on page 7-22, and **Figure 7-15** on page 7-23. **Table 7-3** shows the values of FSL[1:0].

Table 7-3 FSL1 and FSL0 Encoding

FSL1	FSL0	Frame Sync Length	
		RX	TX
0	0	word	word
0	1	word	bit
1	0	bit	bit
1	1	bit	word

Either a hardware $\overline{\text{RESET}}$ signal or a software RESET instruction clears FSL[1:0].

7.4.2.8 CRB Frame Sync Relative Timing (FSR) Bit 9

The FSR bit determines the relative timing of the receive and transmit frame sync signal in reference to the serial data lines for word length frame sync only. When FSR is cleared, the word length frame sync occurs together with the first bit of the data word of the first slot. When FSR is set, the word length frame sync occurs one serial clock cycle earlier (i.e., simultaneously with the last bit of the previous data word).

Either a hardware $\overline{\text{RESET}}$ signal or a software RESET instruction clears FSR.

7.4.2.9 CRB Frame Sync Polarity (FSP) Bit 10

The FSP bit determines the polarity of the receive and transmit frame sync signals. When FSP is cleared, the frame sync signal polarity is positive; that is, the frame start is indicated by the frame sync signal going high. When FSP is set, the frame sync signal polarity is negative; that is, the frame start is indicated by the frame sync signal going low.

Either a hardware $\overline{\text{RESET}}$ signal or a software RESET instruction clears FRB.

7.4.2.10 CRB Clock Polarity (CKP) Bit 11

The CKP bit controls which bit clock edge data and frame sync are clocked out and latched in.

If CKP is cleared, the data and the frame sync are clocked out on the rising edge of the transmit bit clock and latched in on the falling edge of the receive bit clock.

If CKP is set, the data and the frame sync are clocked out on the falling edge of the transmit bit clock and latched in on the rising edge of the receive bit clock.

Either a hardware $\overline{\text{RESET}}$ signal or a software RESET instruction clears CKP.

7.4.2.11 CRB Synchronous/Asynchronous (SYN) Bit 12

SYN controls whether the receive and transmit functions of the ESSI occur synchronously or asynchronously with respect to each other. (See **Figure 7-12** on page 7-20.)

When SYN is cleared, the ESSI is in asynchronous mode, and separate clock and frame sync signals are used for the transmit and receive sections.

When SYN is set, the ESSI is in synchronous mode, and the transmit and receive sections use common clock and frame sync signals. Only in synchronous mode can more than one transmitter be enabled.

Either a hardware $\overline{\text{RESET}}$ signal or a software RESET instruction clears SYN.

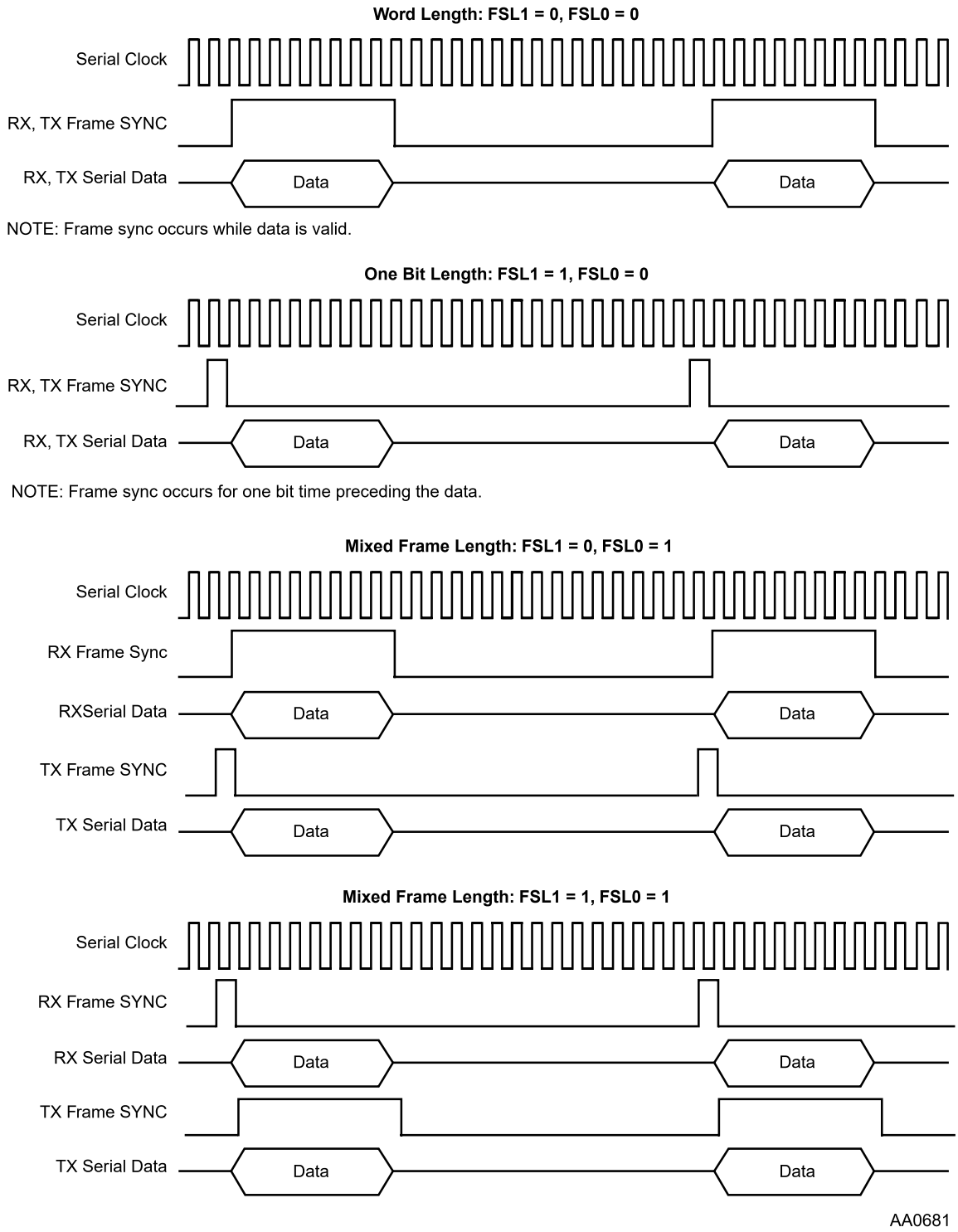


Figure 7-11 CRB FSL0 and FSL1 Bit Operation (FSR = 0)

7.4.2.12 CRB ESSI Mode Select (MOD) Bit 13

MOD selects the operational mode of the ESSI, as in **Figure 7-13** on page 7-21, **Figure 7-14** on page 7-22, and **Figure 7-15** on page 7-23. When MOD is cleared, the normal mode is selected; when MOD is set, the network mode is selected. In normal mode, the frame rate divider determines the word transfer rate: one word is transferred per frame sync during the frame sync time slot. In network mode, a word can be transferred every time slot. For details, see **Section 7.5**. Either a hardware $\overline{\text{RESET}}$ signal or a software RESET instruction clears MOD.

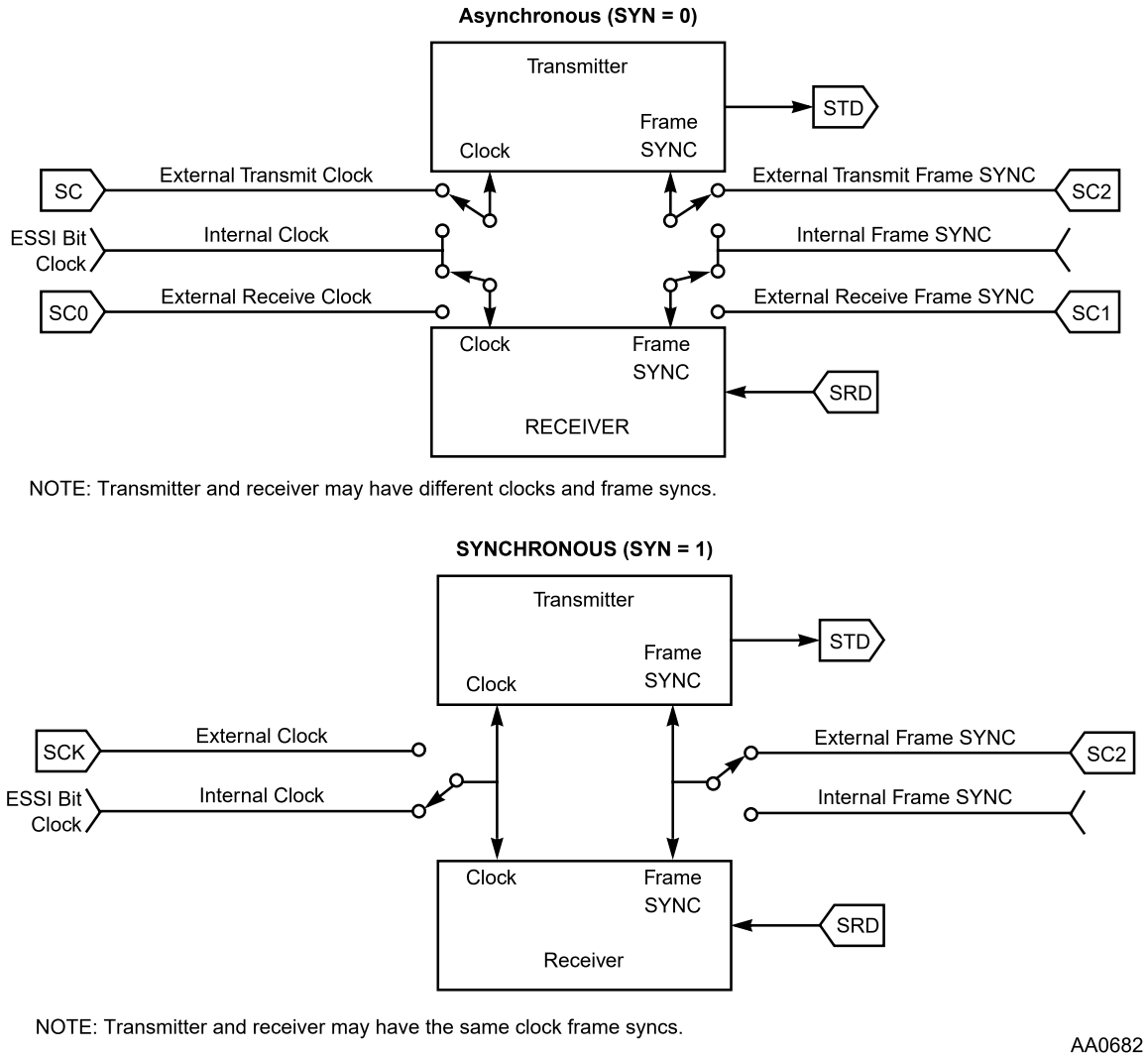


Figure 7-12 CRB SYN Bit Operation

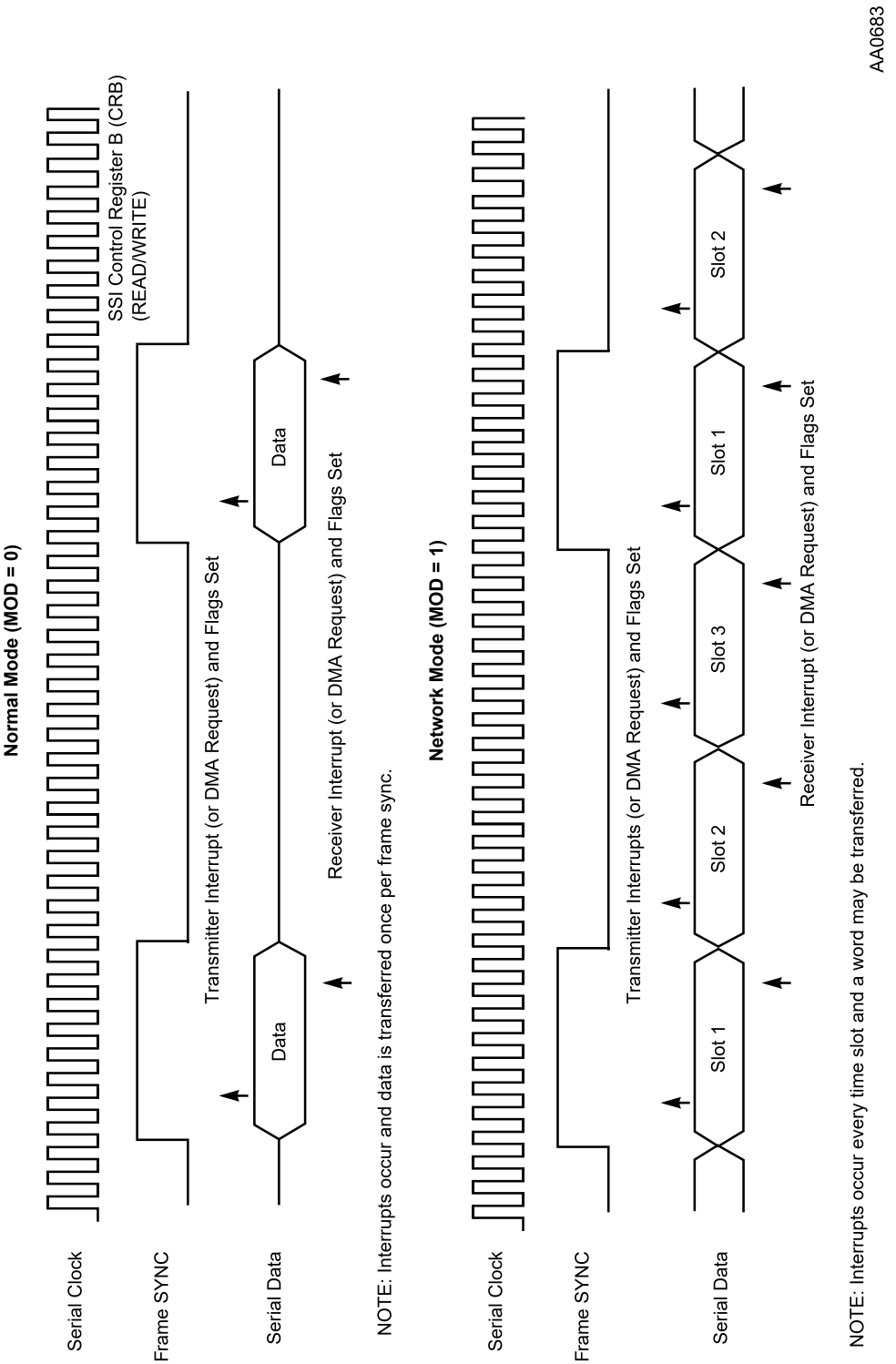


Figure 7-13 CRB MOD Bit Operation

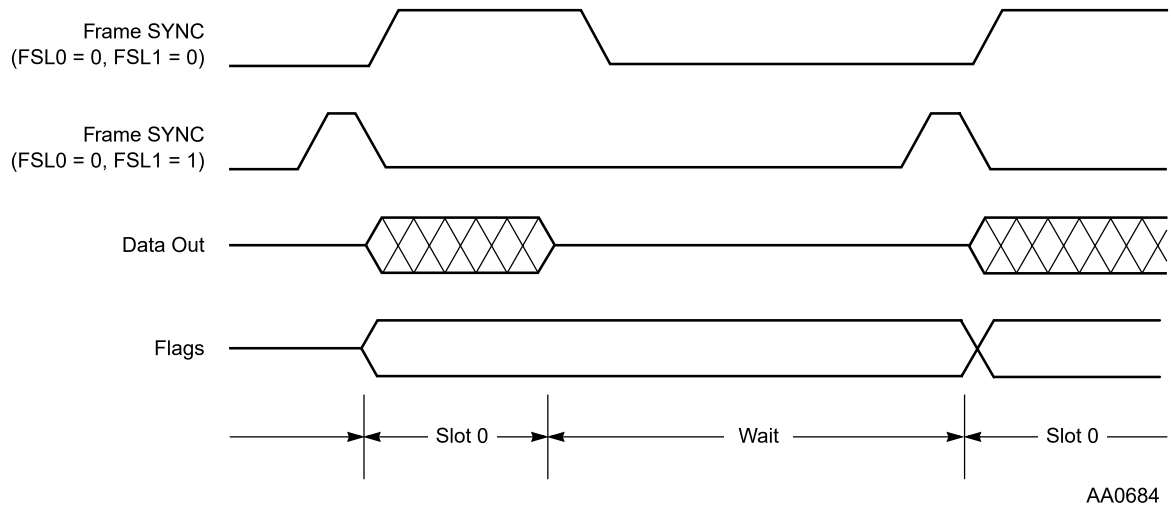


Figure 7-14 Normal Mode, External Frame Sync (8 Bit, 1 Word in Frame)

7.4.2.13 Enabling, Disabling ESSI Data Transmission

The ESSI has three transmit enable bits (TE[2:0]), one for each data transmitter. The process of transmitting data from TX1 and TX2 is the same. TX0 differs from those two bits in that it can also operate in asynchronous mode. The normal transmit enable sequence is to write data to one or more transmit data registers (or the time slot register (TSR)) before you set the TE bit. The normal transmit disable sequence is to set the transmit data empty (TDE) bit and then to clear the TE, transmit interrupt enable (TIE), and transmit exception interrupt enable (TEIE) bits. In network mode, if you clear the appropriate TE bit and set it again, then you disable the corresponding transmitter (0, 1, or 2) after transmission of the current data word. The transmitter remains disabled until the beginning of the next frame. During that time period, the corresponding SC (or STD in the case of TX0) signal remains in a high-impedance state.

7.4.2.14 CRB ESSI Transmit 2 Enable (TE2) Bit 14

The TE2 bit enables the transfer of data from TX2 to transmit shift register 2. TE2 is functional only when the ESSI is in synchronous mode and is ignored when the ESSI is in asynchronous mode.

When TE2 is set and a frame sync is detected, transmitter 2 is enabled for that frame.

When TE2 is cleared, transmitter 2 is disabled after completing transmission of data currently in the ESSI transmit shift register. Any data present in TX2 is not transmitted. If TE2 is cleared, data can be written to TX2; the TDE bit is cleared, but data is not transferred to transmit shift register 2.

If the TE2 bit is kept cleared until the start of the next frame, it causes the SC1 signal to act as a serial I/O flag from the start of the frame in both normal and network mode. The

transmit enable sequence in on-demand mode can be the same as in normal mode, or the TE2 bit can be left enabled.

The TE2 bit is cleared by either a hardware $\overline{\text{RESET}}$ signal or a software RESET instruction.

Note: The setting of the TE2 bit does not affect the generation of frame sync or output flags.

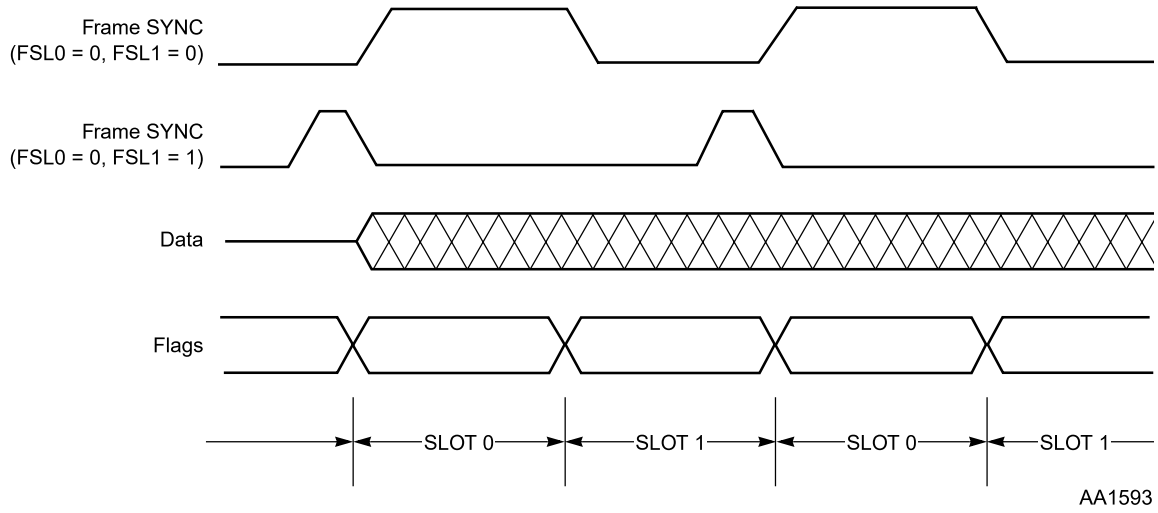


Figure 7-15 Network Mode, External Frame Sync (8 Bit, 2 Words in Frame)

7.4.2.15 CRB ESSI Transmit 1 Enable (TE1) Bit 15

The TE1 bit enables the transfer of data from TX1 to Transmit Shift Register 1. TE1 is functional only when the ESSI is in synchronous mode and is ignored when the ESSI is in asynchronous mode.

When TE1 is set and a frame sync is detected, transmitter 1 is enabled for that frame.

When TE1 is cleared, transmitter 1 is disabled after completing transmission of data currently in the ESSI transmit shift register. Any data present in TX1 is not transmitted. If TE1 is cleared, data can be written to TX1; the TDE bit is cleared, but data is not transferred to transmit shift register 1.

If the TE1 bit is kept cleared until the start of the next frame, it causes the SC0 signal to act as serial I/O flag from the start of the frame in both normal and network mode. The transmit enable sequence in on-demand mode can be the same as in normal mode, or the TE1 bit can be left enabled.

The TE1 bit is cleared by either a hardware $\overline{\text{RESET}}$ signal or a software RESET instruction.

Note: The TE1 bit does not affect the generation of frame sync or output flags.

7.4.2.16 CRB ESSI Transmit 0 Enable (TE0) Bit 16

The TE0 bit enables the transfer of data from TX1 to transmit shift register 0. TE0 is functional when the ESSI is in either synchronous or asynchronous mode.

When TE0 is set and a frame sync is detected, the transmitter 0 is enabled for that frame.

When TE0 is cleared, transmitter 0 is disabled after the transmission of data currently in the ESSI transmit shift register. The STD output is tri-stated, and any data present in TX0 is not transmitted. In other words, data can be written to TX0 with TE0 cleared; the TDE bit is cleared, but data is not transferred to the transmit shift register 0.

The TE0 bit is cleared by either a hardware $\overline{\text{RESET}}$ signal or a software RESET instruction.

The transmit enable sequence in on-demand mode can be the same as in normal mode, or TE0 can be left enabled.

Note: Transmitter 0 is the only transmitter that can operate in asynchronous mode (SYN = 0). TE0 does not affect the generation of frame sync or output flags.

Table 7-4 Mode and Signal Definition Table

Control Bits					ESSI Signals					
SYN	**TE0**	**TE1**	**TE2**	**RE**	**SC0**	**SC1**	**SC2**	**SCK**	**STD**	**SRD**
0	0	X	X	0	U	U	U	U	U	U
0	0	X	X	1	RXC	FSR	U	U	U	RD
0	1	X	X	0	U	U	FST	TXC	TD0	U
0	1	X	X	1	RXC	FSR	FST	TXC	TD0	RD
1	0	0	0	0	U	U	U	U	U	U
1	0	0	0	1	F0/U	F1/T0D/U	FS	XC	U	RD
1	0	0	1	0	F0/U	TD2	FS	XC	U	U
1	0	0	1	1	F0/U	TD2	FS	XC	U	RD
1	0	1	0	0	TD1	F1/T0D/U	FS	XC	U	U
1	0	1	0	1	TD1	F1/T0D/U	FS	XC	U	RD
1	0	1	1	0	TD1	TD2	FS	XC	U	U

Table 7-4 Mode and Signal Definition Table (Continued)

Control Bits					ESSI Signals					
SYN	**TE0**	**TE1**	**TE2**	**RE**	**SC0**	**SC1**	**SC2**	**SCK**	**STD**	**SRD**
1	0	1	1	1	TD1	TD2	FS	XC	U	RD
1	1	0	0	0	F0/U	F1/T0D/U	FS	XC	TD0	U
1	1	0	0	1	F0/U	F1/T0D/U	FS	XC	TD0	RD
1	1	0	1	0	F0/U	TD2	FS	XC	TD0	U
1	1	0	1	1	F0/U	TD2	FS	XC	TD0	RD
1	1	1	0	0	TD1	F1/T0D/U	FS	XC	TD0	U
1	1	1	0	1	TD1	F1/T0D/U	FS	XC	TD0	RD
1	1	1	1	0	TD1	TD2	FS	XC	TD0	U
1	1	1	1	1	TD1	TD2	FS	XC	TD0	RD

TXC = Transmitter clock
RXC = Receiver clock
XC = Transmitter/receiver clock (synchronous operation)
FST = Transmitter frame sync
FSR = Receiver frame sync
FS = Transmitter/receiver frame sync (synchronous operation)
TD0 = Transmit data signal 0
TD1 = Transmit data signal 1
TD2 = Transmit data signal 2
T0D = Transmitter 0 drive enable if SSC1 = 1 & SCD1 = 1
RD = Receive data
F0 = Flag 0
F1 = Flag 1 if SSC1 = 0
U = Unused (can be used as GPIO signal)
X = Indeterminate

7.4.2.17 CRB ESSI Receive Enable (RE) Bit 17

When the RE bit is set, the receive portion of the ESSI is enabled. When this bit is cleared, the receiver is disabled: data transfer into RX is inhibited. If data is being received while this bit is cleared, the remainder of the word is shifted in and transferred to the ESSI receive data register.

RE must be set in both normal and on-demand modes for the ESSI to receive data. In network mode, clearing RE and setting it again disables the receiver after reception of

the current data word. The receiver remains disabled until the beginning of the next data frame.

RE is cleared by either a hardware $\overline{\text{RESET}}$ signal or a software RESET instruction.

Note: The setting of the RE bit does not affect the generation of a frame sync.

7.4.2.18 CRB ESSI Transmit Interrupt Enable (TIE) Bit 18

When the TIE bit is set, it enables a DSP transmit interrupt; the interrupt is generated when both the TIE and the TDE bits in the ESSI status register are set. When TIE is cleared, the transmit interrupt is disabled. The transmit interrupt is documented in **Section 7.5.3**. When data is written to the data registers of the enabled transmitters or to the TSR, it clears TDE and also clears the interrupt.

Transmit interrupts with exception conditions have higher priority than normal transmit data interrupts. If the transmitter underrun error (TUE) bit is set (signaling that an exception has occurred) and the TEIE bit is set, the ESSI requests an SSI transmit data with exception interrupt from the interrupt controller.

TIE is cleared by either a hardware $\overline{\text{RESET}}$ signal or a software RESET instruction.

7.4.2.19 CRB ESSI Receive Interrupt Enable (RIE) Bit 19

When the RIE bit is set, it enables a DSP receive data interrupt; the interrupt is generated when both the RIE and receive data register full (RDF) bit (in the SSISR) are set. When RIE is cleared, this interrupt is disabled. The receive interrupt is documented in **Section 7.5.3**. When the receive data register is read, it clears RDF and the pending interrupt. Receive interrupts with exception have higher priority than normal receive data interrupts. If the receiver overrun error (ROE) bit is set (signaling that an exception has occurred) and the REIE bit is set, the ESSI requests an SSI receive data with exception interrupt from the interrupt controller.

RIE is cleared by either a hardware $\overline{\text{RESET}}$ signal or a software RESET instruction.

7.4.2.20 Transmit Last Slot Interrupt Enable (TLIE) Bit 20

When the TLIE bit is set, it enables an interrupt at the beginning of the last slot of a frame when the ESSI is in network mode. When TLIE is set, the DSP is interrupted at the start of the last slot in a frame regardless of the transmit mask register setting. When TLIE is cleared, the transmit last slot interrupt is disabled. The transmit last slot interrupt is documented in **Section 7.5.3**.

TLIE is cleared by either a hardware $\overline{\text{RESET}}$ signal or a software RESET instruction. TLIE is disabled when the ESSI is in on-demand mode (DC = $0).

7.4.2.21 Receive Last Slot Interrupt Enable (RLIE) Bit 21

When the RLIE bit is set, it enables an interrupt after the last slot of a frame ends when the ESSI is in network mode. When RLIE is set, the DSP is interrupted after the last slot in a frame ends regardless of the receive mask register setting. When RLIE is cleared, the receive last slot interrupt is disabled. The use of the receive last slot interrupt is documented in **Section 7.5.3**.

RLIE is cleared by either a hardware $\overline{\text{RESET}}$ signal or a software RESET instruction. RLIE is disabled when the ESSI is in on-demand mode (DC = $0).

7.4.2.22 Transmit Exception Interrupt Enable (TEIE) Bit 22

When the TEIE bit is set, the DSP is interrupted when both TDE and TUE in the ESSI status register are set. When TEIE is cleared, this interrupt is disabled. The use of the transmit interrupt is documented in **Section 7.5.3**. A read of the status register, followed by a write to all the data registers of the enabled transmitters, clears both TUE and the pending interrupt.

TEIE is cleared by either a hardware $\overline{\text{RESET}}$ signal or a software RESET instruction.

7.4.2.23 Receive Exception Interrupt Enable (REIE) Bit 23

When the REIE bit is set, the DSP is interrupted when both RDF and ROE in the ESSI status register are set. When REIE is cleared, this interrupt is disabled. The receive interrupt is documented in **Section 7.5.3**. A read of the status register followed by a read of the receive data register clears both ROE and the pending interrupt.

REIE is cleared by either a hardware $\overline{\text{RESET}}$ signal or a software RESET instruction.

7.4.3 ESSI Status Register (SSISR)

The SSISR (in **Figure 7-4** on page 7-9) is a 24-bit read-only status register used by the DSP to read the status and serial input flags of the ESSI. The SSISR bits are documented in the following paragraphs.

7.4.3.1 SSISR Serial Input Flag 0 (IF0) Bit 0

The IF0 bit is enabled only when SC0 is an input flag and the synchronous mode is selected; that is, when SC0 is programmed as ESSI in the port control register (PCR), the SYN bit is set, and the TE1 and SCD0 bits are cleared.

The ESSI latches any data present on the SC0 signal during reception of the first received bit after the frame sync is detected. The IF0 bit is updated with this data when the data in the receive shift register is transferred into the receive data register.

If it is not enabled, the IF0 bit is cleared.

A hardware $\overline{\text{RESET}}$ signal, software RESET instruction, ESSI individual reset, or STOP instruction reset all clear the IF0 bit.

7.4.3.2 SSISR Serial Input Flag 1 (IF1) Bit 1

The IF1 bit is enabled only when SC1 is an input flag and synchronous mode is selected; that is, when SC1 is programmed as ESSI in the port control register (PCR), the SYN bit is set, and the TE2 and SCD1 bits are cleared.

The ESSI latches any data present on the SC1 signal during reception of the first received bit after the frame sync is detected. The IF1 bit is updated with this data when the data in the receive shift register is transferred into the receive data register.

If it is not enabled, the IF1 bit is cleared.

A hardware $\overline{\text{RESET}}$ signal, software RESET instruction, ESSI individual reset, or STOP instruction reset all clear the IF1 bit.

7.4.3.3 SSISR Transmit Frame Sync Flag (TFS) Bit 2

When set, TFS indicates that a transmit frame sync occurred in the current time slot. TFS is set at the start of the first time slot in the frame and cleared during all other time slots. If the transmitter is enabled, data written to a transmit data register during the time slot when TFS is set is transmitted (in network mode) during the second time slot in the frame. TFS is useful in network mode to identify the start of a frame. TFS is valid only if at least one transmitter is enabled (i.e., when TE0, TE1, or TE2 is set).

A hardware $\overline{\text{RESET}}$ signal, software RESET instruction, ESSI individual reset, or STOP instruction reset all clear TFS.

Note: In normal mode, TFS is always read as 1 when data is being transmitted because there is only one time slot per frame, the frame sync time slot.

7.4.3.4 SSISR Receive Frame Sync Flag (RFS) Bit 3

When set, the RFS bit indicates that a receive frame sync occurred during the reception of a word in the serial receive data register. In other words, the data word is from the first time slot in the frame. When the RFS bit is cleared and a word is received, it indicates (only in network mode) that the frame sync did not occur during reception of that word. RFS is valid only if the receiver is enabled (i.e., if the RE bit is set).

A hardware $\overline{\text{RESET}}$ signal, software RESET instruction, ESSI individual reset, or STOP instruction reset all clear RFS.

Note: In normal mode, RFS is always read as 1 when data is read because there is only one time slot per frame, the frame sync time slot.

7.4.3.5 SSISR Transmitter Underrun Error Flag (TUE) Bit 4

The TUE bit is set when at least one of the enabled serial transmit shift registers is empty (i.e., there is no new data to be transmitted) and a transmit time slot occurs. When a transmit underrun error occurs, the previous data (which is still present in the TX registers not written) is retransmitted. In normal mode, there is only one transmit time slot per frame. In network mode, there can be up to 32 transmit time slots per frame. If the TEIE bit is set, a DSP transmit underrun error interrupt request is issued when the TUE bit is set.

A hardware $\overline{\text{RESET}}$ signal, software RESET instruction, ESSI individual reset, or STOP instruction reset all clear TUE. The programmer can also clear TUE by first reading the SSISR with the TUE bit set, then writing to all the enabled transmit data registers or to the TSR.

7.4.3.6 SSISR Receiver Overrun Error Flag (ROE) Bit 5

The ROE bit is set when the serial receive shift register is filled and ready to transfer to the receive data register (RX) but RX is already full (i.e., the RDF bit is set). If the REIE bit is set, a DSP receiver overrun error interrupt request is issued when the ROE bit is set.

A hardware $\overline{\text{RESET}}$ signal, software RESET instruction, ESSI individual reset, or STOP instruction reset all clear ROE. The programmer can also clear ROE by reading the SSISR with the ROE bit set and then reading the RX.

7.4.3.7 SSISR ESSI Transmit Data Register Empty (TDE) Bit 6

The TDE bit is set when the contents of the transmit data register of every enabled transmitter are transferred to the transmit shift register. It is also set for a TSR disabled time slot period in network mode (as if data were being transmitted after the TSR has been written). When set, the TDE bit indicates that data should be written to all the TX registers of the enabled transmitters or to the TSR. The TDE bit is cleared when the DSP56307 writes to all the transmit data registers of the enabled transmitters, or when the DSP writes to the TSR to disable transmission of the next time slot. If the TIE bit is set, a DSP transmit data interrupt request is issued when TDE is set.

A hardware $\overline{\text{RESET}}$ signal, software RESET instruction, ESSI individual reset, or STOP instruction reset all clear the TDE bit.

7.4.3.8 SSISR ESSI Receive Data Register Full (RDF) Bit 7

The RDF bit is set when the contents of the receive shift register are transferred to the receive data register. The RDF bit is cleared when the DSP reads the receive data register. If RIE is set, a DSP receive data interrupt request is issued when RDF is set.

A hardware $\overline{\text{RESET}}$ signal, software RESET instruction, ESSI individual reset, or STOP instruction reset all clear the RDF bit.

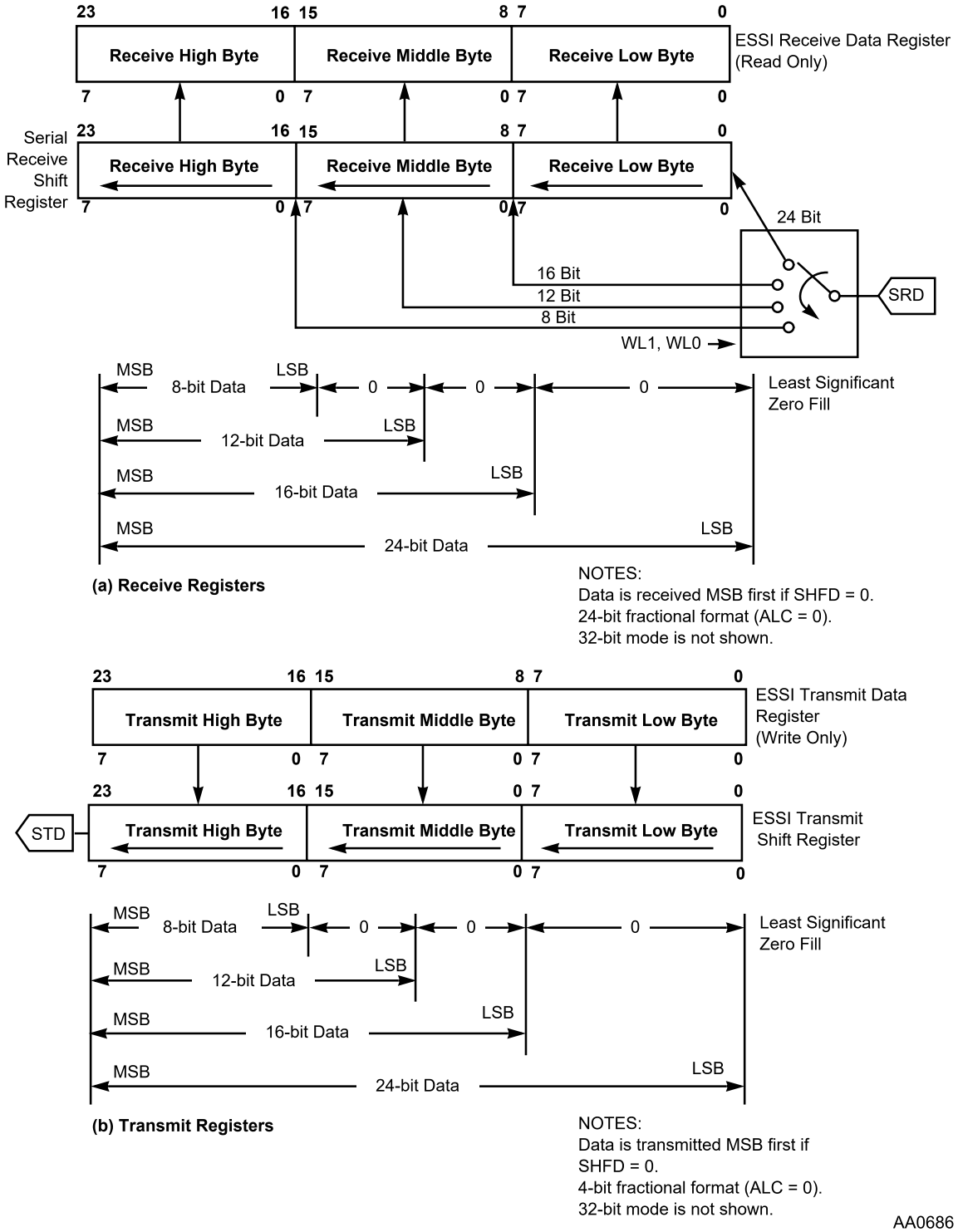


Figure 7-16 ESSI Data Path Programming Model (SHFD = 0)

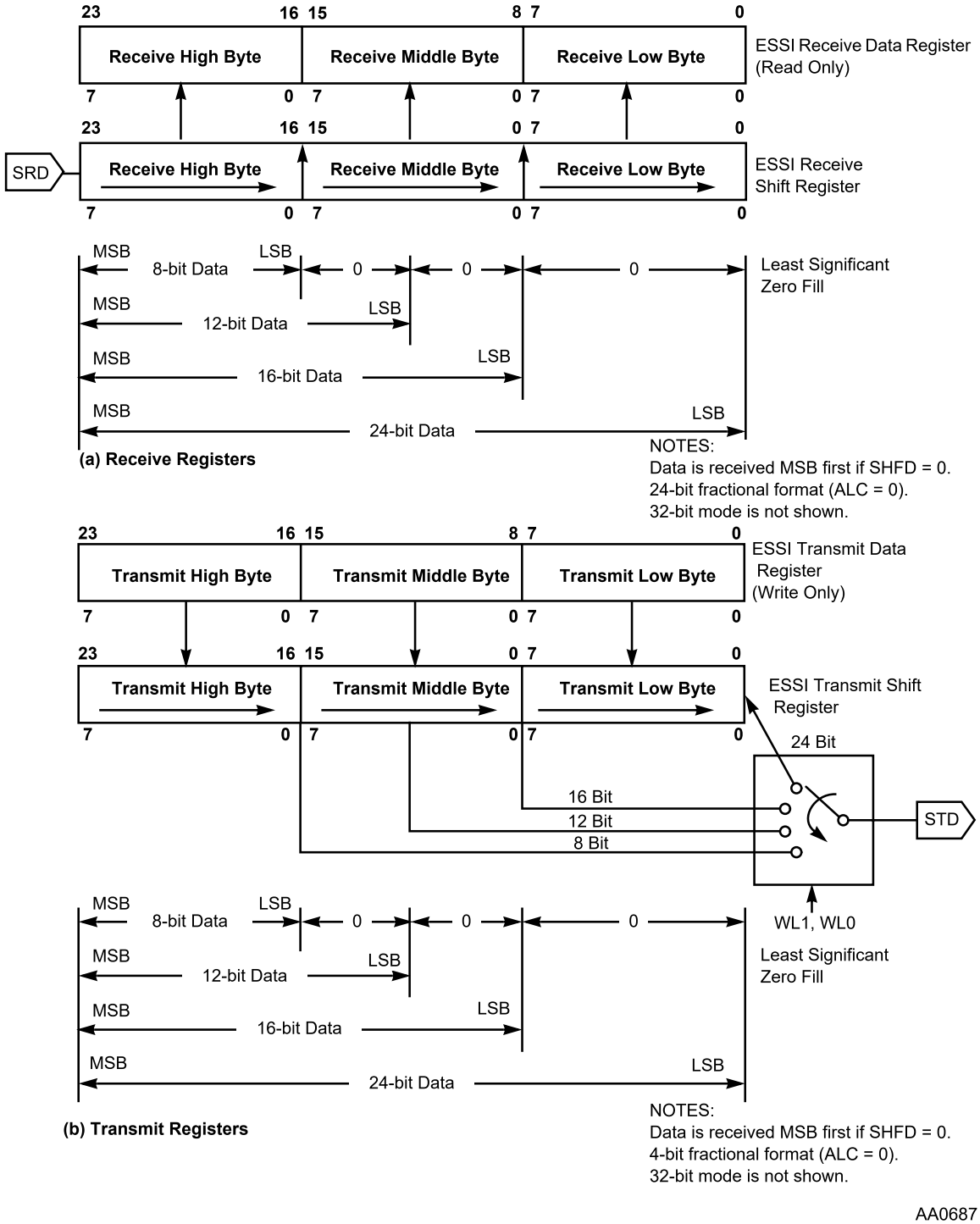


Figure 7-17 ESSI Data Path Programming Model (SHFD = 1)

7.4.4 ESSI Receive Shift Register

The 24-bit receive shift register (see **Figure 7-16** and **Figure 7-17**) receives incoming data from the serial receive data signal. Data is shifted in by the selected (internal/external) bit clock when the associated frame sync I/O is asserted. It is assumed that data is received MSB first if SHFD is cleared and LSB first if SHFD is set. Data is transferred to the ESSI receive data register after 8, 12, 16, 24, or 32 serial clock cycles have been counted, depending on the word-length control bits in the CRA.

7.4.5 ESSI Receive Data Register (RX)

The receive data register (RX) is a 24-bit read-only register that accepts data from the receive shift register as it becomes full, according to **Figure 7-16** and **Figure 7-17**. The data read is aligned according to the value of the ALC bit. When the ALC bit is cleared, the MSB is bit 23, and the least significant byte is unused. When the ALC bit is set, the MSB is bit 15, and the most significant byte is unused. Unused bits are read as 0. If the associated interrupt is enabled, the DSP is interrupted whenever the RX register becomes full.

7.4.6 ESSI Transmit Shift Registers

The three 24-bit transmit shift registers contain the data being transmitted, as in **Figure 7-16** and **Figure 7-17**. Data is shifted out to the serial transmit data signals by the selected (whether internal or external) bit clock when the associated frame sync I/O is asserted. The word-length control bits in CRA determine the number of bits that must be shifted out before the shift registers are considered empty and can be written again. Depending on the setting of the CRA, the number of bits to be shifted out can be 8, 12, 16, 24, or 32.

The data transmitted is aligned according to the value of the ALC bit. When the ALC bit is cleared, the MSB is Bit 23 and the least significant byte is unused. When ALC is set, the MSB is Bit 15 and the most significant byte is unused. Unused bits are read as 0. Data is shifted out of these registers MSB first if the SHFD bit is cleared and LSB first if the SHFD bit is set.

7.4.7 ESSI Transmit Data Registers (TX0-2)

ESSI0:TX20, TX10, TX00; ESSI1:TX21, TX11, TX01

TX2, TX1, and TX0 are 24-bit write-only registers. Data to be transmitted is written into these registers and automatically transferred to the transmit shift registers. (See **Figure 7-16** and **Figure 7-17**.) The data transmitted (8, 12, 16, or 24 bits) is aligned according to the value of the ALC bit. When the ALC bit is cleared, the MSB is Bit 23. When ALC is set, the MSB is Bit 15. If the transmit data register empty interrupt has been enabled, the DSP is interrupted whenever a transmit data register becomes empty.

Note: When data is written to a peripheral device, there is a two-cycle pipeline delay until any status bits affected by this operation are updated. If you read any of those status bits within the next two cycles, the bit does not reflect its current status. For details, see the *DSP56300 Family Manual*, *Appendix B*, *Polling a Peripheral Device for Write*.

7.4.8 ESSI Time Slot Register (TSR)

TSR is effectively a write-only null data register that prevents data transmission in the current transmit time slot. For timing purposes, TSR is a write-only register that behaves like an alternative transmit data register, except that, rather than transmitting data, the transmit data signals of all the enabled transmitters are in the high-impedance state for the current time slot.

7.4.9 Transmit Slot Mask Registers (TSMA, TSMB)

The transmit slot mask registers are two 16-bit read/write registers. When the TSMA or TSMB is read to the internal data bus, the register contents occupy the two low-order bytes of the data bus, and the high-order byte is filled by 0. In network mode the transmitter(s) use these registers to determine which action to take in the current transmission slot. Depending on the setting of the bits, the transmitter(s) either tri-state the transmitter(s) data signal(s) or transmit a data word and generate a transmitter empty condition.

TSMA and TSMB (as in **Figure 7-16** and **Figure 7-17**) can be seen as a single 32-bit register: TSM. Bit n in TSM (TSn) is an enable/disable control bit for transmission in slot number N. When TSn is cleared, all the transmit data signals of the enabled transmitters are tri-stated during transmit time slot number N. The data is still transferred from the enabled transmit data register(s) to the transmit shift register. However, the TDE and the TUE flags are not set. Consequently, during a disabled slot, no transmitter empty

interrupt is generated. The DSP is interrupted only for enabled slots. Data written to the transmit data register when the transmitter empty interrupt request is being serviced is transmitted in the next enabled transmit time slot.

When TSn is set, the transmit sequence proceeds normally. Data is transferred from the TX register to the shift register during slot number N and the TDE flag is set.

The TSM slot mask does not conflict with the TSR. Even if a slot is enabled in the TSM, you can chose to write to the TSR to tri-state the signals of the enabled transmitters during the next transmission slot. Setting the bits in the TSM affects the next frame transmission. The frame being transmitted is not affected by the new TSM setting. If the TSM is read, it shows the current setting.

After a hardware $\overline{\text{RESET}}$ signal or software RESET instruction, the TSM register is reset to $FFFFFFFF; that value enables all 32 slots for data transmission.

7.4.10 Receive Slot Mask Registers (RSMA, RSMB)

The receive slot mask registers are two 16-bit read/write registers. In network mode, the receiver(s) use these registers to determine which action to take in the current time slot. Depending on the setting of the bits, the receiver(s) either tri-state the receiver(s) data signal(s) or receive a data word and generate a receiver full condition.

RSMA and RSMB (as in **Figure 7-16** and **Figure 7-17**) can be seen as one 32-bit register, RSM. Bit n in RSM (RSn) is an enable/disable control bit for time slot number N. When RSn is cleared, all the data signals of the enabled receivers are tri-stated during time slot number N. Data is transferred from the receive data register(s) to the receive shift register(s), but the RDF and ROE flags are not set. During a disabled slot, no receiver full interrupt is generated. The DSP is interrupted only for enabled slots.

When RSn is set, the receive sequence proceeds normally. Data is received during slot number N, and the RDF flag is set.

When the bits in the RSM are set, their setting affects the next frame transmission. The frame currently being transmitted is not affected by the new RSM setting. If the RSM is read, it shows the current setting.

When RSMA or RSMB is read by the internal data bus, the register contents occupy the two low-order bytes of the data bus, and the high-order byte is filled by 0.

After a hardware $\overline{\text{RESET}}$ signal or a software RESET instruction, the RSM register is reset to $FFFFFFFF; that value enables all 32 time slots for data transmission.

7.5 OPERATING MODES

The ESSI operating modes are selected via the ESSI control registers (CRA and CRB). The operating modes are documented in the following paragraphs.

7.5.1 ESSI after Reset

A hardware $\overline{\text{RESET}}$ signal or software RESET instruction clears the port control register and the port direction control register, thus configuring all the ESSI signals as GPIO. The ESSI is in the reset state while all ESSI signals are programmed as GPIO; it is active only if at least one of the ESSI I/O signals is programmed as an ESSI signal.

7.5.2 ESSI Initialization

To initialize the ESSI, do the following:

1. Send a reset: hardware $\overline{\text{RESET}}$ signal, software RESET instruction, ESSI individual reset, or STOP instruction reset.
2. Program the ESSI control and time slot registers.
3. Write data to all the enabled transmitters.
4. Configure at least one signal as ESSI signal.
5. If an external frame sync is used, from the moment the ESSI is activated, at least five (5) serial clocks are needed before the first external frame sync is supplied. Otherwise, improper operation may result.

When the PC[5:0] bits in the GPIO port control register (PCR) are cleared during program execution, the ESSI stops serial activity and enters the individual reset state. All status bits of the interface are set to their reset state. The contents of CRA and CRB are not affected. The ESSI individual reset allows a program to reset each interface separately from the other internal peripherals. During ESSI individual reset, internal DMA accesses to the data registers of the ESSI are not valid, and data read there are undefined.

To insure proper operation of the ESSI, use an ESSI individual reset when you change the ESSI control registers (except for bits TEIE, REIE, TLIE, RLIE, TIE, RIE, TE2, TE1, TE0, and RE).

Here is an example of how to initialize the ESSI.

1. Put the ESSI in its individual reset state by clearing the PCR bits.
2. Configure the control registers (CRA, CRB) to set the operating mode. Disable the transmitters and receiver by clearing the TE[2:0] and RE bits. Set the interrupt enable bits for the operating mode chosen.
3. Enable the ESSI by setting the PCR bits to activate the input/output signals to be used.
4. Write initial data to the transmitters that are in use during operation. This step is needed even if DMA services the transmitters.
5. Enable the transmitters and receiver to be used.

Now the ESSI can be serviced by polling, interrupts, or DMA.

Once the ESSI has been enabled (Step 3), operation starts as follows:

- For internally generated clock and frame sync, these signals start activity immediately after the ESSI is enabled.
- Data is received by the ESSI after the occurrence of a frame sync signal (either internally or externally generated) only when the receive enable (RE) bit is set.
- Data is transmitted after the occurrence of a frame sync signal (either internally or externally generated) only when the transmitter enable (TE[2:0]) bit is set.

7.5.3 ESSI Exceptions

The ESSI can generate six different exceptions. They are discussed in the following paragraphs (ordered from the highest to the lowest exception priority):

1. ESSI receive data with exception status:
   Occurs when the receive exception interrupt is enabled, the receive data register is full, and a receiver overrun error has occurred. This exception sets the ROE bit. The ROE bit is cleared when you first read the SSISR and then read RX.
2. ESSI receive data:
   Occurs when the receive interrupt is enabled, the receive data register is full, and no receive error conditions exist. A read of RX clears the pending interrupt. This error-free interrupt can use a fast interrupt service routine for minimum overhead.
3. ESSI receive last slot interrupt:
   Occurs when the ESSI is in network mode and the last slot of the frame has ended. This interrupt is generated regardless of the receive mask register setting. The

receive last slot interrupt can signal that the receive mask slot register can be reset, the DMA channels can be reconfigured, and data memory pointers can be reassigned. Using the receive last slot interrupt guarantees that the previous frame is serviced with the previous setting and the new frame is serviced with the new setting without synchronization problems.

Note: The maximum time it takes to service a receive last slot interrupt should not exceed N – 1 ESSI bits service time (where N is the number of bits the ESSI can transmit per time slot).

4. ESSI transmit data with exception status:
   Occurs when the transmit exception interrupt is enabled, at least one transmit data register of the enabled transmitters is empty, and a transmitter underrun error has occurred. This exception sets the TUE bit. The TUE bit is cleared when you first read the SSISR and then write to all the transmit data registers of the enabled transmitters, or when you write to TSR to clear the pending interrupt.
5. ESSI transmit last slot interrupt:
   Occurs when the ESSI is in network mode at the start of the last slot of the frame. This exception occurs regardless of the transmit mask register setting. The transmit last slot interrupt can signal that the transmit mask slot register can be reset, the DMA channels can be reconfigured, and data memory pointers can be reassigned. Using the transmit last slot interrupt guarantees that the previous frame is serviced with the previous setting and the new frame is serviced with the new setting without synchronization problems.

Note: The maximum transmit last slot interrupt service time should not exceed N – 1 ESSI bits service time (where N is the number of bits in a slot).

6. ESSI transmit data:
   Occurs when the transmit interrupt is enabled, at least one of the enabled transmit data registers is empty, and no transmitter error conditions exist. Write to all the enabled TX registers or to the TSR to clear this interrupt. This error-free interrupt uses a fast interrupt service routine for minimum overhead (if no more than two transmitters are used).

To configure an ESSI exception, perform the following steps:

1. Configure interrupt service routine (ISR)
   a. Load vector base address register `VBA (b23:8)`
   b. Define I_VEC to be equal to the VBA value (if that is nonzero). If it is defined, I_VEC must be defined for the assembler before the interrupt equate file is included.
   c. Load the exception vector table entry: two-word fast interrupt, or jump/branch to subroutine (long interrupt). `p:I_SI0TD`
2. Configure interrupt trigger; preload transmit data
   a. Enable and prioritize overall peripheral interrupt functionality. `IPRP (S0L1:0)`
   b. Write data to all enabled transmit registers. `TX00`
   c. Enable a peripheral interrupt-generating function. `CRB (TE0)`
   d. Enable a specific peripheral interrupt. `CRB0 (TIE)`
   e. Enable peripheral and associated signals. `PCRC (PC5:0)`
   f. Unmask interrupts at the global level. `SR (I1:0)`

Notes:

1. The example material to the right of the steps above shows register settings for configuring an ESSI0 transmit interrupt using transmitter 0.

2. The order of the steps is optional except that the interrupt trigger configuration must not be completed until the ISR configuration is complete. Since **step c.** may cause an immediate transmit without generating an interrupt, perform the transmit data preload in **step b.** before **step c.** to insure valid data is sent in the first transmission.

3. After the first transmit, subsequent transmit values are typically loaded into TXnn by the ISR (one value per register per interrupt). Therefore, if N items are to be sent from a particular TXnn, the ISR will need to load the transmit register (N – 1) times.

4. **Steps c.** and **d.** be performed in a single instruction.

5. If an interrupt trigger event occurs at a time before all interrupt trigger configuration steps are performed, the event is ignored forever; in other words, the event is not queued.

6. If interrupts derived from the core or other peripherals need to be enabled at the same time as ESSI interrupts, **step f.** should be done last.

7.5.4 Operating Modes: Normal, Network, and On-Demand

The ESSI has three basic operating modes and several data and operation formats. These modes can be programmed using the ESSI control registers. The data and operation formats available to the ESSI are selected when you set or clear control bits in the CRA and CRB. These control bits are WL[2:1], MOD, SYN, FSL[1:0], FSR, FSP, CKP, and SHFD.

7.5.4.1 Normal/Network/On-Demand Mode Selection

You select either normal mode or network mode by clearing or setting the MOD bit in the CRB. In normal mode, the ESSI sends or receives one data word per frame (per enabled receiver or transmitter). In network mode, 2 to 32 time slots per frame may be selected. During each frame, 0 to 32 data words may be received or transmitted (from each enabled receiver or transmitter). In either case, the transfers are periodic.

The normal mode typically transfers data to or from a single device. Network mode is typically used in time division multiplexed networks of codecs or DSPs with multiple words per frame.

Network mode has a submode called on-demand mode. You set the MOD bit in the CRB for network mode, and you set the frame rate divider to 0 (DC = $00000) to select on-demand mode.This submode does not generate a periodic frame sync. A frame sync pulse is generated only when data is available to transmit. The frame sync signal indicates the first time slot in the frame. On-demand mode requires that the transmit frame sync be internal (output) and the receive frame sync be external (input). For simplex operation, synchronous mode could be used; however, for full-duplex operation, asynchronous mode must be used. You can enable data transmission that is data-driven by writing data into each TX. Although the ESSI is double-buffered, only one word can be written to each TX, even if the transmit shift register is empty. The receive and transmit interrupts function normally, using TDE and RDF; however, transmit underruns are impossible for on-demand transmission and are disabled. This mode is useful to interface to codecs requiring a continuous clock.

7.5.4.2 Synchronous/Asynchronous Operating Modes

The transmit and receive sections of the ESSI interface are synchronous or asynchronous. The transmitter and receiver use common clock and synchronization signals in synchronous mode; they use separate clock and sync signals in asynchronous mode. The SYN bit in CRB selects synchronous or asynchronous operation. When the SYN bit is cleared, the ESSI TX and RX clocks and frame sync sources are independent. If the SYN

bit is set, the ESSI TX and RX clocks and frame sync are driven by the same source (either external or internal). Since the ESSI is designed to operate either synchronously or asynchronously, separate receive and transmit interrupts are provided.

Transmitter 1 and transmitter 2 operate only in synchronous mode. Data clock and frame sync signals are generated internally by the DSP or obtained from external sources. If clocks are internally generated, the ESSI clock generator derives bit clock and frame sync signals from the DSP internal system clock. The ESSI clock generator consists of a selectable fixed prescaler with a programmable prescaler for bit rate clock generation and a programmable frame-rate divider with a word-length divider for frame-rate sync-signal generation.

7.5.4.3 Frame Sync Selection

The transmitter and receiver can operate independently. The transmitter can have either a bit-long or word-long frame-sync signal format, and the receiver can have the same or another format. The selection is made by programming FSL[1:0], FSR, and FSP bits in the CRB.

7.5.4.3.1 Frame Sync Signal Format

FSL1 controls the frame-sync signal format.

- If the FSL1 bit is cleared, the RX frame sync is asserted during the entire data transfer period. This frame sync length is compatible with Motorola codecs, serial peripherals that conform to the Motorola SPI, serial A/D and D/A converters, shift registers, and telecommunication pulse code modulation serial I/O.
- If the FSL1 bit is set, the RX frame sync pulses active for one bit clock immediately before the data transfer period. This frame sync length is compatible with Intel and National components, codecs, and telecommunication pulse code modulation serial I/O.

7.5.4.3.2 Frame Sync Length for Multiple Devices

The ability to mix frame sync lengths is useful to configure systems in which data is received from one type of device (e.g., codec) and transmitted to a different type of device. FSL0 controls whether RX and TX have the same frame sync length.

- If the FSL0 bit is cleared, both RX and TX have the same frame sync length.
- If the FSL0 bit is set, RX and TX have different frame sync lengths.

FSL0 is ignored when the SYN bit is set.

7.5.4.3.3 Word Length Frame Sync and Data Word Timing

The FSR bit controls the relative timing of the word length frame sync relative to the data word timing.

- When the FSR bit is cleared, the word length frame sync is generated (or expected) with the first bit of the data word.
- When the FSR bit is set, the word length frame sync is generated (or expected) with the last bit of the previous word.

FSR is ignored when a bit-length frame sync is selected.

7.5.4.3.4 Frame Sync Polarity

The FSP bit controls the polarity of the frame sync.

- When the FSP bit is cleared, the polarity of the frame sync is positive; that is, the frame sync signal is asserted high. The ESSI synchronizes on the leading edge of the frame sync signal.
- When the FSP bit is set, the polarity of the frame sync is negative; that is, the frame sync is asserted low. The ESSI synchronizes on the trailing edge of the frame sync signal.

The ESSI receiver looks for a receive frame sync edge (leading edge if FSP is cleared, trailing edge if FSP is set) only when the previous frame is completed. If the frame sync is asserted before the frame is completed (or before the last bit of the frame is received in the case of a bit frame sync or a word-length frame sync with FSR set), the current frame sync is not recognized, and the receiver is internally disabled until the next frame sync.

Frames do not have to be adjacent; that is, a new frame sync does not have to follow the previous frame immediately. Gaps of arbitrary periods can occur between frames. All the enabled transmitters are tri-stated during these gaps.

7.5.4.4 Byte Format (LSB/MSB) for the Transmitter

Some devices, such as codecs, require a MSB-first data format. Other devices, such as those that use the AES-EBU digital audio format, require the LSB first. To be compatible with all formats, the shift registers in the ESSI are bidirectional. You select either MSB or LSB by programming the SHFD bit in the CRB.

- If the SHFD bit is cleared, data is shifted into the receive shift register MSB first and shifted out of the transmit shift register MSB first.
- If the SHFD bit is set, data is shifted into the receive shift register LSB first and shifted out of the transmit shift register LSB first.

7.5.5 Flags

Two ESSI signals (SC[1:0]) are available for use as serial I/O flags. Their operation is controlled by the SYN, SCD[1:0], SSC1, and TE[2:1] bits in the CRB/CRA.The control bits OF[1:0] and status bits IF[1:0] are double-buffered to and from SC[1:0]. Double-buffering the flags keeps the flags in sync with TX and RX.

The SC[1:0] flags are available in the Synchronous mode only. Each flag can be separately programmed.

Flag SC0 is enabled when transmitter 1 is disabled (TE1 = 0). The flag's direction is selected by the SCD0 bit. When SCD0 is set, SC0 is configured as output. When SCD0 is cleared, SC0 is configured as input.

Similarly, the SC1 flag is enabled when transmitter 2 is disabled (TE2 = 0), and the SC1 signal is not configured as the transmitter 0 drive-enabled signal (Bit SSC1 = 0). The direction of SC1 is determined by the SCD1 bit. When SCD1 is set, SC1 is an output flag. When SCD1 is cleared, SC1 is an input flag.

When programmed as input flags, the value of the SC[1:0] bits is latched at the same time as the first bit of the received data word is sampled. Once the input has been latched, the signal on the input flag signal (SC0 and SC1) can change without affecting the input flag. The value of SC[1:0] does not change until the first bit of the next data word is received. When the received data word is latched by RX, the latched values of SC[1:0] are latched by the SSISR IF[1:0] bits respectively and can be read by software.

When programmed as output flags, the value of the SC[1:0] bits is taken from the value of the OF[1:0] bits. The value of the OF[1:0] bits is latched when the contents of TX are transferred to the transmit shift register. The value on SC[1:0] is stable from the time the first bit of the transmit data word is transmitted until the first bit of the next transmit data word is transmitted. The OF[1:0] values can be set directly by software. This allows the DSP56307 to control data transmission by indirectly controlling the value of the SC[1:0] flags.

7.6 GPIO SIGNALS AND REGISTERS

The GPIO functionality of an ESSI port (whether C or D) is controlled by three registers: port control register (PCRC, PCRD), port direction register (PRRC, PRRD), and port data register (PDRC, PDRD).

7.6.1 Port Control Register (PCR)

The read/write 24-bit PCR controls the functionality of the ESSI GPIO signals. Each of PC[5:0] bits controls the functionality of the corresponding port signal. When a PC[i] bit is set, the corresponding port signal is configured as an ESSI signal. When a PC[i] bit is cleared, the corresponding port signal is configured as a GPIO signal. Either a hardware $\overline{\text{RESET}}$ signal or a software RESET instruction clears all PCR bits.

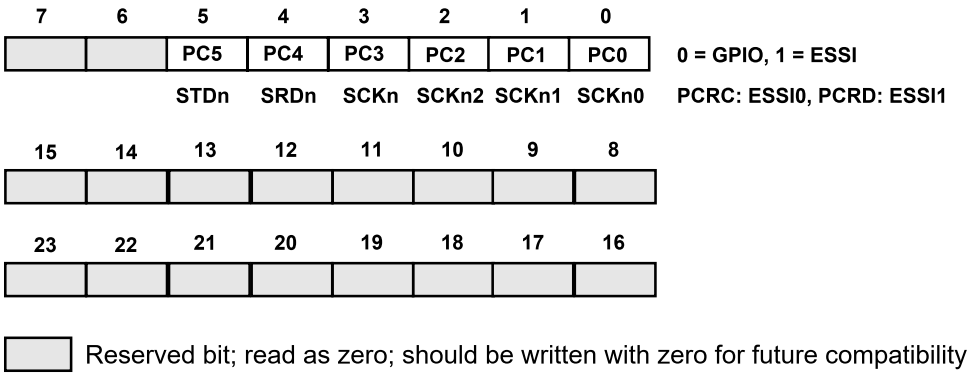


Figure 7-18 Port Control Register (PCR) (PCRC X:$FFFFBF) (PCRD X:$FFFFAF)

7.6.2 Port Direction Register (PRR)

The read/write 24-bit PRR controls the data direction of the ESSI GPIO signals. When PRR[i] is set, the corresponding signal is an output signal. When PRR[i] is cleared, the corresponding signal is an input signal.

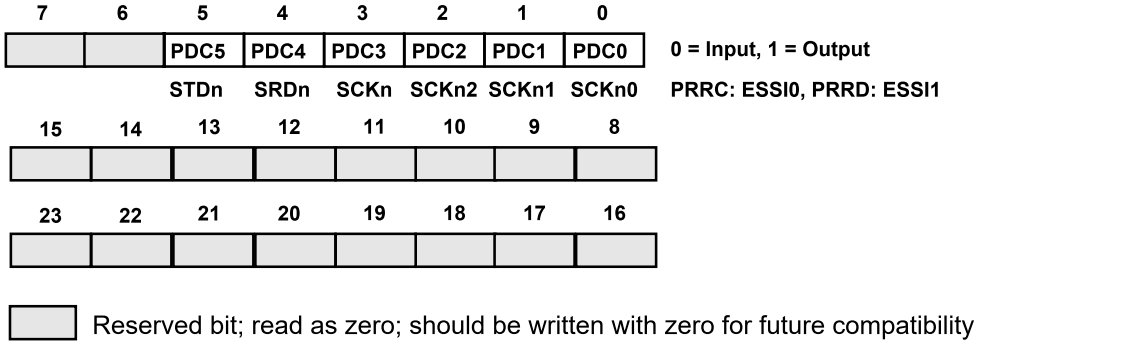


Figure 7-19 Port Direction Register (PRR)(PRRC X:$FFFFBE)
(PRRD X:$FFFFAE)

Note: Either a hardware $\overline{\text{RESET}}$ signal or a software RESET instruction clears all PRR bits.

The following table shows the port signal configurations.

Table 7-5 Port Control Register and Port Direction Register Bits

PC[i]	PDC[i]	Port Signal[i] Function
1	X	ESSI
0	0	GPIO input
0	1	GPIO output
Note: X: The signal setting is irrelevant to Port Signal[i] function.		

7.6.3 Port Data Register (PDR)

The read/write 24-bit PDR is used to read or write data to and from the ESSI GPIO signals. The PD[5:0] bits are used to read or write data from and to the corresponding port signals if they are configured as GPIO signals. If a port signal [i] is configured as a GPIO input, then the corresponding PD[i] bit reflects the value present on this signal. If a

port signal [i] is configured as a GPIO output, then the value written into the corresponding PD[i] bit is reflected on this signal.

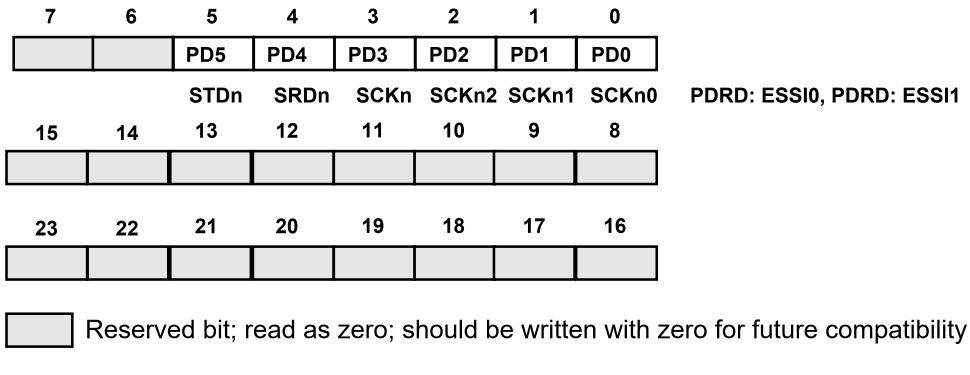


Figure 7-20 Port Data Register (PDR) (PDRC X:$FFFFBD) (PDRD X:$FFFFAD)

Note: Either a hardware $\overline{\text{RESET}}$ signal or a software RESET instruction clears all PDR bits.