# **TABLE OF CONTENTS**

Paragraph Number	Title	Page Number
1 CORE DESCRIPT	TON	1-1
<b>2 EXPANSION POR</b>	RT	2-1
2.1 INTRODUCTION	N	2-1
	ORT SIGNAL DESCRIPTION	
	nd Mode Control	
	Phase-Locked Loop (PLL)	
2.2.3 On-Chip Er	mulator Interface (OnCE)/JTAG Interface	2-3
	Port (Port A)	
	ORT OPERATION	
2.3.1 Static RAM	support	2-7
2.3.1.1 Synch	nronous Static RAM (SSRAM) Support	2-7
2.3.1.2 Async	chronous Static RAM (SRAM) Support	2-11
2.3.2 Dynamic M	lemories Support	2-12
	Port Stalls	
	nal Fetch From Synchronous SRAM	
	Synchronous SRAM Access Immediately Following Sy	
2.3.4 Expansion	port Disable	2-16
	KE AND ARBITRATION	
	tion Signals	
	tion Protocol	
	Scheme	
	tion Example Cases	
	1 – Normal	
	2 – Bus Busy	
	3 – Low Priority	
	4 – Default	
	5 – Bus Lock during RMW	
	6 – Bus Park	
	DRT CONTROL	
2.5.1 AA CONTION	Registers (one for each AA pin)	∠-∠0
•	1:0) - External Access Type and pin definition- bits 1-0 - AA pin Polarity - bit 2	
	I - Program space Enable - bit 3	
2.J. I.J DE EN	i - i Togram space Enable - bit 5	∠-∠∠

### **Table of Contents (Continued) Paragraph Page** Number **Title** Number 2.5.1.8 BNC(3:0) - Number of address bits to Compare - bits 11-8........... 2-23 2.5.2.5 BDFW(4:0)- Default Area Wait control - bits 20-16....................... 2-25 2.5.2.8 BRH - Bus Request Hold - bit 23......2-26 2.5.3 IDentification Register......2-26 2.6.1 DRAM Control Register......2-26 2.6.1.6 BREN - Refresh Enable - bit 13.......2-29 3.2.1 Data Representation ....... 3-6

## **Table of Contents (Continued) Paragraph Page** Number **Title** Number 3.2.4.1 Double Precision Multiply Mode......3-13 3.3 DATA ALU PROGRAMMING MODEL ......3-15 3.4 SIXTEEN BIT ARITHMETIC MODE .......3-15 3.4.1.2 Moves from registers or accumulators.......3-17 4 ADDRESS GENERATION UNIT ......4-1 4.1 AGU ARCHITECTURE .......4-1 4.2 SIXTEEN-BIT COMPATIBILITY MODE ......4-2 4.3 PROGRAMMING MODEL ......4-3 4.3.1.1 Stack Extension Pointer (EP).......4-4 4.3.3 Modifier Register Files (M0 - M3 and M4 - M7).......4-4 4.4 ADDRESSING MODES......4-4 4.4.1 Register Direct Mode.......4-4 4.4.1.1 Data or Control Register Direct......4-5 4.4.2 Address Register Indirect Modes .......4-5 4.4.2.1 No Update (Rn).......4-5 4.4.2.2 Postincrement By 1 (Rn)+......4-5 4.4.2.3 Postdecrement By 1 (Rn)- ......4-5 4.4.2.4 Postincrement By Offset Nn (Rn)+Nn .......4-5 4.4.2.5 Postdecrement By Offset Nn (Rn)-Nn......4-5 4.4.2.6 Indexed By Offset Nn (Rn+Nn) .......4-6

### **Table of Contents (Continued) Paragraph Page** Number **Title** Number 4.4.3.1 Short Displacement PC Relative .......4-6 4.4.3.3 Address Register PC Relative ....... 4-7 4.5 ADDRESS MODIFIER TYPES...... 4-8 4.5.2 Reverse-Carry Modifier (Mn=\$000000) ....... 4-8 4.5.4 Multiple Wrap-Around Modulo Modifier...... 4-11 4.5.5 Address-Modifier-Type Encoding Summary ....... 4-11 5 INSTRUCTION CACHE CONTROLLER....... 5-1 5.2 INSTRUCTION CACHE ARCHITECTURE ......5-1 5.2.1 Instruction Cache Structure......5-1 5.2.2 Cache Programmer's Model ...... 5-2 5.2.3 Cache Operation ...... 5-3 5.2.4 Default Mode On Hardware Reset ...... 5-4 5.2.5 Cache Locking ...... 5-5 5.2.7 Cache Flush ...... 5-6 5.2.8 Sector Replacement Unit ....... 5-7 5.2.9 Data Transfers to/from ICACHE Space ...... 5-7 5.2.10 Cache Observability Via OnCE ......5-8

	Table of Contents (Continued)	
Paragraph	<b>-</b> **41.	Page
Number	Title	Numbe
<b>6 PROGRAM CONT</b>	ROL UNIT	6-1
6.1 OVERVIEW		6-1
	TROL UNIT ARCHITECTURE	
	Pipeline	
	lator	
	G MODEL	
	ounter (PC)	
	e Address Register (VBA)	
6.3.3 Loop Coun	ter Register (LC)	6-5
6.3.4 Loop Addre	ess Register (LA)	6-5
	ick (SS)	
	nsion Pointer (EP)	
	Register (SZ)	
	nter Register (SC)	
	er Register (SP)	
	Pointer (Bits 0–3)	
	Error Flag / P4 bit (Bit 4)	
	flow Flag / P5 bit (Bit 5)	
	gister (SR)	
	y (Bit 0)	
	flow (Bit 1)	
	(Bit 2)	
	ative (Bit 3) ormalized (Bit 4)	
	nsion (Bit 5)	
	(Bit 6)	
	ng (Bit 7)	
	rupt Masks (Bits 8 and 9)	
	aling Mode (Bits 10 and 11)	
	served SR Bit (Bit 12)	
	teen-Bit Compatibility Mode (Bit 13)	
	uble Precision Multiply Mode (Bit 14)	
	-Loop Flag (Bit 15)	
	-Forever flag (Bit 16)	
	teen-Bit Arithmetic Mode (Bit 17)	
	served SR Bit (Bit 18)	
	che Enable (Bit 19)	
6.3.10.19 Arit	hmetic Saturation Mode (Bit 20)	6-15
	Inding Mode (Bit 21)	

### **Table of Contents (Continued) Paragraph Page** Number **Title** Number 6.3.10.21 Core Priority (Bits 22 and 23) ...... 6-15 6.3.11.1 Chip Operating Mode (Bits 0, 1,2 and 3) ...... 6-17 6.3.11.2 External Bus Disable (Bit 4)...... 6-17 6.3.11.8 TA Synchronize Select (Bit 11)...... 6-18 6.3.11.9 Bus Release Timing (Bit 12) ...... 6-19 6.3.11.10 Reserved EOM Bits (Bits 15, 14 and 13)...... 6-19 6.3.11.11 XY Select for Stack extension (Bit 16)...... 6-19 6.3.11.12 Extended Stack Underflow Flag (Bit 17)...... 6-19 6.3.11.13 Extended Stack Overflow Flag (Bit 18)...... 6-19 6.3.11.14 Extended Stack Wrap Flag (Bit 19) ...... 6-20 7 PROCESSING STATES 7-1 7.1 NORMAL PROCESSING STATE......7-1 7.1.1 Instruction Pipeline.......7-1 7.2.1.1 Hardware Interrupt Source .......7-4 7.2.1.2 Software Interrupt Source.......7-5 7.2.2.2 Exception Priorities within an IPL .......7-7

Tal	ble of Contents (Continued)	
Paragraph Number	Title	Page Numbe
7.3 RESET PROCESSIN	IG STATE	7-12
	STATE	
7.5 STOP PROCESSING	STATE	7-13
8 DMA CONTROLLER.		8-1
8.1 DMA CONTROLLER	PROGRAMMING MODEL	8-2
	ddress Register (DSR)	
	n Address Register (DDR)	
	gister (DOR)	
	DCO)	
	ter mode A - single counterter mode B - dual counter	
	ter modes C, D and E- triple counter	
	egister (DCR)	
8.1.5.1 DCR DMA	Channel Enable Bit (DE) Bit 23	8-8
	Interrupt Enable Bit (DIÉ) Bit 22	
8.1.5.3 DCR DMA	Transfer Mode (DTM2-DTM0)- bits 21:19	8-8
	Channel priority(DPR1-DPR0) - bits 18:17	
	Continuous Mode (DCON) - bit 16	
	Request Source (DRS0-DRS4) Bits 15-11	
	three Dimensional mode (D3D)- bit 10	
	Address Mode (DAM5-DAM0)- bits 9:4  Destination Space (DDS0-DDS1) Bits 3, 2	
	A Source Space (DSS0-DSS1) Bits 3, 2	
	gister (DSTR)	
8.1.6.1 DSTR DM	A Channel Transfer Done Status (DTD)- bits 5-0	8-17
	erved bits - bits 23:12 and 7:6	
	A Active state (DACT) - bit 8	
	A Active Channel (DCH2-DCH0) - bits 11:9	
8.2 DMA Restrictions		8-18
9 PLL and CLOCK GEN	NERATOR	9-1
9.1 INTRODUCTION		9-1
	sion	
	iplication	
	n	
	de and Output Stage	
	MM	
	Divider  Cy Detector and Charge Pump Loop Filter	

#### **Table of Contents (Continued) Paragraph Page** Number **Title** Number 9.2.3.3 Crystal Range Bit (XTLR) - Bit 15...... 9-7 9.2.3.5 STOP Processing State Bit (PSTP) - Bit 17 ...... 9-7 9.2.3.7 Clock Output Disable Bit (COD) - Bit 19......9-8 9.2.3.8 PreDivider Factor Bits (PD0-PD3) - Bits 20-23.......9-9 9.2.6 Frequency Divider......9-10 9.3 CLKGEN BLOCK DIAGRAM.......9-10 9.3.4 Synchronization among EXTAL, CLKOUT, and the Internal Clock....... 9-11 9.4 PLL PINS.......9-11 10.2 ON-CHIP EMULATION (OnCE™) PINS.......10-1 10.2.1 Debug Event (DE).......10-2 10.3 OnCE™ CONTROLLER......10-2 10.3.1 OnCE™ Command Register (OCR).......10-3 10.3.1.1 Register Select (RS4-RS0) Bits 0-4...... 10-3 10.3.3.4 Memory Breakpoint Occurrence (MBO) Bit 3 ....... 10-6

Table of Contents (Continued)			
aragraph Number Title	Page Numbe		
10.4 OnCE™ MEMORY BREAKPOINT LOGIC	10-7		
10.4.1 Memory Address Latch (OMAL)	10-7		
10.4.2 Memory Limit Register 0 (OMLR0)	10-7		
10.4.3 Memory Address Comparator 0 (OMAC0)			
10.4.4 Memory Limit Register 1 (OMLR1)	10-8		
10.4.5 Memory Address Comparator 1 (OMAC1)			
10.4.6 Breakpoint Control Register (OBCR)	10-8		
10.4.6.1 Memory Breakpoint Select (MBS0-MBS1) Bits	s 0-110-9		
10.4.6.2 Breakpoint 0 Read/Write Select (RW00-RW01	) Bits 2-3 10-9		
10.4.6.3 Breakpoint 0 Condition Code Select (CC00-Co	C01) Bits4-510-10		
10.4.6.4 Breakpoint1 Read/Write Select (RW10-RW11)			
10.4.6.5 Breakpoint1 Condition Code Select (CC10-CC			
10.4.6.6 Breakpoint 0 and 1 Event Select (BT1-BT0) B	its10-1110-11		
10.4.7 Memory Breakpoint Counter (OMBC)	10-11		
10.5 CACHE SUPPORT			
10.6 OnCE™ TRACE LOGIC	10-13		
10.6.1 Trace Counter (OTC)	10-14		
10.7 METHODS OF ENTERING THE DEBUG MODE	10-14		
10.7.1 External Debug Request During RESET	10-15		
10.7.2 External Debug Request During Normal Activity			
10.7.3 Executing the JTAG DEBUG_REQUEST Instruction			
10.7.4 External Debug Request During STOP			
10.7.5 External Debug Request During WAIT			
10.7.6 Software Request During Normal Activity			
10.7.7 Enabling Trace Mode			
10.7.8 Enabling Memory Breakpoints	10-16		
10.8 PIPELINE INFORMATION AND GDB REGISTER	10-16		
10.8.1 PDB Register (OPDBR)	10-16		
10.8.2 PIL Register (OPILR)			
10.8.3 GDB Register (OGDBR)			
10.9 TRACE BUFFER			
10.9.1 PAB Register for Fetch (OPABFR)	10-17		
10.9.2 PAB Register for Decode (OPABDR)	10-17		
10.9.3 PAB Register for Execute (OPABEX)	10-18		
10.9.4 Trace Buffer	10-18		
10.10 SERIAL PROTOCOL DESCRIPTION	10-19		
10.10.1 OnCE™ Commands			

Tabl	e of Contents (Continued)	
Paragraph Number	Title	Page Number
10.11 TARGET SITE DEBL	JG SYSTEM REQUIREMENTS	10-20
	NG THE OnCETM	
10.12.1 Checking wheth	ner the chip has entered the Debug Mode	10-21
	G instruction shift register	
10.12.3 Saving Pipeline	Information	10-21
10.12.4 Reading the Tra	ace Buffer	10-22
10.12.5 Displaying a spe	ecified register	10-22
10.12.6 Displaying X me	emory area starting at address \$xxxxxx	10-23
	Debug Mode to Normal Mode to current prog	
10.12.8 Returning from	Debug Mode to Normal Mode to a new prog	ram 10-24
10.13 EXAMPLES OF JTA	G-OnCE INTERACTION	10-25
11 JTAG (IEEE 1149.1) Te	est Access Port	11-1
11.1 INTRODUCTION		11-1
11.2.1 JTAG PINS		11-3
	(TCK)	
	Select (TMS)	
	nput (TDI)	
	Dutput (TDO)	
	(TRST~)	
11.2.2 TAP CONTROLL	ÊR	11-3
11.2.3 BOUNDARY SC	CAN REGISTER	11-4
11.2.4 INSTRUCTION F	REGISTER	11-5
11.2.4.1 EXTEST		11-6
11.2.4.2 SAMPLE/P	RELOAD	11-6
		_
	NCE	
——————————————————————————————————————	EQUEST	
11.3 DSP56300 RESTRICT	ΓΙΟΝS	11-9
12 OPERATING MODES	AND MEMORY SPACES	12-1
12.1 CHIP OPERATING M	ODES	12-1
	s (Modes 0 and 8)	
	ation Modes 1-15 (Mode 1-7 and 9-F)	
12.2 DSP56300 CORE ME	MORY MAP	12-2
12.2.1.X Data Memory 9		

Table of Contents (Continued)			
Paragraph Number	Title	Page Numbe	
	a Memory Space		
12.2.3 Progra	am Memory	12-6	
	IT COMPATIBILITY MODE		
12.4 MEMORY S	SWITCH MODE	12-8	
	INSTRUCTION SET		
Appendix A INS	TRUCTION SET	A-3	
A-1 INTRODUCT	ΓΙΟΝ	A-3	
A-2 INSTRUCTION	ON FORMATS AND SYNTAX		
A-2.1 Operan	d Sizes	A-5	
	rganization in Registers		
	LŬ Registers		
	egisters		
	m Control Registers		
	rganization in Memory		
	ON GROUPS		
A-3.1 Arithme	etic Instructions	A-9	
A-3.2 Logical	Instructions	A-11	
	nipulation Instructions		
	structions		
	nstructions		
A-3.6 Program	m Control Instructions	A-15	
A-4 INSTRUČTION	ON GUIDE	A-17	
	TION		
A-5 CONDITION	CODE COMPUTATION	A-22	
A-6 INSTRUCTION	ONS DESCRIPTIONS	A-26	
	te Value (ABS)		
	ng with Carry (ADC)		
	.DD)		
	eft and Add Accumulators (ADDL)		
	ght and Add Accumulators (ADDR)		
	AND (AND)		
A-6.7 AND In	nmediate with Control Register (ANDI)	A-35	
	etic Shift Accumulator Left (ASL)		
	etic Shift Accumulator Right (ASR)		

#### **Table of Contents (Continued) Paragraph Page** Number **Title** Number A-6.14 Branch if Bit Clear (BRCLR).......A-53 A-6.18 Branch to Subroutine if Bit Clear (BSCLR).......A-62 A-6.24 Clear accumulator (CLR)......A-77 A-6.26 Compare Magnitude (CMPM).......A-80 A-6.27 Compare Unsigned (CMPU).......A-82 A-6.33 Start Hardware Loop (DO).......A-91 A-6.35 Start PC Relative Hardware Loop (DOR).......A-97

	Table of Contents (Continued)	
Paragraph Number	Title	Page Numbei
A-6.49	Jump to Subroutine Conditionally (JScc)	A-124
A-6.50	Jump to Subroutine if Bit Clear (JSCLR)	A-126
	Jump if Bit Set (JSET)	
A-6.52	Jump to Subroutine (JSR)	A-131
A-6.53	Jump to Subroutine if Bit Set (JSSET)	A-133
A-6.54	Load PC Relative Address (LRA)	A-136
	Logical Shift Left (LSL)	
A-6.56	Logical Shift Right (LSR)	A-141
	Load Updated Address (LUA)	
	Signed Multiply-Accumulate (MAC)	
	Signed MAC with Immediate Operand (MACI)	
	Mixed Multiply-Accumulate (MAC su/uu)	
	Signed MAC and Round (MACR)	
	Signed MAC and Round with Immediate Operand (MACRI)	
	Transfer by Signed Value (MAX)	
	Transfer by Magnitude (MAXM)	
	Merge Two Half Words (MERGE)	
	Move Data (MOVE)	
	NO Parallel Data Move	
	Immediate Short Data Move (I)	
	Register to Register Data Move (R)	
	Address Register Update (U)	
	X Memory Data Move (X:)	
	X Memory and Register Data Move (X:R)	
	Y Memory Data Move (Y:)	
	Register and Y Memory Data Move (R:Y)	
	Long Memory Data Move (L:)	
	XY Memory Data Move (X: Y:)	
	Move Control Register (MOVEC)	
	Move Program Memory (MOVEM)	
	Move Peripheral Data (MOVEP)	
	Signed Multiply (MPY)	
A-6.81	Mixed Multiply (MPY su/uu)	A-190
	Signed Multiply with Immediate Operand (MPYI)	
	Signed Multiply and Round (MPYR)	
	Signed Multiply and Round with Immediate Operand (MPYRI)	
	Negate Accumulator (NEG)	
	No Operation (NOP)	
Λ 0.00 Δ-6 87	Norm Accumulator Iteration (NORM)	Δ-198
Λ-0.01	Norm / todamatati iteration (NORM)	

	Table of Contents (Continued)	
Paragraph Number	Title	Page Number
	Fast Accumulator Normalization (NORMF)	
	_ogical Complement (NOT)	
	ogical Inclusive OR (OR)	
	OR Immediate with Control Register (ORI)	
	Program-Cache Flush (PFLUSH)	
	Program-Cache Flush Unlock Sectors(PFLUSHUN)	
	Program-Cache Global Unlock (PFREE)	
	Lock Instruction Cache Relative Sector (PLOCKR)	
	Jnlock instruction Cache Sector (PUNLOCK)	
	Jnlock instruction Cache Relative Sector (PUNLOCKR)	
	Repeat Next Instruction (REP)	
	Reset On-Chip Peripheral Devices (RESET)	
	Round Accumulator (RND)	
	Rotate Left (ROL)	
	Rotate Right (ROR)	
	Return from Interrupt (RTI)	
	Return from Subroutine (RTS)	
	Subtract Long with Carry (SBC)	
	Stop Instruction Processing (STOP)	
	Subtract (SUB)	
	Shift Left and Subtract Accumulators (SUBL)	
	Shift Right and Subtract Accumulators (SUBR)	
	Transfer Conditionally (Tcc)	
	Transfer Data ALU Register (TFR)	
A-6.112	Software Interrupt (TRAP)	A-235
	Conditional Software Interrupt (TRAPcc)	
	Test Accumulator (TST)	
A-6.115	Wait for interrupt (WAIT)	A-238
	JCTION PARTIAL ENCODING	
	artial Encodings for Use in Instruction Encoding	
	arallel Instruction Encoding of the Operation Code	
	2.1 Multiply Instruction Encoding	
A-7.2	2.2 NonMultiply Instruction Encoding	A-252
INS	TRUCTION EXECUTION TIM	ING
Appendix B	INSTRUCTION EXECUTION TIMING	B-3

## **Table of Contents (Continued) Paragraph Page** Number **Title** Number B-1 INTRODUCTION......B-3 B-2 INSTRUCTION TIMING ......B-3 B-3 INSTRUCTION SEQUENCE DELAYS ......B-13 B-3.1 External Bus Wait States ......B-13 B-3.2 External Bus Contention ......B-13 B-3.3 Instruction Fetch delays......B-14 B-3.4 Data ALU Interlock.....B-15 B-3.4.1 Arithmetic Stall ......B-15 B-3.4.2 Transfer Stall ......B-15 B-3.4.3 Status Stall ......B-15 B-3.5 Address Registers Interlocks ......B-15 B-3.5.1 Conditional Transfer Interlock ......B-15 B-3.5.2 Address Generation Interlock .......B-15 B-3.6 Stack Extension Delays ......B-17 B-3.7 Program Flow-Control delays ......B-18 B-3.7.1 MOVE to CR.....B-19 B-3.7.2 MOVE from CR ......B-19 B-3.7.3 MOVE to SP/SC ......B-19 B-3.7.4 MOVE to LA register ......B-19 B-3.7.5 MOVE to SR......B-19 B-3.7.6 MOVE to SSH/SSL......B-19 B-3.7.7 JMP to (LA) or to (LA-1) ......B-20 B-3.7.8 RTI to (LA) or to (LA-1)......B-20 B-3.7.9 MOVE from SSH ......B-20 B-3.7.10 Conditional Instructions ......B-20 B-3.7.11 Interrupt Abort ......B-20 B-3.7.12 Degenerated DO loop ......B-20 B-3.7.13 Annulled REP and DO......B-20 B-4 INSTRUCTION SEQUENCE RESTRICTIONS......B-21 B-4.1 Restrictions Near the End of DO Loops......B-21 B-4.1.1 At LA-3 ......B-21 B-4.1.2 At LA-2 ......B-21 B-4.1.3 At LA-1 ...... B-22 B-4.1.4 At LA......B-22 B-4.2 General DO Restrictions ......B-22

Table of Contents (Continued)		
Paragraph Number	Title	Page Number
	t Interrupt Routines	
	P Restrictions	
	ck Extension Restrictions	
	truction Cache General Restrictions	
	al pipeline restrictions	
	ng a peripheral device for write	
B-5.2 Writ	ing to a read-only register	B-26
F	BENCHMARK PROGRAMS	
-		
Appendix C B	ENCHMARK PROGRAMS	
	JCTION	C-3
	BENCHMARKS	
	l Multiply	
	eal Multiplies	
	I Update	
	eal Updates	
	l Correlation Or Convolution (FIR Filter)	
	I * Complex Correlation Or Convolution (FIR Filter)	
	nplex Multiply	
	omplex Multiplies	
C-2.9 Con	nplex Update	
	Complex Updates	
C-2.11 Co	mplex Correlation Or Convolution (FIR Filter)	
C-2.12 Nth	n Order Power Series (Real)	
	d Order Real Biquad IIR Filter	
	Cascaded Real Biquad IIR Filter	
	Radix-2 FFT Butterflies (DIT, in-place algorithm)	
	ue (Exact) LMS Adaptive Filter	
	layed LMS Adaptive Filter	
	R Lattice Filter	
	Pole IIR Lattice Filter	
	neral Lattice Filter	
	rmalized Lattice Filter	
	3][3x3] Matrix Multiplication	
C-2.23 N I	Point 3x3 2-D FIR Convolution	

Table of Contents (Continued)		
Paragraph Number	Title	Page Numbe
C-2 24 Parsing data	straam	C-28
C-2.24 Parsing data stream C-2.25 Creating data stream		
C-2.26 Parsing Hoffman code data stream		
C-3 BENCHMARK OVERVIEW		C-36