1 CORE DESCRIPTION

This document describes the DSP56300 Core, a new core of Motorola's family of programmable CMOS digital signal processors. The DSP56300 is the powerful New DSP Engine (NDE) core capable of executing an instruction on every clock cycle, thus yielding a twofold performance increase as compared to the 56000 core while maintaining object code compatibility with it.

The DSP56300 core is composed of the Expansion Port and DRAM Controller, Data ALU, Address Generation Unit, Instruction Cache Controller, Program Control Unit, DMA Controller, PLL Clock Oscillator, On-chip Emulator and the Peripheral and Memory Expansion Bus.

The cost-effectiveness of the parts is the major factor in the economic success of the DSP family thus the provided solution must be low-cost but powerful enough to meet the computational demands, flexible enough to meet various demands of the customers/applications and have enough degree of integration to minimize the total system cost.

DSP applications require parts capable of very high execution speed in a real-time I/O intensive environment. The DSP56300 core with its capability of executing an instruction per clock cycle has the processing power to meet this demand.

To minimize the total system cost the DSP56300 core incorporates a versatile external memory interface that provides glueless interface to a variety of memories such as Dynamic RAMs (DRAMs), Static RAMs (SRAMs), Synchronous Static RAMs (SSRAMs) etc. by providing on-chip DRAM controller as well as chip select logic. The concurrent Six-Channel DMA Controller augments the data throughput that characterizes the DSP applications. Special attention is paid in the design stage to minimize the chip power consumption. Low power consumption is achieved both in active and in standby modes. Power consumption scale down with clock frequency reduction, use of on-chip memory, use of on-chip peripherals, and use of WAIT and STOP standby modes. External buses are driven only when required. On-chip memory expansion does not increase power dissipation significantly because only memory modules being accessed consume power.

The design priorities for the DSP56300 Core are:

1. Low-cost
2. Low-power dissipation
3. High-performance
4. High integration

DSP56300 Core Features

High performance CPU

- 66/80Million Instructions per Second (Mips) with a 66/80 MHz clock
- Object Code Compatible with the 56K Core
- Fully pipelined 24 x 24 Bit Parallel Multiplier-Accumulator
- 56 Bit Parallel Barrel Shifter
- 16 Bit Arithmetic Support
- Highly Parallel Instruction Set
- Position Independent Code (PIC) support
- Unique DSP Addressing Modes
- On-Chip Memory-Expandable Hardware Stack
- Nested Hardware Do Loops
- Fast Auto-Return Interrupts
- On-Chip user-controllable Instruction Cache
- On-Chip Concurrent Six-Channel DMA Controller
- On-Chip PLL
- On-Chip Emulator (OnCE)
- Program Address Tracing Support
- JTAG port compatible with the IEEE 1149.1 Standard

Reduced power dissipation

- Very low power CMOS design
- Wait and Stop low power standby modes
- Fully-static logic, operation frequency down to DC.

Figure 1-1. DSP56300 Core Block Diagram