9 PLL AND CLOCK GENERATOR

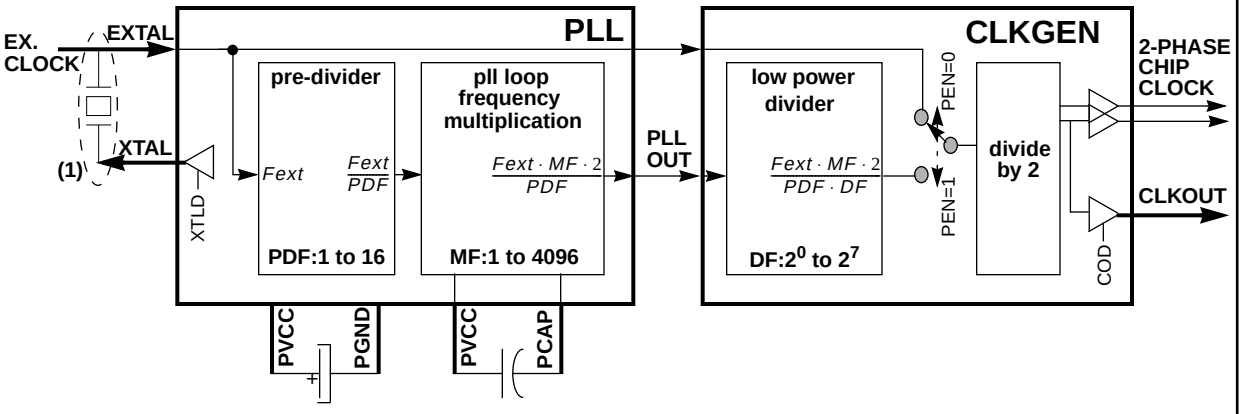
9.1 INTRODUCTION

The DSP56300 Core features a PLL (phase-locked loop) clock oscillator in its central processing module. The PLL allows the processor to operate at a high internal clock frequency using a low frequency clock input, a feature which offers two immediate benefits: Lower frequency clock input reduces the overall electromagnetic interference generated by a system, and the ability to oscillate at different frequencies reduces costs by eliminating the need to add additional oscillators to a system.

The clock generation in the DSP56300 Core is composed of two main blocks:

- Phase Locked Loop (PLL) that performs
  - Clock input division
  - Frequency multiplication
  - Skew elimination
- CLOCK GENERATOR (CLKGEN) that performs
  - Low power division
  - Internal & External clock pulse generation

Figure 9-1. PLL & CLOCK Block Diagram



Note (1): The clock source can be either an external source supplied to EXTAL, or a clock oscillator connected to EXTAL and XTAL.

9.1.1 Clock Input Division

The PLL can divide the input frequency by any integer between 1 and 16. The combination of input division and output low-power division (see Section 9.1.4) enables the user to generate almost every frequency value out of the PLL. The division factor may be modified by changing the value of the Pre-Division Factor Bits (PDF - PD3:0) in the PLL control register. The output frequency of the pre-divider is

$$\frac{Fext}{PDF}$$

9.1.2 Frequency Multiplication

The PLL can multiply the input frequency by any integer between 1 and 4096. The multiplication factor may be modified by changing the value of the Multiplication Factor (MF) Bits MF[11:0] in the PLL control register. The output frequency of the PLL ("PLL OUT" in figure 9-1) is

$$\frac{Fext \cdot MF \cdot 2}{PDF}$$

Notice that this is not the chip operating frequency but rather the input to the CLKGEN block.

9.1.3 Skew Elimination

The PLL is capable of eliminating the skew between the external clock entering the chip (EXTAL) and the internal clock phases and CLKOUT pin, making it useful for tighter synchronous timings. Skew elimination is active only when the PLL is enabled and programmed with a multiplication factor less than or equal to 4. When the PLL is disabled, or when the multiplication factor is greater than 4, or when the pre division factor is greater than 1, clock skew may exist.

Skew elimination is assured only if the input frequency (EXTAL) is greater than a minimum frequency specified in a device's Technical Data Sheet (typically 15 MHz).

9.1.4 Low Power Divide and Output Stage

The Clock-Generator has a divider connected to the output of the PLL. The output frequency of the PLL may be divided by a factor of 2^n (where $0 \leq n \leq 7$). The division factor may be modified by changing the value of the Division Factor Bits (DF - DF2:0) in the PLL control register. This divider permits reducing or restoring the chip operating frequency without losing the PLL lock.

The Output Stage of the Clock-Generator generates the clock signals to the core and the chip peripherals, and drives the CLKOUT pin. The Output Stage divides the frequency by 2. The input source to the Output Stage is selected between:

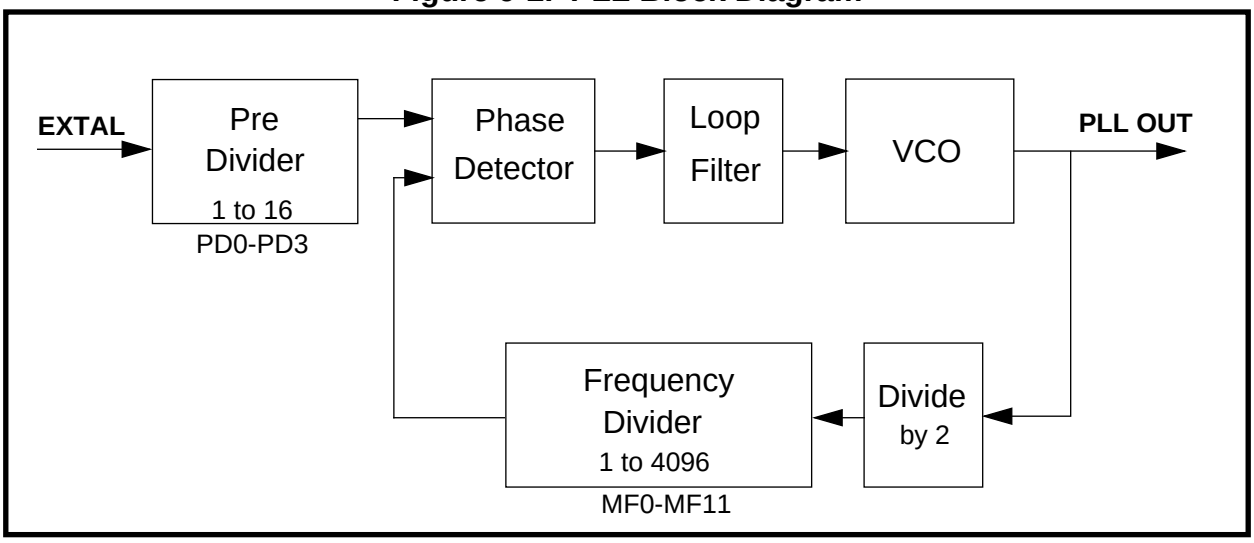
- EXTAL itself (PEN=0 i.e. PLL disabled), that causes chip frequency to be

- Low Power Divider output (PEN=1 i.e. PLL enabled), that cause chip frequency to be

9.2 PLL BLOCK DIAGRAM

The PLL block diagram is shown in Figure 9-2. The components of the PLL are described in the following sections.

Figure 9-2. PLL Block Diagram



9.2.1 Frequency Pre-Divider

Clock input frequency division is accomplished by means of a frequency divider of the input frequency. The programmable division factor ranges from 1 to 16.

9.2.2 Phase Frequency Detector and Charge Pump Loop Filter

The Phase Detector (PD) detects any phase difference between the external clock (EXTAL) and an internal clock phase from the frequency multiplier. At the point where there is negligible phase difference and the frequency of the two inputs is identical, the PLL is in the “locked” state.

The charge pump loop filter receives signals from the PD, and either increases or decreases the phase based on the PD signals. An external capacitor is connected to the PCAP pin (described in Section 9.4) and determines the PLL operation. (See the appropriate Technical Data Sheet for more detailed information about a particular device’s capacitor value.)

After the PLL locks on to the proper phase/frequency, it reverts to the narrow bandwidth mode, which is useful for tracking small changes due to frequency drift of the EXTAL clock.

9.2.3 PLL Control Register (PCTL)

The PLL control register (PCTL) is an X-I/O mapped 24-bit read/write register used to direct the operation of the on-chip PLL. The PCTL control bits are described in the

following sections.

Figure 9-3. PLL Control Register (PCTL)

11	10	9	8	7	6	5	4	3	2	1	0
MF11	MF10	MF9	MF8	MF7	MF6	MF5	MF4	MF3	MF2	MF1	MF0
23	22	21	20	19	18	17	16	15	14	13	12
PD3	PD2	PD1	PD0	COD	PEN	PSTP	XTLD	XTLR	DF2	DF1	DF0

9.2.3.1 Multiplication Factor Bits (MF0-MF11) - Bits 0-11

The Multiplication Factor Bits MF0-MF11 define the multiplication factor MF that will be applied to the PLL input frequency. The multiplication factor MF can be any integer from 1 to 4096. Table 9-1 shows how to program the MF0-MF11 bits. The VCO will oscillate at a frequency of:

Where PDF is the division factor of the Pre-Divider.

The multiplication factor must be chosen to ensure that the resulting VCO output frequency will lay in the range specified in the device's Technical Data Sheet. Any time a new value is written into the MF0-MF11 bits, the PLL will lose the lock condition. After a time delay, the PLL will relock. The multiplication factor bits (MF0-MF11) are set to a predetermined value during hardware reset; the value is implementation dependent and may be found in each DSP56300 based derivative user's manual.

Table 9-1. Multiplication Factor Bits MF0-MF11

MF11-MF0	Multiplication Factor MF
$000	1
$001	2
$002	3
• • •	• • •
$FFE	4095
$FFF	4096

9.2.3.2 Division Factor Bits (DF2-DF0) - Bits 12-14

The Division Factor Bits DF2-DF0 define the divide factor DF of the low power divider. These bits specify any power of two divide factor in the range from 2^0 to 2^7. Table 9-2 shows the programming of the DF2-DF0 bits. Changing the value of the DF2-DF0 bits will not cause a loss of lock condition. Whenever possible, changes of the operating frequency of the chip (for example, to enter a low power mode) should be made by changing the value of the DF2-DF0 bits rather than changing the MF0-MF11 bits. For MF≤4, changing DF2-DF0 may lengthen the instruction cycle following the PLL control register update; this is done in order to keep synchronization between EXTAL and the internal chip clock. For MF>4 such synchronization is not guaranteed and the instruction cycle is not lengthened. These bits are cleared (division by one) by hardware reset.

Table 9-2. Division Factor Bits DF0-DF2

DF2-DF0	Division Factor DF
$0	2^0
$1	2^1
$2	2^2
• • •	• • •
$7	2^7

9.2.3.3 Crystal Range Bit (XTLR) - Bit 15

The Crystal Range (XTLR) bit controls the on-chip crystal oscillator transconductance. If the external crystal frequency is less than 200kHz (“fork crystal”), this bit should be set in order to decrease the transconductance of the input amplifier, otherwise the internal clocks may not be stable. If the external crystal frequency is greater than 200kHz, this bit should be cleared in order to have the full transconductance, otherwise the crystal oscillator may not function at all. The XTLR bit is set to a predetermined value during hardware reset; the value is implementation dependent and may vary between each DSP56300 based derivative.

9.2.3.4 XTAL Disable Bit (XTLD) - Bit 16

The XTAL Disable (XTLD) bit controls the on-chip crystal oscillator XTAL output. When XTLD is cleared, the XTAL output pin is active, permitting normal operation of the crystal oscillator. When XTLD is set, the XTAL output pin is held in the high (“1”) state, disabling the on-chip crystal oscillator. If the on-chip crystal oscillator is not used (EXTAL is driven from an external clock source), it is recommended to set XTLD (disabling XTAL) to minimize RFI noise and power dissipation. The XTLD bit is set to a predetermined value during hardware reset; the value is implementation dependent and may vary between each DSP56300 based derivative.

9.2.3.5 STOP Processing State Bit (PSTP) - Bit 17

The PSTP bit controls the behavior of the PLL and of the on-chip crystal oscillator during the STOP processing state. When PSTP is set, the PLL and the on-chip crystal oscillator will remain operating while the chip is in the STOP processing state. When PSTP is cleared, the PLL and the on-chip crystal oscillator will be disabled when the chip enters

the STOP processing state. For minimum power consumption during the STOP state at the cost of longer recovery time, PSTP should be cleared. To enable rapid recovery when exiting the STOP state, at the cost of higher power consumption, PSTP should be set. PSTP is cleared by hardware reset.

9.2.3.6 PLL Enable Bit (PEN) - Bit 18

The PEN bit enables the PLL operation. When this bit is set, the PLL is enabled and the internal clocks will be derived from the PLL VCO output. When this bit is cleared, the PLL is disabled and the internal clocks are derived directly from the clock connected to the EXTAL pin. When the PLL is disabled, the VCO is not operating in order to minimize power consumption. The PEN bit may be set or cleared by software any time during the chip operation. During hardware reset this bit receives the value of the PLL's PINIT pin, usually connected to the chip's PINIT pin.

A relationship exists between PSTP and PEN where PEN adjusts PSTP's control of the PLL operation. When PSTP is set and PEN (see Table 9-3.) is cleared, the on-chip crystal oscillator remains operating in the STOP state, but the PLL is disabled. This power saving feature enables rapid recovery from the STOP state when the user operates the chip with an on-chip oscillator and with the PLL disabled.

Table 9-3. PSTP and PEN Relationship

PSTP	PEN	Operation during STOP		Recovery Time from STOP	Power Consumption during STOP
		PLL	Oscillator		
0	x	Disabled	Disabled	long	minimal
1	0	Disabled	Enabled	short	lower
1	1	Enabled	Enabled	short	higher

9.2.3.7 Clock Output Disable Bit (COD) - Bit 19

The COD bit controls the output buffer of the clock at the CLKOUT pin. When this bit is set, the CLKOUT pin is held in the high ("1") state. When this bit is cleared, the CLKOUT pin provides a 50% duty cycle clock synchronized to the internal core clock. If the CLKOUT pin is not connected to external circuits, it is recommended to set COD (disabling clock output) to minimize RFI noise and power dissipation. The COD bit is cleared by hardware reset. CLKOUT pin oscillates at all the machine operating states except the STOP processing state.

9.2.3.8 PreDivider Factor Bits (PD0-PD3) - Bits 20-23

The PreDivider Factor Bits PD0-PD3 define the predivision factor PDF that will be applied to the PLL input frequency. The predivision factor PDF can be any integer from 1 to 16. Table 9-1 shows how to program the PD0-PD3 bits. The VCO will oscillate at a frequency of

The predivision factor must be chosen to ensure that the resulting VCO output frequency will lay in the range specified in the device's Technical Data Sheet. Any time a new value is written into the PD0-PD3 bits, the PLL will lose the lock condition. After a time delay, the PLL will relock. The pre-divider factor bits (PD0-PD3) are set to a predetermined value during hardware reset; the value is implementation dependent and may be found in each DSP56300 based derivative user's manual.

Table 9-4. Predivision Factor Bits PD0-PD3

PD3-PD0	Predivision Factor PDF
$0	1
$1	2
$2	3
• • •	• • •
$E	15
$F	16

9.2.4 Voltage Controlled Oscillator (VCO)

The VCO is capable of oscillating at frequencies from the minimum speed specified in a device's Technical Data Sheet (typically 30 MHz) up to the maximum allowed clock input

frequency.

Note: When the PLL is enabled, the chip operating frequency is half of the VCO oscillating frequency.

If EXTAL frequency is less than the VCO's minimum working frequency, the user should hold PINIT pin low during hardware reset and then change (by software) MF to the desired value and change PEN to 1.

9.2.5 Divide by 2

The output of the VCO is divided by 2. This results in a constant x2 multiplication of the PLL clock output used to generate the special chip clock phases.

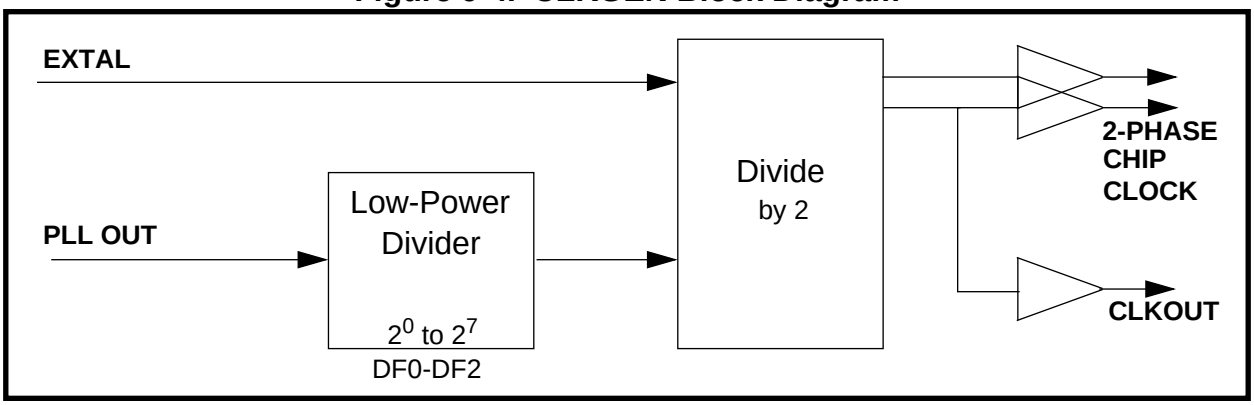
9.2.6 Frequency Divider

The Frequency Divider, connected in the feedback loop of the PLL, is used to multiply the incoming external clock. In the PLL close-loop, the effect of the frequency divider is to multiply the PLL input frequency by its division factor. The programmable division factor ranges from 1 to 4096, resulting in frequency multiplication in the same range.

9.3 CLKGEN BLOCK DIAGRAM

The CLOCK GENERATOR block diagram is shown in Figure 9-4. The components of the CLOCK GENERATOR are described in the following sections.

Figure 9-4. CLKGEN Block Diagram



9.3.1 Low Power Divider (LPD)

The Low Power Divider (LPD**)** divides the output frequency of the VCO by any power of 2 from 2^0 to 2^7. Since the LPD is not in the closed loop of the PLL, changes in the divide factor will not cause a loss of lock condition. This fact is particularly useful for utilizing the

LPD in low power consumption modes when the chip is not involved in intensive calculations. This can result in significant power saving. When the chip is required to exit the low power mode, it can immediately do so with no time needed for clock recovery or PLL lock.

9.3.2 Divide by 2

The EXTAL clock and the output of the Low-Power Divider are selected according to the PEN bit in the PLL control register (PCTL). The selected clock frequency is divided by two and is driven to the internal chip activity and to the CLKOUT pin.

9.3.3 Operating Frequency

The operating frequency of the chip is governed by the frequency control bits in the PLL control register as follows:

$$F_{CHIP} = \frac{F_{EXT} \times MF}{PDF \times DF} = \frac{Fvco}{DF}$$

where MF is the multiplication factor defined by the MF0-MF11 bits, PDF is the predivision factor defined by the PD0-PD3 bits and DF is the division factor defined by the DF0-DF2 bits. F_{CHIP} is the chip operating frequency, and F_{EXT} is the external input frequency to the chip at the EXTAL pin.

9.3.4 Synchronization among EXTAL, CLKOUT, and the Internal Clock

When the PLL is enabled (PEN bit asserted), low clock skew between EXTAL and CLKOUT is guaranteed if MF≤4. CLKOUT and the internal chip clock are fully synchronized.

9.4 PLL PINS

Some of the PLL pins need not be implemented. The specific PLL pin configuration for each DSP56300 Core chip implementation is available in the respective device's user's manual. The following pins are dedicated to the PLL operation:

PVCC VCC dedicated to the analog PLL circuits. The voltage should be well regulated and the pin should be provided with an extremely low

impedance path to the VCC power rail.

PGND GND dedicated to the analog PLL circuits. The pin should be provided with an extremely low impedance path to ground.

PGND1 GND dedicated for isolating the analog PLL circuits. The pin should be provided with an extremely low impedance path to ground.

CLVCC VCC for the CLKOUT output. The voltage should be well regulated and the pin should be provided with an extremely low impedance path to the VCC power rail. This pin doesn't have to be a dedicated one if it can be guaranteed that it is regulated enough.

CLGND GND for the CLKOUT output. The pin should be provided with an extremely low impedance path to ground. This pin doesn't have to be a dedicated one if it can be guaranteed that it is regulated enough.

PCAP Off-chip capacitor for the PLL filter. One terminal of the capacitor is connected to PCAP while the other terminal is connected to PVCC. The capacitor value is specified in the particular device's Technical Data Sheet.

CLKOUT This output pin provides a 50% duty cycle output clock synchronized to the internal processor clock when the PLL is enabled and locked. When the PLL is disabled, the output clock at CLKOUT is derived from, and has half the frequency of, EXTAL. This pin oscillates in all chip processing states except STOP processing state and except a condition when bit COD in the PCTL register is implicitly set. When the chip is in the WAIT processing state, the CLKOUT pin continues to oscillate.

PINIT During the assertion of hardware reset, the value at the PINIT input pin is written into the PEN bit of the PLL control register. After hardware reset is negated, the PINIT pin is ignored by the PLL and can have a different function in the chip.

PLOCK The PLOCK output originates from the Phase Detector. The chip asserts PLOCK when the PLL is enabled and has locked on the proper phase and frequency of EXTAL. The PLOCK output is deasserted by the chip if the PLL is enabled and has not locked on the proper phase and frequency. PLOCK is asserted if the PLL is disabled. PLOCK is a reliable indicator of the PLL lock state only after exiting the hardware reset state. This pin is optional and will not be implemented in all the DSP56300-Core based derivatives.