12 OPERATING MODES AND MEMORY SPACES

12.1 CHIP OPERATING MODES

The DSP56300 Core mode pins, MODA, MODB, MODC and MODD determine the reset vector address that should point to the start-up procedure when the chip leaves the reset state. The MODA, MODB, MODC and MODD pins are sampled as the chip leaves the reset state. The sampled state of these pins is subject to a mask programmed look-up table that may be used as a filter to disable the user from entering to some of the operating modes. This filtered state is written to MD,MC,MB and MA bits in the chip Operating Mode Register (OMR). When the reset state is exited, the MODA, MODB, MODC and MODD pins become general-purpose interrupt pins, IRQA, IRQB, IRQC and IRQD, respectively. When not in the RESET state, the OMR mode bits (MA, MB, MC and MD) can be changed by software.

Table 12-1 depicts the mode assignments in the DSP56300 core. The reset vector is chosen from three mask programmed addresses: RESET1, RESET2 and RESET3. Each reset vector is mask programmed to one of two different values, according to Table 12-1.

Table 12-1. DSP56300 Core reset vectors

RESET1 possible values	RESET2 possible values	RESET3 possible values
$000000	$004000	$000000
$C00000	$008000	$FF0000

Table 12-2. DSP56300 Core operating modes

MOD{D:A}	Operating mode	Description	Reset Vector
0000	0	Expanded Mode	RESET1
0001-0111	1-7	System Configuration Mode 1-7	RESET3
1000	8	Expanded Mode	RESET2
1001-1111	9-F	System Configuration Mode 8-14	RESET3

12.1.1 Expanded Modes (Modes 0 and 8)

In the Expanded Modes 0 and 8, a hardware reset causes the DSP56300 Core to jump to the mask programmed external program memory location RESET1 or RESET2 respectively, and execute the code fetched from this location.

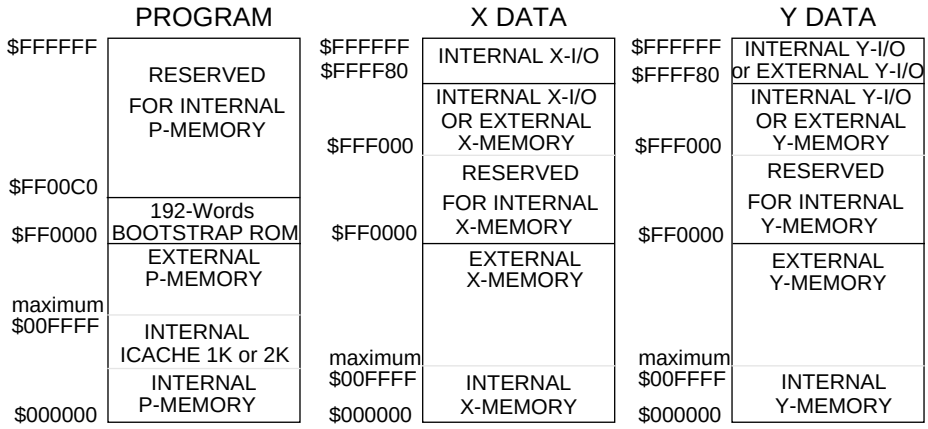
12.1.2 System Configuration Modes 1-15 (Mode 1-7 and 9-F)

In the System Configuration Modes 1-15, a hardware reset causes the DSP56300 Core to jump to the mask programmed internal program memory (usually ROM) location RESET3, and execute the code fetched from this location.

12.2 DSP56300 CORE MEMORY MAP

The memory space of the DSP56300 Core is partitioned into program memory space (P), X data memory space and Y data memory space. The data memory space is divided into X data memory and to Y data memory in order to work with the two address arithmetic logic units (ALUs) and to feed two operands simultaneously to the data ALU. Each memory space may include internal RAM, internal ROM and can be expanded off-chip under software control. The three independent memory spaces of the DSP56300 Core: X data, Y data, and program, are shown in Figure 12-1.

Figure 12-1. DSP56300 Core Memory Map



12.2.1 X Data Memory Space

The X data memory space is divided into five parts:

- **Internal X I/O space**. The on-chip peripheral registers (X I/O) occupy the top 128 locations of the X data memory space ($FFFF80–$FFFFFF) and can be accessed by MOVE, MOVEP instructions and by bit oriented

instructions (BCHG, BCLR, BSET, BTST, BRCLR, BRSET, BSCLR, BSSET, JCLR, JSET, JSCLR and JSSET). Some of the DSP56300 Core registers are mapped onto the internal X I/O space, as described in Table 12-3.

Table 12-3. Internal X I/O Space Map

Register	BLOCK	Address	Register Name and Description
IPRC	PIC	$FFFFFF	INTERRUPT PRIORITY REGISTER CORE
IPRP		$FFFFFE	INTERRUPT PRIORITY REGISTER PERIPHERAL
PCTL	PLL	$FFFFFD	PLL CONTROL REGISTER
OGDB	OnCE	$FFFFFC	ONCE GDB REGISTER
BCR	PORT A	$FFFFFB	BUS CONTROL REGISTER
DCR		$FFFFFA	DRAM CONTROL REGISTER
AAR0		$FFFFF9	ADDRESS ATTRIBUTE REGISTER 0
AAR1		$FFFFF8	ADDRESS ATTRIBUTE REGISTER 1
AAR2		$FFFFF7	ADDRESS ATTRIBUTE REGISTER 2
AAR3		$FFFFF6	ADDRESS ATTRIBUTE REGISTER 3
IDR		$FFFFF5	ID REGISTER
DSTR	DMA	$FFFFF4	DMA STATUS REGISTER
DOR0		$FFFFF3	DMA OFFSET REGISTER 0
DOR1		$FFFFF2	DMA OFFSET REGISTER 1
DOR2		$FFFFF1	DMA OFFSET REGISTER 2
DOR3		$FFFFF0	DMA OFFSET REGISTER 3
DSR0	DMA Channel 0	$FFFFEF	DMA SOURCE ADDRESS REGISTER
DDR0		$FFFFEE	DMA DESTINATION ADDRESS REGISTER
DCO0		$FFFFED	DMA COUNTER
DCR0		$FFFFEC	DMA CONTROL REGISTER

Register	BLOCK	Address	Register Name and Description
DSR1	DMA Channel 1	$FFFFEB	DMA SOURCE ADDRESS REGISTER
DDR1		$FFFFEA	DMA DESTINATION ADDRESS REGISTER
DCO1		$FFFFE9	DMA COUNTER
DCR1		$FFFFE8	DMA CONTROL REGISTER
DSR2	DMA Channel 2	$FFFFE7	DMA SOURCE ADDRESS REGISTER
DDR2		$FFFFE6	DMA DESTINATION ADDRESS REGISTER
DCO2		$FFFFE5	DMA COUNTER
DCR2		$FFFFE4	DMA CONTROL REGISTER
DSR3	DMA Channel 3	$FFFFE3	DMA SOURCE ADDRESS REGISTER
DDR3		$FFFFE2	DMA DESTINATION ADDRESS REGISTER
DCO3		$FFFFE1	DMA COUNTER
DCR3		$FFFFE0	DMA CONTROL REGISTER
DSR4	DMA Channel 4	$FFFFDF	DMA SOURCE ADDRESS REGISTER
DDR4		$FFFFDE	DMA DESTINATION ADDRESS REGISTER
DCO4		$FFFFDD	DMA COUNTER
DCR4		$FFFFDC	DMA CONTROL REGISTER
DSR5	DMA Channel 5	$FFFFDB	DMA SOURCE ADDRESS REGISTER
DDR5		$FFFFDA	DMA DESTINATION ADDRESS REGISTER
DCO5		$FFFFD9	DMA COUNTER
DCR5		$FFFFD8	DMA CONTROL REGISTER
Reserved	On-Chip X-I/O mapped Registers	$FFFFD7	Reserved for On-Chip X-I/O mapped Register
		..	Reserved for On-Chip X-I/O mapped Register
		..	Reserved for On-Chip X-I/O mapped Register
		..	Reserved for On-Chip X-I/O mapped Register
		$FFFF80	Reserved for On-Chip X- I/O mapped Register

- **Switchable Internal X I/O or External X-I/O Memory.** The X memory

space located at locations $FFF000-$FFFF7F can mask configured to be either external X-memory or internal X-I/O for on-chip memory-mapped peripheral registers.

- **Reserved Space for X ROM or RAM.** The X memory space located at locations $FF0000-$FFEFFF is reserved for inclusion of X data ROM or RAM modules, 2048 locations each.
  The importance of modular organization of the X ROM/RAM is visible in case of DMA access to the internal X memory simultaneous to core access to the same space. DMA and CORE accesses to different banks can be completed at full speed, while accesses to the same bank halt the DMA until a P memory slot will be available.

- **External X Memory.** The X memory space located at locations $000000-$FEFFFF is used for expanding to external X memory. The starting address of the external X memory space is mask programmed.

- **Internal X RAM.** The X memory space located at locations $000000-$00FFFF is used for internal X RAM modules, 256 locations each. The last address of the internal X memory is mask programmed and is dependent on the amount of X memory modules in the chip.
  The importance of modular organization of the X RAM is visible in case of DMA access to the internal X memory simultaneous to core access to the same space. DMA and CORE accesses to different banks can be completed at full speed, while accesses to the same bank halt the DMA until a P memory slot will be available.

12.2.2 Y Data Memory Space

The Y data memory space is divided into five parts:

- **Internal/External Y-I/O space**. The off-chip or on-chip peripheral registers (Y-I/O) occupy the top 128 locations of the Y data memory space ($FFFF80–$FFFFFF) and can be accessed by MOVE, MOVEP instructions and by bit oriented instructions (BCHG, BCLR, BSET, BTST, BRCLR, BRSET, BSCLR, BSSET, JCLR, JSET, JSCLR and JSSET).
  This space is partitioned into eight equal parts, 16 locations each. Each part can be mask programmed to be either external Y-I/O or internal Y-I/O.

- **Switchable Internal Y-I/O or External Y-I/O Memory.** The Y memory space located at locations $FFF000-$FFFF7F can be mask configured to be either external Y-memory or internal Y-I/O for on-chip memory-mapped peripheral registers.

- **Reserved Space for Y ROM or RAM.** The Y memory space located at

locations $FF0000-$FFEFFF is reserved for inclusion of Y data ROM or RAM modules, 2048 locations each.
The importance of modular organization of the Y ROM/RAM is visible in case of DMA access to the internal Y memory simultaneous to core access to the same space. DMA and CORE accesses to different banks can be completed at full speed, while accesses to the same bank halt the DMA until a P memory slot will be available.

- **External Y Memory.** The Y memory space located at locations $000000-$FEFFFF is used for expanding to external Y memory. The starting address of the external Y memory space is mask programmed.

- **Internal Y RAM.** The Y memory space located at locations $000000-$00FFFF is used for internal Y RAM modules, 256 locations each. The last address of the internal Y memory is mask programmed and is dependent on the amount of Y memory modules in the chip.
The importance of modular organization of the Y RAM is visible in case of DMA access to the internal Y memory simultaneous to core access to the same space. DMA and CORE accesses to different banks can be completed at full speed, while accesses to the same bank halt the DMA until a P memory slot will be available.

12.2.3 Program Memory

The Program memory space is divided into four parts:

- **192-Words Bootstrap ROM.** The P memory space located at locations $FF0000-$FF00BF is used for the internal Bootstrap ROM. The ROM contains 192 words combining the bootstrap program for the DSP56300-based derivative. The Bootstrap ROM cannot be accessed by DMA.

- **Reserved Space for Program ROM.** The P memory space located at locations $FF00C0-$FFFFFF is reserved for inclusion of Program ROM modules, 2048 locations each. Program ROM may be used to contain some operating-system program or other application-specific pre-defined user programs.
The importance of modular organization of the P ROM is visible in case of DMA access to the internal P memory simultaneous to core access to the same space. DMA and CORE accesses to different banks can be completed at full speed, while accesses to the same bank halt the DMA until a P memory slot will be available.

- **External Program Memory.** The Program memory space located at locations $000000-$FEFFFF is used for expanding to external Program memory. The starting address of the external Program memory space is

mask programmed and is dependent on the amount of on-chip Program RAM or ICACHE in the chip.

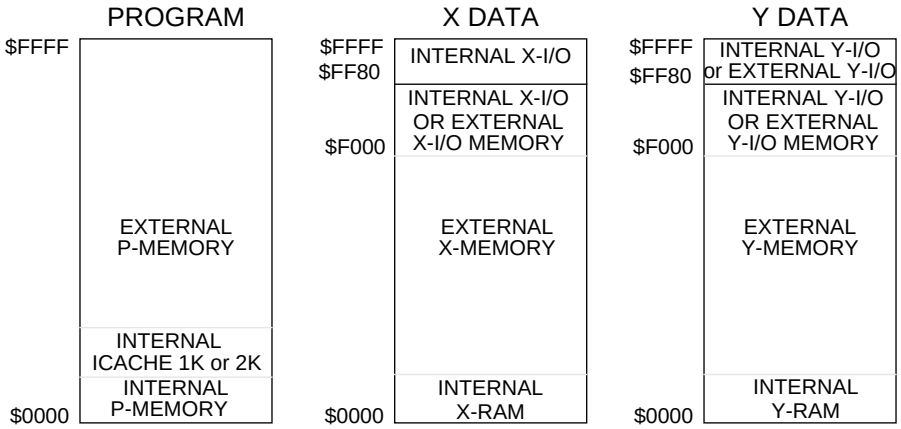
- **Internal Program RAM.** The Program memory space located at locations $000000-$00FFFF is used for internal Program RAM modules, 256 locations each. The last address of the internal Program RAM is masked programmed.
  The importance of modular organization of the P RAM is visible in case of DMA access to the internal P memory simultaneous to core access to the same space. DMA and CORE accesses to different banks can be completed at full speed, while accesses to the same bank halt the DMA until a P memory slot will be available.
  Program RAM provides a method of changing the program dynamically, allowing efficient overlaying of DSP software algorithms.

- **Internal Instruction Cache (ICACHE) RAM.** The Program memory space located at locations $000000-$00FFFF is used for internal Instruction Cache RAM modules, 256 locations each. The size of the Icache is mask programmed and can be either 1024 or 2048 words (4 or 8 RAM modules). The starting address of the Icache space is above the internal Program RAM and is also mask programmed. The Icache can be disabled by clearing the CE bit (Cache Enable) in the chip SR. If CE bit is cleared, the Icache ram becomes the high part of the internal program ram.
  The Instruction Cache is used to minimize the contention with accesses to external program memory space. A complete description of the Instruction Cache is provided in Chapter 5.

12.3 SIXTEEN-BIT COMPATIBILITY MODE

When the SIXTEEN-BIT COMPATIBILITY mode bit (see Figure 6-5 on page 6-10) is set, the memory map is changed to allow easy access to memory mapped I/O, as described in the following figure:

Figure 12-2. DSP56300 Core Memory Map (SC = 1)



For more information about this mode, its effects on the AGU, and restrictions, refer to Section 4.2.

12.4 MEMORY SWITCH MODE

when the MEMORY SWITCH MODE bit (see Figure 6-6 on page 6-17) is set, addresses of internal data memory (X, Y or both) become part of the chip internal program ram. The addresses are in the higher part of the internal ram which resides in the lower part of the data memory, and the amount of addresses is a multiplication of 256 and determined by via programing.

Due to pipelining, a change in the bit takes affect only after the following four instruction cycles. Inserting four NOP instructions after the instruction that changes the value of this bit will guarantee proper operation.