
LIST of FIGURES

| Figure Number | Title | Page Number |
|---------------|---|-------------|
| 1 | CORE DESCRIPTION | |
| Figure 1-1. | DSP56300 Core Block Diagram | 1-3 |
| 2 | EXPANSION PORT | |
| Figure 2-1. | Bus operation - zero wait states Sync. SRAM access | 2-9 |
| Figure 2-2. | Bus operation - one wait state Sync. SRAM access..... | 2-10 |
| Figure 2-3. | Synchronous Static RAM connection diagram..... | 2-10 |
| Figure 2-4. | Bus operation one wait state - SRAM access..... | 2-11 |
| Figure 2-5. | Static RAM connection diagram..... | 2-12 |
| Figure 2-6. | Dynamic RAM connection diagram..... | 2-14 |
| Figure 2-7. | Bus operation two wait states - DRAM read access (in-page)..... | 2-14 |
| Figure 2-8. | Bus operation two wait states - DRAM write access (in-page) | 2-15 |
| Figure 2-9. | Bus Arbitration scheme..... | 2-18 |
| Figure 2-10. | Address Attribute Registers (AAR3-0) | 2-20 |
| Figure 2-11. | Bus Control Register (BCR)..... | 2-24 |
| Figure 2-12. | DRAM Control Register (DCR) | 2-27 |
| 3 | DATA ARITHMETIC LOGIC UNIT | |
| Figure 3-1. | Data ALU Block Diagram | 3-3 |
| Figure 3-2. | Bit Weighting and Alignment of Operands | 3-7 |
| Figure 3-3. | Integer/Fractional Multiplication | 3-7 |
| Figure 3-4. | Convergent Rounding (no scaling) | 3-9 |
| Figure 3-5. | Two's Complement Rounding (no scaling) | 3-10 |
| Figure 3-6. | DMAC Implementation..... | 3-12 |
| Figure 3-7. | Double Precision Multiplication Using DMAC | 3-13 |
| Figure 3-8. | Double precision algorithm | 3-14 |
| Figure 3-9. | DSP56300 Core Programming Model | 3-15 |
| Figure 3-10. | Sixteen Bit Arithmetic Mode Data Organization..... | 3-16 |
| Figure 3-11. | Pipeline Conflicts - Arithmetic stall..... | 3-20 |
| Figure 3-12. | Pipeline Conflicts - Status stall..... | 3-21 |
| Figure 3-13. | Pipeline Conflicts - Transfer stall | 3-22 |

List of Figures (Continued)

| Figure Number | Title | Page Number |
|------------------|-------|----------------|
|------------------|-------|----------------|

4 ADDRESS GENERATION UNIT

| | | |
|-------------|----------------------------|-----|
| Figure 4-1. | AGU Block Diagram..... | 4-1 |
| Figure 4-2. | AGU Programming Model..... | 4-3 |

5 INSTRUCTION CACHE CONTROLLER

| | | |
|-------------|--------------------------------------|-----|
| Figure 5-1. | Instruction Cache Block Diagram..... | 5-2 |
|-------------|--------------------------------------|-----|

6 PROGRAM CONTROL UNIT

| | | |
|-------------|---|------|
| Figure 6-1. | Program Control Unit Architecture | 6-2 |
| Figure 6-2. | Seven Stage Pipeline..... | 6-3 |
| Figure 6-3. | Program Control Unit Programming Model..... | 6-4 |
| Figure 6-4. | SP Register Format | 6-7 |
| Figure 6-5. | Status Register Format | 6-10 |
| Figure 6-6. | Operating Mode Register (OMR) Format..... | 6-17 |
| Figure 6-7. | Central Processor Programming Model..... | 6-21 |

7 PROCESSING STATES

| | | |
|-------------|--|-----|
| Figure 7-1. | Interrupt Priority Register C (IPRC) | 7-6 |
| Figure 7-2. | Interrupt Priority Register P (IPRP)..... | 7-7 |

8 DMA CONTROLLER

| | | |
|-------------|----------------------------|------|
| Figure 8-1. | DMA Control Register | 8-8 |
| Figure 8-2. | DMA Status Register | 8-17 |

9 PLL and CLOCK GENERATOR

| | | |
|-------------|-----------------------------------|------|
| Figure 9-1. | PLL & CLOCK Block Diagram | 9-1 |
| Figure 9-2. | PLL Block Diagram | 9-4 |
| Figure 9-3. | PLL Control Register (PCTL) | 9-5 |
| Figure 9-4. | CLKGEN Block Diagram..... | 9-10 |

10 ON-CHIP EMULATOR (OnCE™)

| | | |
|--------------|--|------|
| Figure 10-1. | OnCE™ Block Diagram..... | 10-1 |
| Figure 10-2. | OnCE Multiprocessor Configuration | 10-2 |
| Figure 10-3. | OnCE™ Controller | 10-3 |
| Figure 10-4. | OnCE™ Command Register | 10-3 |
| Figure 10-5. | OnCE™ Status and Control Register (OSCR) | 10-5 |

| List of Figures (Continued) | | |
|------------------------------------|---|------------------------|
| Figure Number | Title | Page Number |
| <hr/> | | |
| Figure 10-6. | OnCE™ Memory Breakpoint Logic 0 | 10-8 |
| Figure 10-7. | Breakpoint Control Register..... | 10-9 |
| Figure 10-8. | Circular Tags Buffer (TAGB)..... | 10-13 |
| Figure 10-9. | OnCE™ Trace Logic Block Diagram..... | 10-14 |
| Figure 10-10. | OnCE™ Pipeline Information and GDB Registers | 10-16 |
| Figure 10-11. | OnCE™ Trace Buffer | 10-19 |
| 11 | JTAG (IEEE 1149.1) Test Access Port | |
| Figure 11-1. | JTAG Block Diagram | 11-2 |
| Figure 11-2. | TAP Controller State Machine | 11-4 |
| Figure 11-3. | Instruction Register | 11-6 |
| Figure 11-4. | Bypass Register..... | 11-7 |
| Figure 11-5. | Identification Register Configuration | 11-7 |
| 12 | OPERATING MODES AND MEMORY SPACES | |
| Figure 12-1. | DSP56300 Core Memory Map..... | 12-2 |
| Figure 12-2. | DSP56300 Core Memory Map (SC = 1) | 12-8 |
| Appendix A | INSTRUCTION SET | |
| Figure A-1. | General Formats of an Instruction Word..... | A-4 |
| Figure A-2. | Reading and Writing the ALU Extension Registers | A-7 |
| Figure A-3. | Reading and Writing Control Registers..... | A-8 |
| Appendix B | INSTRUCTION EXECUTION TIMING | |
| Appendix C | BENCHMARK PROGRAMS | |
