JOINT INSTITUTE
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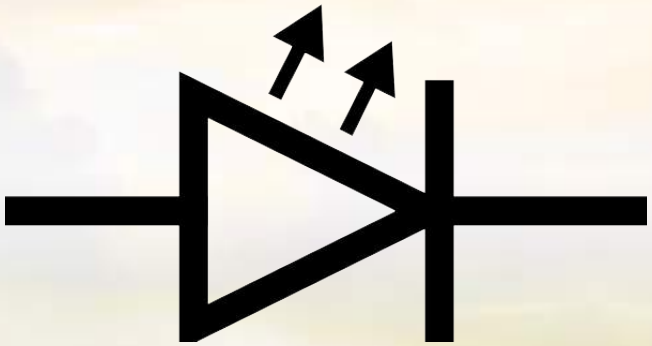
UM–SJTU JOINT INSTITUTE

DIGITAL INTEGRATED CIRCUIT
(VE312)

FINAL PROJECT

8-BIT MULTIPLIER



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Date: 8 December 2017

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Prof. Yaping Dan

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1 Energy Delay Product of out Design

1.1 EDP of static CMOS

1.2 EDP of pass transmission gate

$$\begin{aligned}\textbf{EDP} &= \text{worst case delay} \times \text{energy} \\ &= 4.027 \times 4.119 \times 10^{-3} \\ &= 16.59(ns \cdot mW)\end{aligned}$$

2 Preface

Our group tried two versions of 8-bit multiplier: one is use static CMOS and the other is to use pass-transmission gate. From the text book we know both methods has their advantages and disadvantages.

In terms of delay time, static CMOS should be larger than pass-transmission gate owing to the logic effort as well as the NAND/NOR implementation of logic.

In terms of energy consumption, static CMOS should be less than pass-transmission gate since there is no static power consumption.

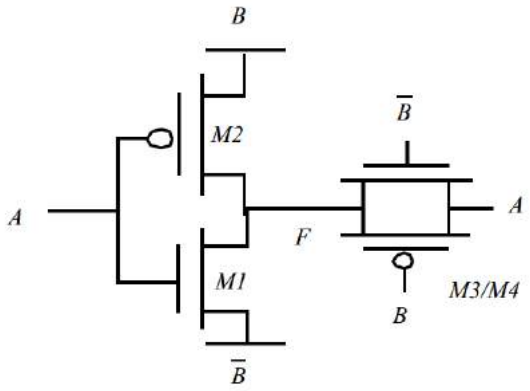
The purpose of our design is to explore which has the lowest EDP as well as some potential issues regarding transmission gate. (such as lower voltage swing)

3 Design of static CMOS

4 Design of pass-transmission gate

4.1 Overall description

After a comprehensive review of our static CMOS design, we think the XOR part in SPG module is the critical path, and could be optimized by using pass-transmission gate. For static CMOS, we need to use a inverter cascaded with a NAND gate, which in total becomes two stages. But by using of a transmission gate, we can reduce to only one stage. The idea of XOR comes from prof. Dan's lecture:

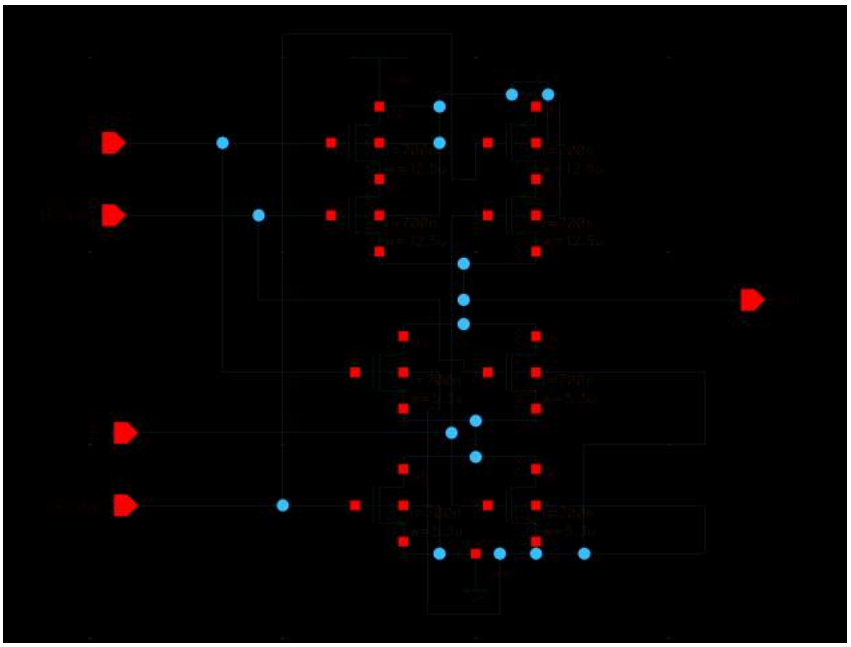


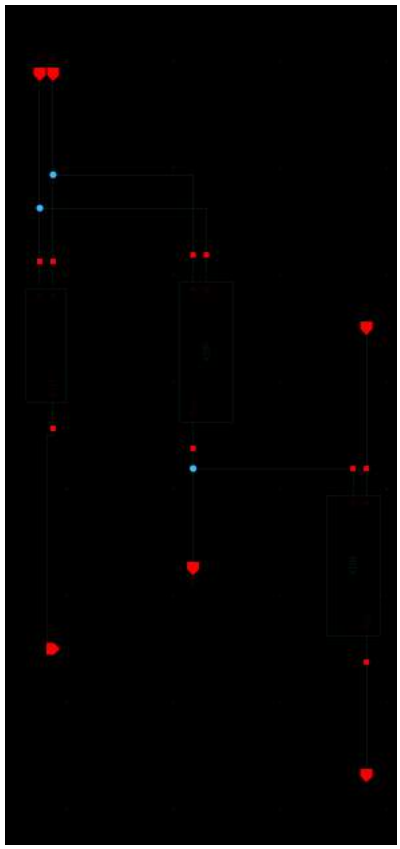
We find that when $B = 0$, the left side of output F is in high impedance, and the right side is connected to A, so in this case $F = A\bar{B}$

When B =1, the right side is in high impedance, the left side works as an inverter, so the logic now becomes $F = \bar{A}B$

And the total logic is just $F = A \oplus B$

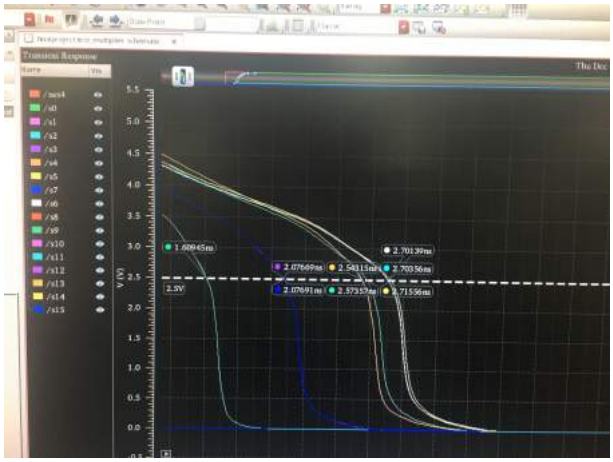
4.2 Schematics in Cadence



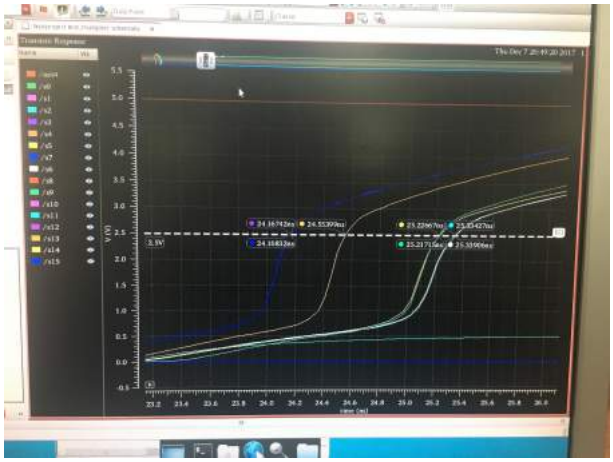


4.3 Simulation result

below are the simulation results:

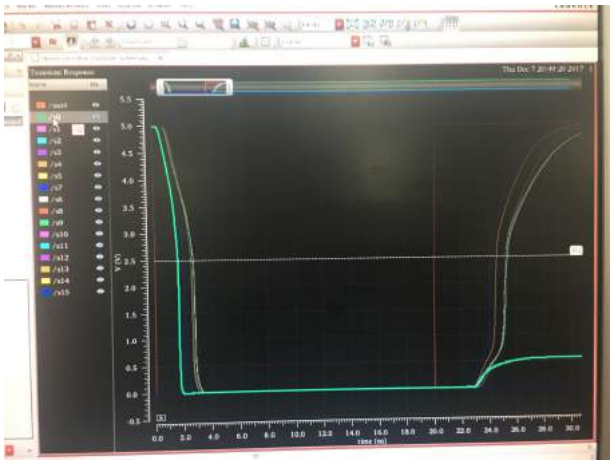


t_{pHL}

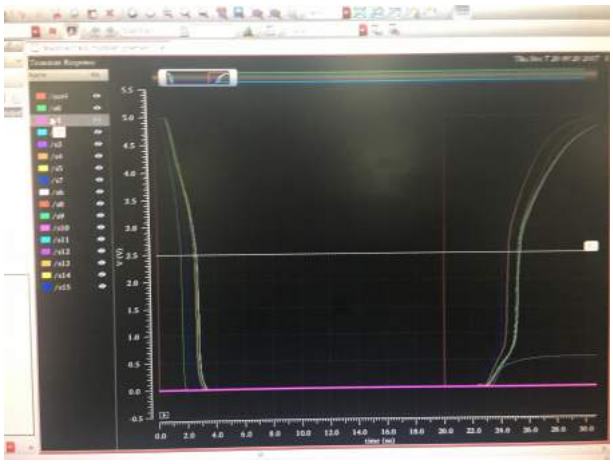


t_{pLH}

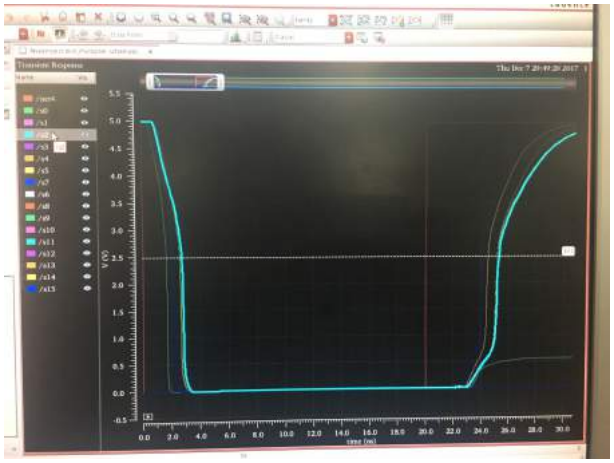
Figure 1: Delay for pass-transmission gate



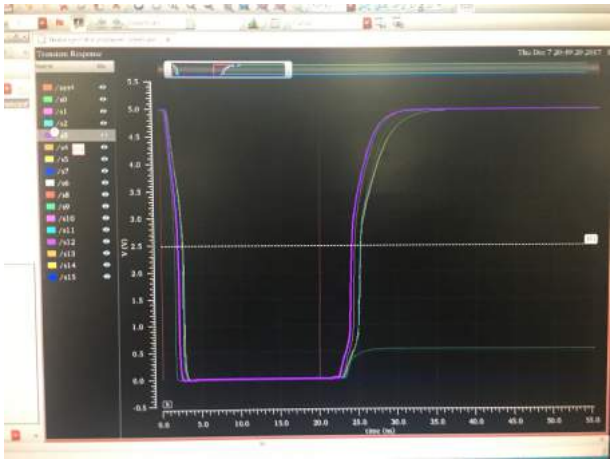
S_0



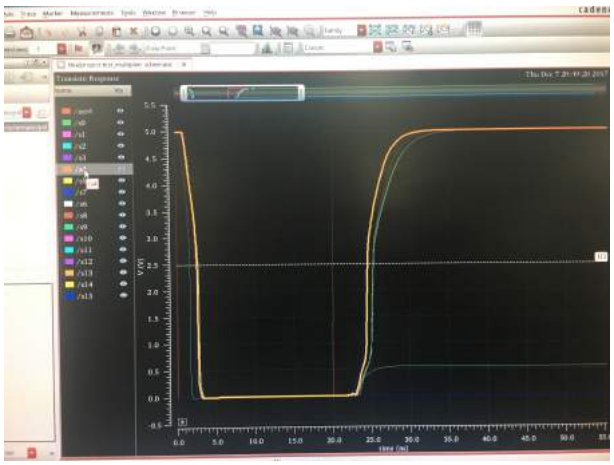
S_1



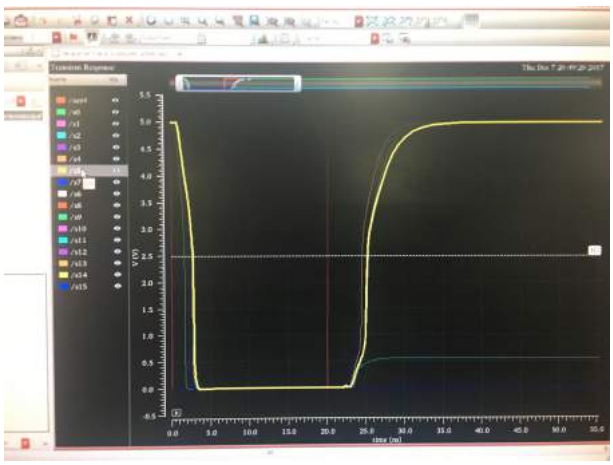
S_2



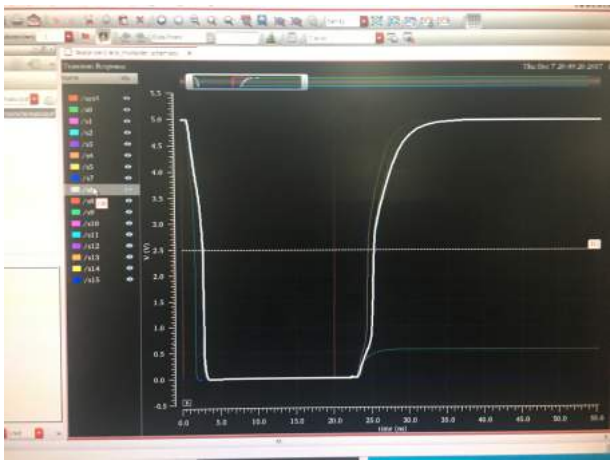
S_3



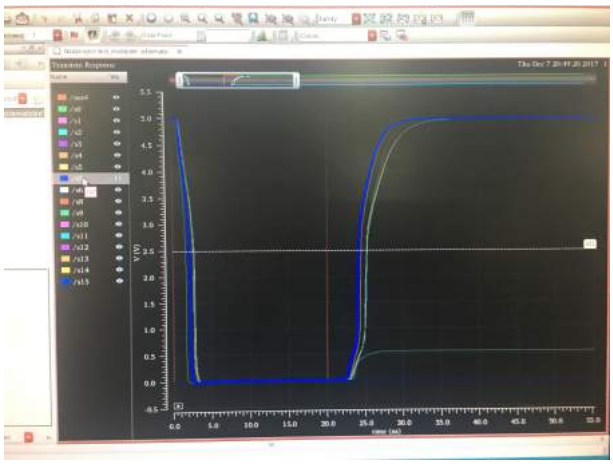
S_4



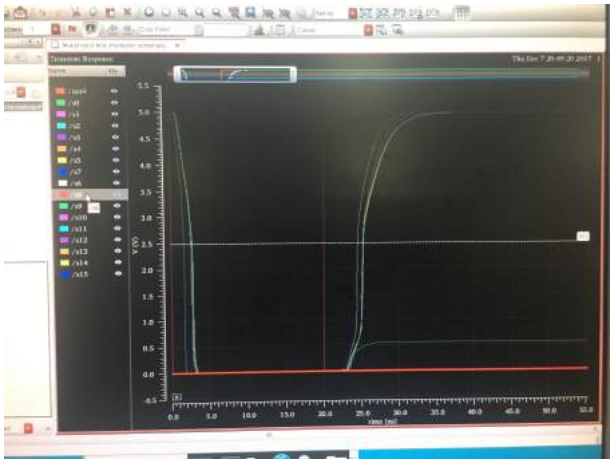
S_5



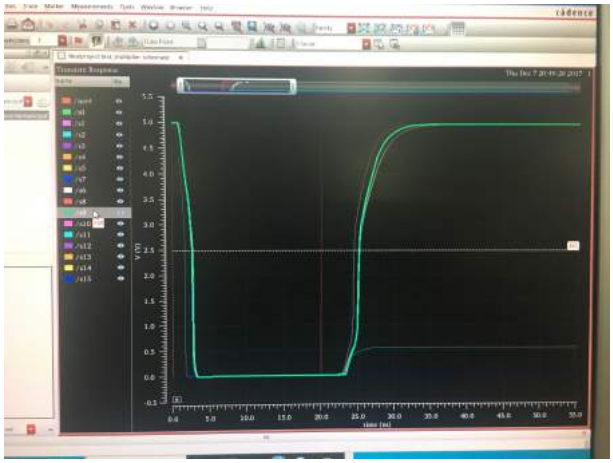
S_6



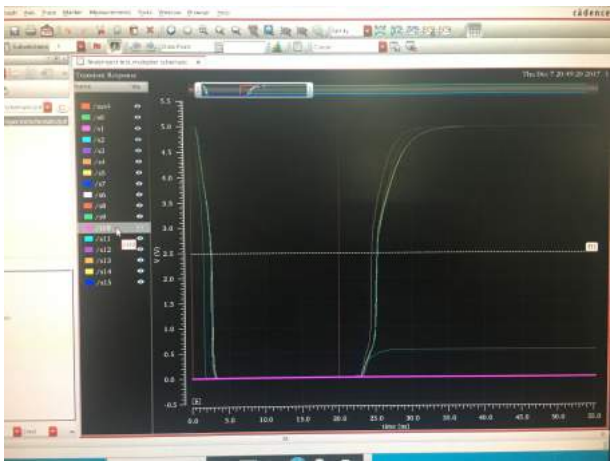
S_7



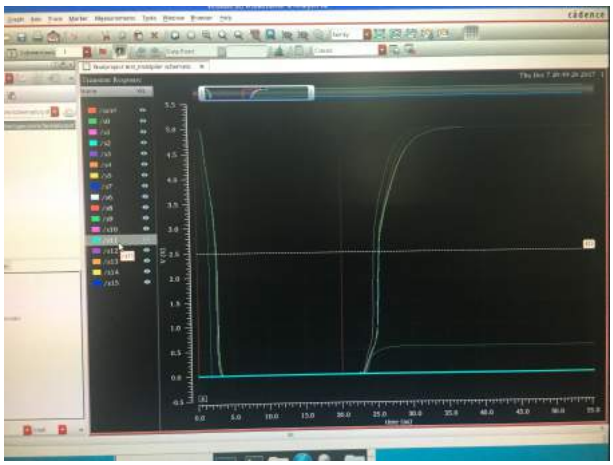
S_8



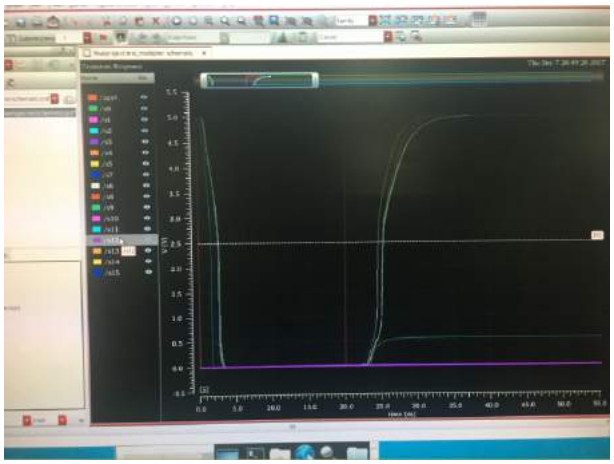
S_9



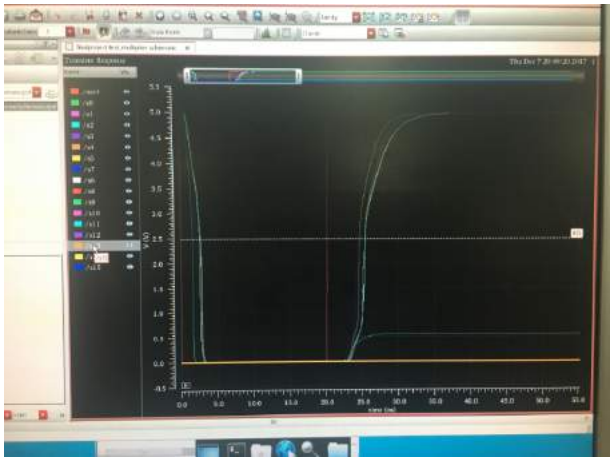
S_{10}



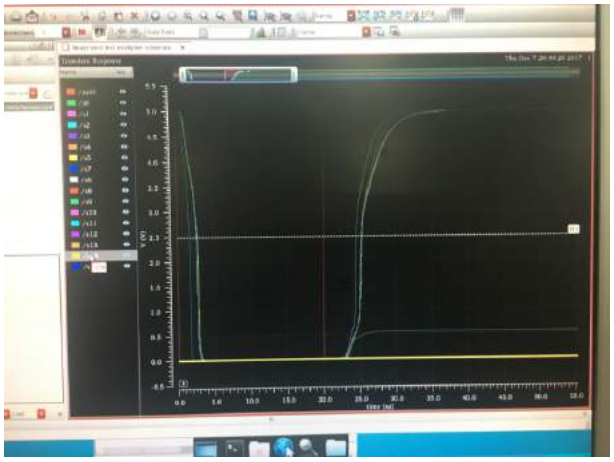
S_{11}



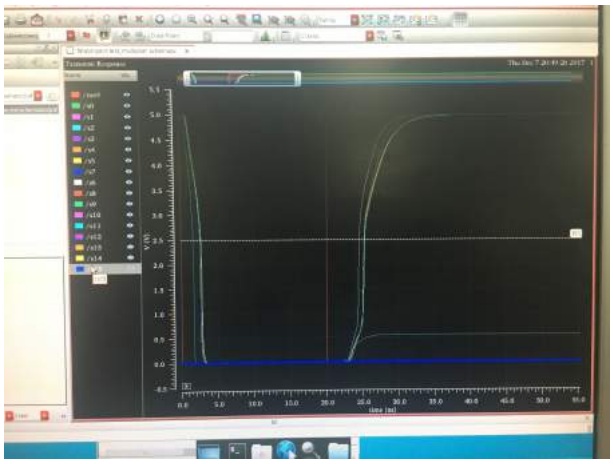
S_{12}



S_{13}

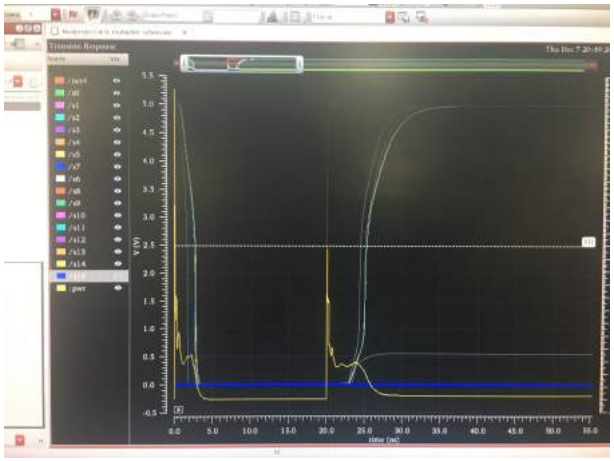


S_{14}

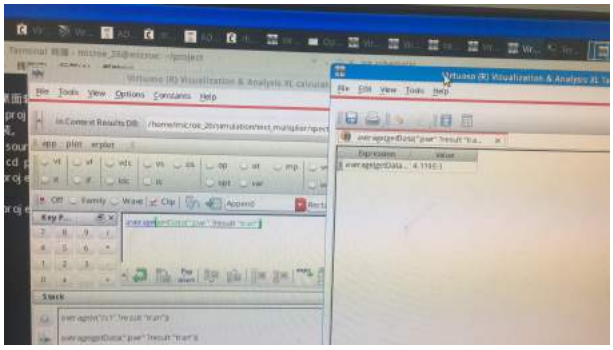


S_{15}

Power:



Power Spectrum



Power

Figure 2: Energy for pass transistor design

4.4 t_{pHL}, t_{pLH}, energy

From the figure above, we can calculate:

$$t_{pHL} = 2.71556ns$$

$$t_{pLH} = 5.33906ns$$

So $t_p = 1/2t_{pHL} + t_{pLH} = 4.027ns$

$$\text{Power} = 4.119mW$$

The result is 0000001011111101

5 Analyze and Discuss

5.1 Characteristic of pass transmission gate

As we can see from the picture, by using a pass transmission gate to implement XOR, t_{pHL} is greatly reduced. However, t_{pLH} is increased even greater, so the overall performance is worse than static CMOS.

Furthermore, we find when we use pass transmission gate to charge other gate(t_{pLH}), there always be a long response time. Perhaps that's the reason making t_{pLH} big. Another thing we Want to emphasis is that since pass transmission gate is ratio logic, it can not reach a full voltage swing, so as you can see, s0 can not be charged to vdd, but to only about 0.6V. We have tried to solve this problem by increasing the size of XOR gate, and here is the result we get from increasing size:

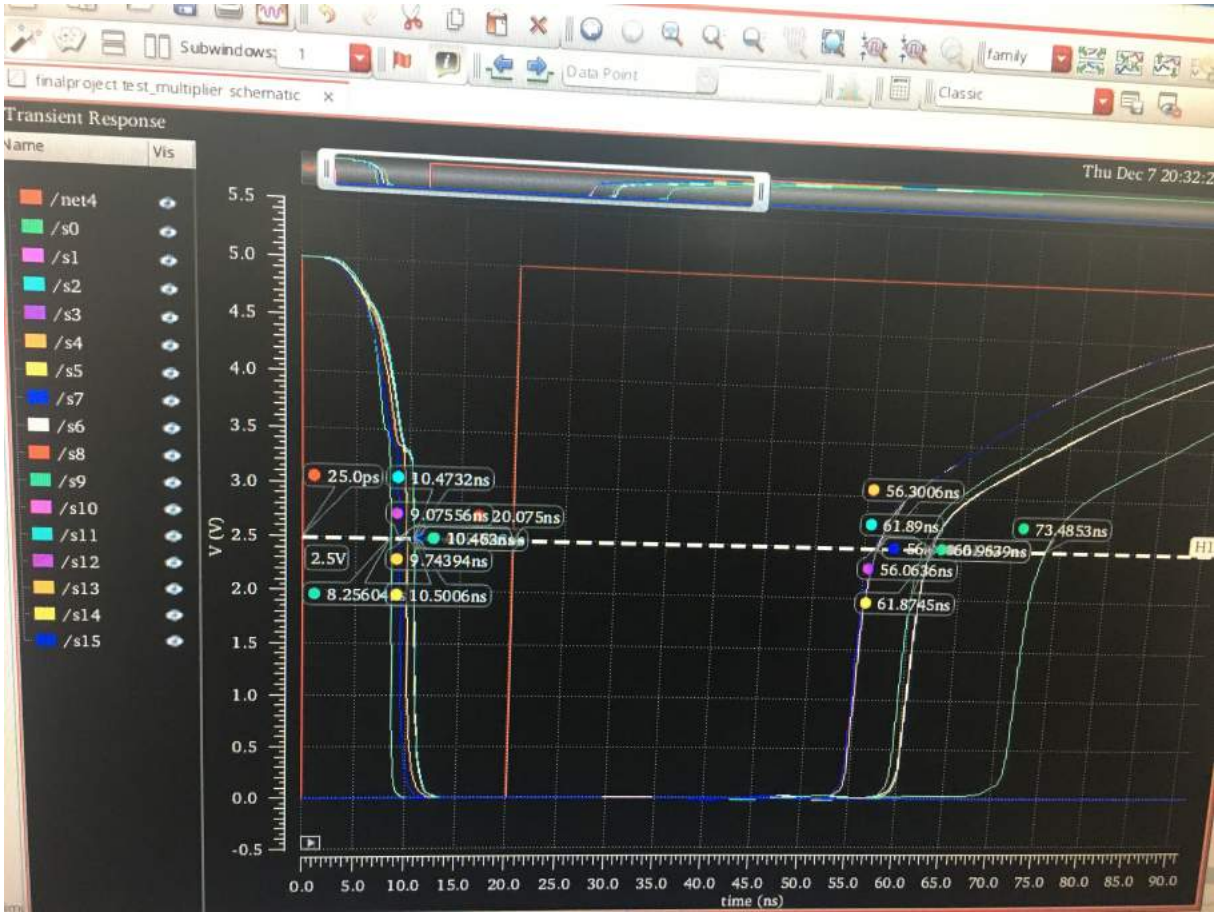
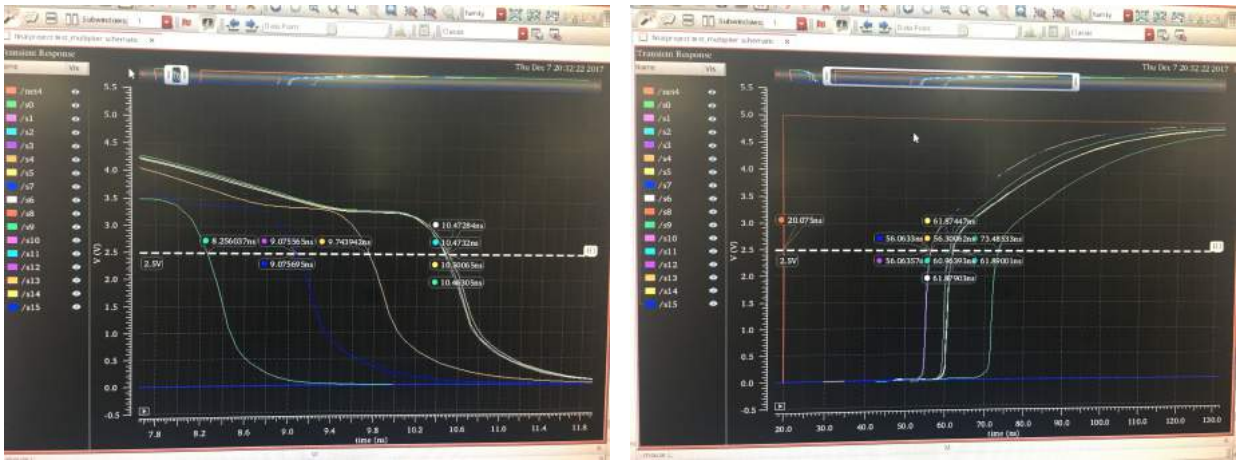


Figure 3: Delay



t_{pHL} t_{pLH}

Figure 4: Energy for pass transistor design

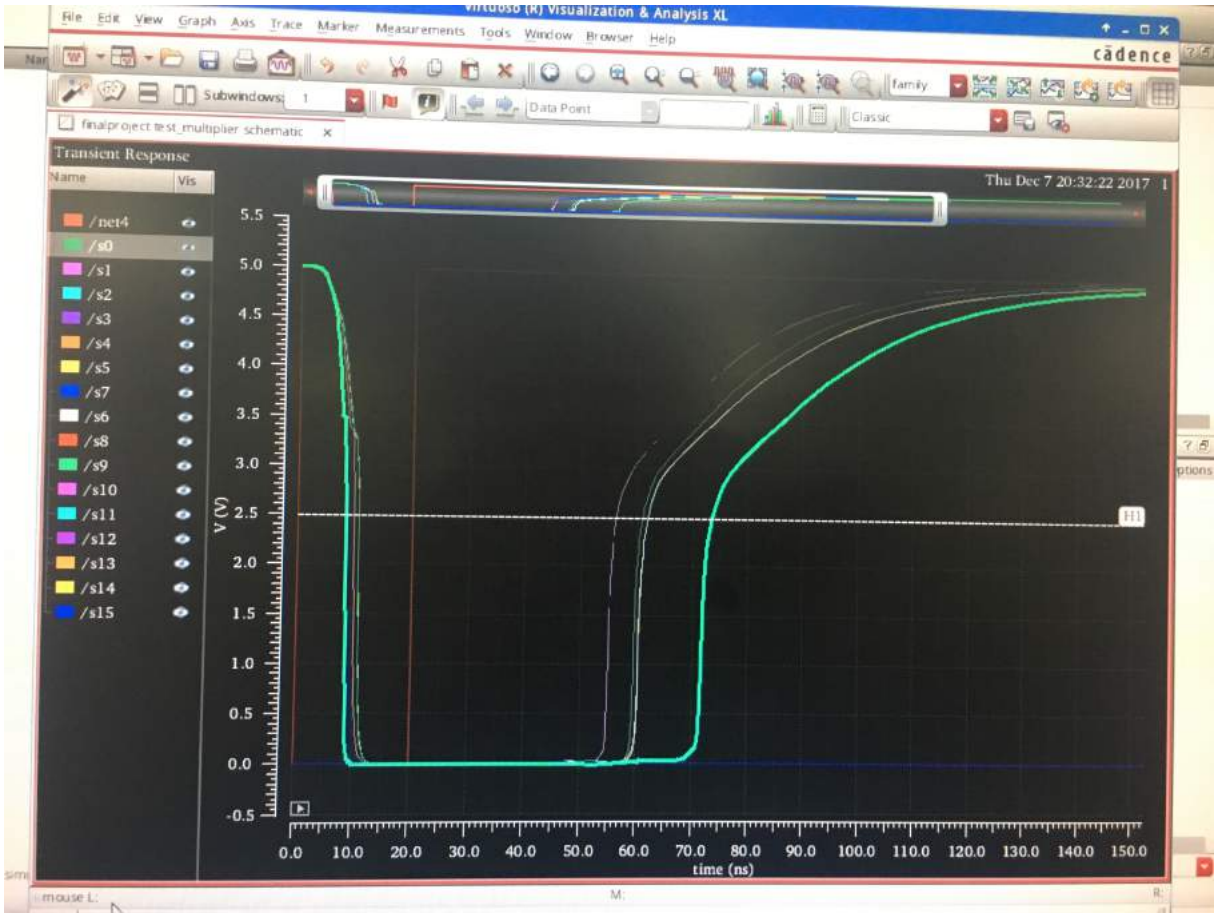


Figure 5: s0

Power:

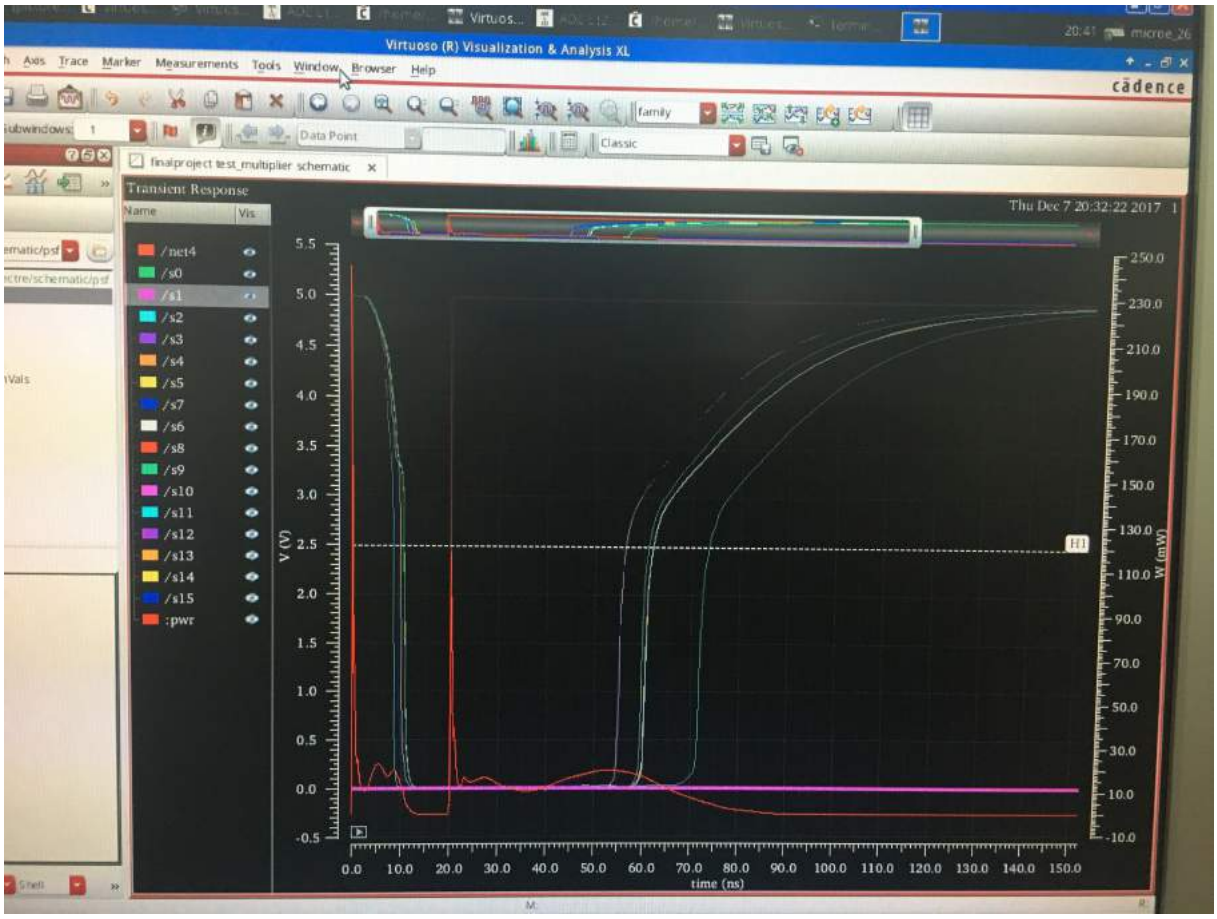


Figure 6: s0

As we can see from this picture, when we increasing the size of NMOS and PMOS, S0 can be charged to VDD, but the delay time and power are increasing a lot.

From this experience, we can conclude that using pass transmission gate can not guarantee a satisfying outcome compare to static CMOS. It's ratio logic, so the size should be properly designed to get the correct result. But one thing is for sure, using transmission gate can save lots of components. (PMOS, NMOS)