Ve370 Introduction to Computer Organization
Project 2

PROJECT DESCRIPTION

Model both single cycle and pipelined implementation of MIPS computer in Verilog that support a subset of MIPS instruction set including:

- The memory-reference instructions load word (`lw`) and store word (`sw`)
- The arithmetic-logical instructions `add`, `addi`, `sub`, `and`, `andi`, `or`, and `slt`
- The jumping instructions branch equal (`beq`), branch not equal (`bne`), and jump (`j`)

Use Figure 1 as a top level block diagram of your single cycle implementation and Figure 2 for the pipelined structure. Note: there may be some components and control signals omitted from the figures that you will have to add to support all instructions listed above. Forwarding should be implemented in the pipelined structure to handle data and control hazards. (*source: Computer Organization and Design, by Patterson and Hennessy, Morgan Kaufmann Publishers*)

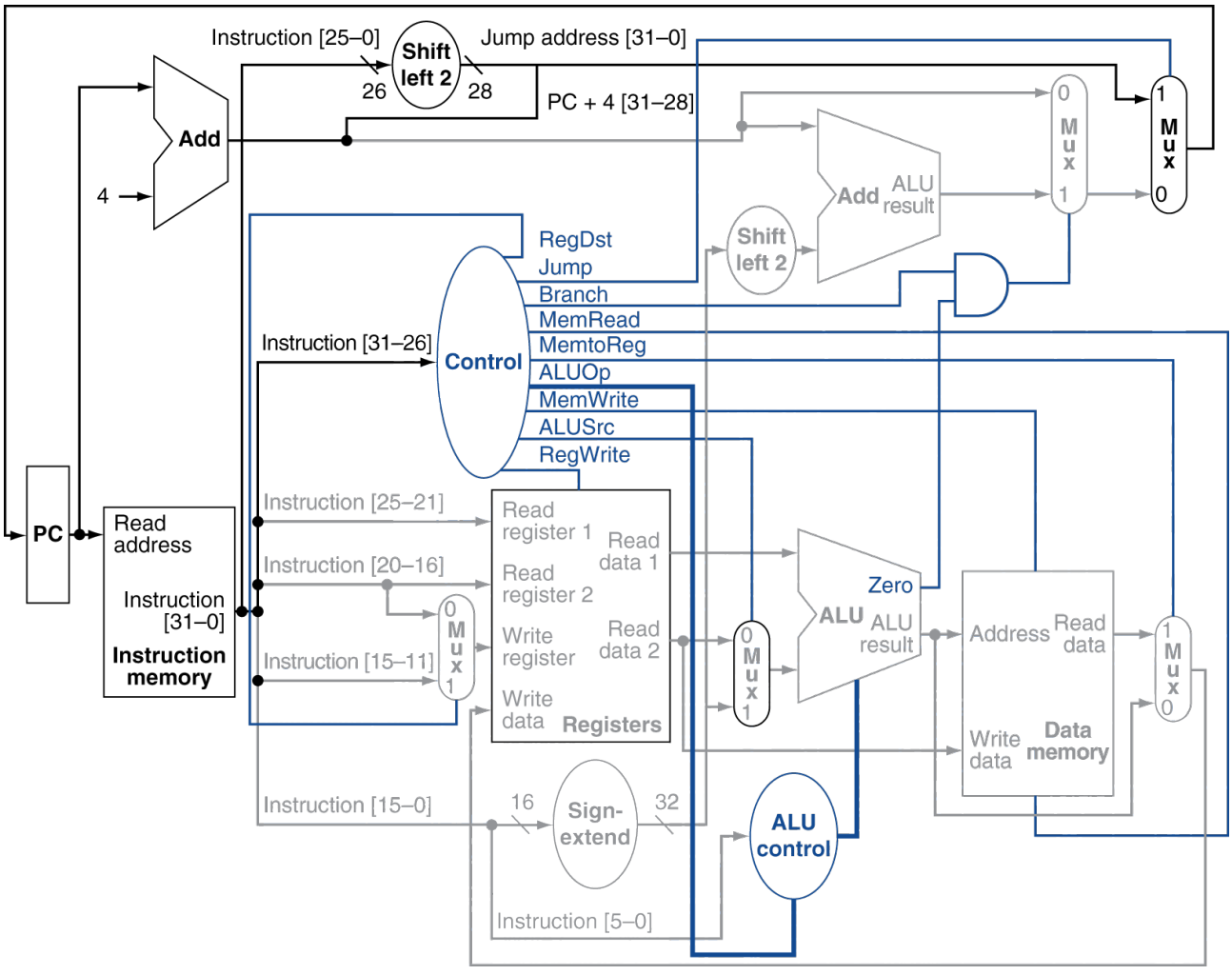

Figure 1. Single cycle implementation of MIPS architecture

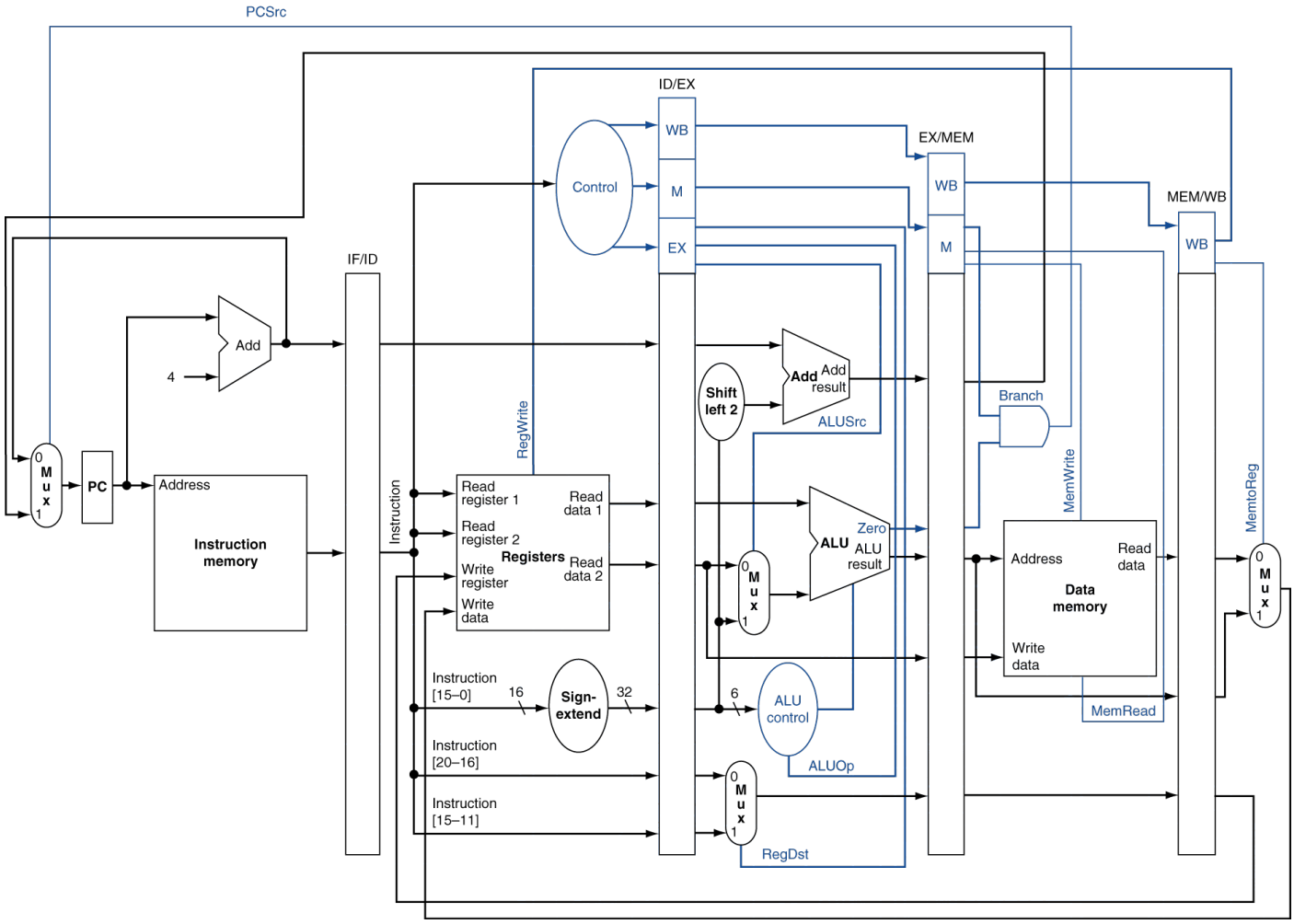

Figure 2. Pipelined implementation of MIPS architecture

PROJECT REQUIREMENTS

This project must be modeled and simulated in Verilog HDL and synthesized by using Xilinx synthesis tool. A simple MIPS assembly program using the supported instructions will be provided to you to verify that the processor can execute those instructions continuously and correctly.

You must implement your pipelined processor in the Xilinx FPGA meeting the following requirements:

- Error free in the simulation
- Be able to demonstrate on the FPGA board
- Demonstration results must coincide with your simulation results
- Demonstrate before the specified deadline.

TEAM ORGANIZATION

The Project 2 shall be team work. The work should be evenly divided and distributed among all team members.

DELIVERABLES

All deliverables should be submitted electronically on Canvas. The project must be demonstrated to the TAs.

- Project report – The project report should be a written report including all the elaborated aspects of the project. One submission is required for each team and should be submitted electronically by one of the team members. Make sure names of all team members are clearly shown on the cover page of the report.
- **Peer Evaluation report - Each team member must also submit a peer evaluation report describing your own contribution to the lab and to evaluate the performance of every other team member.**
- Simulation result – In the final report, screen shots and explanations of simulation results must be included. This will help you to earn partial credits if a project is not completed.
- RTL schematic – Generate the RTL schematic of your Verilog design by using Xilinx ISE (click **View (or Generate) RTL Schematic** under **Synthesize** step in the **Processes** tab). Include the schematic in the project report.
- Source files – Include all your Verilog and any other source files in the report as appendix.

GRADING

- Working Verilog model (simulation): 40%
- Demonstrable and working FPGA implementation: 30%
- Project report: 20%
- Peer Evaluation: 10%

DUE DATE

The project report and all required source code are due by **11:59pm, November 23, 2017**
Demonstration is due by **4:00pm, November 23, 2017**