



**One\_bit\_ALU**

**LIBRARY ieee ;**

**USE ieee.std\_logic\_1164.all ;**

**USE work.fulladd\_package.all ;**

**USE work.seven\_segment\_display\_package.all ;**

**USE work.mux4to1\_package.all ;**

**USE ieee.std\_logic\_signed.all ;**

**ENTITY one\_bit\_ALU IS**

**PORT ( carryin : IN STD\_LOGIC ;**

**w : IN STD\_LOGIC\_VECTOR(3 DOWNTO 0) ;**

**s : IN STD\_LOGIC\_VECTOR(1 DOWNTO 0) ;**

**f,set,carryout, : OUT STD\_LOGIC ;**

**A,B,C,D,E,F,G : OUT STD\_LOGIC\_VECTOR(1 DOWNTO 0)) ;**

**END one\_bit\_ALU ;**

**ARCHITECTURE Structure OF one\_bit\_ALU IS**

**BEGIN**

**with s select**

**f <= w0 when "00",**

**w1 when "01",**

**w2 when "10",**

**w3 when OTHERS ;**

**W0 <= seven\_segment\_display PORT MAP (WW(0),XX(0),YY(0),ZZ(0),A(0),B(0),C(0),D(0),E(0),F(0),G(0));**

**m1: mux4to1 PORT MAP ( '0', X(0), Y(0), S(0), C(1) ) ;**

**END Structure ;**

**Mux4to1**

**LIBRARY ieee ;**

**USE ieee.std\_logic\_1164.all ;**

**ENTITY mux4to1 IS**

**PORT ( w0,w1,w2,w3 : IN STD\_LOGIC ;**

**s : IN STD\_LOGIC\_VECTOR(1 DOWNTO 0) ;**

**f : OUT std\_logic );**

**END mux4to1 ;**

**ARCHITECTURE LogicFunc OF mux4to1 IS**

**BEGIN**

**with s select**

**f <= w0 when "00",**

**w1 when "01",**

**w2 when "10",**

**w3 when OTHERS ;**

**END LogicFunc ;**

**Mux4to1\_package**

**LIBRARY ieee ;**

**USE ieee.std\_logic\_1164.all ;**

**PACKAGE mux4to1\_package IS**

**COMPONENT mux4to1**

**PORT ( w0,w1,w2,w3 : IN STD\_LOGIC ;**

**s : IN STD\_LOGIC\_VECTOR(1 DOWNTO 0) ;**

**f : OUT std\_logic );**

**END COMPONENT ;**

**END fulladd\_package ;**