

**One\_bit\_ALU**

**LIBRARY ieee ;**

**USE ieee.std\_logic\_1164.all ;**

**USE work.fulladd\_package.all ;**

**USE work.seven\_segment\_display\_package.all ;**

**USE work.mux4to1\_package.all ;**

**USE ieee.std\_logic\_signed.all ;**

**ENTITY one\_bit\_ALU IS**

**PORT ( carryin : IN STD\_LOGIC ;**

**w : IN STD\_LOGIC\_VECTOR(3 DOWNTO 0) ;**

**s : IN STD\_LOGIC\_VECTOR(1 DOWNTO 0) ;**

**f,set,carryout, : OUT STD\_LOGIC ;**

**A,B,C,D,E,F,G : OUT STD\_LOGIC\_VECTOR(1 DOWNTO 0)) ;**

**END one\_bit\_ALU ;**

**ARCHITECTURE Structure OF one\_bit\_ALU IS**

**BEGIN**

**with s select**

**f <= w0 when "00",**

**w1 when "01",**

**w2 when "10",**

**w3 when OTHERS ;**

**W0 <= seven\_segment\_display PORT MAP (WW(0),XX(0),YY(0),ZZ(0),A(0),B(0),C(0),D(0),E(0),F(0),G(0));**

**m1: mux4to1 PORT MAP ( '0', X(0), Y(0), S(0), C(1) ) ;**

**END Structure ;**

**Mux4to1**

**LIBRARY ieee ;**

**USE ieee.std\_logic\_1164.all ;**

**ENTITY mux4to1 IS**

**PORT ( w0,w1,w2,w3 : IN STD\_LOGIC ;**

**s : IN STD\_LOGIC\_VECTOR(1 DOWNTO 0) ;**

**f : OUT std\_logic );**

**END mux4to1 ;**

**ARCHITECTURE LogicFunc OF mux4to1 IS**

**BEGIN**

**with s select**

**f <= w0 when "00",**

**w1 when "01",**

**w2 when "10",**

**w3 when OTHERS ;**

**END LogicFunc ;**

**Mux4to1\_package**

**LIBRARY ieee ;**

**USE ieee.std\_logic\_1164.all ;**

**PACKAGE mux4to1\_package IS**

**COMPONENT mux4to1**

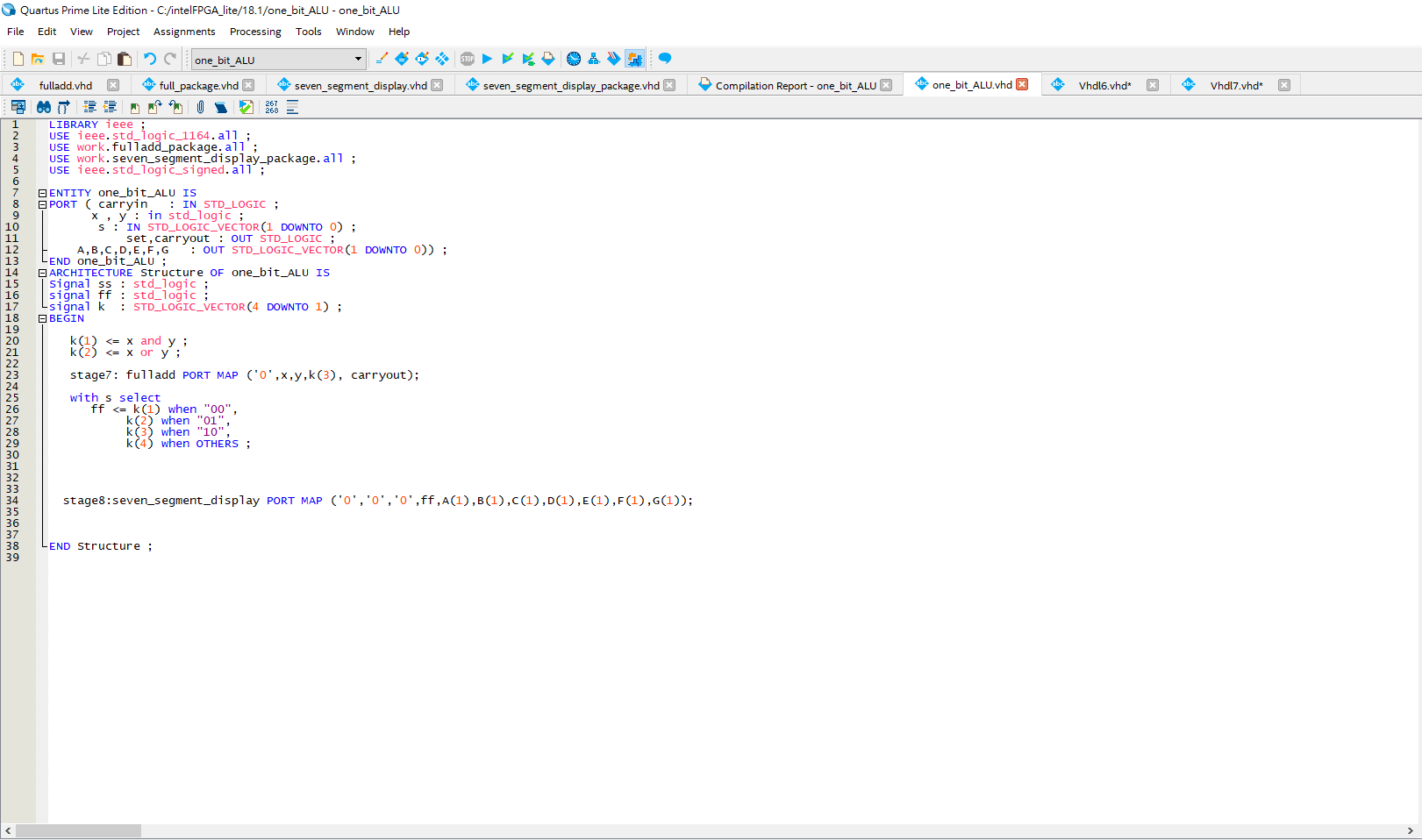
**PORT ( w0,w1,w2,w3 : IN STD\_LOGIC ;**

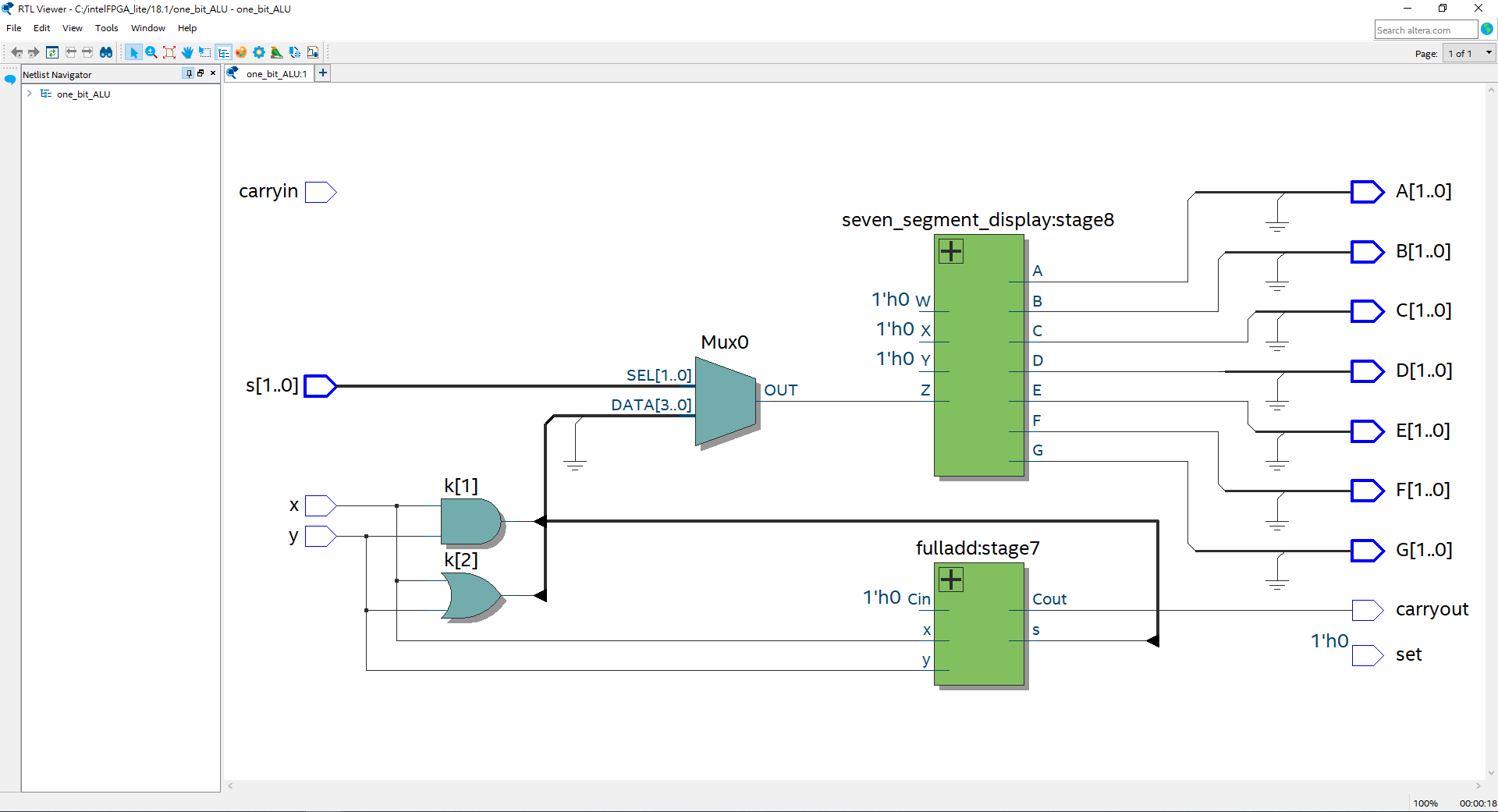
**s : IN STD\_LOGIC\_VECTOR(1 DOWNTO 0) ;**

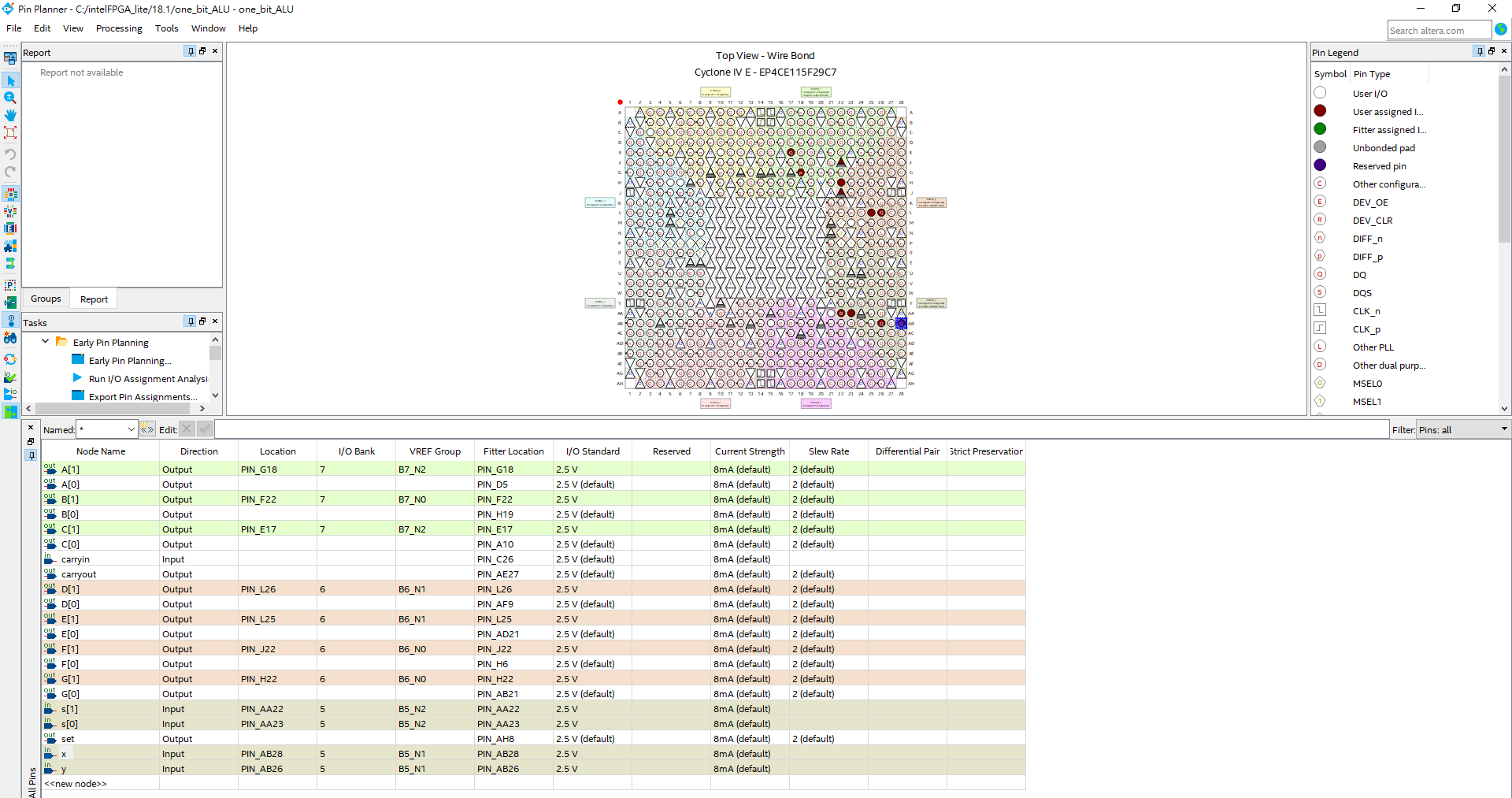
**f : OUT std\_logic );**

**END COMPONENT ;**

**END fulladd\_package ;**

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**LIBRARY ieee ;**

**USE ieee.std\_logic\_1164.all ;**

**USE work.fulladd\_package.all ;**

**USE work.seven\_segment\_display\_package.all ;**

**USE ieee.std\_logic\_signed.all ;**

**ENTITY one\_bit\_ALU IS**

**PORT ( carryin : IN STD\_LOGIC ;**

**x , y : in std\_logic ;**

**s : IN STD\_LOGIC\_VECTOR(1 DOWNTO 0) ;**

**set,carryout : OUT STD\_LOGIC ;**

**A,B,C,D,E,F,G : OUT STD\_LOGIC\_VECTOR(1 DOWNTO 0)) ;**

**END one\_bit\_ALU ;**

**ARCHITECTURE Structure OF one\_bit\_ALU IS**

**Signal ss : std\_logic ;**

**signal ff : std\_logic ;**

**signal k : STD\_LOGIC\_VECTOR(4 DOWNTO 1) ;**

**BEGIN**

**k(1) <= x and y ;**

**k(2) <= x or y ;**

**stage7: fulladd PORT MAP ('0',x,y,k(3), carryout);**

**with s select**

**ff <= k(1) when "00",**

**k(2) when "01",**

**k(3) when "10",**

**k(4) when OTHERS ;**

**stage8:seven\_segment\_display PORT MAP ('0','0','0',ff,A(1),B(1),C(1),D(1),E(1),F(1),G(1));**

**END Structure ;**

**LIBRARY ieee ;**

**USE ieee.std\_logic\_1164.all ;**

**USE work.fulladd\_package.all ;**

**USE work.seven\_segment\_display\_package.all ;**

**USE ieee.std\_logic\_signed.all ;**

**ENTITY one\_bit\_ALU IS**

**PORT ( carryin : IN STD\_LOGIC ;**

**x , y : in std\_logic ;**

**s : IN STD\_LOGIC\_VECTOR(1 DOWNTO 0) ;**

**set,carryout : OUT STD\_LOGIC ;**

**A,B,C,D,E,F,G : OUT STD\_LOGIC\_VECTOR(1 DOWNTO 0)) ;**

**END one\_bit\_ALU ;**

**ARCHITECTURE Structure OF one\_bit\_ALU IS**

**Signal ss : std\_logic ;**

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**k(1) <= x and y ;**

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**with s select**

**ff <= k(1) when "00",**

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**k(3) when "10",**

**k(4) when OTHERS ;**

**stage8:seven\_segment\_display PORT MAP ('0','0','0',ff,A(1),B(1),C(1),D(1),E(1),F(1),G(1));**

**END Structure ;**

**LIBRARY ieee ;**

**USE ieee.std\_logic\_1164.all ;**

**USE work.one\_ALU\_package.all ;**

**ENTITY mux16to1 IS**

**PORT ( w : IN STD\_LOGIC\_VECTOR(0 TO 15) ;**

**s : IN STD\_LOGIC\_VECTOR(3 DOWNTO 0) ;**

**f : OUT STD\_LOGIC ) ;**

**END mux16to1 ;**

**ARCHITECTURE Structure OF mux16to1 IS**

**SIGNAL m : STD\_LOGIC\_VECTOR(0 TO 3) ;**

**BEGIN G1:**

**FOR i IN 0 TO 3 GENERATE**

**Muxes: one\_ALU PORT MAP ( w(4\*i), w(4\*(i+1)), w(4\*(i+2)), w(4\*(i+3)), s(1 DOWNTO 0), m(i) ) ;**

**END GENERATE ;**

**Mux5: one\_ALU PORT MAP ( m(0), m(1), m(2), m(3), s(3 DOWNTO 2), f ) ;**

**stage8:seven\_segment\_display PORT MAP (m(0), m(1), m(2), m(3),A(1),B(1),C(1),D(1),E(1),F(1),G(1));**

**stage8:seven\_segment\_display PORT MAP ('0', '0', '0', f,A(1),B(1),C(1),D(1),E(1),F(1),G(1));**

**END Structure ;**

**LIBRARY ieee ;**

**USE ieee.std\_logic\_1164.all ;**

**USE work.fulladd\_package.all ;**

**USE ieee.std\_logic\_signed.all ;**

**ENTITY one\_ALU IS**

**PORT (w : IN STD\_LOGIC\_VECTOR(0 TO 3) ;**

**x , y : in std\_logic ;**

**s : IN STD\_LOGIC\_VECTOR(1 DOWNTO 0) ;**

**set,carryout : OUT STD\_LOGIC ;**

**A,B,C,D,E,F,G : OUT STD\_LOGIC\_VECTOR(1 DOWNTO 0)) ;**

**END one\_ALU ;**

**ARCHITECTURE Structure OF one\_ALU IS**

**Signal ss : std\_logic ;**

**signal ff : std\_logic ;**

**BEGIN**

**w(0) <= x and y ;**

**w(1) <= x or y ;**

**stage7: fulladd PORT MAP ('0',x,y,w(2), carryout);**

**with s select**

**ff <= w(0) when "00",**

**w(1) when "01",**

**w(2) when "10",**

**w(3) when OTHERS ;**

**END Structure ;**